Design and Experimental Assessment of a Robust Voltage Control for DC-DC Converters Considering Components Parametric Uncertainties

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ABSTRACT This study presents the design and evaluation of a robust controller, based on frequency-domain, in order to enhance the performance of dc-dc power converters under parametric uncertainties. This robust control approach takes into account all possible uncertainties in the system such as load and input voltage variations. Thereby, the robust controller design is based on the constraints of the gain and/or phase margins delimited by these uncertainties in order to ensure robust performance and stability of the system. Assessments on the performance of the proposed robust control are conducted. Comparisons with other control methods are also provided. Experimental validations on a dc-dc buck converter system test board are carried out to verify the theoretical claims.

INDEX TERMS Buck converter, dc-dc converter, frequency-domain, power electronics, parametric uncertainties, robust control.

I. INTRODUCTION

Nowadays, the dynamic performance of dc-dc converters is a subject of paramount importance. Such class of power electronic converters are presented in a wide range of applications, ranging from interfacing renewable power sources to regulation of different voltage levels in telecommunication and biomedical systems, just to name a few. In order to functioning properly, dc-dc converters relies on feedback control strategies, to operate under varying operating conditions and subject to many sources of uncertainties, such as parametric components uncertainties. Therefore, the design of robust control systems for dc-dc converter is an open research field which is increasingly attracting the attention of many investigators [1]–[5].

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Several researches are focused on the controller design in order to improve the performance and stability, where the main goals are simplicity in structure, high power density, high efficiency, high quality in conversion, low cost and reliability [1]–[5].

Some modern processes in industries require high-dynamic-performance of power converters, thus different types of converters are applied in some applications such as in variable speed DC motor drives [6], renewable energy systems [7], transportation system [8], hybrid energy storage [9], [10], communication systems [11].

In order to enhance power converter efficiency and dynamic performance, several advanced control techniques been proposed by researchers. State feedback techniques are reported in [12] as current mode control method that satisfies the required converter specification using the pole-placement technique. In [13], the design tool integrating

frequency-based design techniques for a given dynamic specification, i.e. taking into account the set of achievable crossover frequencies and phase margin requirements, is proposed, in addition, this work presents the algorithms to calculate the performance space and analyze their impact on the controller design. In [14], a novel direct digital design method for discrete controller with PID structure + filter, namely PIDF controller, is introduced. The proposed controller is evaluated in both simulation and experimental tests performed in dc-dc buck converters. The controller design is carryied out by pole-zero cancellation method with an analytical design methodology based on inversion formulae. The work developed in [15] addressed a regulation of a dc-dc Boost converter subject to parametric uncertainties, i.e. load and input voltage variation, and unmodeled dynamics. This methodology combines a predesigned cascade controller and nested reduced order PI observers to maintain the desirable voltage regulation performance. Several simulation and experimental tests were performed to ratify the effectiveness of this technique. Two control methodologies are presented in [16] to control mismatched dc-dc buck converter. The first method uses a multiple surface sliding mode control to handle mismatched load uncertainty, meanwhile the second method is based on simultaneous state and disturb observer that are added into the loop. Furthermore, several works that combine sensorless structures with second order sliding mode control applied in dc-dc buck converters are discussed in the literature [17]–[19]. In [20] a proportional integral sliding function for dc-dc buck converter was investigated, the proposed sliding mode was modified to improve the steady state and dynamic performance by using a adaptive tuning controller to compensate the load variations, furthermore, the closed-loop stability was proved in steady state and several tests were carried out to evaluate the performance and stability of the control strategy proposed in comparison with the classical strategies. In [21] a novel sliding mode controller is introduced to mismatched uncertainties applied in dc-dc converters. Then, an uncertainty and disturbance estimator was developed based on sliding mode control approach, aiming to improve the performance and stability of the power converters. Thereby, simulation and experimental tests proved the good performance of the proposed methodology in presence the uncertainties and disturbance.

In [4], a sample-data output feedback control problem was investigated applied in a dc-dc buck converter taking into account components uncertainties. Then, a reduced observer and a robust output feedback controller was designed, both devices in the sampled data form, which were evaluated in presence of uncertainties. Furthermore, numerical simulations and experimental results were analyzed to ratify the good performance of the controller, in addition, the stability analysis was addressed taking into account the uncertainties parameters. In [22], a generalized proportional-integral observer (GPIO) with a robust output feedback control problem applied in the dc-dc converter was investigated. Then, a general class of time-varying disturbances occurred in the

dc-dc buck converter were analyzed and the results showed that the proposed methodology allows to compensate for this kind of disturbance. furthermore, experimental results showed the efficiency of this methodology. In [23], a robust stability analysis of the dc-dc buck converter when the system is subjected to a multiple parametric uncertainties was performed. This work proposed a practical approach to apply the μ method in the robust stability analysis taking into account several uncertainties. Several numerical and experimental tests were performed to demonstrate the efficiency of this stability analysis. Reference [24] deals about the constrained stability problem and tracking problem by using the Takagi-Sugeno (T-S) fuzzy positive systems, thereby, the author used the linear programming to insert the constrained in the design phase. Numerical simulations were carried out to show the success of the proposed methodology. In [25], a generalized minimum variance (GMV) controller is proposed to regulate the output of the dc-dc buck converter in order to decrease the impact of the noise in the system performance. This controller is compared with a linear controller and shows better characteristics, significantly reducing their variances, i.e. the GMV controller uses less energy causing less switching losses, improving the efficiency of the buck converter.

Given the state-of-the-art above presented, it is possible to verify that exists a lack contribution in the experimental investigation of robust control methodologies applied in power electronic converters to ensure the gain and phase margin when the system is subjected to parametric uncertainties (load and input voltage variations).

The aim of this work is to investigate a robust control methodology based on frequency response to ensure the phase and gain margin when the system is subjected to a family of parametric uncertainty. The proposed control methodology is applied in a dc-dc buck converter and several tests (load variations; input voltage variations and voltage setpoint variation) are performed to assess the performance and stability of the system when the dc-dc buck converter is subjected to a specific family of uncertainties. Furthermore, these tests are addressed to evaluate the control performance of the proposed methodology.

The novel contributions of this work are summarized as follows:

- A robust methodology of controller design, based on frequency response analysis, is proposed for dc-dc power converters to ensure the desired phase and gain margin when the system is subjected to a family of parametric uncertainty.
- The proposed robust methodology provides the desired phase and gain margin of the system, ensuring robust stability and robust performance for an entire predefined uncertainty region.
- The proposed robust methodology is exhaustively evaluated in both simulation and experimental tests by using simulation models (MATLAB/Simulink) and experimental plant (dc-dc power converter board), respectively,

to ratify the robustness and effectiveness of the proposed controller. The Integral Squared Error (ISE) performance index is computed to analyze the control methodologies compared in this work. The results show the proposed robust methodology outperforms the other approaches.

The remainder of this paper is organized as follows. Section II introduces the mathematical model of dc-dc buck converter using the state-pace averaging technique. Section III presents a brief analysis of interval systems with parametric uncertainties. Section VI presents a brief review about parametric robust control background based on frequency-domain response. The proposed design methodology for robust controller is also introduced. Section V presents an assessment of the simulation results and experimental data. Finally, Section VI presents the main conclusions about this work.

II. SYSTEM DESCRIPTION

Fig. 1 shows a typical topology of buck converter, which is comprised of the switching component (Q_1) with a PWM gate drive controlled switch $d(t)$, a diode (D_1), a capacitor (C), a inductor (L), and a Load resistance (R_L).
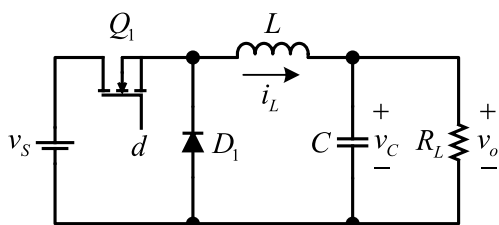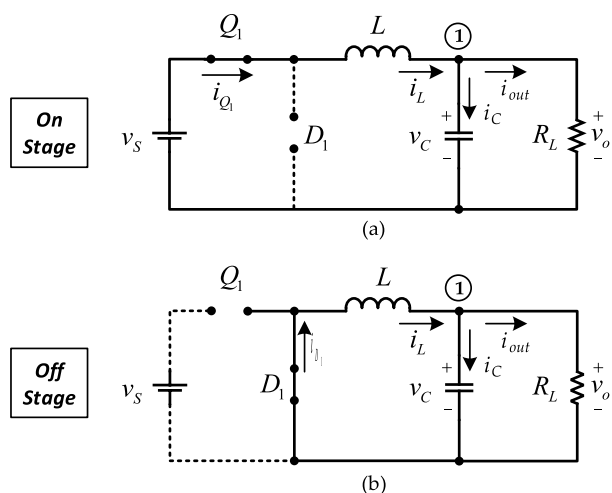

FIGURE 1. Buck Converter Topology.

FIGURE 2. Power Stages of Buck converter. (a) On Stage; (b) Off Stage.

A. OPERATION MODE OF BUCK CONVERTER

In this work, the dc-dc buck converter operates in continuous conduction mode (CCM). Thus, the converter exhibits two circuit states as shown in Fig. 2.

The first state is when the switching component (Q_1) is turned on (cf. Fig. 2(a)). During this interval (dT_s), the inductor L is in a charging phase, and hence i_L increase linearly. The second state is when the switching component (Q_1) is turned off (cf. Fig. 2(b)). During this interval (($1 - d)T_s$), L is in a discharging phase; L discharges the stored energy to output. Thus, i_L decrease linearly, but will be not clamped to zero.

B. MODELING OF A BUCK CONVERTER BY STATE-SPACE AVERAGING TECHNIQUE

The state-space equations of the buck converter for the on and off states of the switching component are given by (1) and (2).

$$ON \Rightarrow \begin{cases} \dfrac{di_L(t)}{dt} = -\dfrac{1}{L}v_c(t) + \dfrac{1}{L}v_s(t) \\ \dfrac{dv_c(t)}{dt} = \dfrac{1}{C}i_L(t) - \dfrac{1}{R_L C}v_c(t) \end{cases} \quad (1)$$

$$OFF \Rightarrow \begin{cases} \dfrac{di_L(t)}{dt} = -\dfrac{1}{L}v_c(t) \\ \dfrac{dv_c(t)}{dt} = \dfrac{1}{C}i_L(t) - \dfrac{1}{R_L C}v_c(t) \end{cases} \quad (2)$$

The output voltage, $v_o(t) = v_c(t)$, is a dc voltage that contains small ripple due to the switching action.

By rewriting Eqs (1)–(2) in matrix form, the state-space matrices and the input vectors for each stage can be found.

$$A_1 = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix}, \quad A_2 = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$C_1 = C_2 = \begin{bmatrix} 0 & 1 \end{bmatrix}, \quad E_1 = E_2 = \begin{bmatrix} 0 \end{bmatrix}$$

In CCM, the averaged behavior of the converter over one switching period is defined as follows

$$\begin{cases} \dfrac{dx(t)}{dt} = A_s x(t) + B_s v_s(t) \\ v_o(t) = C_s x(t) + E_s v_s(t) \end{cases} \quad (3)$$

where:
$A_s = d(t)A_1 + (1 - d(t))A_2$, $B_s = d(t)B_1 + (1 - d(t))B_2$, $C_s = d(t)C_1 + (1 - d(t))C_2$ and $E_s = d(t)E_1 + (1 - d(t))E_2$.

Hence, the state-space averaged model of the buck converter in CCM can be written according to (3).

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} \dfrac{d(t)}{L} \\ 0 \end{bmatrix}v_s(t) \quad (4)$$

C. SMALL-SIGNAL AVERAGED MODEL OF THE BUCK CONVERTER

Equation (4) is a nonlinear continuous-time equation. Therefore, it can be linearized by small-signal perturbation with

$i_L(t) = I_L + \tilde{i}_L(t)$, $v_c(t) = V_c + \tilde{v}_c(t)$, $v_s(t) = V_s + \tilde{v}_s(t)$, and $d(t) = D + \tilde{d}(t)$, where: $\tilde{i}_L$, $\tilde{v}_c$, $\tilde{v}_s$, $\tilde{d}$ represent a small signal value, and I_L, V_c, V_s, and D represent the dc value, i.e., the operating point. It is important to note that $I_L \gg \tilde{i}_L(t)$, $V_c \gg \tilde{v}_c(t)$, $V_s \gg \tilde{v}_s(t)$, and $D \gg \tilde{d}(t)$. The perturbation yields the linear small-signal state-space equations in (5) and (6).

$$\frac{d}{dt}\begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} = A\begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} + B\tilde{v}_s(t) + B_d\tilde{d}(t) \quad (5)$$

$$\tilde{v}_o(t) = C\begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} + E\tilde{v}_s(t) + E_d\tilde{d}(t) \quad (6)$$

where,

$$A = DA_1 + (1 - D)A_2,$$
$$B = DB_1 + (1 - D)B_2,$$
$$C = DC_1 + (1 - D)C_2,$$
$$E = DE_1 + (1 - D)E_2,$$
$$B_d = (A_1 - A_2)\begin{bmatrix} I_L \\ V_c \end{bmatrix} + (B_1 - B_2)V_s$$
$$E_d = (C_1 - C_2)\begin{bmatrix} I_L \\ V_c \end{bmatrix} + (E_1 - E_2)V_s.$$

Hence, the linear small-signal averaged model (7)–(8) of the buck converter operating in CCM is

$$\frac{d}{dt}\begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_L C} \end{bmatrix}\begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix}$$
$$+ \begin{bmatrix} \dfrac{D}{L} \\ 0 \end{bmatrix}\tilde{v}_s(t) + \begin{bmatrix} \dfrac{V_s}{L} \\ 0 \end{bmatrix}\tilde{d}(t) \quad (7)$$

$$\tilde{v}_o(t) = \begin{bmatrix} 0 & 1 \end{bmatrix}\begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix} + [\,0\,]\tilde{v}_s(t) + [\,0\,]\tilde{d}(t) \quad (8)$$

D. THE DUTY CYCLE-TO-OUTPUT VOLTAGE TRANSFER FUNCTION

The duty cycle-to-output voltage transfer function is calculated as follows,

$$G_{vd}(s) = \left.\frac{\tilde{v}_o(s)}{\tilde{d}(s)}\right|_{\tilde{v}_s(s)=0} = C(sI - A)^{-1}B_d + E_d \quad (9)$$

Therefore, the duty cycle-to-output voltage transfer function of the buck converter is found by solving (9).

$$G_{vd}(s) = \left.\frac{\tilde{v}_o(s)}{\tilde{d}(s)}\right|_{\tilde{v}_s(s)=0} = \frac{\dfrac{V_s}{LC}}{s^2 + \dfrac{1}{R_L C}s + \dfrac{1}{LC}} \quad (10)$$

The nominal values of the plant parameters, operational point, uncertainties and the meaning of each symbol in (10) are presented in Table 1.

III. PARAMETRIC UNCERTAINTIES ANALYSIS

In the robust control theory, there are two main approaches for taking into account uncertainties: parametric and non parametric approaches. The second one focuses on prior

TABLE 1. Parameters of the Buck converter system.

Par.	Unit	Min Val.	Max Val.	Nom. Val.	Description
V_s	V	15.0	19.0	15.0	Source input voltage
V_o	V	4.0	8.0	4.0	Output voltage
L	μH	–	–	2.0	Filter inductor
C	μF	–	–	2200	Output Capacitor
R_L	Ω	1.0	4.0	4.0	Resistive Load
f_s	kHz	–	–	5.0	Switching frequency

knowledge of modeling errors that, for instance, come from neglect parasitic effects at high frequency range. In this kind of uncertainties, modeling can be unnecessarily conservative, sometimes leading to high-order controllers with poor performance. In contrast, the first approach, namely parametric uncertainties, allows to take into account from the outset in the controller design process a priory knowledge about the possible range assumed for the values of system's physical parameters, incorporating available information about components (resistors, inductors, and capacitors) tolerances. Therefore, the parametric uncertainty modeling approach seems to be suitable for the design of control systems for power electronic converters [26], being the approach used in this paper. As dc-dc buck converters have electronic switches, resistors, inductors and capacitors, as their main components, the parametric approach shows to be a worthy tool for taking into account the possible interval range of components' values (cf. Table 1), giving by the respective component tolerance.

A. PARAMETRIC UNCERTAINTY AND INTERVAL POLYNOMIAL

Let a be a real parameter assuming an uncertain value which belongs to a pre-specified real interval range $[a^-, a^+]$, where the real numbers $[a^-, a^+]$ are, respectively, the minimal and maximal values delimited by a uncertainty box region, which is known. Therefore, the parameter a may assume any value within the uncertainty box region at any time. In short notation, $a \in [a^-, a^+]$.

Let $x_0, x_1, \ldots, x_n$ be uncertain parameters assuming values in the corresponding pre-specified intervals $[x_0^-, x_0^+]$, $[x_1^-, x_1^+], \ldots, [x_n^-, x_n^+]$, then an interval polynomial $X(s)$, on the Laplace's complex variable s, is defined as

$$X(s) = x_0 + x_1 s + \cdots + x_n s^n \quad (11)$$

where $x_0 \in [x_0^-, x_0^+]$, $x_1 \in [x_1^-, x_1^+], \ldots, x_n \in [x_n^-, x_n^+]$.

An interval polynomial $X(s)$ may also be expressed in the following compact and suitable form

$$X(s) = [x_0^-, x_0^+] + [x_1^-, x_1^+]s + \cdots + [x_n^-, x_n^+]s^n \quad (12)$$

An interval polynomial $X(s)$ is a compact representation of a family of polynomials which has infinite members. An interval polynomial $X(s)$ is robustly Hurwitz stable if all its members are Hurwitz stable (a polynomial is Hurwitz

stable if all its roots are contained on the left half-plane (LHP) of the *s*-plane). Therefore, it would be necessary to check stability of an infinite number of polynomials to ensure the robust stability for a given interval polynomial $X(s)$. Fortunately, the Russian scientist Kharitonov proved that it is necessary and sufficient to test the Hurwitz stability of only the following four polynomial [27], [28], which belong to the $X(s)$ family, to ensure the robust stability of $X(s)$.

$$
\begin{aligned}
X^{(1)}(s) &= x_0^- + x_1^- s + x_2^+ s^2 + x_3^+ s^3 + \dots \\
X^{(2)}(s) &= x_0^- + x_1^+ s + x_2^+ s^2 + x_3^- s^3 + \dots \\
X^{(3)}(s) &= x_0^+ + x_1^- s + x_2^- s^2 + x_3^+ s^3 + \dots \\
X^{(4)}(s) &= x_0^+ + x_1^+ s + x_2^- s^2 + x_3^- s^3 + \dots
\end{aligned}
\tag{13}
$$

The four polynomial (13) are called Kharitonov polynomials and play a role in the analysis and design of control systems for plants having parametric uncertainties [28]. They are, therefore, instrumental for the dc-dc buck converter control method proposed in this paper.

B. INTERVAL SYSTEMS

A strictly proper interval transfer function $G(s) = \frac{N(s)}{D(s)}$ can be described in the form of following ratio of interval polynomials:

$$
G(s) = \frac{[n_0^-, n_0^+] + [n_1^-, n_1^+]s + \dots + [n_m^-, n_m^+]s^m}{[d_0^-, d_0^+] + [d_1^-, d_1^+]s + \dots + [d_n^-, d_n^+]s^n}
\tag{14}
$$

where the numerator, $N(s)$, and the denominator, $D(s)$, are interval polynomials having fixed integer degrees m and n, respectively, with the constraint that $n > m$. The real values of n_i^-, n_i^+, d_j^- and d_j^+ with $i = 0, 1, 2, \dots, m$ and $j = 0, 1, 2, \dots, n$, are the lower and upper limits of each coefficient of the interval plant (14), defining the range of variation of each uncertain coefficient.

Since $N(s)$ and $D(s)$ are both interval polynomials, hence, four Kharitonov polynomials are associated for $N(s)$ (15) and other four Kharitonov polynomials for $D(s)$ (16).

$$
\begin{aligned}
K_N^{(1)}(s) &= n_0^- + n_1^- s + n_2^+ s^2 + n_3^+ s^3 + \dots \\
K_N^{(2)}(s) &= n_0^- + n_1^+ s + n_2^+ s^2 + n_3^- s^3 + \dots \\
K_N^{(3)}(s) &= n_0^+ + n_1^- s + n_2^- s^2 + n_3^+ s^3 + \dots \\
K_N^{(4)}(s) &= n_0^+ + n_1^+ s + n_2^- s^2 + n_3^- s^3 + \dots
\end{aligned}
\tag{15}
$$

$$
\begin{aligned}
K_D^{(1)}(s) &= d_0^- + d_1^- s + d_2^+ s^2 + d_3^+ s^3 + \dots \\
K_D^{(2)}(s) &= d_0^- + d_1^+ s + d_2^+ s^2 + d_3^- s^3 + \dots \\
K_D^{(3)}(s) &= d_0^+ + d_1^- s + d_2^- s^2 + d_3^+ s^3 + \dots \\
K_D^{(4)}(s) &= d_0^+ + d_1^+ s + d_2^- s^2 + d_3^- s^3 + \dots
\end{aligned}
\tag{16}
$$

C. EXTREMAL SET AND POLYNOMIAL SEGMENT

Given two polynomials $X^{(1)}(s)$ and $X^{(2)}(s)$, a polynomial segment, here denoted by $[X^{(1)}(s), X^{(2)}(s)]$, is a family of polynomial generated by the following convex combination

$$
[X^{(1)}(s), X^{(2)}(s)] = \left\{ \lambda X^{(1)}s + (1-\lambda)X^{(2)}s \right\}
\tag{17}
$$

where $\lambda \in [0, 1]$

Given three polynomials $N^{(1)}(s)$, $N^{(2)}(s)$, and $D(s)$, a line segment of plants is defined by following ratio of a polynomial segment $[N^{(1)}(s), N^{(2)}(s)]$ divided by a fixed polynomial $D(s)$.

$$
G^{(1,2)}(s) = \frac{[N^{(1)}(s), N^{(2)}(s)]}{D(s)}
\tag{18}
$$

Conversely, given three polynomials $N(s)$, $D^{(1)}(s)$, $D^{(2)}(s)$, define an *arc segment* of plants in the form of the following ratio of a fixed polynomial $N(s)$ divided by a segment polynomial $[D^{(1)}(s), D^{(2)}(s)]$.

$$
G_{(1,2)}(s) = \frac{N(s)}{[D^{(1)}(s), D^{(2)}(s)]}
\tag{19}
$$

Bhattacharyya and co-authors [28] recently proved that, for analysis and synthesis of control systems such interval plant model (14), it is sufficient to consider a set comprised of 32 plant segments, named extremal set of the interval plant $G(s)$, as follow (with $\lambda \in [0, 1]$)

Line Segments:

$$
G_1(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(2)}(s)]}{K_D^{(1)}(s)}, \quad G_2(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(3)}(s)]}{K_D^{(1)}(s)}
$$

$$
G_3(\lambda, s) = \frac{[K_N^{(2)}(s), K_N^{(4)}(s)]}{K_D^{(1)}(s)}, \quad G_4(\lambda, s) = \frac{[K_N^{(3)}(s), K_N^{(4)}(s)]}{K_D^{(1)}(s)}
$$

$$
G_5(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(2)}(s)]}{K_D^{(2)}(s)}, \quad G_6(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(3)}(s)]}{K_D^{(2)}(s)}
$$

$$
G_5(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(2)}(s)]}{K_D^{(2)}(s)}, \quad G_6(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(3)}(s)]}{K_D^{(2)}(s)}
$$

$$
G_7(\lambda, s) = \frac{[K_N^{(2)}(s), K_N^{(4)}(s)]}{K_D^{(2)}(s)}, \quad G_8(\lambda, s) = \frac{[K_N^{(3)}(s), K_N^{(4)}(s)]}{K_D^{(2)}(s)}
$$

$$
G_9(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(2)}(s)]}{K_D^{(3)}(s)}, \quad G_{10}(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(3)}(s)]}{K_D^{(3)}(s)}
$$

$$
G_{11}(\lambda, s) = \frac{[K_N^{(2)}(s), K_N^{(4)}(s)]}{K_D^{(3)}(s)}, \quad G_{12}(\lambda, s) = \frac{[K_N^{(3)}(s), K_N^{(4)}(s)]}{K_D^{(3)}(s)}
$$

$$
G_{13}(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(2)}(s)]}{K_D^{(4)}(s)}, \quad G_{14}(\lambda, s) = \frac{[K_N^{(1)}(s), K_N^{(3)}(s)]}{K_D^{(4)}(s)}
$$

$$
G_{15}(\lambda, s) = \frac{[K_N^{(2)}(s), K_N^{(4)}(s)]}{K_D^{(4)}(s)}, \quad G_{16}(\lambda, s) = \frac{[K_N^{(3)}(s), K_N^{(4)}(s)]}{K_D^{(4)}(s)}
\tag{20}
$$

Line Segments:

$$
G_{17}(\lambda, s) = \frac{K_N^{(1)}(s)}{[K_D^{(1)}(s), K_D^{(2)}(s)]}, \quad G_{18}(\lambda, s) = \frac{K_N^{(2)}(s)}{[K_D^{(1)}(s), K_D^{(2)}(s)]}
$$

$$G_{19}(\lambda,s) = \frac{K_N^{(3)}(s)}{\left[K_D^{(1)}(s), K_D^{(2)}(s)\right]}, \quad G_{20}(\lambda,s) = \frac{K_N^{(4)}(s)}{\left[K_D^{(1)}(s), K_D^{(2)}(s)\right]}$$

$$G_{21}(\lambda,s) = \frac{K_N^{(1)}(s)}{\left[K_D^{(1)}(s), K_D^{(3)}(s)\right]}, \quad G_{22}(\lambda,s) = \frac{K_N^{(2)}(s)}{\left[K_D^{(1)}(s), K_D^{(3)}(s)\right]}$$

$$G_{23}(\lambda,s) = \frac{K_N^{(3)}(s)}{\left[K_D^{(1)}(s), K_D^{(3)}(s)\right]}, \quad G_{24}(\lambda,s) = \frac{K_N^{(4)}(s)}{\left[K_D^{(1)}(s), K_D^{(3)}(s)\right]}$$

$$G_{25}(\lambda,s) = \frac{K_N^{(1)}(s)}{\left[K_D^{(2)}(s), K_D^{(4)}(s)\right]}, \quad G_{26}(\lambda,s) = \frac{K_N^{(2)}(s)}{\left[K_D^{(2)}(s), K_D^{(4)}(s)\right]}$$

$$G_{27}(\lambda,s) = \frac{K_N^{(3)}(s)}{\left[K_D^{(2)}(s), K_D^{(4)}(s)\right]}, \quad G_{28}(\lambda,s) = \frac{K_N^{(4)}(s)}{\left[K_D^{(2)}(s), K_D^{(4)}(s)\right]}$$

$$G_{29}(\lambda,s) = \frac{K_N^{(1)}(s)}{\left[K_D^{(3)}(s), K_D^{(4)}(s)\right]}, \quad G_{30}(\lambda,s) = \frac{K_N^{(2)}(s)}{\left[K_D^{(3)}(s), K_D^{(4)}(s)\right]}$$

$$G_{31}(\lambda,s) = \frac{K_N^{(3)}(s)}{\left[K_D^{(3)}(s), K_D^{(4)}(s)\right]}, \quad G_{32}(\lambda,s) = \frac{K_N^{(4)}(s)}{\left[K_D^{(3)}(s), K_D^{(4)}(s)\right]} \tag{21}$$

By using the 32 plant segments defined in (20) and (21), calculated for $s = j\omega$, in a given frequency point ω, a suitable template of parametric uncertainties can be generated in the complex plane of the loop transfer function. In Fig.3, it is presented a polynomials segments family for the interval parameters given in Table 1 and for frequency $\omega = 1.0$ rad/s. Therefore, extended frequency domains tools, such as Nyquist and Bode diagrams can be used, allowing the analysis and design of robust controllers taking into account parametric uncertainties.
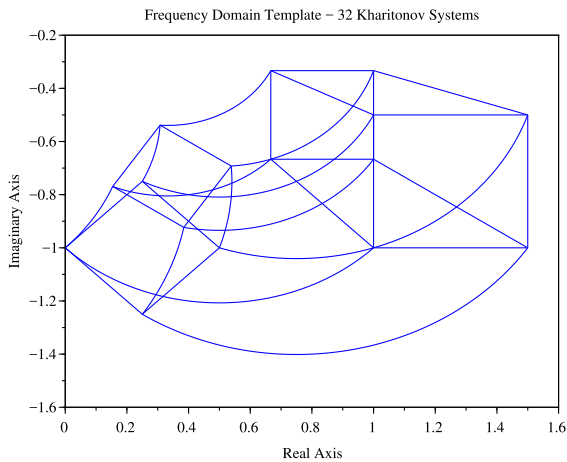
FIGURE 3. Frequency domain template $G(j\omega)$ at $\omega = 1.0$ rad/s.

IV. BACKGROUND OF FREQUENCY-DOMAIN METHODOLOGY

In this paper, the proposed controller is represented in the Lead-Lag structure and the parameters are designed considering the performance desired in closed-loop in the gain crossover frequency, ω_{gc}. The controller and the parameters are given by:

$$LL(s) = K_c \frac{Ts + 1}{\alpha Ts + 1}. \tag{22}$$

where, T, α and K_c are the controller parameters. Note that T and α define the pole and zero of the controller, and K_c is the controller gain. Such parameters are designed considering the gain and phase margins desired [29].

A. CLASSICAL DESIGN METHOD OF LEAD-LAG CONTROLLER

The controller design method based on the frequency-domain considering a plant of fixed parameters $G(s)$, aims to satisfy a closed-loop performance to a desired phase and gain margin, φ_m and A_m, respectively. Let $L(s) = LL(s)G(s)$ be the loop transfer function, thus, the phase condition Eq. (23) defines the poles and zeros of the Lead-Lag controller $LL(s)$,

$$\angle L(j\omega_{gc}) = \angle LL(j\omega_{gc}) + \angle G(j\omega_{gc}) = \pi + \varphi_m \tag{23}$$

where:

- $\angle LL(j\omega_{gc})$ is the phase compensation of the Lead-Lag controller at the gain crossover frequency, ω_{gc};
- $\angle G(j\omega_{gc})$ is the phase angle of the plant at the gain crossover frequency, ω_{gc};
- φ_m is the desired phase margin.

Using the phase condition defined in Eq. (23), the parameters, α and T, of the Eq. (22), can be obtained by following relations,

$$\alpha = \sqrt{\frac{1 - \sin(\phi_c)}{1 + \sin(\phi_c)}} \tag{24}$$

$$T = \frac{1}{\omega_{gc}\sqrt{\alpha}} \tag{25}$$

where, $\phi_c = \angle LL(j\omega_{gc})$.

On the other hand, the module condition of the Lead-Lag controller $LL(s)$, at the gain crossover frequency, ω_{gc}, is given by

$$\left|G(j\omega_{gc})\right| \left|LL(j\omega_{gc})\right| = 1 \tag{26}$$

where:

- $\left|G(j\omega_{gc})\right|$ is the module of the plant at the gain crossover frequency, ω_{gc};
- $\left|LL(j\omega_{gc})\right|$ is the module of the controller Lead-Lag at the gain crossover frequency, ω_{gc}. And based on Eq. (23) it is possible to represent Eq. (26) as

$$K_c = \frac{1}{\left|G(j\omega_{gc})\right| \left|LL(j\omega_{gc})\right|} \tag{27}$$

where:

- K_c is the Lead-Lag controller gain at the gain crossover frequency, ω_{gc};
- $\left|LL(j\omega_{gc})\right|$ become only the module of the Lead-Lag part (poles and zeros) at the gain crossover frequency, ω_{gc}, and is given by,

$$|LL(j\omega_{gc})| = \sqrt{\frac{1 + (\omega_{gc}T)^2}{1 + (\omega_{gc}\alpha T)^2}} \qquad (28)$$

where α and T are the Lead-Lag controller parameters, calculated by Eqs. (24) and (25); and ω_{gc} is gain crossover frequency desired.

B. ANALYSIS OF THE LINEAR SMALL-SIGNAL AVERAGED MODEL OF THE BUCK CONVERTER WITH INTERVAL PARAMETRIC UNCERTAINTIES

The classical methodology to design controllers is based in the controller parameter tuning using a fixed parameters system model. Thus, it is common to use nominal models to tune the controller. However, the real system is subjected to parametric uncertainties, and, therefore, the controller must ensure system stability and desired minimum performance for all kinds of transfer functions that represent the whole set of uncertainties. Thereby, when the small-signal model of the Buck converter in (10) is subjected to uncertainties parametric, it becomes an interval plant, given by

$$G(s) = \frac{[n_0{}^-, n_0{}^+]}{s^2 + [d_1^-, d_1^+]s + [d_2^-, d_2^+]}, \qquad (29)$$

where, the nominal parameters of interval plant (29) are: $n_o = \frac{V_s}{LC}$, $d_1 = \frac{1}{R_L C}$, and $d_2 = \frac{1}{LC}$. Note that the lower- and upper-bound of each parameter is limited by the box region of uncertainties (cf. Table 1), where the root locus for the poles of the interval polynomial of (29) is presented in Fig. 4.
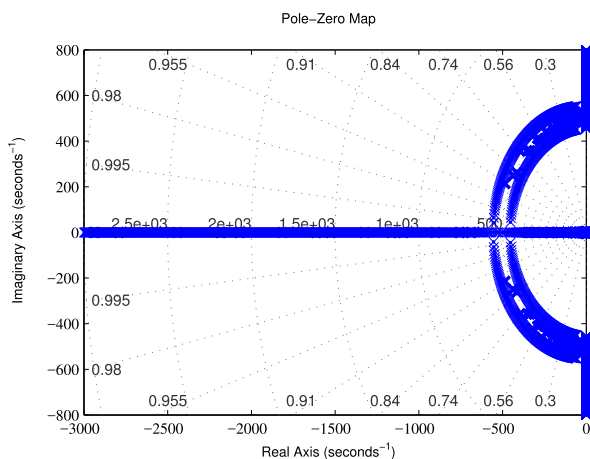

FIGURE 4. Root-Locus for the poles of the interval parameters of the buck converter.

According to [28], a interval plant (29) generates an extreme set with 32 interval plants of Kharitonov. Fig. 4 shows the poles of the interval plant (29) for all plants of Kharitonov delimited by the region of uncertainties.

To evaluate the frequency-domain response, Nyquist diagram of the nominal plant, Eq. (10), is presented in Fig. 5(a) and Nyquist diagram of the interval plant, Eq. (29), for 32 interval plants of Kharitonov is presented in Fig. 5(b).

The boundaries of the extremal set of $G(s)$ (c.f. Fig. 5(b)) are defined by the border transfer functions of the extremal
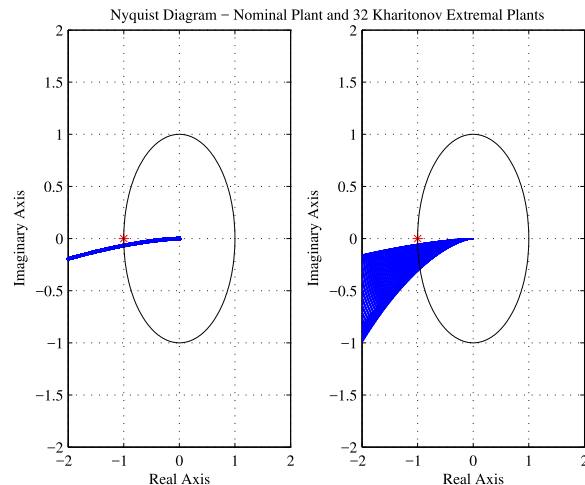
FIGURE 5. Nyquist diagram for a) Nominal plant b) Extremal set.

set of $G(s)$. Therefore, the robust controller design is based on the constrains of the gain and/or phase margins for the limits of this uncertainties region, defined as the "worst case".

According to [28], the controller is considered robustly stable for the transfer functions set of the extremal set, if the Nyquist diagram of the loop transfer function to satisfy the performance criteria predefined for the "worst case".

C. ROBUST DESIGN METHOD OF LEAD-LAG CONTROLLER

The proposed methodology for robust controller design using extremal analysis must meet the design performance criteria of the extremal set for the transfer function family of $G(s)$. As mentioned above, if the controller meets the design performance criteria for the "worst case" of the $G(s)$ transfer function family, the controller will be robustly stable for all transfer function family of $G(s)$. Hence, the proposed robust controller is designed for the "worst case" of the $G(s)$ transfer function family (29).

For the experiments tests, a controller in the Lead-Lag structure was selected (22). Whose controller parameters were calculated by (30), (31) and (32).

$$\alpha = \frac{1 - \sin\phi_c}{1 + \sin\phi_c} \qquad (30)$$

$$T = \frac{1}{\omega_{gc}\sqrt{\alpha}} \qquad (31)$$

$$K_c = \frac{1}{|G(j\omega_{gc})|}\sqrt{\frac{1 + (\alpha T\omega_{gc})^2}{1 + (T\omega_{gc})^2}} \qquad (32)$$

In order to design the robust controller, the first requirement is to define settling time to regulate the output of the dc-dc buck converter: the settling time value (t_r) chosen was 15 times less than $t_r = 0.00314$s, that represents the settling time value of the open-loop plant. A heuristic relation was defined in Ho [30], in which the product of the bandwidth value by the settling time value is approximately constant and equal to 0.9.

$$\omega_{gc}\, t_r = 0.9 \qquad (33)$$

Thus, from (31) the gain crossover frequency value corresponding to the desired settling time is $\omega_{gc} = 4312$ rad/s. This relation defines the closed-loop desired performance.

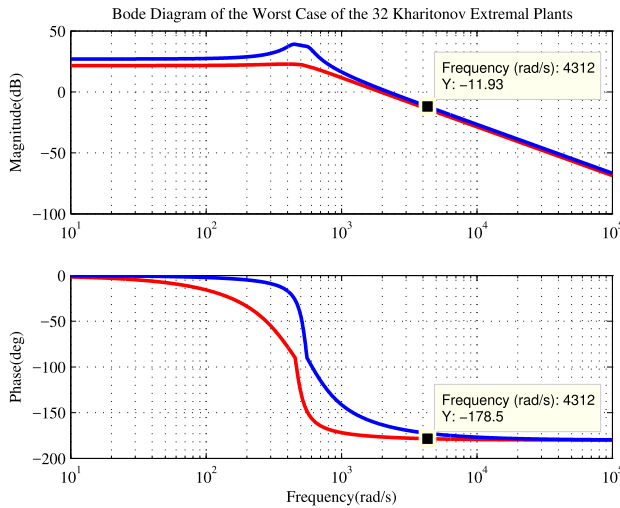Fig. 6 represents the Bode diagram of the Loop transfer function.

FIGURE 6. Bode Diagram of the Loop Transfer Function $L(j\omega gc) = G(j\omega gc)$.

Notice that the lower and upper limits of the magnitude and phase curves of the Loop transfer function ($L(s)$), correspond to the limits that delimit the function family of $G(s)$ considering the parametric uncertainties.

From Fig. 6, the desired gain crossover frequency value $\omega_{gc} = 4312$ rad/s defines, in the phase bode diagram, the phase margin of the open-loop $G(s)$ plant for the "worst case", which is $\angle G(j\omega_{gc}) = -178.5° = 3.11$ rad.

The desired phase margin is added to the phase margin of the plant for the "worst case", the value obtained corresponds to the advance provided by the Lead-Lag part of the controller. From [29], the desired phase margin considering the desired relative damping, $\xi_d = 0.3$, is $\varphi_m = 35°$, and using equation (23) in degrees, it is obtained:

$$\angle LL(j\omega_{gc}) = 180° + \varphi_m - \angle G(j\omega_{gc}),$$
$$\angle LL(j\omega_{gc}) = 393.5° - 360° = 33.5°. \quad (34)$$

where 360° corresponds to the surplus that must be subtracted to exposed the true value of the phase to be must compensated by Lead-Lag controller.

Thereby, the positive value of the phase compensation given by controller in (32), corresponds to a lead of 33.5° in the desired gain crossover frequency, providing a threshold phase margin for the "worst case" of $\phi_c = 35°$ or $\phi_c = 0.5847$ rad. And the controller parameters α and T can be calculated using (28) and (29), as follows:

$$\alpha = \frac{1 - \sin(0.5847)}{1 + \sin(0.5847)} = 0.2887,$$

$$T = \frac{1}{\omega_{gc}\sqrt{\alpha}} = 0.43288 \text{ ms.}$$

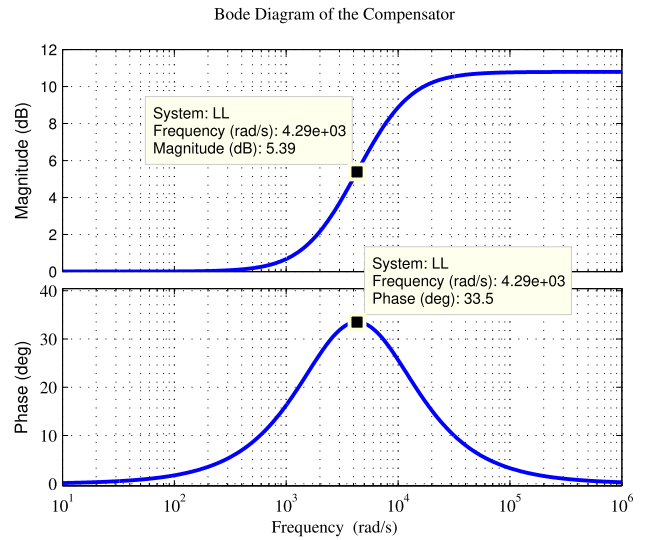The phase lead given by the controller in the Lead-Lag structure is shown in Fig. 7.

FIGURE 7. Bode Diagram Lead-Lag Compensator ($C(j\omega gc)$).

Defined the phase compensation of the Lead-Lag parcel in (24). Then the module condition must be satisfied as follows using (30):

$$K_c = \frac{1}{\left|G(j\omega_{gc})\right|\left|C(j\omega_{gc})\right|} = 2.1219,$$

where

$$\left|C(j\omega_{gc})\right| = \sqrt{\frac{1 + (\omega_{gc}T)^2}{1 + (\omega_{gc}\alpha T)^2}} \approx 5.3953 \text{ dB} \approx 1.8611,$$

$$\left|G(j\omega_{gc})\right| = -11.93 \text{ dB} \approx 0.2532.$$

The $\left|G(j\omega_{gc})\right|$ module and the $\left|C(j\omega_{gc})\right|$ module, can be obtained from Figs. 6 and 7 for the new gain crossover frequency ω_{gc}, whose values obtained by graphic analysis were $\left|G(j\omega_{gc})\right| = 11.93$ and $\left|C(j\omega_{gc})\right| = 5.39$.

Fig. 8 shows the Bode diagram for the Loop transfer function with the designed compensator.

Notice that the desired phase margin to the worst case (cf. Fig. 8) is reached at the gain crossover frequency. Thereby, according [28], it is concluded that the designed controller is robustly stable, meeting the performance criteria in the range of parametric uncertainties of the extremal set of $G(s)$.

Fig. 9 represents the Nyquist diagram of the loop transfer function $L(s)$. Analysing the Nyquist diagram, it is observed that the minimum phase margin is reached at a point on the extremal set that correspond to the "worst case" of the loop transfer function set. In this case, the desired phase margin of 35° was reached and satisfied the worst case criterion, and as discussed in [28], the controller designed is robustly stable.

Finally, an integrator is added into the Lead-Lag controller structure to ensure zero steady-state error. Thereby, the controller design process ends resulting in the following
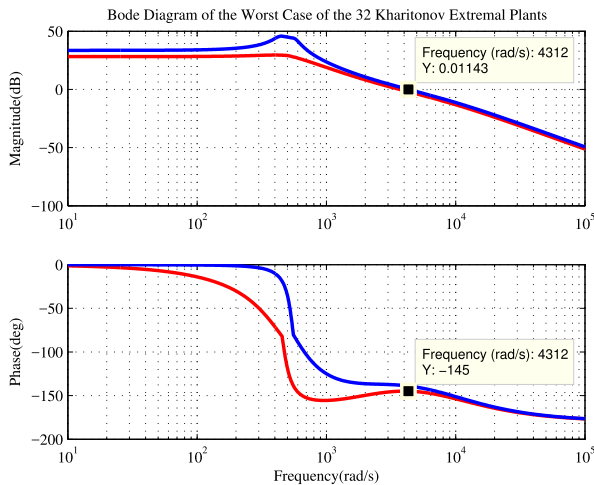
FIGURE 8. Bode Diagram Loop Transfer Function $L(j\omega gc) = G(j\omega gc)C(j\omega gc)$.
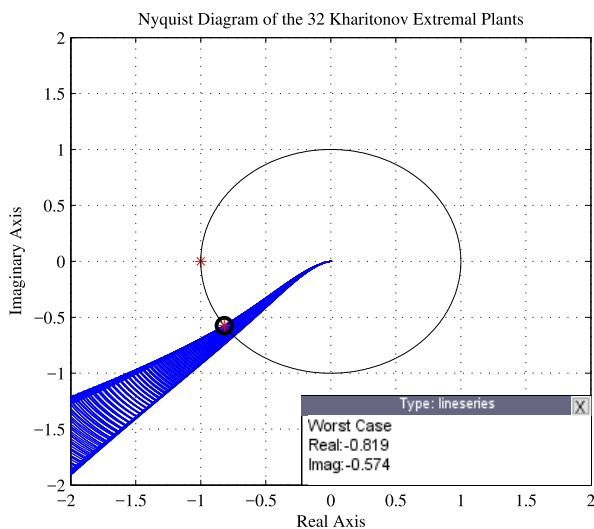
FIGURE 9. Nyquist Diagram Loop Transfer Function $L(j\omega gc) = G(j\omega gc)C(j\omega gc)$.

controller structure (35).

$$C(s) = \frac{1}{s}LL(s) = \frac{K_{LL}}{s}\left(\frac{Ts+1}{\alpha Ts+1}\right) \qquad (35)$$

D. IMPLEMENTATION OF THE PROPOSED ROBUST CONTROL METHODOLOGY

The flowchart of the proposed control implementation is depicted in Fig. 10.

The proposed control design process is summarized as follows: In step 1, the box region of uncertainties is built based on a previously specified uncertainty range delimited by the designer. The lower-and upper-bound of each parameter are provided in Table 1. In step 2, the phase margin of the open-loop transfer function for the "worst case" analysing the extremal Bode diagram (cf. Fig. 6). After that, the desired phase margin φ_m is chosen (step 3) to satisfy

the "worst case" condition. In step 4, the Lead-Lag phase compensation is calculated by using the relationship defined in (23). Then, the Lead-Lag controller parameters, α and T, are tuned using the relationship defined in Eqs. (30) and (31), respectively (step 5). The Lead-Lag controller gain, K_{LL} (32), is computed using the modulus condition (26) in step 6. The phase condition for the "worst case" is verified in step 7, in case of achieving it, advance to step 8, if not, go back to step 3, where the desired phase margin must be redefined. After that, the Lead-Lad controller, $LL(s)$, is tuned (step 8). In order to ensure zero steady-state error, an integrator is added into the Lead-Lag controller structure (step 9). Aim to obtain a discrete equivalent controller the Tustin Method is used (Step 10) to perform the discrete approximation. Finally, step 11 presents the generic form for obtaining the discrete gains of the digital controller to be implemented.

V. RESULTS ANALYSIS

This section presents and discusses the main results of the tests described in the next subsections, aiming to evaluate the control performance of the proposed controller in comparison with a robust controller, proposed by Keel and S. P. Bhattacharyya [31], and a classical controller based on pole-placement methodology, proposed by Aström [32].

These experiments aim to show that the proposed robust controller is able to better compensates for the oscillations caused by parametric uncertainties (load and input voltage variations). In addition to ensuring better reference tracking.

All the experiments are performed with simulations in Matlab/Simulink. Moreover, a dc-dc buck converter system board is developed, as shown in Fig. 11, in order to validate the theoretical claims. The controller has been implemented by using a 32-bit ARM core microcontroller AT91SAM3×8E (cf. Fig. 11). The desired set point values are provided by a microcomputer system via USB communication.

A. SETPOINT VOLTAGE VARIATION

In order to evaluate the controller performance for different operating condition of voltage reference (V_{ref}), the dc-dc buck converter system is subjected to different operating condition after achieving its nominal operating point (cf. Table 1). Thereby, a reference voltage variation (ΔV_{ref}) is performed (t = 3.0s) within amplitude range from 1 to 4 V.

Fig. 12 shows the simulated and experimental responses performed in the dc-dc buck converter with variations in the voltage reference (V_{ref}) under the three control approaches where sub-figures A1, B1, C1 and D1 refer to the simulation tests and sub-figures A2, B2, C2 and D2 refer to the practical tests.

The simulated results show that, for the proposed robust controller, the voltage overshoot is very small, thus ending in fast voltage tracking compared to the other control approaches. The experimental results again confirm the superior performance of the proposed robust controller in the regulation over the voltage reference.
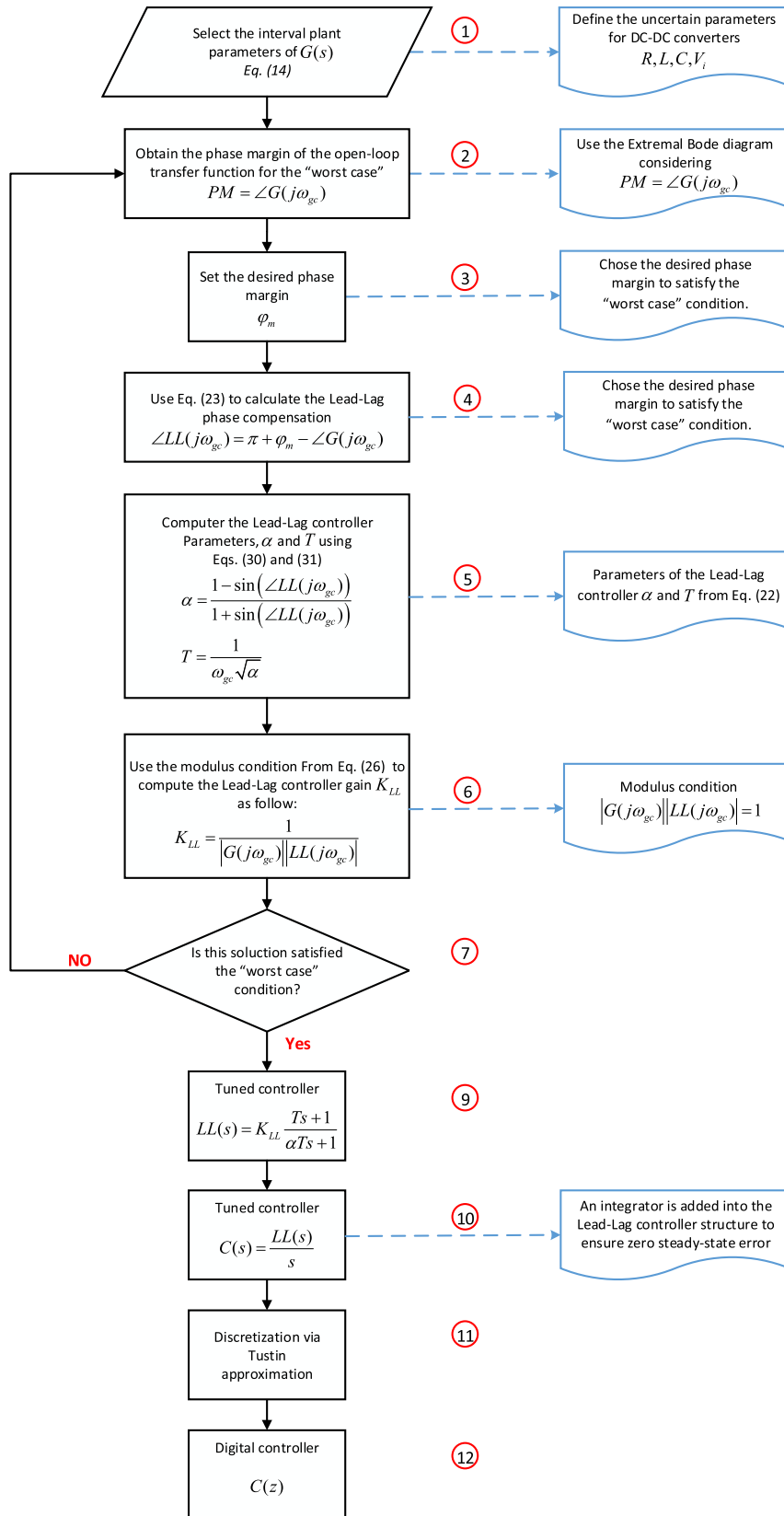
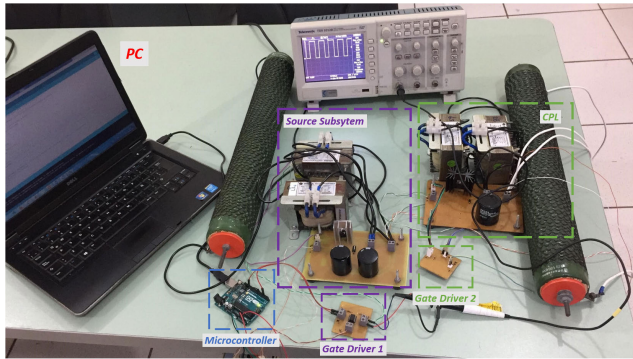**FIGURE 10.** Flowchart of the robust controller design methodology.
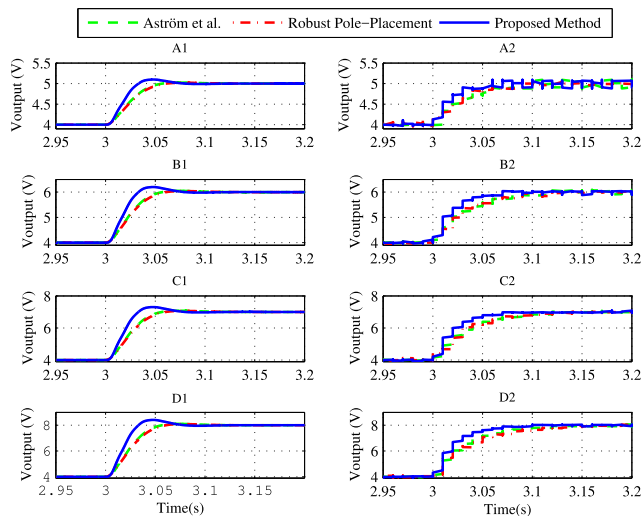
FIGURE 11. DC-DC buck converter board developed.

FIGURE 12. Reference Voltage Variation ΔV_{ref}. (A) $\Delta V_{ref} = 1V$; (B) $\Delta V_{ref} = 2V$; (C) $\Delta V_{ref} = 3V$; (D) $\Delta V_{ref} = 4V$.

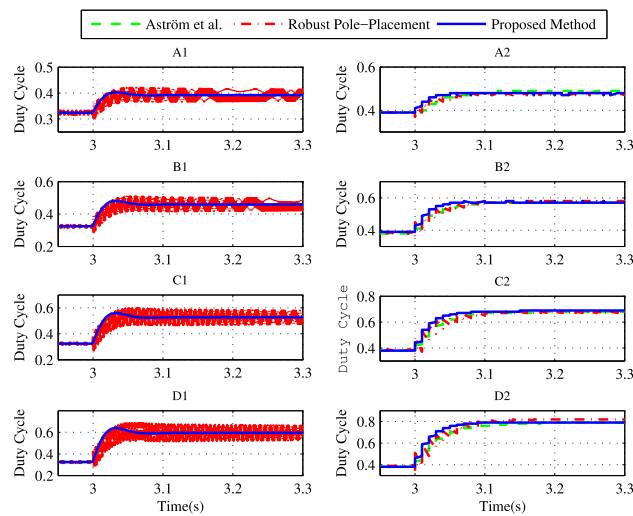**FIGURE 13.** Control Signal for the Reference Voltage Variation Test ΔV_{ref}. (A) $\Delta V_{ref} = 1V$; (B) $\Delta V_{ref} = 2V$; (C) $\Delta V_{ref} = 3V$; (D) $\Delta V_{ref} = 4V$.

Fig. 13 shows the duty cycle control for this experiment under the three control approaches. Note that the saturation of the control signal does not occur at any time. The controller

efforts of the evaluated controllers is almost similar under variations in the operation voltage, according to the simulated and experimental results (cf. Fig. 13).

Therefore, all controllers are able to track the reference voltage, meeting the pre-established performance requirements, however, the proposed robust controller achieves better performance with fast response in comparison with other controllers.

B. DC INPUT VOLTAGE VARIATION

In this subsection, the dc-dc buck converter is subjected to a variation in the input dc voltage (V_s), within amplitude range from 1 to 4 V, after achieving its nominal operation point. Note that the closed-loop characteristic polynomial depends on plant parameters (V_s, L, C, R_L, see Eq. (10)) and controller parameters, thus, changing one of these parameters modifies the closed-loop poles of the system. Thereby, it is justified the robust controller design strategy based on parametric uncertainties to enhance the performance of the dc-dc buck converter under input voltage variation.
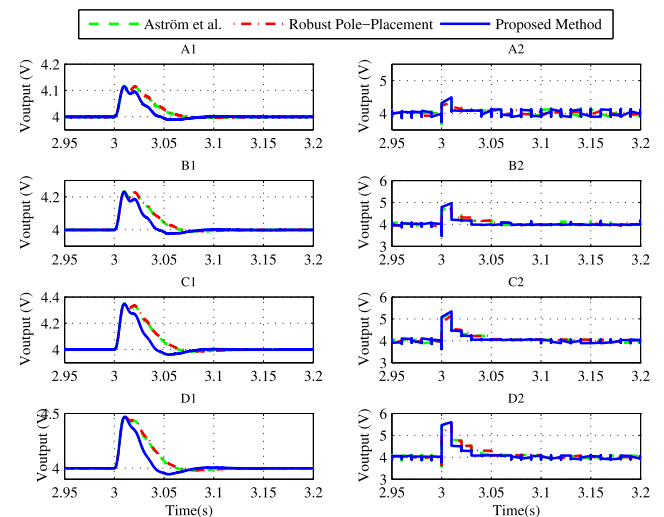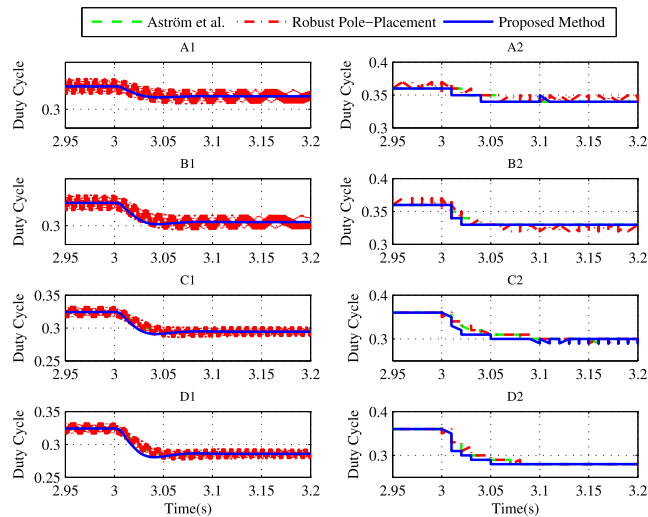

FIGURE 14. Input Voltage Variation ΔV_s. (A) $\Delta V_s = 1V$; (B) $\Delta V_s = 2V$; (C) $\Delta V_s = 3V$; (D) $\Delta V_s = 4V$.

Fig. 14 shows the simulated and experimental results of closed-loop system performance for input voltage variation under the three control approaches where sub-figures A1, B1, C1 and D1 refer to the simulation tests and sub-figures A2, B2, C2 and D2 refer to the practical tests. After the system reaches its steady state, some variations in the input voltage (V_s) are performed (t = 3.0s) with amplitudes of 1V, 2V, 3V, and 4V, respectively, as shown in sub-figures A, B, C and D, respectively (cf. Fig. 14).

The simulated results (see sub-figures A1, B1, C1 and D1) show that the proposed controller more effectively compensates the oscillations caused by input voltage variations reducing the oscillation amplitude and settling time in comparison with other control approaches. The effectiveness and robustness of the proposed robust controller is ratified in the

experimental results (see sub-figures A2, B2, C2 and D2) where, for larger perturbation in the input voltage source, the proposed control methodology outperforms the other control approaches. Therefore, the impact of input voltage variation is lower for the proposed robust controller.

Fig. 15 shows the duty cycle control signal for variation of the input voltage source under the three control approaches. The saturation of the control signal did not occur in any of the evaluated methods, preserving the integrity of the switching circuit and, consequently, the operation of the controllers.

FIGURE 15. Control Signal for the Input Voltage Variation ΔV_S.
(A) $\Delta V_S = 1V$; (B) $\Delta V_S = 2V$; (C) $\Delta V_S = 3V$; (D) $\Delta V_S = 4V$.

C. LOAD RESISTANCE VARIATION

In this subsection, the dc-dc buck converter is subjected to a variation in the load resistance (R_L), after achieving its nominal operation point. Each test resistance variation is achieved by combining up to four parallel resistances of 4.0 Ω each. Considering the nominal value of the load resistance equal $R_L = 4.0$ Ω (cf. Table 1), the experiments are performed to a variation in the load resistance value for $R_L = 2.0$ Ω, 1.33 Ω and 1.0 Ω.

Fig. 16 shows the simulated and experimental results of closed-loop system performance for load variation under the three control approaches where sub-figures A1, B1, C1 and D1 refer to the simulation tests and sub-figures A2, B2, C2 and D2 refer to the practical tests.

All controllers achieve the desired performance requirement, ensuring system stability and null regime error for the load resistance variation test. The transient response seems to be almost similar for both simulated and experimental results, however, for larger variation in the load resistance (R_L), the proposed robust controller outperforms the other controllers, reducing the oscillation amplitude in comparison with faster transient, as shown in sub-figure C2 (cf. Fig 16).

Fig. 17 present the duty cycle control signal for this case. Note that the control signals of the simulated model do not
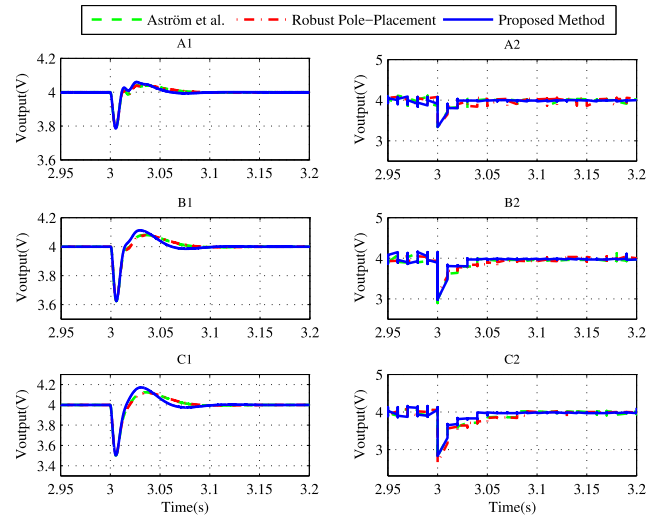
FIGURE 16. Load Resistance Variation ΔR_L. (A) $\Delta R_L = 2\Omega$; (B) $\Delta R_L = 1.33\Omega$; (C) $\Delta R_L = 1\Omega$.
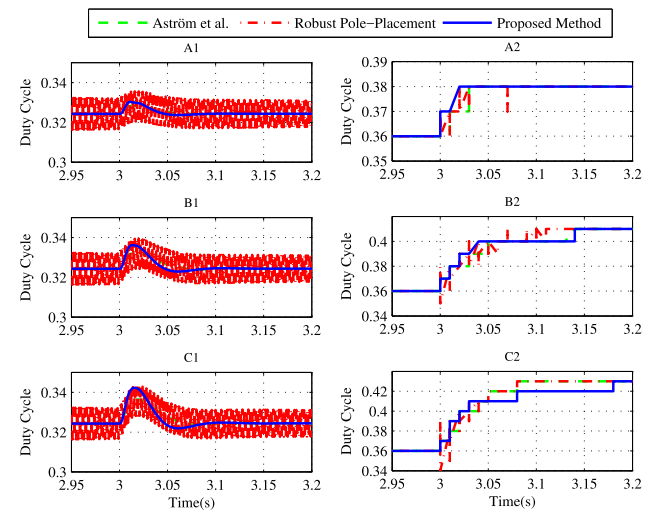
FIGURE 17. Control Signal for Load Resistance Variation ΔR_L.
(A) $\Delta R_L = 2\Omega$; (B) $\Delta R_L = 1.33\Omega$; (C) $\Delta R_L = 1\Omega$.

correspond faithfully to the results obtained of the control signals in the experimental tests. This behavior can be justified by the fact that the simulated nonlinear model does not observe all the dynamics of the real system. However, the main observation to be made is the fact that in none of the load variation cases there was control signal saturation.

D. PERFORMANCE INDEX ANALYSIS

In order to perform a quantitative evaluation of the evaluated control design methodologies for the aforementioned tests, the Integral of Squared Error (ISE) and the Integral of Square Control Signal (ISCS) are used as a metric of performance indexes.

Fig. 18 shows the ISE index performance for voltage setpoint variation (sub-figure A1 and A2), input voltage variation (sub-figure B1 and B2) and load resistance variation (sub-figure C1 and C2) tests, respectively, where sub-figures A1, B1, C1 and D1 refer to the simulation tests and sub-figures A2, B2, C2 and D2 refer to the practical tests.
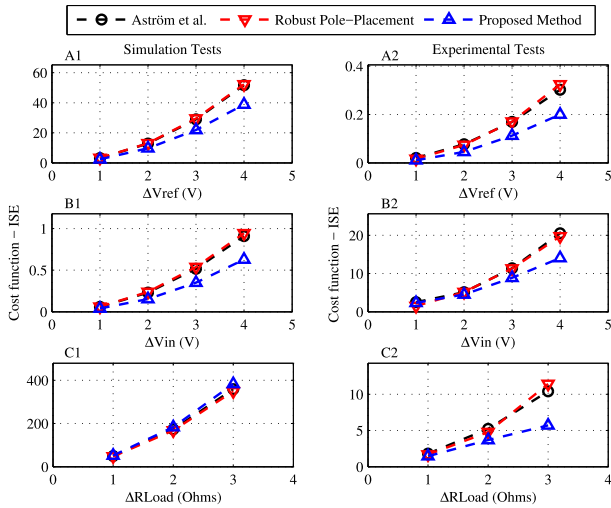
FIGURE 18. Integral of Squared Error (ISE). (A) ΔV_{ref}; (B) ΔV_{in}; (C) ΔR_L.

The ISE index performance ratifies the effectiveness of the proposed robust controller for tracking reference for both simulated and experimental tests (see sub-figures A1 and A2).

For the input voltage variation test, the control system performance is enhance when the buck converter is regulated by the proposed robust controller according to the ISE index performance, as shown in sub-figures B1 and B2 (cf. Fig. 18). Therefore, the impact of input voltage variation is lower for the proposed robust controller controller.

In the simulation case of the load resistance variation test, the control system performance is almost similar for the three control approaches. However, for the experimental case, the proposed robust controller presents a minor performance degradation, being more evident for large load variations. These claims are ratifying by the ISE index performance in sub-figures C1 and C2 (cf. Fig. 18).
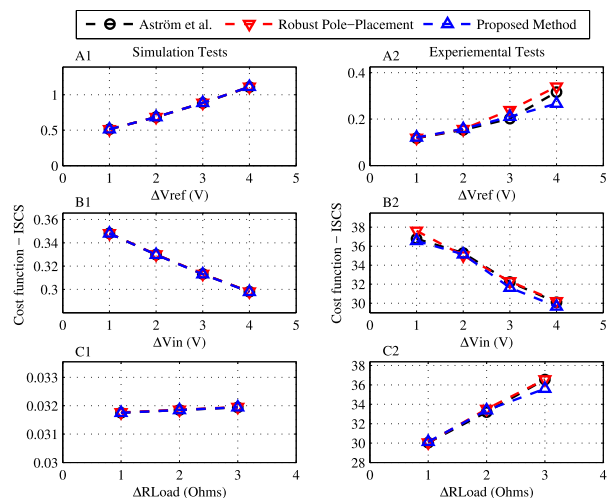

FIGURE 19. Integral of Square Control Signal (ISCS). (A) ΔV_{ref}; (B) ΔV_{in}; (C) ΔR_L.

Fig. 19 presents the ISCS index performance for voltage setpoint variation (sub-figure A1 and A2), input voltage

variation (sub-figure B1 and B2) and load resistance variation (sub-figure C1 and C2) tests, respectively, where sub-figures A1, B1, C1 and D1 refer to the simulation tests and sub-figures A2, B2, C2 and D2 refer to the practical tests. Notice that the proposed robust controller ensure the lowest energy effort, mainly in the region outside the nominal operating point, as shown in sub-figures A2, B2 and C2 (cf. Fig. 19).

VI. CONCLUSION

This paper addresses a control approach for designing fixed order robust controller based on frequency-domain, to enhance the performance of dc-dc power converters.

The proposed control approach reduces the impact of the parametric uncertainties in dc-dc power converter systems, ensuring robust stability and robust performance for an entire predefined uncertainty region.

The proposed control methodology has been exhaustively evaluated in both computational simulations as well as by means of experiments performed in a 20 W dc buck converter. The proposed robust controller performance is compared with a classical controller based on pole-placement and a robust controller based on Kharitonov Theorem.

For both simulated and experimental results, the proposed controller shows a better dynamic behavior, such as minor overshoot and fast transient response. Moreover, the performance indicators comparison show that the proposed controller more effectively compensates for disturbances offering robust performance and stability, ensuring the desired performance.

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