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Optimized Space-Vector Modulation to Reduce Neutral Point Current for Extending Capacitor Lifetime in Three-Level Inverters

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ABSTRACT In this paper, an optimized space-vector modulation (SVM) to reduce DC-link ripple current in three-level inverters is presented. Various types of capacitors can be utilized to balance the voltage in the DC-link of voltage source inverters. Electrolytic capacitors are widely used owing to their large capacitance per volume. However, electrolytic capacitors have a short lifespan because the allowable ripple current is low. A conventional SVM that is focused on improving harmonic characteristics. Therefore, it cannot balance the DC-link ripple current properly because using some voltage vectors increases the DC-link ripple current. To overcome this limitation and extend the lifespan of the capacitors, an optimized SVM is proposed to reduce the DC-link ripple current. The proposed modulation scheme synthesizes the reference voltage by choosing voltage vectors that cause smaller increases in the DC-link ripple current, avoiding those that cause larger increases. The effectiveness of the proposed optimized SVM is verified by simulations and experimental results.

INDEX TERMS Three-level inverter, dc-link ripple current, capacitor, space-vector modulation, reliability.

I. INTRODUCTION

Currently, voltage source inverters (VSIs) are widely used in renewable energy generation systems and motor drives because they have high efficiency, low harmonic content, and high power factor [1]. VSIs are typically classified as two- or multi-level inverters [2]. Three-level inverters are frequently utilized as an interface between the grid and distributed power generation systems in high-power applications owing to their high efficiency, small filter size, and low harmonic content characteristics [3]–[7].

Three-level inverters are commonly classified as standard neutral-point-clamped (NPC) and T-type NPC inverters [8]. Conventional NPC inverters consist of four switches and two clamping diodes. The four switches are connected in series, which reduces the voltage blocked by each semiconductor. Therefore, standard NPC inverters are more suitable for high-voltage large-capacity power conversion systems than two-level VSIs [9], [10]. T-type NPC inverters employ an active bidirectional switch at the DC-link neutral point [11]. Some advantages of T-type NPC inverters are simple operation, low losses, and excellent output voltage quality [12]. However, because these inverters have the same number of external switches as two-level inverters, their use in high-voltage, large-capacity designs is limited. The proposed method is applicable to both types of three-level inverters, and the standard NPC inverter is considered in the following section.

Capacitors are used in VSIs to stabilize the voltage level in the DC-link. Electrolytic capacitors are widely used in the DC-link owing to their low cost and large capacity per unit volume [13]. The DC-link capacitors are under constant stress due to the ripple current, which increases the core temperature, internal self-heating, and equivalent series resistance (ESR) of the capacitors [14]. Electrolytic capacitors are also vulnerable to electrothermal stress, which accelerates

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the electrolyte evaporation. To relieve the burden of these stresses, a large capacitor with a high allowable ripple current must be used or the capacitors must be connected in series. However, such solutions increase the system volume and manufacturing costs.

To overcome the above challenges, several studies have investigated ways to reduce the DC-link ripple current. In [15], [16], a novel pulse width modulation (PWM) algorithm was proposed to reduce the DC-link ripple current of the back-to-back converter. Other studies have investigated DC-link ripple current reduction using two-level VSIs or modular multi-level converters connected in parallel [17], [18]. Although the performance of these solutions was excellent, they do not apply to three-level inverters. An analytical closed-form expression of DC-link ripple current for three-level NPC-type inverters has been proposed [19]. Based on analysis using this expression, an optimized switching method was introduced to reduce the DC-link ripple current for three-level inverters [20]. However, the DC-link ripple current reduction achieved by this method was not sufficient.

This paper proposes an optimized space-vector modulation (SVM) strategy to reduce the DC-link ripple current in three-level VSIs. The proposed modulation strategy is implemented by substituting the voltage vectors that generate high ripple current flow into the DC-link capacitor. The DC-link current ripple is effectively reduced, relieving the electrothermal stress on the capacitor. As a result, the working life of the DC-link capacitor is increased. The performance and validity of the proposed modulation strategy are demonstrated by various simulations and experimental results.

II. RELIABILITY OF CAPACITORS

An electrolytic capacitor with a large capacitance per volume is a typical DC-link filter in VSIs. As shown in Fig. 1, the capacitor is the weakest component in a power converter. Therefore, the reliability of the capacitor is crucial to the reliability of the power conversion system [21]. Failure modes of electrolytic capacitors include short-circuit failure, open-circuit failure, and wear-out failure. Because short-circuit and open-circuit failures are accidental failures that are caused primarily by manufacturing defects, they are considered uncontrollable failure modes. Wear-out failure is inevitable because of long-term degradation, and its rate varies with the operating condition of the VSIs. That is, capacitor reliability can be improved by appropriately adjusting operating conditions.

Determining the power loss and hot-spot temperature of a capacitor is required to predict the capacitor lifetime. The power loss of a capacitor is expressed as

$$P_{loss} = \sum_{i=1}^{n} [I_{rms}^2(f_i) \times ESR(f_i)], \tag{1}$$

where $I_{rms}(f_i)$ and $ESR(f_i)$ are the root mean square (RMS) values of capacitor current and ESR in f_i, respectively.

The hot-spot temperature of a capacitor is calculated as

$$T_{hot-spot} = T_{amb} + R_{eq-ha} \times P_{loss}, \tag{2}$$

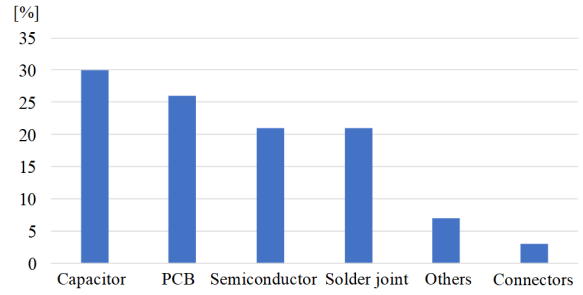

FIGURE 1. Failure rates of power converter components.

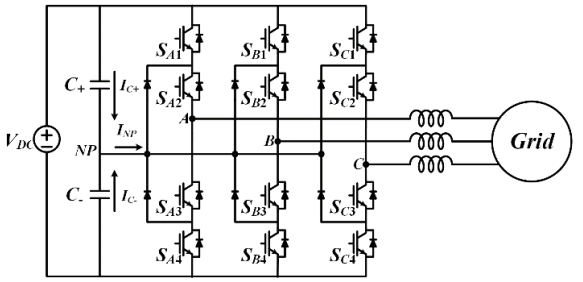

FIGURE 2. Configuration of a grid-connected NPC-type inverter.

where $T_{hot-spot}$, T_{amb}, and R_{eq-ha} represent the hot-spot temperature, ambient temperature, and equivalent thermal resistance between the ambient and hot-spot temperatures of the capacitor, respectively [22].

A conventional lifetime model of a capacitor is proposed in [13], [14] and expressed as

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n_1} \times 2^{\frac{T_0 - T_{hot-spot}}{n_2}}, \tag{3}$$

where L, L_0, V, and V_0 are the estimated lifetime, rated lifetime, operating voltage, and rated voltage, respectively. T_0 is the allowable hot-spot temperature and n_1 and n_2 are coefficients provided by the manufacturer. According to Eq. (3), the working life of a capacitor is a function of the hot-spot temperature. That is, the working life of an electrolytic capacitor can be extended by reducing the current ripple flowing through the capacitor.

III. DC-LINK RIPPLE CURRENT WITH A CONVENTIONAL SVM

As shown in Fig. 2, the DC-link capacitor of a three-level NPC inverter is divided into a top and bottom capacitor to create a neutral point and to output zero voltage. The sum of the top and bottom capacitor currents I_{C+} and I_{C-} equals the neutral point current (I_{NP}), as shown in Eq. (4).

$$I_{NP} = I_{C+} + I_{C-}, \tag{4}$$

Therefore, reducing the I_{NP} is the same as lowering the DC-link ripple currents I_{C+} and I_{C-}.

In a three-level inverter, there are three switching states: [P], [O], and [N]. When the switches S_{x1} ($x = A, B, C$) and

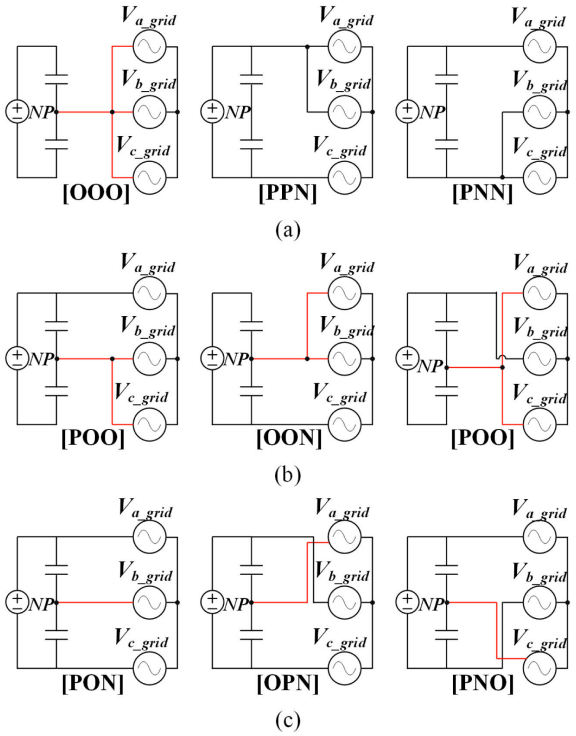

FIGURE 3. Connection of each phase leg and neutral point, (a) zero vector and large vectors, (b) small vectors, (c) medium vectors.

S_{x2} are turned on and the switches S_{x3} and S_{x4} are turned off, the switching state is [P]. Likewise, the switching state is [O] or [N] when the switches S_{x2} and S_{x3} or S_{x3} and S_{x4} are turned on. Fig. 3 depicts the connection of each phase leg and neutral point according to the voltage vectors. As shown in Fig. 3 (a), when all phase legs or no legs are connected to the neutral point, the voltage vectors do not affect the I_{NP}. In contrast, the small and medium voltage vectors that have one or two O-states do affect I_{NP}, as shown in Figs. 3 (b) and 3(c). Table 1 shows the I_{NP} according to the switching states.

Widely used PWM methods for driving VSIs include sinusoidal PWM, discontinuous PWM, and space-vector PWM (SVPWM). SVPWM is widely used because of its outstanding total harmonic distortion (THD) characteristics. The space-vector diagram of a three-level VSI is shown in Fig. 4.

A three-level inverter has three switching states in each phase, so the total number of switching combinations is 27. The medium and large vectors (V_7-V_{18}) have only one switching combination per vector. Further, the small vectors (V_1-V_6) have two switching combinations per vector, and the zero vector (V_0) has three switching combinations. In conventional SVM, a reference voltage is synthesized by using the small, medium, and large vectors closest to the reference voltage vector (V_{ref}). For example, in Fig. 5 (b) SECTOR 1-(B), the V_{ref} is generated by using the small vector V_1, medium vector V_7, and large vector V_{13}, and the switching order is [ONN]-[PNN]-[PON]-[POO]-[PON]-[PNN]-[ONN]. As

TABLE 1. Neutral point current according to the switching state.

Vector	Switching state	Neutral point current
Zero vector	[PPP], [OOO], [NNN]	0
Small vector	[POO]	$I_B + I_C = -I_A$
	[OPO]	$I_A + I_C = -I_B$
	[OOP]	$I_A + I_B = -I_C$
	[NOO]	$I_B + I_C = -I_A$
	[ONO]	$I_A + I_C = -I_B$
	[OON]	$I_A + I_B = -I_C$
Medium vector	[OPN]	I_A
	[PON]	I_B
	[PNO]	I_C
	[ONP]	I_A
	[NOP]	I_B
	[NPO]	I_C
Large vector	[PPN], [PNP], [NPP], [NNP], [NPN], [PNN]	0

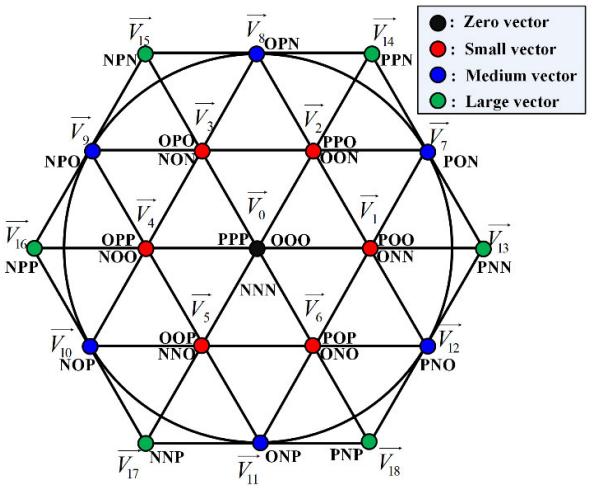

FIGURE 4. Space-vector diagram of a three-level VSI.

analyzed above, the current of a phase leg with O-state flows into the neutral point. Fig. 6 shows the I_{NP} according to the switching states. When the [ONN] or [POO] state, which are the switching state combinations for small vector V_1, are applied, phase A current flows into the neutral point. In SECTOR 1-(B), the order of magnitude for the phase current is phase A, phase C, and phase B. Thus, in a conventional SVM, the highest magnitude phase current flows into the neutral point by the small vector in the same SECTOR as the V_{ref}.

IV. PROPOSED OPTIMIZED SVM

To mitigate the neutral point ripple current, an optimized SVM is proposed in this section. The optimized SVM generates the V_{ref} without using the small vector in the same

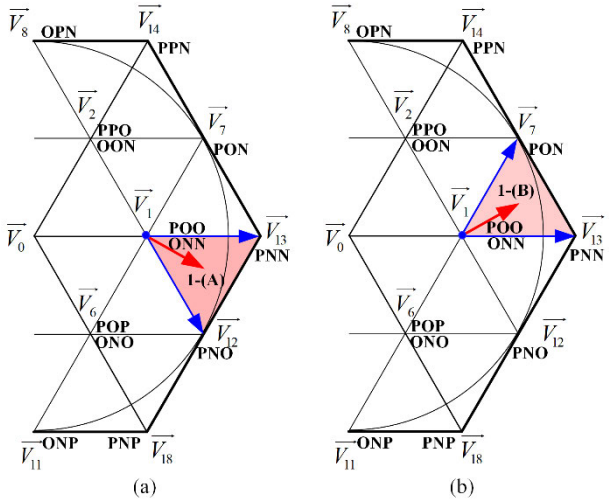

FIGURE 5. Space-vector diagrams and reference voltage vectors, (a) SECTOR 1-(A), (b) SECTOR 1-(B).

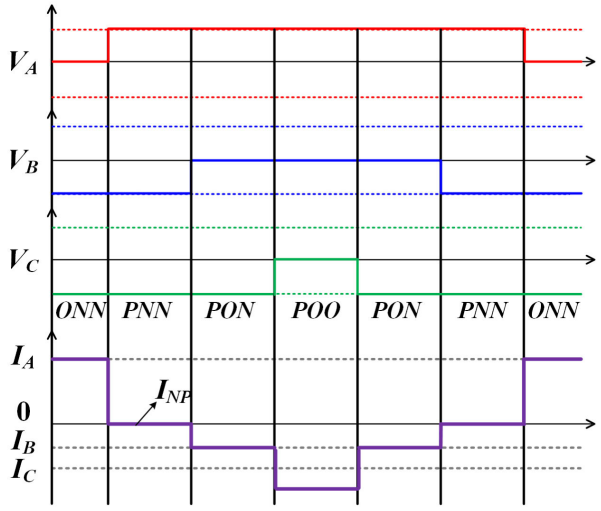

FIGURE 6. Neutral point current and pole voltages for the conventional space-vector pule width modulation in SECTOR 1-(B).

SECTOR as the V_{ref}. The space-vector diagram and sector segmentation of the proposed method is shown in Fig. 7.

To synthesize the V_{ref}, a conventional SVM utilizes the small, medium, and large vectors that are adjacent to the V_{ref}. As shown in Fig. 8, the proposed method replaces the small vector in the current SECTOR by combining the small vector in the other SECTOR and the medium vector in the current SECTOR. The following equation expresses the selection of an alternative small vector, according to the SECTOR of the reference voltage vector:

$$V_{\text{small\_substituted}} = \begin{cases} \overrightarrow{V_{n+1}}, & \text{when } V_{ref} \text{ is in the SECTOR } n\text{-(A)} \\ \overrightarrow{V_{n-1}}, & \text{when } V_{ref} \text{ is in the SECTOR } n\text{-(B)} \end{cases} \quad (n = 1, 2, \cdots, 6). \quad (5)$$

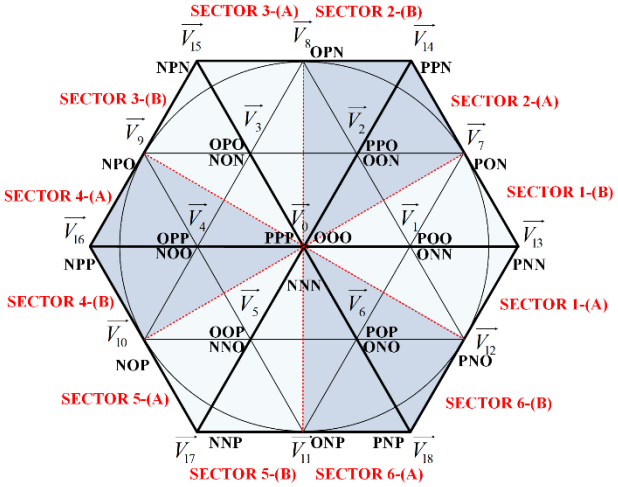

FIGURE 7. Sector segmentation of the space-vector diagram for the proposed method.

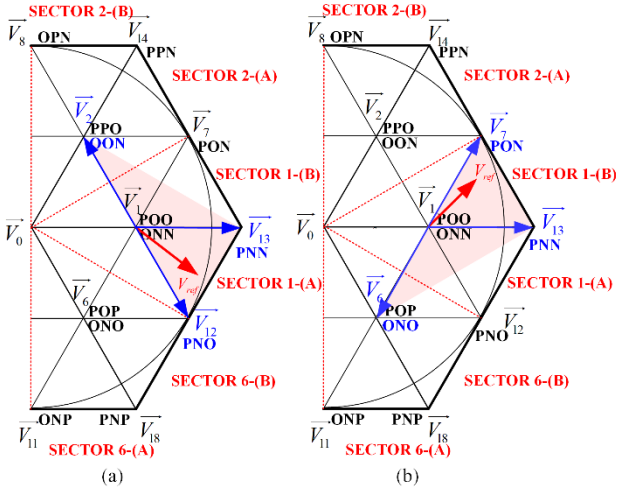

FIGURE 8. Space-vector diagrams and reference voltage vectors for the proposed SVM, (a) SECTOR 1-(A), (b) SECTOR 1-(B).

For example, instead of using the small vector $\overrightarrow{V_1}$ to synthesize the V_{ref} in SECTOR 1-(B), the small vector $\overrightarrow{V_6}$ in the previous SECTOR and the medium vector $\overrightarrow{V_7}$ in SECTOR 1-(B) are used.

The switching states and I_{NP} for the optimized SVM are shown in Fig. 9. When applying the proposed optimized SVM, the switching order is converted to [ONO]-[PNN]-[PON]-[PON]-[PON]-[PNN]-[ONO] instead of [ONN]-[PNN]-[PON]-[POO]-[PON]-[PNN]-[ONN]. The switching states [ONN] and [POO], which cause the highest I_{NP}, are replaced by the switching states [ONO] and [PON]. By applying the switching states [ONO] and [PON], the lowest phase current in SECTOR 1-(B) (I_B or $-I_B$) flows into the neutral point. It is also possible to substitute the switching states [OON] and [PNO] for the small vector of SECTOR 1-(B) based on the methodology proposed in [19]. However, when

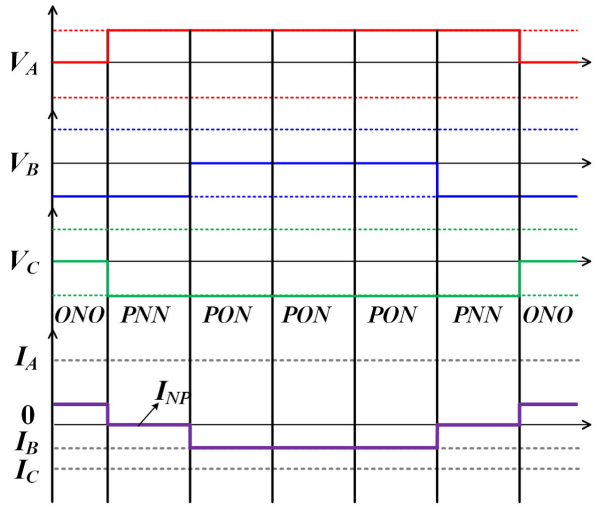

FIGURE 9. Neutral point current and pole voltage for the proposed method in SECTOR 1-(B).

[OON] and [PNO] are substituted, the second-largest current in SECTOR 1-(B) (I_C or $-I_C$) flows into the neutral point. Therefore, it is more effective to apply the proposed optimized SVM. The sector segmentation, substituted small vectors, and switching sequences for applying the proposed optimized SVM are shown in Table 2. Because the lowest current among the three-phase output currents flows into the neutral point, the RMS value of the neutral current decreases; as a consequence, the working life of the DC-link capacitor is extended. In addition, neutral point voltage has AC ripple, and it is divided into the 3rd harmonic component and switching frequency band component. With the proposed technique, switching frequency component of AC ripple is reduced. Because the current flowing through the capacitor is 0 or the smallest current among the 3 phase currents, the slope of the neutral point voltage also decreases.

When applying the proposed optimized SVM, however, the time interval maintaining the same switching state increases during the switching period. In SECTOR 1-(B), for example, in the switching sequence [ONN]-[PNN]-[PON]-[POO]-[PON]-[PNN]-[ONN] with conventional SVM, the switching state is changed six times in total. On the other hand, the switching sequence with the proposed optimized SVM is [ONO]-[PNN]-[PON]-[PON]-[PON]-[PNN]-[ONO], and the switching states change 4 times. The smaller number of state changes means increase in the dwelling time of the certain switching state. As shown in Table 2, when the proposed method is applied, the middle three switching states keep the same in the switching sequence. The output current increases or decreases depending on the switching state. While the switching state maintains the same state, the output current continues to increase or decrease with the constant slope. Therefore, the extension of the dwelling time with same switching state increases the switching ripple of the output currents which degrades

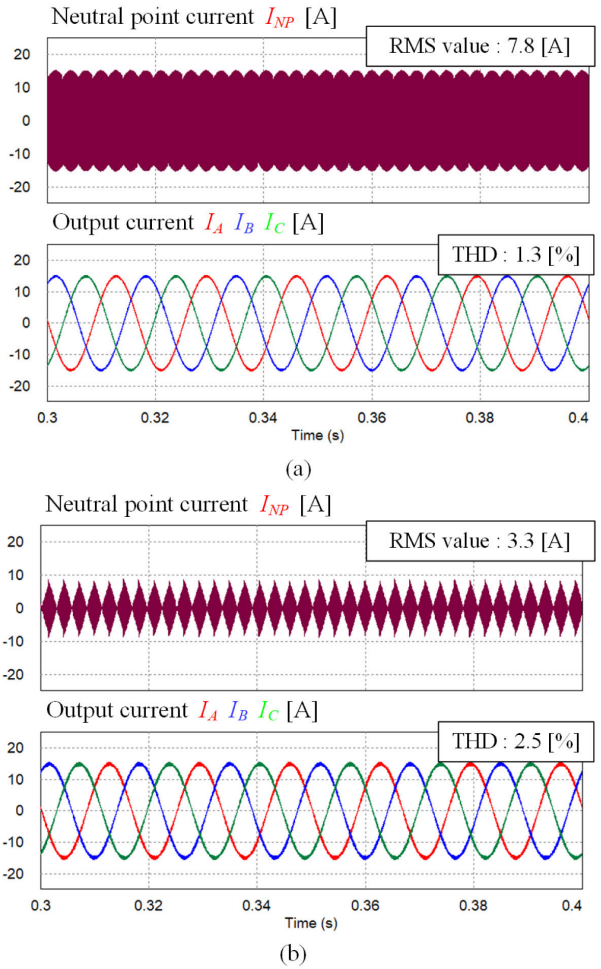

FIGURE 10. Simulation waveforms of neutral point current and output current, (a) conventional SVM, (b) proposed optimized SVM.

THD of the output currents. According to the above analysis, it is confirmed that there is a trade-off between neutral point reduction performance and output current quality.

V. SIMULATION RESULTS

The proposed optimized SVM was simulated using the power electronics simulator (PSIM) software to evaluate its performance. The simulation specifications are shown in Table 3.

The simulation waveforms of the I_{NP} and the three-phase output currents that result from applying a conventional SVM and the proposed optimized SVM are shown in Fig. 10. As shown in Fig. 10 (a), there are some regions in which the highest phase current flows into the neutral point when a conventional SVM is applied. The RMS value of the I_{NP} is 7.8 A, and the THD of the output current is 1.3%.

When the proposed method is applied, as shown in Fig. 10 (b), some small vectors are replaced with vectors that allow the lowest current to flow into the neutral point. Therefore, the RMS value of the I_{NP} is reduced to 3.3 A, and the THD of the current is increased to 2.5%. The proposed technique does not cause additional switching or conduction

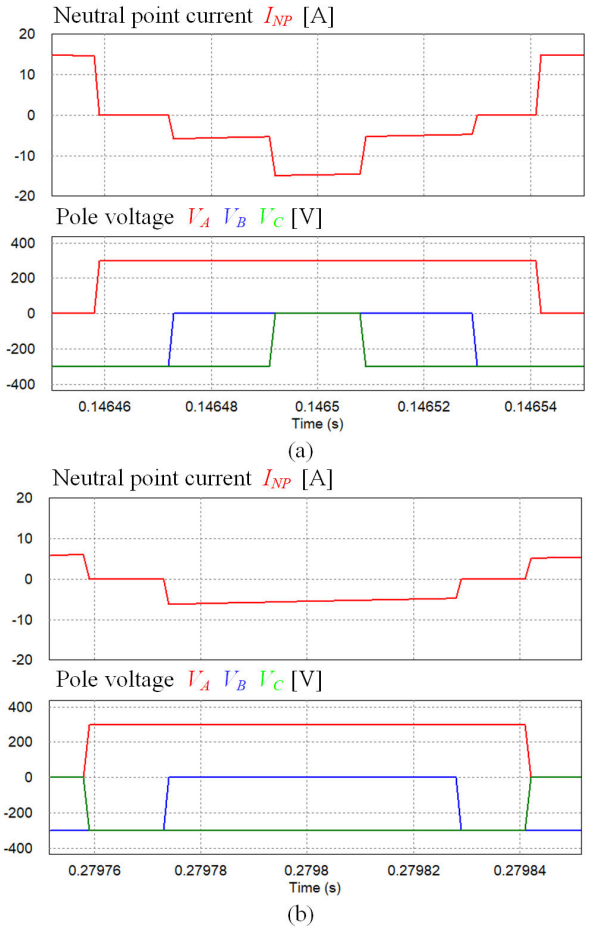

FIGURE 11. Simulation waveforms of neutral point current and pole voltages, (a) conventional SVM, (b) proposed optimized SVM.

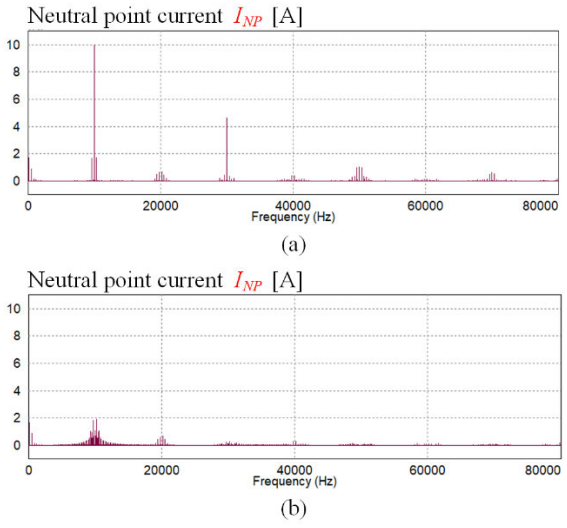

FIGURE 12. Fast Fourier transform (FFT) analysis of neutral point current, (a) conventional SVM, (b) proposed optimized SVM.

losses. This is because the switching count and turn-on time in the proposed method are the same as the conventional SVM. However, the proposed optimized SVM increases the

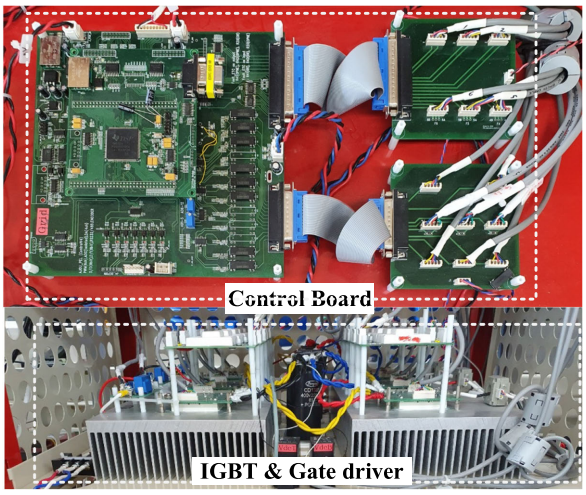

FIGURE 13. Experimental setup.

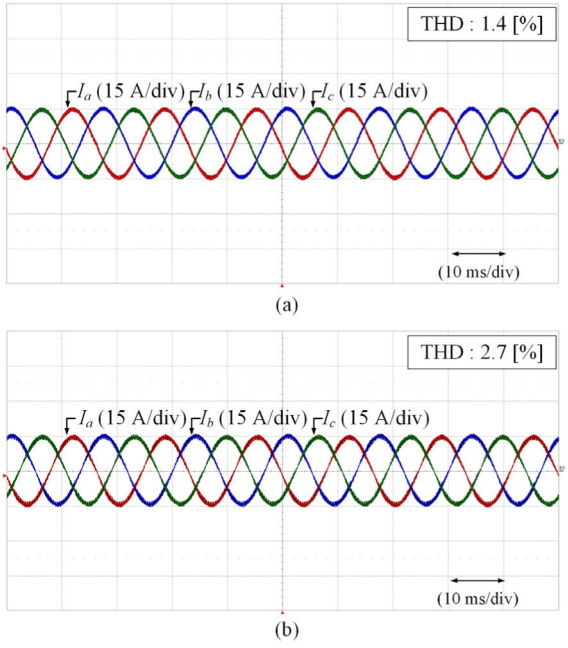

FIGURE 14. Experimental waveforms of three-phase output current, (a) conventional SVM, (b) proposed optimized SVM.

dwelling time of medium vectors due to the voltage vector substitution and this increases the harmonics in output currents. Due to THD degradation, additional losses occur in the load inductor. Based on the 3.3kW simulation environment, the loss increased from 1.3W to 2.3W. When applying the proposed method, the overall efficiency is reduced by 0.03%.

Although the THD of the current is increased, the DC-link ripple current is reduced by approximately 60% when the proposed technique is applied. Reducing the I_{NP} extends the working life of the capacitor, which increases system reliability. A 60% reduction in the DC-link ripple current extends the working life of the DC-link capacitor from 7.75 to 15.1 years (based on CD138S/Jianghai).

TABLE 2. Switching sequences and substituted small vectors according to the sector segmentation.

SECTOR	Substituted small vector	Switching sequence
1-(A)	$\overrightarrow{V_2}$	[OON]-[PNN]-[PNO]-[PNO]-[PNO]-[PNN]-[OON]
1-(B)	$\overrightarrow{V_6}$	[ONO]-[PNN]-[PON]-[PON]-[PON]-[PNN]-[ONO]
2-(A)	$\overrightarrow{V_3}$	[OPO]-[PNN]-[PON]-[PON]-[PON]-[PPN]-[OPO]
2-(B)	$\overrightarrow{V_1}$	[POO]-[PPN]-[OPN]-[OPN]-[OPN]-[PPN]-[POO]
3-(A)	$\overrightarrow{V_4}$	[NOO]-[NPN]-[OPN]-[OPN]-[OPN]-[NPN]-[NOO]
3-(B)	$\overrightarrow{V_2}$	[OON]-[NPN]-[NPO]-[NPO]-[NPO]-[NPN]-[OON]
4-(A)	$\overrightarrow{V_5}$	[OOP]-[NPP]-[NPO]-[NPO]-[NPO]-[NPP]-[OOP]
4-(B)	$\overrightarrow{V_3}$	[OPO]-[NPP]-[NOP]-[NOP]-[NOP]-[NPP]-[OPO]
5-(A)	$\overrightarrow{V_6}$	[ONO]-[NNP]-[NOP]-[NOP]-[NOP]-[NNP]-[ONO]
5-(B)	$\overrightarrow{V_4}$	[NOO]-[NNP]-[ONP]-[ONP]-[ONP]-[NNP]-[NOO]
6-(A)	$\overrightarrow{V_1}$	[POO]-[PNP]-[ONP]-[ONP]-[ONP]-[PNP]-[POO]
6-(B)	$\overrightarrow{V_5}$	[OOP]-[PNP]-[PNO]-[PNO]-[PNO]-[PNP]-[OOP]

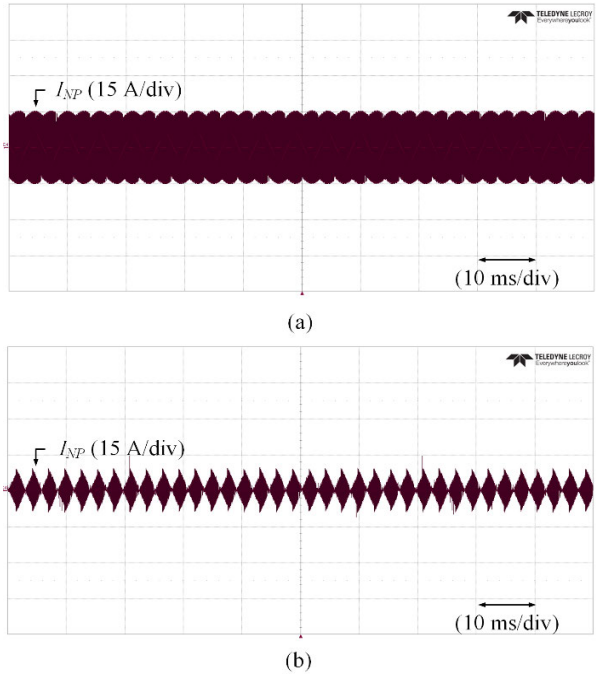

FIGURE 15. Experimental waveforms of neutral point current, (a) conventional SVM, (b) proposed optimized SVM.

The simulation waveforms of the I_{NP} and the pole voltages in SECTOR 1-(B) are shown in Fig. 11. The pole voltages are the same as those in Fig. 6. In Fig. 11 (a), the switching sequence is [ONN]-[PNN]-[PON]-[POO]-[PON]-[PNN]-[ONN]. The switching sequence is converted to [ONO]-[PNN]-[PON]-[PON]-[PON]-[PNN]-[ONO] in Fig. 11 (b). By replacing the [ONN] and [POO] vectors with [ONO] and [PON], respectively, the B-phase current flows into the neutral point instead of the A-phase current.

TABLE 3. Simulation specifications.

Parameters	Value
Rated power, P_{rated}	10 kW
Switching frequency, f_{sw}	10 kHz
DC-link voltage, V_{DC}	600 V
DC-link capacitor, C_{DC}	1000 μF
Load inductor, L_{load}	2 mH
Load resistor, R_{load}	10 Ω

Frequency spectra from a fast Fourier transform (FFT) analysis of the I_{NP} for a conventional SVM and the proposed optimized SVM are shown in Fig. 12. The amplitude of the 10 kHz component is considerably reduced, and other frequency band components are reduced to near zero when the optimized SVM is applied.

VI. EXPERIMENTAL RESULTS

The experimental setup of the three-level NPC inverter used to confirm the feasibility and performance of the

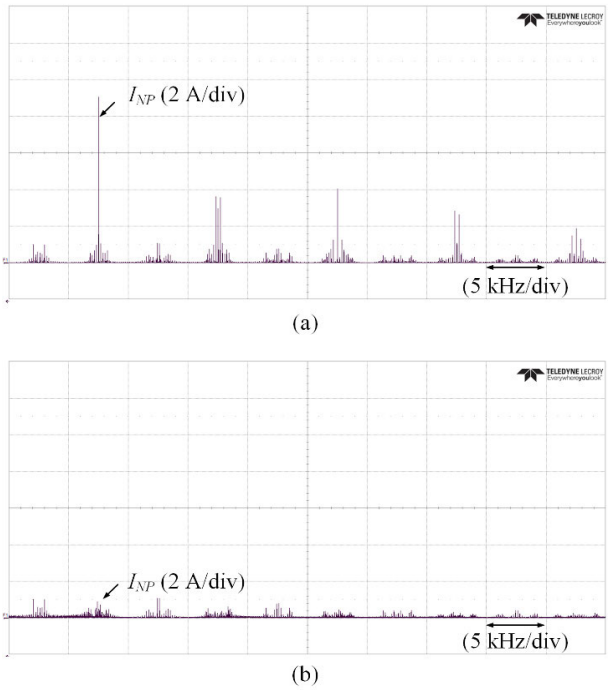

FIGURE 16. Fast Fourier transform (FFT) analysis of neutral point current, (a) conventional SVM, (b) proposed optimized SVM.

proposed optimized SVM is shown in Fig. 13. The parameters are the same as the simulation specifications listed in Table 3. The control schemes were implemented with a TMS320F28335 digital signal processor from Texas Instruments.

The experimental results of three-phase output currents are shown in Fig. 14. The THD of the three-phase output current is 1.4% before applying the proposed method. Using the proposed method increases the THD to 2.7%. These results are similar to the simulation results.

The effect of the proposed optimized SVM on reducing the I_{NP} is shown in Fig. 15. The RMS value of the I_{NP} decreases from 7.9 A to 3.3 A by applying the proposed optimized SVM. The reduction rate is 60%, which increases the working life of the DC-link capacitor by approximately twofold.

The FFT analysis of the I_{NP} is shown in Fig. 16. By applying the proposed method, the odd harmonics (e.g., 1st, 3rd, and 5th harmonics) of the neutral point ripple current are dramatically reduced.

VII. CONCLUSION

In this study, an optimized SVM strategy to reduce DC-link ripple current in three-level VSIs was proposed. Using detailed analysis, the voltage vectors that cause high DC-link current were defined. By applying the proposed modulation strategy, voltage vectors that generate high DC-link current were replaced by voltage vectors that generate low DC-link current. Using the proposed method reduced the RMS value of the DC-link current by approximately 60%, which will extend the working life of the DC-link capacitor by approximately 7 years. In addition, the trade-off between the above advantages and the quality of the output currents was analyzed. The performance and feasibility of the proposed optimized SVM were verified by simulations and experimental results.

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