A 28-GHz Cascode Inverse Class-D Power Amplifier Utilizing Pulse Injection in 22-nm FDSOI

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ABSTRACT Current Mode Class-D (CMCD) Power Amplifiers are of particular interest in outphasing transmitters or Doherty configuration. This is because the output capacitance can be absorbed in the RLC output matching network and 100% theoretical efficiency. In this paper, a 28 GHz current mode (inverse) Class-D power amplifier was simulated, implemented, and measured in 22nm FDSOI. In order to overcome the breakdown voltages of the devices, the amplifier employs a stacked topology, which enables higher output powers and efficiency. The stacked transistors are also pulse injected to further increase the efficiency. Measurement results shows a peak PAE of 46%, peak drain efficiency (DE) of 71% and a saturated output power of 19 dBm. The implemented CMCD PA reports the best performance in literature compared to other CMOS based CMCD PAs.

INDEX TERMS Current mode class-D, FDSOI CMOS, high efficiency, power added efficiency (PAE), power amplifier (PA), stacking.

I. INTRODUCTION

The performance of a power amplifier (PA) is an essential factor in the performance of a transmitter as a whole specifically when it comes to efficiency. The PA is the most power hungry component; hence, having a high efficiency PA results in less power consumption, cooling, and overall cost [1]. Switching PAs, in specific, have been of particular interest due to their ability to achieve 100% efficiency theoretically [2]–[4].

Switched-mode PAs (SMPA) are usually designed to operate at the maximum efficiency with the highest output power. This scheme is suitable for signals with a constant envelope. However, emerging technologies such as 5G employ signals with high peak-to-average power ratio (PAPR) since more complex modulation schemes are used. This means that the input signal has varying power levels which the PA needs to maintain its high efficiency at. With higher frequencies, the efficiency of SMPAs is limited due to the device parasitics and the limited switching speed [5].

SMPAs are able to achieve high efficiencies due to minimizing the overlap between the drain voltage and current.

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Such PAs are Class-E, Class-F, and Class-D (both voltage and current mode) [6], [7]. Table 1 shows a comparison in the performance of various switching amplifiers. From the table, current mode (inverse) Class-D (CMCD), introduced in [8], is able to achieve the largest peak power with a theoretically 100% efficiency. Inverse Class-D PA can also provide higher bandwidth compared to other SMPAs in case a wideband input matching is used [9]. CMCD also has the advantage of having the output drain capacitance absorbed into the output matching network allowing it to operate at higher frequencies compared to other SMPAs along with a relatively simple output matching network [10].

Some work in literature as in [4], [10]–[14] have implemented CMCD PAs with various CMOS technology or III-V technologies at lower frequencies. This work will utilize the high power capabilities of 22nm FDSOI technology with high f_{max} of 371 GHz (NFET) at RF frequencies due to reduced parasitic to the substrate [15] along with the capability of CMCD to operate at high frequencies compared to other SMPAs.

This paper presents design, simulation, and measurements of a CMCD PA at 28 GHz utilizing Globalfoundries 22nm FDSOI technology. In order to overcome the breakdown

TABLE 1. Comparison of different switched mode PA classes.

Class	DE	Peak Drain Voltage	Peak Drain Current	Max. Output Power	Power[a] Capability
D	100	V_{dd}	$\frac{V_{dd}}{R}$	$\frac{(2V_{dd})^2}{\frac{\pi}{2R}}$	0.32
D^{-1}	100	πV_{dd}	$\frac{\pi V_{dd}}{R}$	$\frac{(\pi V_{dd})^2}{2R}$	-
E	100	$3.6V_{dd}$	$\frac{1.7V_{dd}^2}{R}$	$\frac{0.577V_{dd}^2}{R}$	0.098
F	100	$\frac{8V_{dd}}{\pi}$	$\frac{8V_{dd}}{\pi R}$	$\frac{4V_{dd}^2}{\frac{\pi}{2R}}$	0.16

[a] Ratio of actual output power to the product of the maximum device voltage and current.

voltage of the devices, increase efficiency, and deliver more output power, the implemented PA utilizes the cascode (stacking) topology [16]. In order to maximize efficiency, a new technique, pulse injection from the input transistor to the stacked transistor is proposed. The paper is organized as follows: Section II will discuss the principle of operation of the classical CMCD, Section III will present the design methodology of the proposed CMCD and introduce the concept of utilizing a cascode topology along with pulse injection. Section IV will discuss measurement results and comparison to the state-of-the-art CMCD PAs and section V will conclude the paper.

II. CONVENTIONAL CMCD PA
Unlike linear PAs, the transistors in SMPAs act as a switch. In a voltage mode class-D (VMCD) such as in Fig. 1, a square input signal is applied, an LC resonant tank is inserted in series with the load resistance to enable a sinusoidal current to pass through. This results in a non-overlapping peak drain voltage of *VDD* and peak drain current of VDD/R_L. This non-overlapping behavior results in a 100% theoretical efficiency. However, the VMCD PA results in a large power dissipation at GHz frequencies. The CMCD PA overcomes this by utilizing an LC tank resonating at the fundamental frequency that absorbs the parasitic drain capacitance into the output network as shown in Fig. 2.
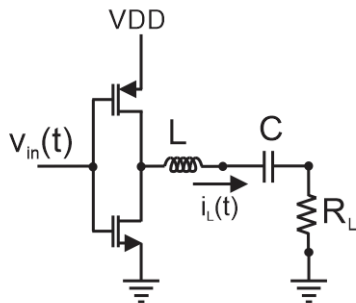

FIGURE 1. Schematics of VMCD PA.

The output voltage is sinusoidal where the overlap between current and voltage is also minimized. The drain voltages of
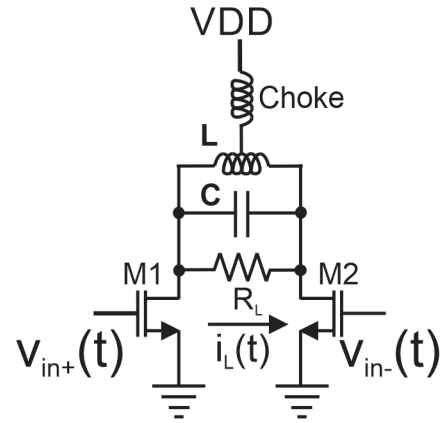

FIGURE 2. Schematics of a conventional CMCD PA.

each transistor (V_{D1}, V_{D2}) are half sinusoidal. The current waveforms (i_{D1}, i_{D2}) are square wave. The transistor currents i_{D1} and i_{D2} can be described as:

$$i_{D1} = \frac{V_{D1}}{R_{on}} \left[\frac{1}{2} + \frac{2}{\pi} \sum_{k(odd)}^{inf} \frac{sin(k\phi)}{k} \right]$$

$$i_{D2} = \frac{V_{D2}}{R_{on}} \left[\frac{1}{2} - \frac{2}{\pi} \sum_{k(odd)}^{inf} \frac{sin(k\phi)}{k} \right] \quad (1)$$

where R_{on} is the ON resistance of the device. The voltage on R_{load} can then be expressed as:

$$V_{out} = V_{D1} - V_{D2} = Acos(\phi) + Bsin(\phi) \quad (2)$$

where A and B are the amplitudes of the two drain-source voltages with phase ϕ. Since the RLC tank allows only the resonance frequency current through the load, a sinusoidal voltage at f_0 is seen at R_{load}. The output power can then be defined as:

$$P_{out} = \frac{V_{out}}{2R_L} = \frac{A^2 + B^2}{2R_L} = \frac{A^2}{R_L} \quad (3)$$

assuming A and B are equal; and the DC current through the transistors would be calculated as:

$$I_{DC} = \frac{VDD - A/\pi}{2R_{on}} \quad (4)$$

The DC power P_{DC} can then be defined as:

$$P_{DC} = VDD * I_{DC} = \frac{VDD(VDD - A/\pi)}{2R_{on}} \quad (5)$$

The drain efficiency (DE) of the CMCD PA can then be represented by:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{A^2}{R_L} \frac{2R_{on}}{VDD(VDD - A/\pi)} \quad (6)$$

From the equation above, it can be deduced that in order to increase the efficiency R_{on} must be increased, which means a smaller device size. This then, is conducive to lower output peak power. In order to distribute the voltage stress, use
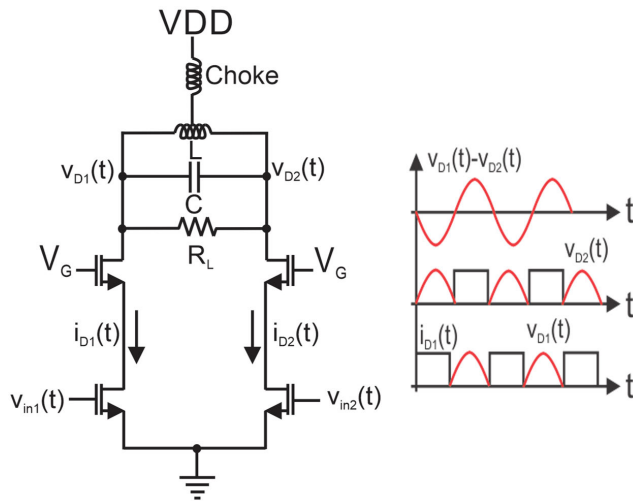
FIGURE 3. Schematic and the ideal waveforms of the drain voltages V_{D1}, V_{D2}, I_{D1} of a cascode CMCD PA.
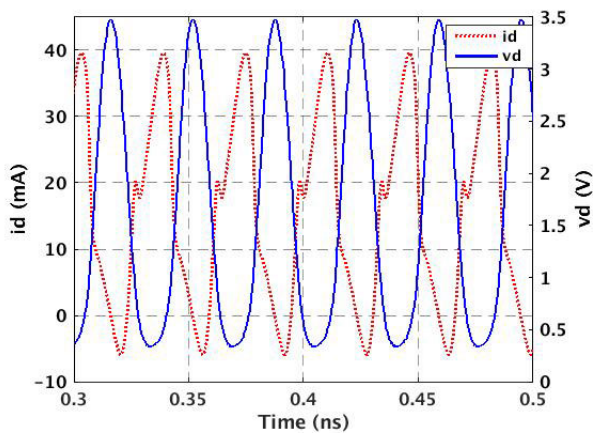
FIGURE 4. Simulated non-overlapping drain voltage (V_{D1}) and current (i_{D1}).

a higher supply voltage and deliver higher output power, a cascode configuration could be used with a relatively larger transistor size.

Fig. 3 shows the topology of a cascode CMCD PA. The two input transistors are driven by equal input signals that are 180° out of phase. The cascode transistors are biased at a constant DC input and serve the purpose of overcoming the breakdown voltage of the devices by allowing for a higher *VDD*. The circuit is symmetrical and the RLC tank results in a a sinusoidal voltage output at the drain. Fig. 3 shows the current and voltage waveforms of an ideal stacked CMCD PA. So an ideal CMCD PA should see an open circuit with no current for even harmonics and short circuit for all odd harmonics resembling a push-pull version of inverse Class-F PA [17].

III. PROPOSED CMCD TOPOLOGY

In order to enable the use of high output power, a higher supply voltage is needed. However, due to the limited breakdown

voltage of the devices, this is limited. Thus, a cascode configuration is used.

Adding a cascode transistor, however, affects the charging and discharging time of the capacitance at the middle node negatively. This additional capacitance can be tuned out by adding a parallel inductor at the common node between the input transistors and the stacked ones. This helps achieve Zero Voltage Switching (ZVS) at high frequencies. Fixed gate bias of stacked CMCD PA suffers from efficiency degradation. The output capacitance increases by the gate-source capacitance of the cascode transistor resulting in a resonance frequency shift to a lower frequency.

In order to minimize the output parasitic capacitance, different gate biasing techniques can be used. A novel technique called pulse injection is proposed that entails the injection of signal from the input transistor to the output transistor (see Fig. 5). This way, we prevent the input transistor to turn on when the cascode transistor is off. Fig. 6 shows the improvement in peak DE when using pulse injection against having a fixed gate bias at the cascode transistor by 28%.

The input RF signal is applied to the gates of the under transistor and cascode transistor through transmission lines terminated on their characteristic impedance used also for biasing the gates of the cascode and under transistor to two different gate voltages VG2 and VG1. The lines are designed to have 100 Ω so at the RF inputs we "see" 50 Ω. The inductor L2 serves to resonate out the gate-source capacitances of the transistors M2 and M4 and the parasitic drain capacitances of the transistors M1 and M3. The capacitance seen at the intermediate nodes can be defined as:

$$C_{P1} = (C_{DS_1} + C_{DG_1}) \parallel C_{GS_2}$$
$$C_{P2} = (C_{DS_3} + C_{DG_3}) \parallel C_{GS_4} \qquad (7)$$

Since the frequency of operation is defined by:

$$f_{RF} = \frac{1}{2\pi\sqrt{L_2 C_{P_{Total}}}} \qquad (8)$$

We can define the total parasitic capacitance $C_{P_{Total}}$ as:

$$\frac{1}{C_{P_{Total}}} = \frac{1}{C_{P1}} + \frac{1}{C_{P2}}$$
$$= \frac{C_{P1} + C_{P2}}{C_{P1} C_{P2}}$$
$$\approx \frac{2}{C_{P1,2}} \qquad (9)$$

Therefore, the value of L2 becomes:

$$L_2 = \frac{1}{4\pi^2 f_{RF}^2 C_{P_{Total}}}$$
$$C_{P_{Total}} = \frac{C_{P1,2}}{2} \qquad (10)$$

The value of the inductor L2 was accordingly designed to the maximum value without compromising on the quality factor. The center-tap inductor L1 connects to the supply voltage through a transmission line in order to choke the
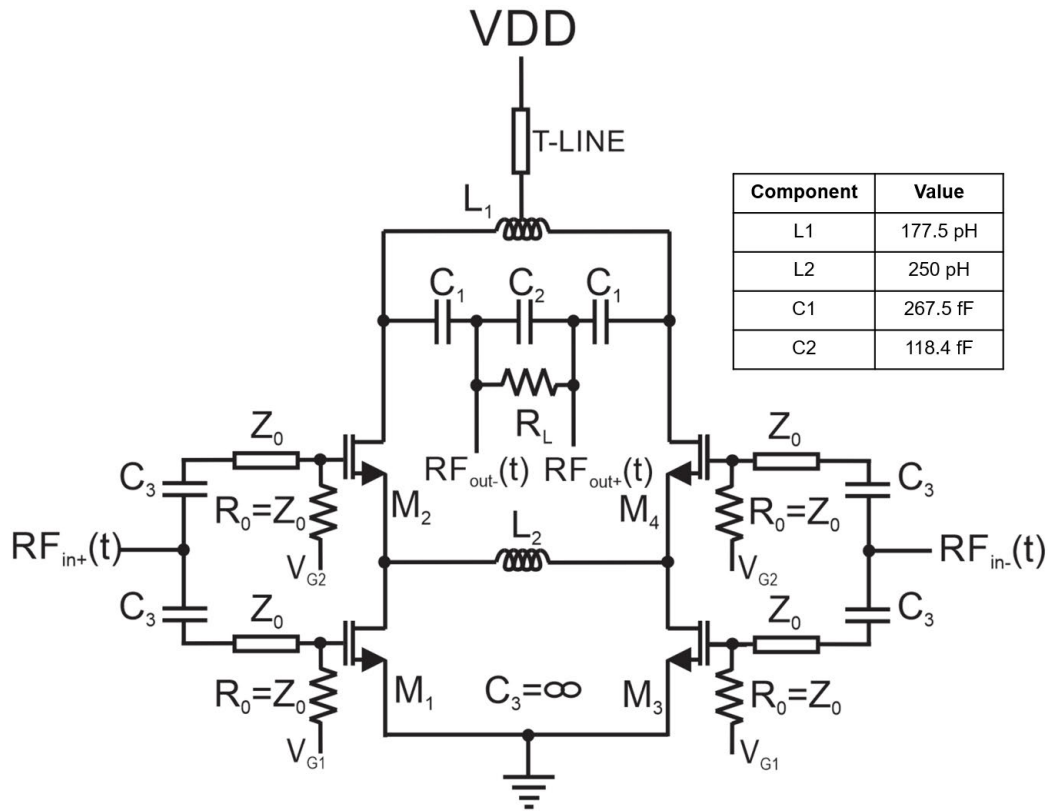
Component	Value
L1	177.5 pH
L2	250 pH
C1	267.5 fF
C2	118.4 fF

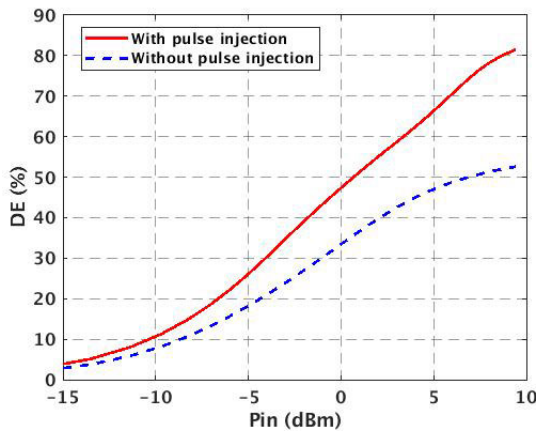**FIGURE 5.** The proposed pulse injected cascode CMCD PA.

FIGURE 6. Simulated DE for fixed gate bias of the cascode transistor and using pulse injection. Improvement in DE using pulse injection against using a fixed gate bias by 28%.
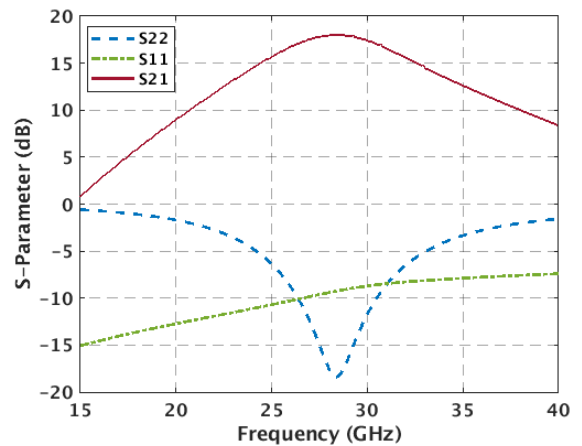

FIGURE 7. Simulated characteristics of the small signal parameters of the proposed CMCDA (*S*11, *S*22, *S*21) with broadband input matching.

fundamental current of the tank. The load is resonant with inductor L1 and the capacitors C1-C2-C1. The purpose of the capacitive divider is to transform the high impedance of the tank to a differential impedance of 100 Ω. This can apply to a 100 Ω differential antenna or a single ended 50 Ω antenna if one of the outputs is terminated with a dummy on-chip 50 Ω resistance. The values of the capacitive divider C1-C2-C1 represented in Fig. 8 can be calculated

as follows. To resonate at frequency f_{RF}, the equivelant capacitance C_{eq} is:

$$C_{eq} = \frac{2C1C2}{C1 + 2C2} \tag{11}$$

The quality factor Q can then be calculated as:

$$Q = \frac{f_{RF}}{BW} = w_0 R_{in} C_t = \frac{R_{in}}{w_0 L1/2} \tag{12}$$

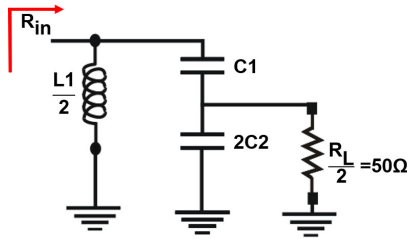$$R_{in} = \pi f_{RF} L1 Q \tag{13}$$

FIGURE 8. Equivalent circuit of one branch of the capacitive divider.

where C_t is the total capacitance. Setting the BW to 1 GHz, the quality factor (Q) is 28. Since L1, Q and f_{RF} is known, then:

$$\frac{R_{in}}{R_{L/2}} \approx (1 + \frac{2C2}{C1})^2 \qquad (14)$$

Replacing into the equation for f_{RF}:

$$f_{RF} = \sqrt{\frac{1}{4\pi^2(\frac{L1}{2}\frac{2C1C2}{C1+2C2})}} \qquad (15)$$

C1 and C2 can the be calculated by:

$$C2 = \frac{\sqrt{\frac{2R_{in}}{R_L}}}{f_{RF}^2 4\pi^2 L1}$$

$$C1 = \frac{\sqrt{\frac{2R_{in}}{R_L}}}{f_{RF}^2 2\pi^2 L1(\sqrt{\frac{2R_{in}}{R_L}} - 1)} \qquad (16)$$

Fig. 5 shows the schematic of the pulse injected CMCD PA. The gate-source capacitance of the stacked transistor is 40 fF. With a 50 Ω input, the impedance at the gate is very low (37 Ω) and the cut-off frequency is much higher than 28 GHz. This provides a broadband input bandwidth without adding any additional capacitance at the gate of the stacked transistors. Fig. 4 shows the simulated non-overlapping drain voltage and current waveforms of the output transistor using harmonic balance simulation at peak PAE. Fig. 7 shows the small signal parameters of the PA with broadband input matching.

IV. MEASUREMENTS RESULTS

The chip in Fig. 9 was implemented in the Global Foundries CMOS 22nm FDSOI technology. The testing was done on-chip using the Elite 300 semi-automatic probe station. The input and output signals are measured using ground-signal-ground-signal-ground (GSGSG) probes while the DC signals are applied through a multi-wedge probe.

The applied out-of-phase input signals were supplied from two signal generators frequency locked to the same reference and adjusted in anti-phase (180°) from their phase control knob. The measurements took into account the losses of the connected wires. Fig. 11 shows the simulated and measured
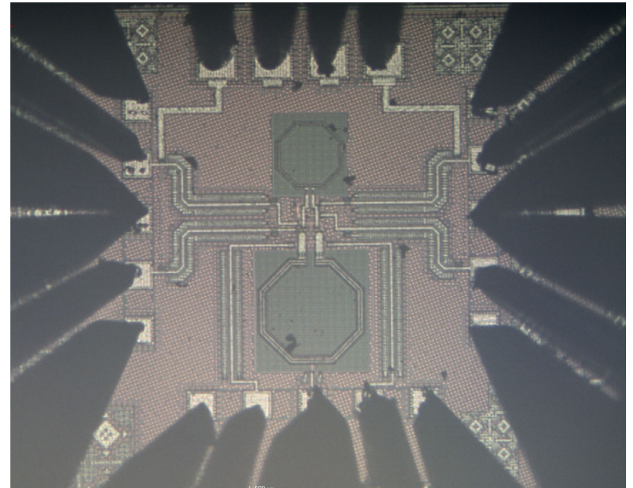

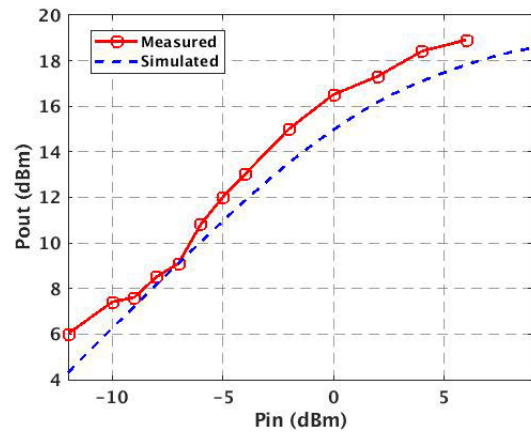**FIGURE 9.** CMCD PA chip microphotograph (0.62 mm × 0.67 mm) with GSGSG probes.

FIGURE 10. Measured and simulated P_{out} Vs P_{in}. The CMCD PA shows a maximum output power of 19 dBm.

PAE and DE. The PAE is measured as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \qquad (17)$$

The measured Peak PAE and DE shows 46%/72% respectively (see Fig. 11) with peak PAE at 0 dBm input power. Fig. 10 shows a maximum output power of 19 dBm with a power gain of 17 dB to a 50 Ω load. The frequency was swept from 26 GHz to 30 GHz and output power was recorded. The CMCD PA shows a narrow-band response as shown in Fig. 13 with output power greater then 15 dBm for a 1 GHz bandwidth. In order to measure power delivering capabilities, the supply voltage was increased and output power was recorded (see Fig. 12). The CMCD PA is able to deliver higher power with a higher *VDD*; however, it is limited to the breakdown voltage of the device.

TABLE 2. Comparison between the proposed 22nm FDSOI CMCD PA and related work in literature.

| Ref.	Technology	Freq. (GHz)	P_{out} (dBm)	Peak PAE (%)	Peak DE (%)	Gain (dB)	Class
This work	22nm FDSOI CMOS	28	19	46	71	17	stacked CMCD
[4]	GaAs HBT	0.7	29.5	68.5	N/A	11	CMCD
[10]	130nm CMOS	1.8	26.8	45	46	N/A	stacked CMCD
[11]	65nm CMOS	2.25	21.8	44.2	78	N/A	CMCD
[12]	180nm CMOS	1.85-1.91	17.5	17.5	N/A	18.91	CMCD
[13]	GaN	2.6	29.5	62	N/A	14.4	CMCD
[14]	130nm CMOS[a]	2.4	19.75	58	74.1	19.5	CMCD
[18]	40nm CMOS	60	17.9	20.5	N/A	21.5	Class-E/F$_2$
[19]	0.13 μm SiGe HBT	46	28.9	18.4	N/A	13	Stacked Class-E
[20]	130nm SiGe	34	25.5	26	28	13	Stacked Class-K
[21]	45nm SOI	47.5	19.1	16	24.5	8.2	Stacked Class-E
[22]	45nm SOI	40	18.5	10	N/A	15	Class-D

[a] Post layout simulation.
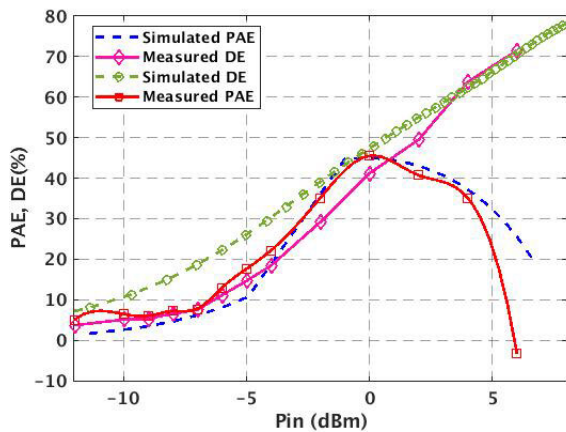
FIGURE 11. Measured and simulated PAE and DE. The CMCD PA shows a peak PAE of 46% and peak DE of 72%.
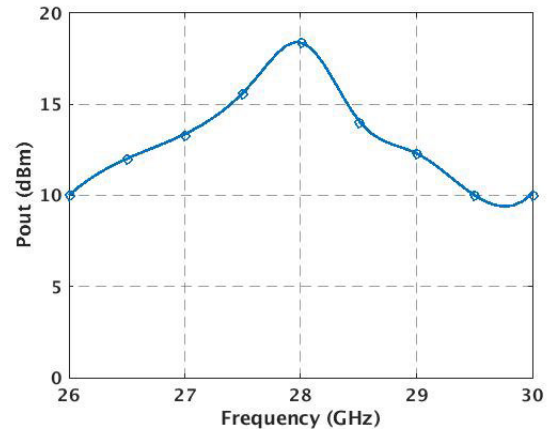

FIGURE 13. Output power (P_{out}) Vs. frequency shows a narrow-band behavior maintaining $P_{out} > 15$ for a BW of 1 GHz.
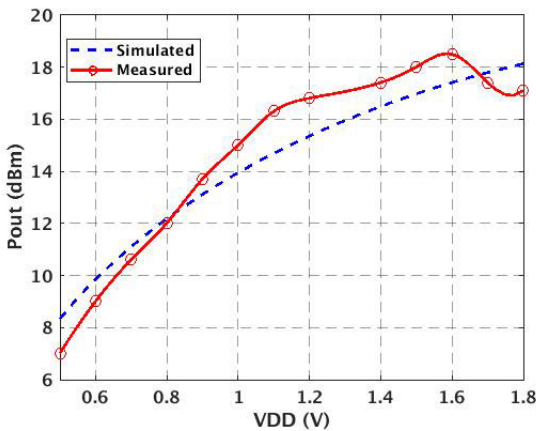

FIGURE 12. Measured output power (P_{out}) Vs. supply voltage (*VDD*). Output power increases with supply voltage but limited to the breakdown voltage of the device.

A. COMPARISON WITH STATE-OF-THE-ART CMCD PAS

Table 2 shows a comparison between the performance of the proposed pulse injected CMCD PA and other switching PAs reported in literature in various technologies. When comparing the performance of PAs, it is important to keep in mind the

operating frequency compared to the f_{max} of the devices used. We are able to report the best measured peak PAE in literature compared to other CMCD PAs in CMOS. Our design also utilizes much less area due to a less number of passive elements; by only using 2 inductors compared to other designs using 5 such as in [12]. Other technologies such as GaAs HBT and GaN are able to report higher efficiencies and output power on the expense of cost and integration capabilities such as in [4], [13] at lower frequency bands. Overall, we are able to report the best performance at RF frequencies as high as 28 GHz compared to similar work reporting compatible efficiencies at 2.25 GHz in [10], [11] and better efficiency compared to other switching PAs near 28 GHz in [18]–[20]. To the best of our knowledge, no other work in literature reports similar performance at similar frequency bands.

V. CONCLUSION

In this paper, a novel 28 GHz Current mode class-D was implemented and measured in 22nm FDSOI. In order to overcome the limited breakdown voltage of the devices, use a higher supply voltage and deliver high output power, the architecture relies on stacked topology. A novel technique, pulse injection, was implemented to the cascode

transistors to improve efficiency. The measured CMCD PA reports a peak PAE of 46% and a peak DE of 71% with output power of 19 dBm. It represents the highest performance reported for a CMCD PA in CMOS at 28 GHz. This amplifier is suitable for outphasing transmitters or a Doherty configuration to improve efficiency and handle large PAPR signals.

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