

Received May 1, 2020, accepted May 16, 2020, date of publication May 20, 2020, date of current version June 3, 2020. *Digital Object Identifier 10.1109/ACCESS.2020.2995889*

Low-Voltage Stress Buck-Boost Converter With a High-Voltage Conversion Gain

BINXIN ZH[U](https://orcid.org/0000-0001-8820-3088)^O, (Senior Memb[er,](https://orcid.org/0000-0001-6971-6275) IEEE)[,](https://orcid.org/0000-0001-7407-4473) SHISHI HU^O, GUANGHUI LIU^O, YU HUANG[®][,](https://orcid.org/0000-0002-9896-7310) AND XIAOLI SHE[®]

Hubei Provincial Research Center on Microgrid Engineering Technology, College of Electrical Engineering and New Energy, China Three Gorges University, Yichang 443002, China

Corresponding author: Binxin Zhu (zhubinxin40@163.com)

This work was supported in part by the National Natural Science Foundation of China under Grant 51707103, and in part by the Industry-Education Cooperation Program of Ministry of Education of China under Grant 201901165004.

ABSTRACT The conventional buck-boost converter has the advantages of simple structure, low cost, and the capability to achieve both voltage step-up and down. However, due to the negative impacts of the parasitic parameters of the device, the voltage conversion gain of the conventional buck-boost converter is greatly limited. A low-voltage stress buck-boost converter with a high voltage conversion gain based on a coat circuit is proposed in this paper to address the problem. Similar to a coat that can enhance human's resistance to cold weather, by adding the proposed coat circuit to the conventional buck-boost converter, not only the range for the voltage conversion can be extended, but also the voltage stresses of the semiconductor components are effectively reduced. In this work, comprehensive analysis on the working principles and performance characteristics of the coat converter are provided. Experimental results are obtained and analyzed to validate of the theoretical analysis based on a 300W closed-loop prototype platform.

INDEX TERMS Buck-boost, coat circuits, high voltage conversion gain, voltage stress.

I. INTRODUCTION

Renewable energy generation systems based on wind, solar, and biomass have been rapidly developed around the world in recent years [1], and it leads to increasing research interest in DC/DC converters with high voltage conversion [2]–[4]. Coupled inductors have been commonly used to increase the voltage conversion gain of DC/DC converters [5]–[7], but the existence of leakage inductance can cause unwanted voltage spikes. Additional auxiliary circuit is needed to solve this issue while such a method requires more complex design [8]. Alternatively, many high step-up DC/DC converters based on the switched-inductor or switched-capacitor have been proposed [9]–[11]. However, these converters require a large number of switches and driving circuits [12], [13]. Cascaded structures can be used to increase the step-up voltage gain [14]–[16], but some issues will be introduced. On the one hand, multiple stages are needed and the number of devices is large. On the other hand, the system efficiency is low due to the energy needs to undergo multi-stage conversion.

Many different voltage multipliers (VMs) have been used to improve the voltage conversion ratio of boost converters in [17]–[20], not only the voltage conversion ratio of these converters can be improved but also the voltage stresses on components can be decreased.

However, most of the above-mentioned high step-up DC/DC converters are developed based on the boost converters for voltage step-up. It is impossible to use such converters in the applications that require voltage step-down, such as portable devices, LED drivers, light-emitting diode products, and car electronic devices [21], [22]. Recently, researchers have proposed a few converters that have high voltage conversion ratio ability and they can also achieve voltage step-down. For example, a step-up/down converter based on the Zeta converter has been proposed in [23], whose voltage conversion ratio is twice as that of the traditional buck-boost converter. References [24] and [25] have proposed two high-voltageconversion-gain converters based on the buck-boost converter and the SEPIC converter, respectively, and their voltage ratios are three times as that of the conventional ones. A quadratic buck-boost converter is proposed in [26]. This converter is cascaded with two conventional buck-boost converters, and

The associate editor coordinating the review of this manuscript and approving it for publication was Canbing Li.

FIGURE 1. Topology of the proposed converter: (a) the general topology; (b) the topology with one basic cell.

it can realize the square of the voltage conversion ratio of the conventional buck-boost converter, but the semiconductor devices suffer from high voltage stress.

Different kinds of coat circuits for basic DC/DC converters have been proposed in [27], and the Ćuk converter has been taken as an example to discuss in detail, the boost converter with the coat circuit has been analyzed in detail in [28].

In this paper, the working principles and the performance characteristics of a buck-boost converter with the coat circuit have been analyzed in detail in Sections II and III, respectively. The static and dynamic experimental results of the prototype are given in Sections IV and V, respectively.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The topology of the proposed converter is shown in Fig. 1(a). It consists of a basic buck-boost converter and the proposed coat circuit of which the number of basic units is adjustable. Each basic unit contains two capacitors, an inductor, and a diode. In order to simplify the analysis process, this paper takes the converter with one basic unit as an example to analyze its working principle, as shown in Fig. 1(b). The following assumptions are considered:

[\(1\)](#page-2-0) All devices are ideal, ignoring the influence of circuit and devices parasitic parameters;

[\(2\)](#page-2-1) The capacitance value is large enough to ignore the effect of voltage ripple on the capacitors.

FIGURE 2. Key waveforms of the converter within one period.

FIGURE 3. Equivalent circuits: (a) mode 1; (b) mode 2.

The converter can be worked in two modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). There are two operation modes when working in CCM mode. Fig. 2 shows the key waveforms of the converter in one switching period under rated operating conditions. The detailed working process is as follows:

Mode $1 [t_0-t_1]$: The equivalent circuit is shown in Fig. 3(a). During this mode, the switch S_1 is turned ON and the diode D_1 and D_{11} are reverse blocking. The current of the inductor *L*¹ and *L*¹¹ increase linearly under the excitation of the input voltage source u_{in} , the capacitor C_{11} is charged and the capacitor C_1 is discharged, the capacitor C_{12} supplies power to the load. The equations of inductance voltages can be obtained

as follows:

$$
\begin{cases}\nu_{L1} = u_{in} \\
u_{L11} = u_{in} + u_{C1} - u_{C11}\n\end{cases} (1)
$$

Mode 2 $[t_1-t_2]$: During this period, the switch S_1 is turned OFF and the diode D_1 and D_{11} are turned ON, as shown in Fig. 3(b). The *L*¹ and *L*¹¹ are demagnetized. The capacitor C_1 and C_{12} are charged by the inductor L_1 . The capacitor C_{11} is discharged. The relevant equations can be written as follows:

$$
\begin{cases}\nu_{L1} = -u_{C1} \\
u_{L11} = u_{C1} - u_0 = -u_{C11}\n\end{cases}
$$
\n(2)

III. PERFORMANCE CHARACTERISTICS

A. VOLTAGE CONVERSION RATIO

By applying volt-second balance on the inductors *L*¹ and *L*¹¹ which are shown in (1) and (2) , equations (3) and (4) can be derived:

$$
\begin{cases}\nDu_{\rm in} = (1 - D)u_{\rm C1} \\
u_{\rm in} + u_{\rm C1} - u_{\rm C11} = (1 - D)(u_{\rm o} - u_{\rm C1}) = (1 - D)u_{\rm C11} \\
(3)\n\end{cases}
$$

$$
\begin{cases}\nu_{\text{C1}} = \frac{u_{\text{in}} \cdot D}{1 - D} \\
u_{\text{C11}} = \frac{u_{\text{in}}}{1 - D} \\
u_{\text{o}} = u_{\text{C12}} = \frac{u_{\text{in}} \cdot 2D}{1 - D}\n\end{cases} (4)
$$

Based on [\(4\)](#page-2-2), the voltage conversion ratio (*M*) can be found as follows:

$$
M = \frac{u_0}{u_{\text{in}}} = \frac{2D}{1 - D}
$$
 (5)

Extending to the proposed converter with *n* basic cells:

$$
\begin{cases}\nu_{C1} = u_{C11} = u_{C21} = \dots = u_{Cn1} = \frac{u_{in} \cdot D}{1 - D} \\
u_{Ci2} = \frac{u_{in} \cdot (i + 1) \cdot D}{1 - D} \\
u_0 = u_{Cn2} = \frac{u_{in} \cdot (n + 1) \cdot D}{1 - D} \\
M = \frac{(n + 1) \cdot D}{1 - D}\n\end{cases} (6)
$$

B. VOLTAGE AND CURRENT STRESSES OF COMPONENTS

As shown in Fig. 1(b), the voltage stresses of the switch S_1 , the diode D_1 and D_{11} can be denoted as u_{S1} , u_{D1} and u_{D11} , respectively. According to [\(4\)](#page-2-2), equation [\(8\)](#page-2-3) can be obtained:

$$
\begin{cases}\n u_{\text{S1}} = u_{\text{D1}} = u_{\text{in}} + u_{\text{C1}} = \frac{u_{\text{in}}}{1 - D} \\
 u_{\text{D11}} = u_{\text{o}} - u_{\text{C11}} + u_{\text{in}} = \frac{u_{\text{in}}}{1 - D}\n\end{cases}
$$
\n(8)

Based on equation [\(6\)](#page-2-4), the voltage stresses of switch and diodes can be found as follows when extending to the proposed converter with *n* basic cells:

$$
\begin{cases}\n u_{S1} = u_{D1} = \frac{u_{in}}{1 - D} \\
 u_{D11} = u_{D21} = ... = u_{Dn1} = \frac{u_{in}}{1 - D}\n\end{cases}
$$
\n(9)

To simplify the current stress analysis, ignoring the small ripple term, the currents of inductor L_1 , L_{11} and the output current are denoted as *I*L1, *I*L11, and *I*o, respectively. According to the ampere-second balance of the capacitors C_1 , C_{11} and C_{12} , the following equations are derived as follows:

$$
\begin{cases}\n-D \cdot I_{L11} = (1 - D) \cdot (I_{L11} - I_{D1}) \\
D \cdot I_{L11} = (1 - D) \cdot (I_{D11} - I_{L11}) \\
-D \cdot I_0 = (1 - D) \cdot (I_0 - I_{D11})\n\end{cases} (10)
$$

$$
I_{D1} = I_{D11} = I_{L11} = I_0
$$
 (11)

If the converter loss is ignored and the input power is equal to the output power, the input-output current relationship can be obtained through equation [\(5\)](#page-2-5):

$$
I_{S1} = I_0 \cdot \frac{2D}{1 - D} \tag{12}
$$

From Fig. 3 (a), the average current of the switch S_1 can be obtained as follows:

$$
I_{S1} = D \cdot (I_{L1} + I_{L11}) \tag{13}
$$

From $(11)-(13)$ $(11)-(13)$ $(11)-(13)$, equation (14) can be obtained:

$$
I_{L1} = I_o \cdot \frac{1+D}{1-D} \tag{14}
$$

The above current stress analysis is extended to the proposed converter with *n* basic cells, we have:

$$
\begin{cases}\nI_{D1} = I_{D11} = I_{D21} = ... = I_{Dn1} = I_o \\
I_{L11} = I_{L21} = ... = I_{Ln1} = I_o \\
I_{L1} = I_o \cdot \frac{1 + n \cdot D}{1 - D} \\
I_{S1} = I_o \cdot \frac{(n+1) \cdot D}{1 - D}\n\end{cases} (15)
$$

C. DISCONTINUES CONDUCTION MODE

When the input voltage and the output voltage remain unchanged while the load power decreases (the dc load current decreases), it can be seen from [\(11\)](#page-2-6) and [\(14\)](#page-2-8) that the average currents of inductors *L*¹ and *L*¹¹ will decrease, but the ripple magnitude of inductors *L*¹ and *L*¹¹ are kept constant, as shown in Fig. 2. When the load current drops to a specific value, in each switching cycle, there will be a part of time that the switch and the diodes are not conducted, that is, the converter will work in Discontinues conduction mode (DCM). The converter can be divided into four modes during each switching period.

In order to simplify the analysis process, it is assumed that $L_1 = L_{11} = L$. Due to the fact that the peak-to-peak current ripples of inductor L_1 and L_{11} are equal to the product of the slope (the applied inductor voltage divided by L) and the length of mode 1, [\(16\)](#page-3-0) can be obtained based on [\(1\)](#page-2-0)-[\(3\)](#page-2-2). The key waveforms of the proposed converter under the condition of DCM during one switching period are shown in Fig. 4. The mode 1 (t_0-t_1) and mode 2 (t_1-t_2) in DCM are same as that of CCM. When the current i_{L11} of the inductor L_{11} drops to

FIGURE 5. Equivalent circuits of the proposed converter at DCM operation: (a) mode 3; (b) mode 4.

zero at time t_2 and then reverses, the converter enters mode 3, the equivalent circuit is shown in Fig. 5(a). During the period from t_2 to t_3 , i_{L1} decreases and i_{L11} increases in the opposite direction, and the amplitudes of i_{L1} and i_{L11} are equal at t_3 , which is denoted as I_M . In mode $4(t_3-t_4)$, the diodes D_1 and D_{11} are turned off, i_{L1} and i_{L11} remain unchanged in this mode, and the equivalent circuit is shown in Fig. 5(b).

$$
\Delta i_{L1} = \Delta i_{L11} = \frac{u_L(t)}{L} = \Delta i_L = \frac{u_{in} \cdot DT_s}{L}
$$
 (16)

[\(17\)](#page-3-1) and [\(18\)](#page-3-1) can be obtained by using volt-second balance on inductors L_1 and L_{11} .

$$
\begin{cases}\nu_{\text{C1}} = u_{\text{in}} \cdot \frac{D}{D_M} \\
u_{\text{C11}} = u_{\text{in}} \cdot \frac{D}{D_M} \\
u_{\text{o}} = u_{\text{C12}} = u_{\text{in}} \cdot \frac{2D}{D_M} \\
M = \frac{2D}{D_M}\n\end{cases} (17)
$$

where D_M is the duty cycle in mode 2 and mode 3 at DCM, as shown in Fig. 4. The duty cycle *D* is the control signal of the converter, which can be considered known, but D_M is unknown. Therefore, another equation must be found to eliminate D_M to obtain the voltage conversion ratio M.

The currents through the diodes D_1 and D_{11} during diodes conduction can be expressed as follows:

$$
\begin{cases}\nI_{\text{D1}} = I_{\text{L1}} - I_{\text{C11}} \\
I_{\text{D11}} = I_{\text{C11}} + I_{\text{L11}}\n\end{cases} (19)
$$

$$
I_{D1} + I_{D11} = I_{L1} + I_{L11}
$$
 (20)

According to [\(11\)](#page-2-6), the average currents of the diodes D_1 , and D_{11} are equal to the average output current I_0 . The sum of the average currents of the diodes D_1 and D_{11} can be achieved:

$$
I_{\rm D} = I_{\rm D1} + I_{\rm D11} = \frac{2u_{\rm o}}{R_{\rm L}}\tag{21}
$$

According to Fig. 4 and equation [\(20\)](#page-3-2), it can be obtained that the sum of the peak currents i_{D-peak} of the diodes D_1 and D_{11} :

$$
i_{\text{D-peak}} = i_{\text{L-peak}} = i_{\text{L1-peak}} + i_{\text{L11-peak}} = \frac{u_{\text{in}} \cdot D \cdot T_{\text{S}}}{L_{\text{eq}}} \quad (22)
$$

$$
\frac{1}{L_{\text{eq}}} = \frac{1}{L_1} + \frac{1}{L_{11}} = \frac{2}{L} \tag{23}
$$

$$
L_{\text{eq}} = \frac{L}{2} \tag{24}
$$

According to Fig. 4, the sum of the average currents of the diodes D_1 and D_{11} during one switching period can be obtained as follows:

$$
I_{\rm D} = I_{\rm D1} + I_{\rm D11} = \frac{1}{2} \times D_{\rm M} \times i_{\rm D\text{-peak}} = \frac{u_{\rm in} \cdot D_{\rm M} \cdot D \cdot T_{\rm S}}{2L_{\rm eq}}
$$
(25)

According to [\(18\)](#page-3-1)-[\(25\)](#page-3-3), the voltage conversion ratio of the converter in discontinues conduction mode can be earned as follows:

$$
M = \frac{u_0}{u_{\text{in}}} = \sqrt{\frac{D^2 R_L T_S}{L}}
$$
 (26)

When the proposed converter is working in the boundary condition mode (BCM), the voltage conversion ratio in CCM is consistent with DCM. The boundary factor (α) can be

TABLE 1. Comparison of the proposed converter with other topologies.

Topology	Proposed	Converter in	Converter	Converter	Converter	Traditional
	Converter	[23]	in $[26]$	in $[17]$	in $[21]$	buck-boost
Number of switches						
Number of diodes	$1+n$			2n	$1+2n$	
Number of inductors	$1+n$				$1+n$	
Number of capacitors	$1+2n$			2n	$1 + n$	
Voltage conversion ratio	$(n+1)\cdot D$ $(1-D)$	2D $(1-D)$		2n $1-D$	n $D (1 - D)$	$(1 - D)$
Switch voltage stress	u_o $(n+1)\cdot D$	u_o 2 D	u_o n^2	$\frac{u_o}{\sqrt{2}}$ 2n	$\frac{u_o}{}$	$u_{\rm o}$

obtained by combing (5) and (26) , as shown in (27) . When α is less than 1, the converter works in CCM and when α is larger than 1, the converter operates in DCM.

$$
\alpha = \frac{(1 - D)^2 \cdot T_{\rm S} \cdot R_{\rm L}}{4L} \tag{27}
$$

Extending to the proposed converter with *n* basic cells:

$$
M = \frac{u_{\rm o}}{u_{\rm in}} = \sqrt{\frac{(n+1)D^2 R_{\rm L} T_{\rm S}}{2L}}\tag{28}
$$

$$
\alpha = \frac{(1 - D)^2 \cdot T_S \cdot R_L}{2(n + 1) \cdot L} \tag{29}
$$

D. COMPARISON OF THE PROPOSED CONVERTER WITH OTHER TOPOLOGIES

Table 1 shows the performance comparison of several other high-gain DC/DC converters, traditional buck-boost converter, and the converter proposed in this paper. Fig. 6 shows the comparison of the voltage conversion ratio of the proposed converter with one basic cell, the traditional buck-boost converter, and the converters proposed in [21], [26]. Compared with the traditional buck-boost converter, the proposed converter can decrease the voltage stresses on devices, and increase the voltage gain by introducing the proposed coat circuit. The converters proposed in [17], [21] can also change the voltage gain by changing the number of VMs, but they use two switches and have no step-down voltage capacity. The voltage gain of the converter proposed in [26] is significantly higher than that of the converter proposed with one VM, and the voltage gain of the converter proposed in [23] is equal to that of the proposed converter with one basic cell, but their topology is fixed and their voltage gain is not adjustable.

IV. EXPERIMENTAL RESULTS

In order to verify the accuracy of the above theoretical analysis, an experimental prototype containing two basic cells was established. The specifications of the experimental prototype are shown in Table 2.

The experimental waveforms are shown in Fig. 7. Fig. 7(a) illustrates the waveforms of u_{gs} , u_{in} , u_{S1} and u_0 . When the voltage conversion ratio is 8.33, the duty cycle is near 0.735, which is consistent with (7) . The voltage waveforms of diodes D_1 , D_{11} and D_{21} are given in Fig. 7(b), and the voltage

FIGURE 6. Voltage conversion ratio comparison between the proposed converter and other converters at CCM operation.

TABLE 2. Specifications of the experimental prototype.

Values				
48 V				
400 V				
300 W				
100 kHz				
IRFB4332				
IDT12S60C				
C_1 , C_{11} , C_{21} , C_{12} , C_{22} , C_2 : 4 uF				
L ₁ : 300 uH, L ₂ , L ₁₁ , L ₂₁ : 950 uH				
R_i : 533.3 Ω				

stresses of diodes and switch is around 181 V, which is consistent with equation [\(9\)](#page-2-9). Fig. 7(c) and Fig. 7(d) show the voltage waveforms of each capacitor, in which u_{C1} is about 133 V, *u*_{C12} is about 266V, *u*_{C22} is about 400 V, *u*_{C11} and u_{C21} are about 133 V. The above results are consistent with equation [\(6\)](#page-2-4). Fig. 7(e) shows the current waveforms of each inductor, in which the average current of the inductor *L*¹ is about 6.99 A, and the average currents of the remaining inductors is about 0.75 A, which is consistent with equation [\(15\)](#page-2-10).

The efficiency of the converter was tested under different output voltages and output power, and the results are shown

FIGURE 7. Experimental waveforms when the input voltage is 48V: (a) duty cycle, input voltage, output voltage and switch s_1 voltage; (b) diodes voltage; (c) and (d) capacitors voltage; (e) inductor current.

FIGURE 8. Efficiency waveforms of the proposed converter: (a) the output voltage varies from 40 V to 400 V; (b) the output power varies between 30-360 W.

FIGURE 9. Experimental prototype loss distribution.

in Fig. 8. Fig. 8(a) shows the prototype efficiency curve with different output voltages when the input voltage is 48 V. Obviously, the prototype efficiency increases first and then decreases with the increase of duty cycle. When the duty cycle is 0.661 and the output voltage is 280 V, the maximum efficiency is close to 94.8%. By changing the load resistance, the prototype efficiency changes with the output power, as shown in Fig. 8(b). When the output power is 240 W, the maximum efficiency is about 94.3%.

The calculated loss distribution of the experimental prototype is shown in Fig. 9. The main losses are on the switch, inductors and the diodes, which are about 6.91 W, 6.4 W and 3.38 W, respectively.

FIGURE 10. Averaged switch model of the prosed converter.

FIGURE 11. Experimental circuit under double-loop control.

V. MATHEMATICAL MODEL AND CLOSED LOOP TEST

By using the circuit averaging technique proposed in [29] to replace the converter switches with voltage and current sources, and the averaged switch model of the proposed converter is obtained, as shown in Fig. 10. The symbol $(∧)$ represents the dynamic changes of the parameter, as shown in [\(30\)](#page-6-0) and [\(31\)](#page-6-1). T_p represents the primary winding of the transformer, T_{S1} , T_{S2} , ..., T_{Sn} are transformer secondary windings.

$$
\langle d(t) \rangle_{Ts} = D + \hat{d}(t)
$$

\n
$$
\langle u_{\rm in}(t) \rangle_{Ts} = U_{\rm in} + \hat{u}_{\rm in}(t)
$$

\n
$$
\langle u_{\rm o}(t) \rangle_{Ts} = U_{\rm o} + \hat{u}_{\rm o}(t)
$$

\n
$$
\langle u_{\rm Ci}(t) \rangle_{Ts} = U_{\rm Ci} + \hat{u}_{\rm Ci}(t)
$$

\n
$$
\langle i_{\rm Lj}(t) \rangle_{Ts} = I_{\rm Lj} + \hat{i}_{\rm Lj}(t)
$$
 (30)

where *i* is 1, 11, 12, ..., n1 or n2, and *j* is 1, 11, 21, ... n1.

$$
\begin{cases}\n u_1 = \hat{d}(t) \cdot \frac{U_{\text{in}}}{D \cdot D'} \\
 i_1 = i_2 = \dots = i_{n+1} = \hat{d}(t) \cdot \frac{I_0}{D \cdot D'}\n\end{cases} (31)
$$

The voltage-current double-loop control scheme is designed, as shown in Fig. 11, where $G_V(s)$ and $G_i(s)$ are the compensation functions of the voltage and current controllers

FIGURE 12. The experimental waveforms: (a) the input voltage jumps from 58 V to 48 V; (b) the input voltage jumps from 48 V to 58 V; (c) the output power jumps from 300 W to 400 W; (d) The output power jumps from 400 W to 300 W.

respectively. $1/V_M$ is the transfer function of the PWM modulator. In addition, $H_1(s)$ and $H_2(s)$ are voltage and current measurement gains, respectively.

The experimental results are shown in Fig. 12. Fig. 12(a) and Fig. 12(b) show the output voltage response when the input voltage changes from 58 V to 48 V and from 48 V to 58V, respectively. The DC and AC quantities of the output

voltage response are shown in Fig. 12(c) and (d) when the output power changes from 300 W to 400 W and from 400 W to 300 W. Obviously, due to the input voltage changes slowly, the output voltage hardly fluctuates when the input voltage changes. The output voltage changes nearly to 10 V when the load jumps, and it returns to the steady-state in 3 ms.

VI. CONCLUSION

In this paper, the application of the coat circuits in the buckboost converter has been discussed in detail. Theoretical analysis and experimental results show that the converter has the following advantages: only one switch is needed, the control and driving circuit are simple which are similar to the conventional buck-boost converter; voltage conversion gain of the buck-boost converter has been improved effectively, and a wide range input/output voltage conversion can be realized; the number of basic cells in the coat circuit can be adjusted according to the needs of the application so that it can be used in many occasions. The above characteristics make the converter suitable for wide input/output voltages applications, like photovoltaic, fuel cell power generation systems.

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BINXIN ZHU (Senior Member, IEEE) was born in Anhui, China, in 1986. He received the B.S. degree from the Hefei University of Technology, Hefei, China, in 2008, and the Ph.D. degree from Chongqing University, Chongqing, China, in 2013, all in electrical engineering. In 2014, he joined the College of Electrical Engineering and New Energy, China Three Gorges University, China, as a Lecturer. He became an Associate Professor and the Group Leader of the Power Elec-

tronics Group, in 2016. His research interests include high power and high step-up dc–dc converters.

SHISHI HU received the bachelor's degree from Anhui Polytechnic University, Anhui, China, in 2018. He is currently pursuing the master's degree in electrical engineering with China Three Gorges University. His research interest includes high step-up voltage conversion ratio dc–dc converter used in renewable energy generation systems.

YU HUANG received the bachelor's degree from the Taiyuan University of Science and Technology, Shanxi, China, in 2018. He is currently pursuing the master's degree in electrical engineering with China Three Gorges University. His research interest includes wide voltage conversion ratio dc–dc converter used in photovoltaic power generation systems.

GUANGHUI LIU received the bachelor's degree from China Three Gorges University, Hubei, China, in 2018, where he is currently pursuing the master's degree in electrical engineering. His research interest includes wide voltage conversion ratio dc–dc converter used in renewable energy generation systems.

XIAOLI SHE received the B.S. and M.S. degrees in electrical engineering from China Three Gorges University, Hubei, China, in 2011 and 2014, respectively. In 2012, she joined the College of Electrical Engineering and New Energy, China Three Gorges University, as a Teaching Assistant. She is currently a Lecturer. Her research interest includes the application of dc–dc converter in renewable energy generation.

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