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Voltage Balancing Control of Cascaded Single-Phase VIENNA Converter Based on One Cycle Control With Unbalanced Loads

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ABSTRACT A research study on a type of cascaded single-phase VIENNA converter (CSVC) is presented in this paper. And a type of DC voltage balancing control strategy for each cascaded module of the CSVC based on improved one-cycle control (I-OCC) is proposed, in which voltage balancing signals are added to the conventional OCC (C-OCC) control loop to cause a difference in the modulation signals of each of the cascaded modules, so that the DC voltages of all modules can be quickly balanced under unbalanced loads. At the same time, the average modulation wave maintains a constant value so that the CSVC achieves a unity power factor operation. The operating principle of the I-OCC strategy is discussed in detail, and the corresponding mathematical relationships are derived. In the proposed strategy, the ability to adjust the DC voltages is also analyzed. Finally, the simulation and experiment results are provided to verify the validity and feasibility of this I-OCC-based voltage balancing control strategy. The control strategy proposed by this paper is also applicable to all other cascaded unidirectional rectifiers.

INDEX TERMS Cascaded single-phase VIENNA converter (CSVC), multilevel converter, unbalanced loads, one cycle control (OCC), voltage balancing control.

I. INTRODUCTION

Line-frequency transformerless cascaded multilevel converters (TCMCs) have attracted significant attention in recent years owing to their potential for use in applications such as the next generation medium voltage power conversion system for adjustable AC speed drives or in constructing an advanced grid interface for renewable energy-based distributed generation systems [1]–[8]. By employing a cascaded H-bridge rectifier (CHB) as the front stage, the TCMC can be connected directly to the medium/high voltage power grid without involving a bulky and expensive line-frequency transformer, which is usually used by conventional multilevel converters [9], [10]. However, the CHB in TCMCs requires a large number of fully controlled power switches that render the converter more complicated during control, gate driving and protection circuits. This eventually reduces the system reliability and increases the implementation costs [11].

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However, in many industrial applications, such as AC speed regulation with pumps or fans, switching power supplies for telecommunications and electric vehicle (EV) battery chargers for level I, bidirectional power flow is not required [12], [13]. In these applications, unidirectional power converters are usually the preferred choices due to advantages of simple control and fewer fully controlled power switch requirements. In [14], a cascaded single-phase bridgeless rectifier (CBR) is proposed, which contains 2 fully controlled switching devices in each module. In [15], a cascaded single-phase diode H-bridge rectifier (CDHR) is proposed, which contains only 1 fully controlled switching devices in each module. In the two unidirectional cascaded rectifiers, the complexity of the control and the cost of the system are both greatly reduced. However, in each module of the above two unidirectional topologies, the switching devices are required to withstand the whole DC side voltage. In this paper, a type of cascaded single-phase VIENNA converter (CSVC) is proposed as shown in Fig. 1, in which each module adopts one switching device and each device

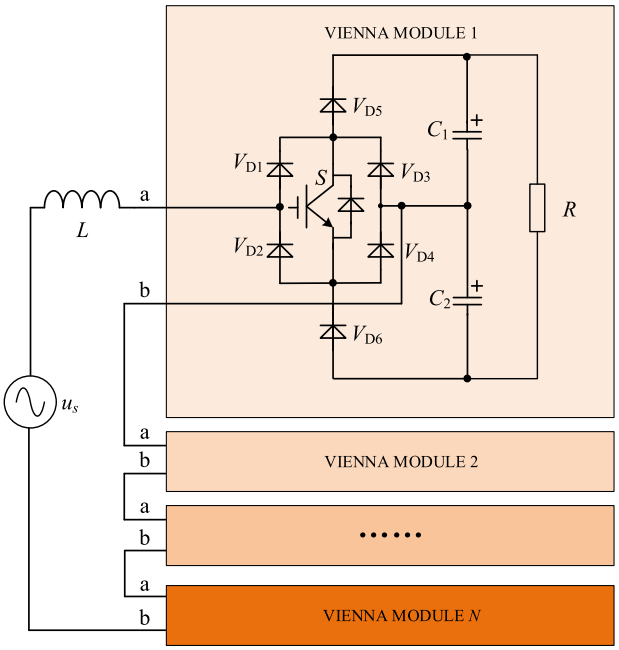

FIGURE 1. Cascaded single-phase VIENNA converter.

withstands only half of the DC side voltage. The proposed CSVC topology has an AC high-voltage input and multiple DC outputs. Compared with CHB, the number of fully controlled switches contained in each module is reduced by 3, and unit power factor operation can still be achieved. A disadvantage of CSVC is that energy cannot flow backwards, however, in applications where only unidirectional power is required, CSVC can be a better choice.

One-cycle control was proposed by K. M. Smedley in 1991 [16]. Since then, it has become increasingly popular in controlling single-phase and three-phase alternating current/direct current (AC/DC) pulse-width modulation (PWM) converters [17]–[20]. When OCC is used in boost-type PWM rectifiers, the input current is automatically forced to be in phase with the grid voltage in the sinusoidal waveform with no requirement for the phase-locked loop (PLL), grid voltage sensors and frame transformation [21]–[23]. These unique features make OCC much easier to implement. However, despite the abovementioned advantages, DC voltage balancing issues need to be considered when OCC is applied to cascaded multilevel converters.

The methods of DC voltage balancing control of cascaded multilevel converters can be divided into two categories by whether it has individual DC voltage controller for each cell [24]. In [25]–[27], each module contains a voltage controller and the PLL is needed in the algorithm, which is a type of category. In [28], the balance of the DC voltage is achieved by changing the modulation wave according to the order of DC voltages, which is another type of category. In the field of OCC, individual PI controller for each cell is used to balance DC voltages in [29], and this type of OCC is called conventional OCC (C-OCC). In [30], an algorithm combining virtual loop mapping and OCC is used to achieve the same purpose, which needs to sort the DC voltages. However, the methods mentioned above in this paragraph are all applied to the cascaded multilevel converters of energy bidirectional flow such as cascaded H-bridges. There is currently no paper discussing the OCC method which needs to sort the DC voltages to realize the voltage balancing control in a cascaded topology with unidirectional power flow, such as the CSVC.

In this paper, an improved OCC (I-OCC) strategy is proposed based on phase-shift PWM, in which the modulation wave of each module is adjusted separately, while the average modulation wave always maintains a constant value determined by the load power. In this way, the duty ratio of the different modules can be adjusted by the different values, so that, the DC voltage of each module with various loads can be quickly balanced. Moreover, all the other abovementioned advantages exhibited by the C-OCC scheme are also retained by the I-OCC scheme. I-OCC has a certain increase in the amount of calculation due to the addition of the voltage balancing part, but it does not cause a large computational burden. For such calculations, such as voltage sequencing, mainstream DSP can be fully competent. In addition, I-OCC can be applied not only to CSVC, but also to other cascaded topologies with unidirectional power flow such as CBR, CDHR.

This paper is organized as follows. In Section II, the core equation of C-OCC applied to the CSVC is derived. Furthermore, the strategy diagram and the PWM modulation diagram of the C-OCC are explained in detail. The principle of voltage regulation on the DC side of the CSVC is briefly illustrated at the end of this section. In Section III, the undistorted condition of the grid side AC current of the CSVC is presented. Based on this condition, the I-OCC is proposed and described in detail. The adjustment ability of this strategy is also discussed. Sections IV and V verify the static and dynamic performance of the proposed I-OCC based on the simulation and experiment results. Finally, Section VI summarizes the conclusions.

II. BASIC PRINCIPLES OF THE CSVC

A. C-OCC FOR CSVC

Applying Kirchhoff's voltage law (KVL) to the switching-cycle average model for the single-phase VIENNA converter shown in Fig. 2 yields:

$$\tilde{u}_{ab} = \tilde{u}_s - j\omega L \cdot \tilde{i}_L \tag{1}$$

where L is the input inductor, i_L is the current of L, u_s is the grid AC voltage, ω is the angular frequency of u_s, u_{ab} is the voltage between point a and point b, $\tilde{u}_s$, $\tilde{u}_{ab}$ and $\tilde{i}_L$ are the phasors of u_s, u_{ab} and i_L, respectively. Considering high-power applications, the value of L is very small. Moreover, in a 50 Hz or 60 Hz power grid, the voltage of L ($j\omega L \cdot \tilde{i}_L$) is also very small relative to the grid AC voltage, and thus can be ignored. Equation (1) can be simplified to:

$$u_{ab} = u_s. \tag{2}$$

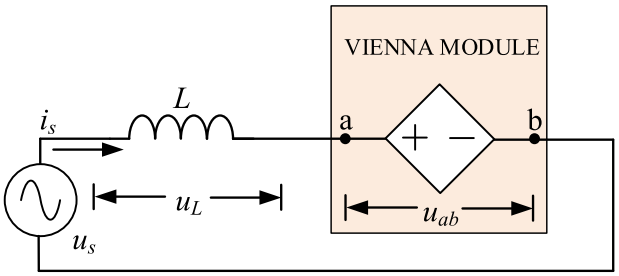

FIGURE 2. Switching cycle average model for the single-phase VIENNA converter.

In a single-phase VIENNA converter, the average voltage of u_{ab} in each switching cycle can be written as:

$$u_{ab} = \begin{cases} (1-d)\cdot\dfrac{E}{2}, & i_L \geq 0 \\ -(1-d)\cdot\dfrac{E}{2}, & i_L < 0 \end{cases} \tag{3}$$

where E is the output DC voltage of the single-phase VIENNA converter and d is the duty cycle of the switching device S [31]. Equation (3) can be simplified as:

$$u_{ab} = (1-d)\cdot\frac{E}{2}\cdot sign(i_L) \tag{4}$$

where $sign(i_L)$ is a sign function that represents the sign of inductor current i_L:

$$sign(i_L) = \begin{cases} 1, & i_L \geq 0 \\ -1, & i_L < 0 \end{cases} \tag{5}$$

Substituting (4) into (2) yields:

$$(1-d)\cdot sign(i_L) = \frac{2}{E}\cdot u_s \tag{6}$$

Considering unity power factor condition, the relationship of u_s and i_L can be expressed as:

$$u_s = R_e \cdot i_L \tag{7}$$

where R_e is the equivalent resistance of the single-phase VIENNA converter. Combining (6) and (7) gives:

$$V_m \cdot (1-d)\cdot sign(i_L) = Rs \cdot i_L \tag{8}$$

where R_s is the sampling resistance of inductor current i_L and V_m is the output value of proportional integral (PI) controller of the output DC voltage in a single-phase VIENNA converter. V_m can be given by:

$$V_m = \frac{E\cdot R_s}{2\cdot R_e} \tag{9}$$

Fig.2 indicates that the grid AC current i_s and the input inductor current i_L are the same current:

$$\begin{cases} i_L = i_s \\ \dfrac{i_L}{sign(i_L)} = |i_L| \end{cases} \tag{10}$$

Applying (10) to (8) yields:

$$V_m \cdot (1-d) = R_s \cdot |i_s| \tag{11}$$

Equation (11) is the core control equation of the C-OCC for single-phase VIENNA converter. To make the above equations applicable for CSVC, some symbols are redefined, where E is the total output DC voltage of the CSVC and R_e is the total equivalent resistance of the CSVC.

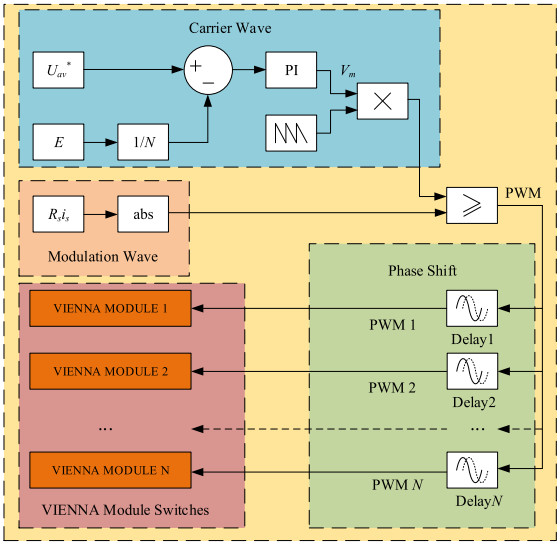

FIGURE 3. C-OCC diagram for CSVC.

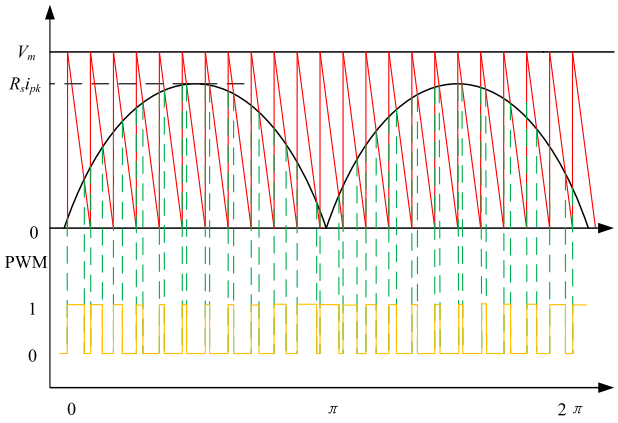

FIGURE 4. PWM modulation diagram of C-OCC.

According to (11), the basic control scheme and its PWM modulation diagram are shown in Fig.3 and Fig.4, respectively, where U_{av}^* is the desired average output DC voltage of N cascaded modules in a CSVC, namely, the rated output DC voltage of each module of the CSVC. In addition, there is one necessary PI controller to maintain the total CSVC DC output voltage. $|R_s i_s|$ is adopted as the unipolar modulation wave in the C-OCC and the carrier wave is a type of sawtooth wave. The actual modulating frequency is far higher than the diagram shown in Fig. 4.

A phase-shift PWM technique is applied to C-OCC for the CSVC to generate multilevel waves ($2N + 1$ types). This technique uses N PWM waves with uniformly-spaced phase differences (π/N) to control the switching devices of N cascaded modules in a CSVC.

B. THE PRINCIPLE OF REGULATION OUTPUT DC VOLTAGE OF CSVC

The N cascaded modules of the CSVC are relatively independent shown in Fig.1. Thus, the principle of regulating the output DC voltage can be separately analyzed through a CSVC module. Referring to Fig.4, when the carrier wave is higher than the modulation wave, the signal of the PWM outputs 1 (high) and the switching device of the corresponding module is in the on state. Therefore, the voltage between point a and point b of the AC input terminal is equipotential and no power flows past the module. The power of the corresponding DC load R is supplied with support capacitors C_1 and C_2. Thus, the output DC voltage of the module decreases. In contrast, when the carrier wave is lower than the modulation wave, the signal of the PWM outputs 0 (low), and the switching device is in the off state. Therefore, the power of R, C_1 and C_2 are supplied by the AC grid (when the grid AC current i_s is positive, C_1 is charged, otherwise C_2 is charged). Thus, the output DC voltage of the module increases.

Therefore, when the value of the modulation wave in each carrier period is increased, the time when the carrier wave is higher than the modulation wave is reduced. Therefore, the time at which the output DC voltage falls decreases. Correspondingly, the time when the carrier wave is lower than the modulation wave is increased. In addition, the time at which the output DC voltage rises increases, the output DC voltage rises to a new steady state value as a whole. In contrast, when the value of the modulation wave in each carrier period is decreased, the output DC voltage decreases to a new steady state value.

According to the actual situation, different modulation waves are used for each single-phase VIENNA module, so that the DC side output voltage of each VIENNA module in the CSVC can be individually controlled. In C-OCC, in addition to a PI controller in the carrier wave part, each module has one to balance the DC voltage, which contains $N + 1$ PI controllers.

III. VOLTAGE BALANCING CONTROL STRATEGY BASED ON I-OCC UNDER UNBALACED LOADS

A. UNDISTORTED CONDITION OF THE GRID SIDE AC CURRENT OF CSVC

Section II-B shows that the CSVC can individually control the DC side output voltage of each module by using different modulation waves, which indicates that the CSVC has the ability to balance the DC side output voltages under unbalanced loads. However, while balancing voltages, it must be ensured that the grid side AC current is undistorted.

The modulation wave of the nth VIENNA module is expressed as $|R_s i_s|\, n, n = 1, 2, \cdots, N$. Thus, the average modulation wave of each VIENNA module in the CSVC is:

$$|R_s i_s|_{average} = (|R_s i_s|\, 1 + \cdots + |R_s i_s|\, N)/N \tag{12}$$

As shown in Fig. 4, in C-OCC, the modulation wave of each VIENNA module in the CSVC is $|R_s i_s|$, hence:

$$|R_s i_s|_{average} = |R_s i_s| \tag{13}$$

The I-OCC proposed in this paper adjusts the modulation waves of the VIENNA modules so that they are not always equal $|R_s i_s|$. Moreover, the modulation waves must satisfy (13), which ensures that the CSVC still satisfies (11) and guarantees that the grid side AC current is undistorted.

B. I-OCC STRATEGY

If there is no voltage balancing control part, when the loads of the CSVC are unbalanced, the DC side output voltages will also be unbalanced. Under the control of the total DC side output voltage PI regulator (in the carrier wave part), the total DC side output voltage of the CSVC remains constant. Therefore, it is assumed that when the DC side output voltage of a VIENNA module is lower than the rated value, there must be another module whose DC voltage is higher than the rated value. In this way, the two VIENNA modules form a control group. In the control group, the higher DC voltage of a module needs to be reduced, and the other one needs to be increased.

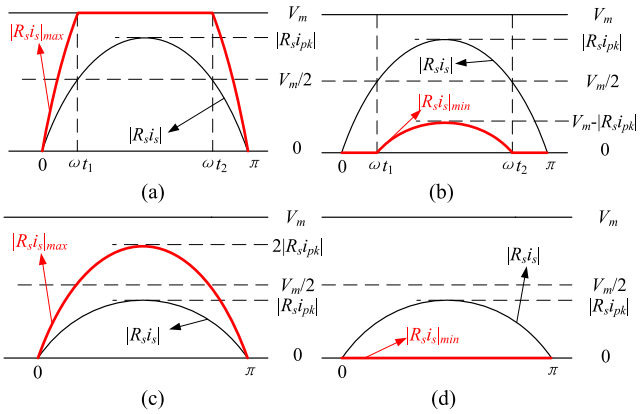

FIGURE 5. Modulation method of I-OCC diagram.

The modulation waves of the two VIENNA modules in a control group is shown in Fig.5. In addition, $\left|R_s i_{pk}\right|$ is the peak value of $|R_s i_s|$. For the convenience of discussion, a ratio M is defined as:

$$M = \frac{\left|R_s i_{pk}\right|}{V_m} \tag{14}$$

According to M, the modulation method can be divided into two cases: At $0.5 < M \leq 1$, as shown in (a) and (b) of Fig. 5, the module with a lower DC side output voltage is modulated by the modulation wave $|R_s i_s|_{max}$. As seen

from Section II-B, the value of the modulation wave in each carrier cycle is increased, thereby increasing the DC side output voltage. Similarly, the module with a higher DC output voltage uses the modulation wave $|R_s i_s|_{min}$ to reduce the voltage. At $0 < M \leq 0.5$, the modulation waves used in the control group are $|R_s i_s|_{max}$ in (c) and $|R_s i_s|_{min}$ in (d) of Fig. 5. There are two reasons for using this modulation method:

1) The modulation process must satisfy the undistorted condition of the grid side AC current of the CSVC (III-A). The average value of $|R_s i_s|_{max}$ and $|R_s i_s|_{min}$ is $|R_s i_s|$, so the condition is satisfied.

2) To balance the DC side output voltage as quickly as possible, the modulation wave is selected as the limit value under undistorted condition. For instance, at $0.5 < M \leq 1$ and in the time range $0 \sim \omega t_1$, if $|R_s i_s|_{max}$ is increased by a certain amount and $|R_s i_s|_{min}$ has reached the minimum. Thus, the average value of $|R_s i_s|_{max}$ and $|R_s i_s|_{min}$ will be greater than $|R_s i_s|$, and distortion of i_s will occur.

In detail, in (a) and (b) of Fig.5, at $0 \leq \omega t < \omega t_1$ and $\omega t_2 \leq \omega t \leq \pi$, $|R_s i_s|_{min} = 0$, this means that the module with voltage drop has no energy input. For the topology with unidirectional energy flow, since energy cannot be fed back, the input without energy is the fastest way to reduce the voltage. Similarly, at $\omega t_1 \leq \omega t < \omega t_2$, $|R_s i_s|_{max} = 1$,this shows that the module is maximizing the input of energy, and the voltage is increased to the maximum speed. At this time, $|R_s i_s|_{min} \neq 0$ and has a little energy input, which is to satisfy the formula (13) to achieve one-cycle control while adjusting the DC voltages.

There are N VIENNA modules in the CSVC. When N is even, $N/2$ control groups are formed. When N is odd, $(N-1)/2$ control groups and a separate VIENNA module are formed. The modulation wave used by this separate module is $|R_s i_s|$. From the above analysis, the average modulation wave of each control group is $|R_s i_s|$, then:

$$(\frac{N-1}{2} \cdot |R_s i_s| \cdot 2 + |R_s i_s|)/N = |R_s i_s| \tag{15}$$

Equation (15) shows that under the condition that N is odd, the I-OCC strategy still satisfies the undistortion condition.

The control groups are allocated, as shown in Fig. 6. When $U_1, U_2, \cdots, U_N$ and U_N are the instantaneous values of the DC side output voltages of each module and $U_{max}, \cdots, U_{mid}, \cdots, U_{min}$ are the voltages of the DC side after sorting, obviously $U_{max} \geq \cdots \geq U_{mid} \geq \cdots \geq U_{min}$. The voltage adjustment amount is defined as the difference between the instantaneous voltage value and its rated value. To make the voltage adjustment amount of the two VIENNA modules in one control group close to each other, the VIENNA module with the highest voltage and the lowest voltage is combined into one control group, the VIENNA modules with the second highest voltage and the second lowest voltage form a control group, and so on. If N is odd, the VIENNA module corresponding to U_{mid} is independently controlled.

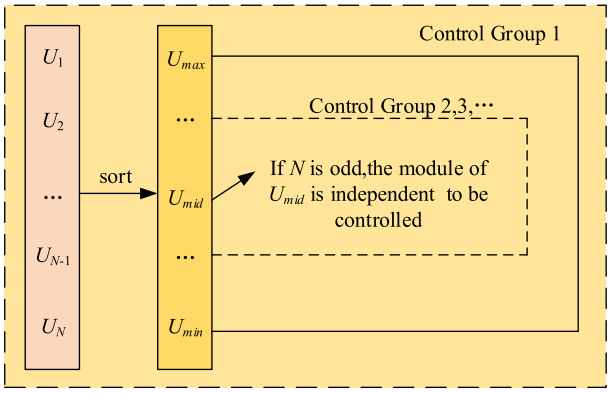

FIGURE 6. Distribution method of control groups.

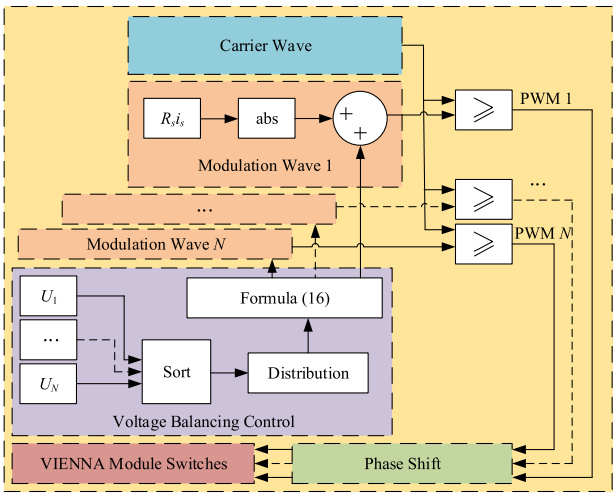

FIGURE 7. I-OCC diagram for CSVC.

Based on the above discussion, the I-OCC diagram for the CSVC is shown in Fig. 7. Compared with the C-OCC, the carrier wave part, the carrier phase shifting part and the VIENNA module switching part of the I-OCC are still maintained. The difference is that the voltage balancing control part is added, and the number of modulation waves is also increased to N to separately control of the N VIENNA modules in the CSVC. It should be noted that I-OCC has only one necessary total DC side output voltage PI regulator, but C-OCC has $N+1$ PI regulators. The steps of I-OCC are summarized as follows:

1) Sort of DC side output voltages of the VIENNA modules in the CSVC in real time.

2) Distribute the control group, as shown in Fig. 6.

3) Produce the modulation wave in the control group, as shown in Fig. 5, and calculate the modulation amount $\Delta |R_s i_s|$ of the modulation wave according to (16):

$$\Delta |R_s i_s| = \begin{cases} Vm - |R_s i_s|, & M > 0.5 \text{ and } \omega t_1 \leq \omega t < \omega t_2 \\ |R_s i_s|, & \text{other conditions.} \end{cases} \tag{16}$$

4) Finally, the modulation waves of I-OCC are obtained by subtracting (higher DC side output voltage of all control groups) or adding (lower DC side output voltage of all control groups) $\Delta |R_s i_s|$ on the basis of $|R_s i_s|$.

$$|R_s i_s|\, n = |R_s i_s| \pm \Delta |R_s i_s| \tag{17}$$

When N is odd, the modulation wave of the DC side output voltage sorted in the middle is $|R_s i_s|$.

C. ADJUSTMENT ABILITY ANALYSIS

In the following, the adjustment ability of the I-OCC is analyzed when the loads are unbalanced. Under I-OCC, the CSVC satisfies (11) and operates at a unity power factor:

$$\begin{cases} R_e = \dfrac{u_s}{i_L} = \dfrac{u_s}{i_s} = \dfrac{U_s}{I_s} \\ P_{in} = U_s \cdot I_s \end{cases} \tag{18}$$

where U_s and I_s are the root mean square (RMS) values of the grid side AC voltage and current of the CSVC, respectively, and P_{in} is the input power of the CSVC.

According to (18):

$$Re = \frac{U_s^2}{P_{in}} \tag{19}$$

Substitute (19) into (9):

$$V_m = \frac{E \cdot R_s}{2U_s^2} \cdot P_{in} \tag{20}$$

The peak value of AC side current of the CSVC is:

$$\left|i_{pk}\right| = \sqrt{2} I_s = \frac{\sqrt{2}}{U_s} \cdot P_{in} \tag{21}$$

Combining (20), (21) and (14) yields:

$$\frac{\left|R_s i_{pk}\right|}{V_m} = \frac{2\sqrt{2} U_s}{E} = M \tag{22}$$

It is known from (22) that in a given system, U_s, E, and R_s are determined, so the ratio M is a constant value regardless of the DC loads. The ratio of $\left|R_s i_{pk}\right|$ and V_m is constant.

The adjustment of the DC side output voltage of the CSVC is essentially the redistribution of the output power. Since the RMS of the grid side AC voltage is constant, the magnitude of the RMS value of the grid side AC current can reflect the level of the power by the second equation in (18). From Section II-A, $|R_s i_s|$ is the average modulation wave in one period and $R_s I_s$ is the RMS of $|R_s i_s|$. Additionally, R_s is determined, and $R_s I_s$ can also reflect the level of the power.

At $0.5 < M \leq 1$, as shown in Fig.5 (a) and (b), the RMS values of $|R_s i_s|_{max}$ and $|R_s i_s|_{min}$ reflect the limit value of the output power in the control group. The maximum regulated power ratio Pr_{max} is defined as (23), shown at the bottom of this page.

Based on the definition of the RMS, $RMS\,(|R_s i_s|_{max})$ and $RMS\,(|R_s i_s|_{min})$ are calculated by using (24) and (25), as shown at the bottom of this page, respectively. It can be seen that $R_s I_s$ is eliminated by the mathematical relationship in Pr_{max} and ωt_1 is actually a function of M:

$$\omega t_1 = arcsin(\frac{1}{2M}) \tag{26}$$

Thus, Pr_{max} is uniquely determined by M. When the ratio of the output power of two VIENNA modules in a control group is higher than the maximum regulated power ratio Pr_{max}, I-OCC will exceed the adjustment ability. Taking Fig. 8 as an example, in a given CSVC system, the maximum power ratio plane is calculated according to (23). R_a and R_b

$$Pr_{max} = RMS(|R_s i_s|_{max}) / RMS(|R_s i_s|_{min}) \tag{23}$$

$$\begin{aligned} RMS(|R_s i_s|_{max}) &= \sqrt{\frac{1}{\pi}\int_0^{\pi} |R_s i_s|_{max}^2 d\omega t} \\ &= \sqrt{\frac{1}{\pi}\left(\int_0^{\omega t_1} (2\sqrt{2} R_s I_s sin\omega t)^2 d\omega t + \int_{\omega t_1}^{\omega t_2} (V_m)^2 d\omega t + \int_{\omega t_2}^{\pi} (2\sqrt{2} R_s I_s sin\omega t)^2 d\omega t\right)} \\ &= \sqrt{\frac{1}{\pi}\left[8Rs^2 Is^2 (\omega t_1 - \frac{sin(2\omega t_1)}{2}) + V_m^2(\pi - 2\omega t_1)\right]} \\ &= \sqrt{\frac{1}{\pi}\left[8(\omega t_1 - \frac{sin(2\omega t_1)}{2}) + \frac{2}{M^2}(\pi - 2\omega t_1)\right]} \cdot R_s I_s \end{aligned} \tag{24}$$

$$\begin{aligned} RMS(|R_s i_s|_{min}) &= \sqrt{\frac{1}{\pi}\int_0^{\pi} |R_s i_s|_{min}^2 d\omega t} \\ &= \sqrt{\frac{1}{\pi}\left(\int_{\omega t1}^{\omega t2} (2\sqrt{2} R_s I_s sin\omega t - V_m)^2 d\omega t\right)} \\ &= \sqrt{\frac{1}{\pi}\{4\,[\pi - 2\omega t1 + sin(2\omega t1)] + \frac{2}{M^2}(\pi - 2\omega t1) - \frac{16}{M} cos(\omega t1)\}} \cdot R_s I_s \end{aligned} \tag{25}$$

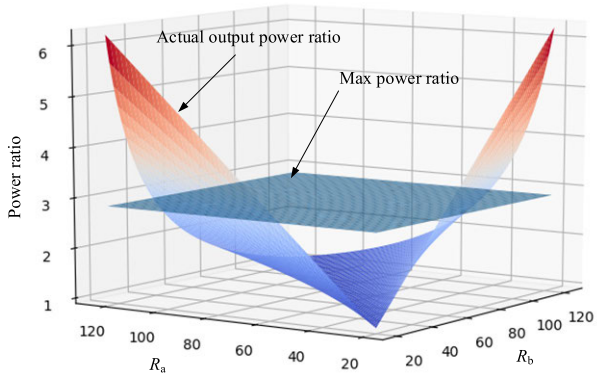

FIGURE 8. Max power ratio diagram with I-OCC under unbalanced loads condition.

are the DC loads of two VIENNA modules in one control group. Under the control of I-OCC, the DC voltages are balanced, so the magnitude of the DC loads reflects the output power of the VIENNA module, and the actual output power ratio can be calculated. Below the maximum power ratio plane, the actual output power ratio is lower than Pr_{max}, which is the I-OCC controllable area, and the intersection line is the critical area. While above the plane, the actual output power ratio is higher than Pr_{max}, which is the I-OCC uncontrollable area, where I-OCC loses its ability to regulate. To ensure the normal adjustment of the I-OCC, it is necessary to ensure that the actual output power ratio of the two modules in the control group is lower than Pr_{max}, which is called the maximum power ratio condition.

At $M < 0.5$, as shown in Fig.5 (c) and (d), the RMS of $|R_s i_s|_{min}$ is 0. Therefore, the maximum regulated power ratio Pr_{max} tends to infinity. In this case, the I-OCC does not have a maximum power ratio condition.

IV. SIMULATION RESULTS

To verify the correctness and effectiveness of I-OCC, simulation studies have been conducted by using Simulink. Simulation parameters are shown in Table 1.

TABLE 1. The Parameters of Simulation of CSVC.

Parameter	Quantity	Values
u_s	grid side input voltage	220 V
U_{av}^*	rated output voltage of a module	250 V
	number of cascaded modules	3
L	input inductor	2.2 mH
C_1, C_2	DC support capacitor	4400 μF
f_{sw}	switch frequency	20 kHz

Fig. 9 shows the simulation results of the CSVC with the above configuration when the balanced loads are abruptly changed to unbalanced and when the C-OCC without DC voltages balancing part is changed to I-OCC. R_1, R_2 and R_3 are defined as the DC side loads of the three VIENNA modules of the CSVC. As shown in Fig. 9 (a), at $t = 0s$ and

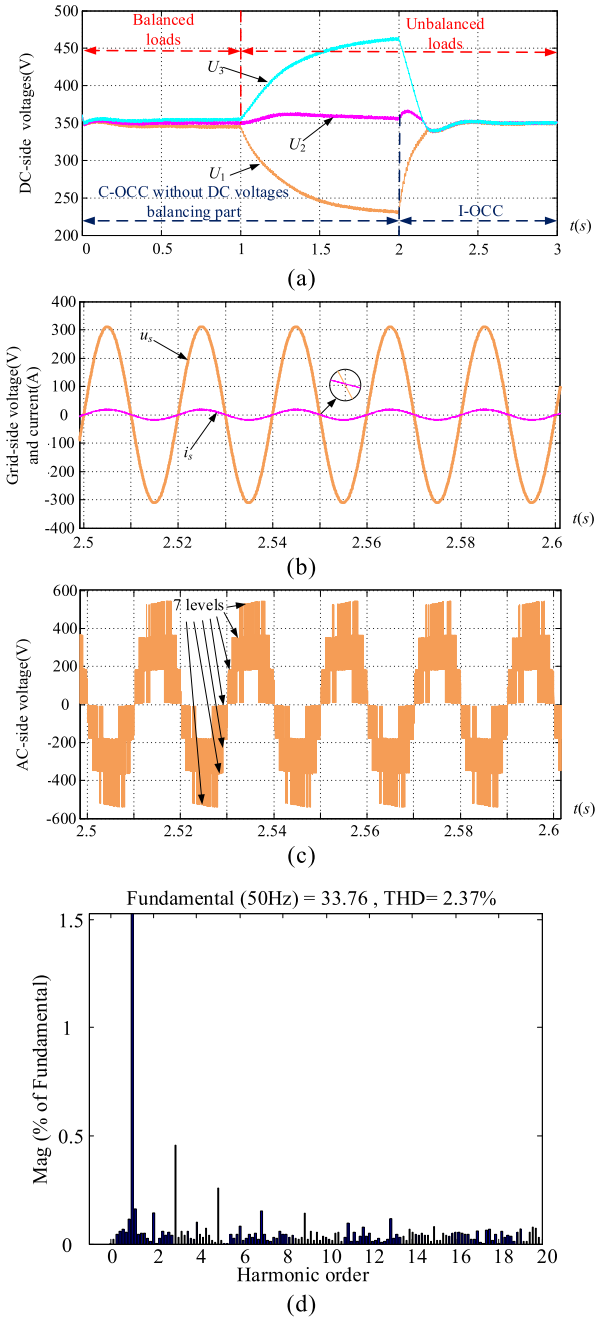

FIGURE 9. Simulation result without and with I-OCC under unbalanced loads condition (a) dc side voltages of CSVC without and with I-OCC (b) grid-side voltage and current with I-OCC (c) ac side multilevel voltage with I-OCC (d) the THD of grid side current with I-OCC.

$R_1 = R_2 = R_3 = 150\Omega$, C-OCC is applied, and the loads are balanced. At this time, due to the role of carrier phase-shift control, even if the DC side loads are in a balanced state, there are significant differences in the DC side output voltages U_1, U_2, and U_3, but they are basically balanced. At $t = 1s$, the DC side loads are changed to unbalanced: $R_1 = 100\Omega$, $R_2 = 150\Omega$, and $R_3 = 200\Omega$. At this time, the output voltages are severely unbalanced. At $t = 2s$, the control method is changed to I-OCC, and it can be seen that the DC side output

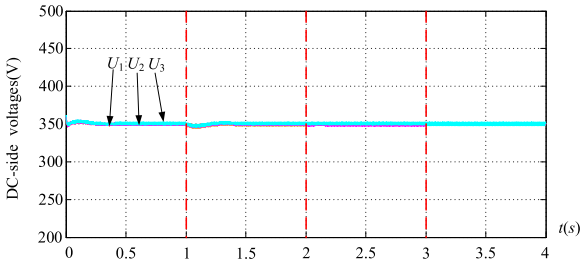

FIGURE 10. DC side voltages simulation result of CSVC with I-OCC under variable unbalanced loads conditions.

TABLE 2. The Parameters of DC Side Loads in Fig. 10.

Time (t/s)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
0	150	150	150
1	100	150	200
2	300	100	120
3	150	200	150

voltages are quickly adjusted to reach balanced state and follow the rated voltage U_{av}^*. The effect of the unbalanced loads along with the carrier phase-shift control on the DC side output voltages is eliminated. Fig. 9 (b), (c) and (d) are the simulation results of the waveform of the grid side AC voltage and current, the AC side voltage simulation waveform and the grid side AC current total harmonic distortion (THD) under an unbalanced load and I-OCC control, respectively. Fig. 9 (b) illustrates that the I-OCC satisfies the control requirements for the grid side AC voltage and current to achieve unity power factor operation. Fig. 9 (c) shows that I-OCC can generate multilevel voltages by carrier phase shifting. This figure also shows that the CSVC is a type of multilevel converter (MC). Three cascaded modules are used in this simulation, so a total of 7 levels of voltages are produced. Fig. 9 (d) shows that the I-OCC satisfies the requirement for the grid side AC current THD. In this simulation, the THD of grid side AC current is only 2.37%, and the waveform is basically a sine wave.

To further verify the dynamic characteristics of the I-OCC, the DC side loads are continually changed several times. The parameters of DC side loads are shown in Table 2 and the simulation results are shown in Fig. 10. During the adjustment process, the DC voltage of each module is dynamically changed. When the voltage changes, the voltage order also changes, and regroups to change the modulation waves. It can be seen that during the entire process, the DC side output voltages keep in balance, and only slight fluctuations occur when the simulation parameters change, which reflects the excellent dynamic performance of the I-OCC.

To verify the adjustment speed of the I-OCC to the DC side output voltages, the C-OCC with PI-based voltages balancing control part is compared, and the simulation results are shown in Fig. 11. At the same time, parameters of PI controller are selected by using Simplex Method. At $t = 0s$ and $R_1 = R_2 = R_3 = 150\Omega$, the loads are balanced, then both control

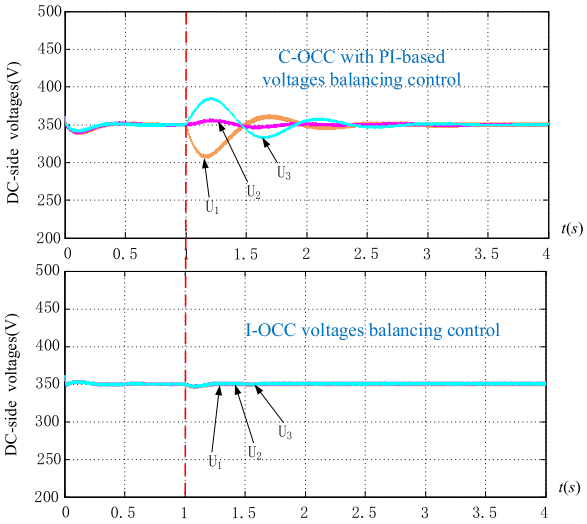

FIGURE 11. DC side voltages simulation result of CSVC with PI-based voltage balancing control and I-OCC under unbalanced loads conditions.

TABLE 3. The parameters of the CSVC prototype.

Parameter	Quantity	Values
u_s	grid side input voltage	80 V
U_{av}^*	rated output voltage of a module	120 V
	number of cascaded modules	3
L	input inductor	2.2 mH
C_1, C_2	DC support capacitor	2200 μF
f_{sw}	switch frequency	20 kHz

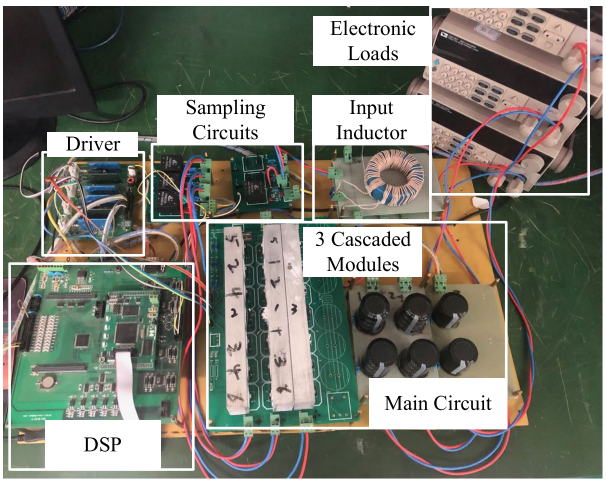

FIGURE 12. Scaled-down experiment prototype.

methods are effective. At $t = 1s$, the DC side loads are changed to unbalanced: $R_1 = 100\Omega$, $R_2 = 150\Omega$, and $R_3 = 200\Omega$. The voltage balancing control with the PI regulator can also finally balance the voltages. However, compared with the I-OCC, it is obvious that the dynamic response is poorer, the adjustment period is longer, and the fluctuation range is larger. Under the control of I-OCC, there is only a slight fluctuation at the moment of the mutation, and the DC side output voltages are quickly adjusted to keep in balance.

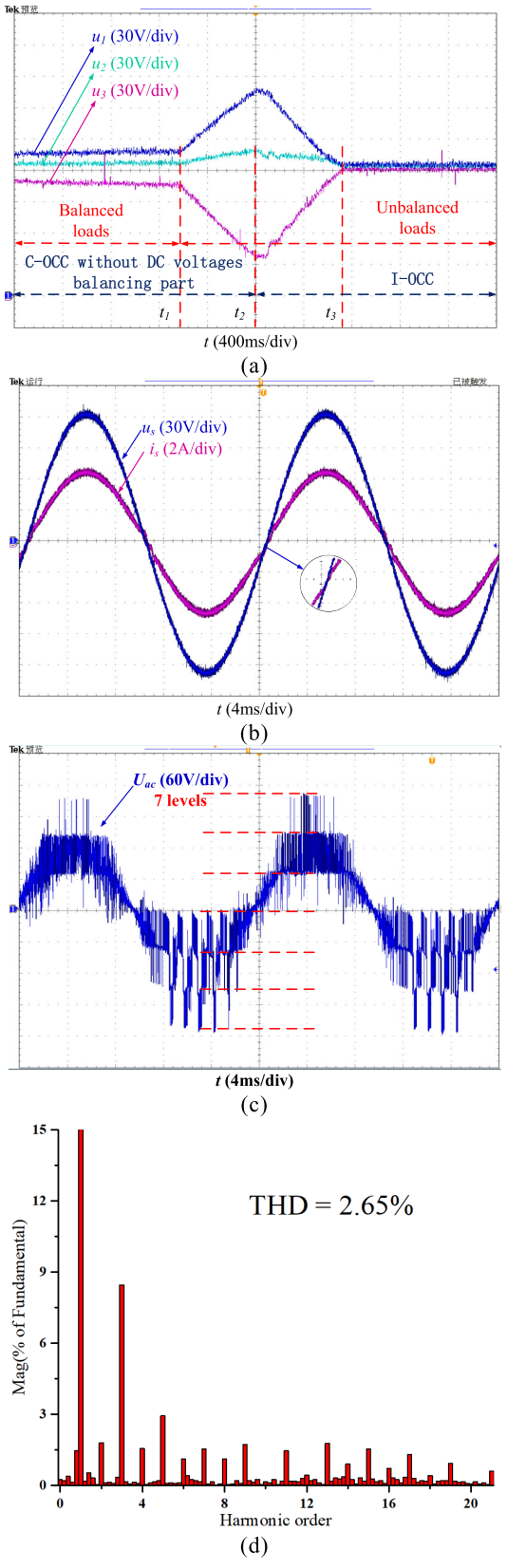

FIGURE 13. Experiment results without and with I-OCC under unbalanced loads conditions: (a) DC side voltages of CSVC without and with I-OCC, (b) grid-side voltage and current with I-OCC, (c) AC side multilevel voltage with I-OCC and (d) the THD of the grid side current with I-OCC.

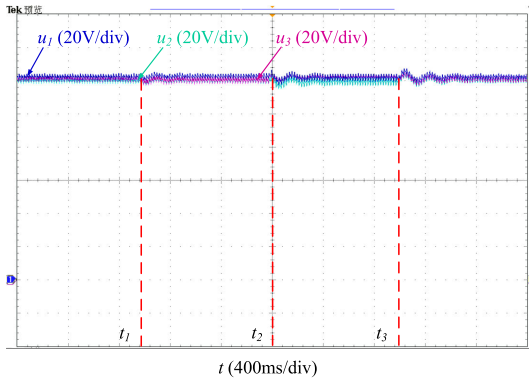

FIGURE 14. DC side voltages experiment result of the CSVC with I-OCC under variable unbalanced load conditions.

V. EXPERIMENT RESULTS

A scaled-down experiment CSVC prototype with three cascaded modules is built to further verify the I-OCC performance. The parameters are shown in Table 3. Fig. 12 shows the prototype and a TMS320F28335 digital signal processor (DSP) is used to the achieve control method.

The experimental design follows the simulation. As shown in Fig. 13(a), the loads are balanced, and the C-OCC without DC voltages balancing control part is applied at the beginning. The difference between output DC voltages is due to the influence of the phase-shift PWM control. At t_1, the DC output loads are suddenly changed to unbalanced ($R_1 = R_2 = R_3 = 150\Omega$ at the beginning, and $R_1 = 100\Omega$, $R_2 = 150\Omega$, $R_3 = 200\Omega$ at t_1), and the difference becomes more obvious. The DC voltages of the CSVC start to quickly adjust when the I-OCC is used at t_2. Finally, the voltages are completely balanced at t_3. Fig. 13(b) shows that unity power factor operation is achieved and the grid side input current is undistorted. As an multilevel converter, the experiment CSVC prototype with three cascaded modules has 7 types of AC side voltages, as shown in Fig. 13(c), and the THD of the grid side input current is low (2.65%), as shown in Fig. 13(d).

Subsequently, the CSVC prototype is always controlled by using I-OCC, as shown in Fig. 14. The loads are suddenly changed at t_1, t_2 and t_3, as shown in Table 2. It can be seen that the output voltages quickly reach a balanced state when there is only a slight fluctuation in the moment of sudden load change. This behavior means that the control of I-OCC is strongly robust.

Fig. 15 shows a comparative experiment of balancing voltages between the I-OCC and C-OCC with PI-based DC voltages balancing control part. Under the same condition ($R_1 = R_2 = R_3 = 150\Omega$ at the beginning, and $R_1 = 100\Omega$, $R_2 = 150\Omega$, $R_3 = 200\Omega$ at t_1), the PI-based control method spends more time balancing the voltages when the loads are changed to the unbalanced state. At the same time, the voltage fluctuation under C-OCC with PI-based DC voltages balancing control is more severe. This severity reflects the rapidity of the I-OCC control method.

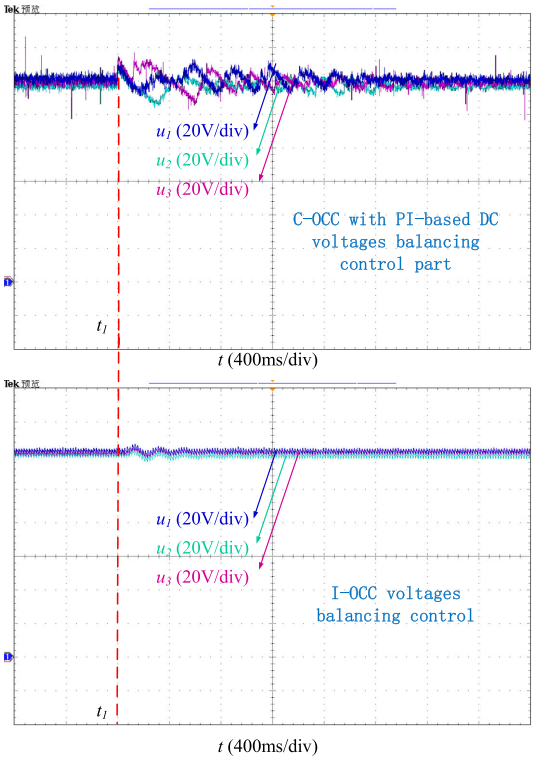

FIGURE 15. DC side voltages experiment result of the CSVC with PI-based voltage balancing control and I-OCC under unbalanced load conditions.

VI. CONCLUSION

This paper proposes an improved one-cycle control strategy. Based on the conventional one-cycle control, the proposed strategy adds a voltage balancing control part and expands the application capability of one-cycle control, which rapidly balances the voltages of DC loads. The two operating states classified by the ratio M of the CSVC are discussed. In addition, the adjustment ability of the improved strategy is also studied. Simulations and experiments verify the correctness and effectiveness of the improved strategy. On the other hand, the proposed I-OCC is compared with the C-OCC with PI-based DC voltages balancing control method and I-OCC has satisfied dynamic performance.

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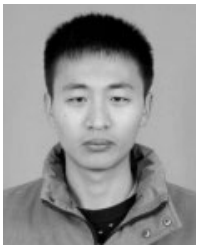

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