IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received May 10, 2020, accepted May 16, 2020, date of publication May 20, 2020, date of current version June 4, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2995853

An Ultra-Low Power, Adaptive All-Digital Frequency-Locked Loop With Gain Estimation and Constant Current DCO

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This work was supported by the National Research Foundation of Korea (NRF) Grant funded by the Korean Government (MSIP) under Grant 2014R1A5A1011478.

ABSTRACT In this paper, an ultra-low power, adaptive all-digital integer frequency-locked loop (FLL) with gain estimation and constant current digitally controlled oscillator (DCO) for Bluetooth low energy (BLE) transceiver in Internet-of-Things (IoT) is presented. For locking DCO frequency closest to the target channel, it adaptively controls capacitor banks with binary algorithm. With decrease in frequency resolution, DCO clock counts for each capacitor bank bit evaluation dynamically increases with the proposed technique for accurate frequency tracking. For compensating PVT variations and finding the BLE frequency deviation, the configurable digital DCO gain estimation is incorporated. The low power and constant current DCO operates in sub-threshold region and its power consumption is minimized by g_m/I_D methodology optimization, constant current source for limiting current in DCO core through adaptive low-dropout regulator (LDO) and lowering the supply voltage. The proposed design is integrated in an ADPLL for BLE transceiver and it is fabricated with 1P6M TSMC 55 nm CMOS technology. The all-digital adaptive FLL is fully synthesizable and its area is 1800 μm^2 with 1.233 K gate count. The RMS current consumption is 103.32 μA from 1 V voltage supply with 103.32 μW power requirement. The experimental results reveal, DCO draws 480 μA current from 0.55 V supply voltage at center frequency. It has frequency resolution of 4.8 kHz. The oscillator PN, FOM and FOM_T at 1-MHz offset frequency from 2.44 GHz carrier frequency are −122.85 dBc/Hz, 196.38 dBc/Hz and 208.19 dBc/Hz, respectively.

INDEX TERMS Adaptive controller, all-digital frequency locked loop, digitally controlled oscillator, gain estimation, constant current, LDO, ultra-low power, synthesizable.

I. INTRODUCTION

Recently, the research on IoT devices for low power applications are increasing rapidly [1]–[4]. Ultra-low power, small area and low cost designs are the fundamental requirements for battery operated IoT devices. The BLE is very famous low power wireless connectivity standard in IoT applications. The BLE standard has been adopted as a popular solution for wireless connectivity in the IoT applications [5]–[8]. Similar to other wireless RF transceivers, BLE supported devices place a design challenges on the jitter performance, phase noise (PN) and modulation bandwidth of frequency locked loop. In RF transceiver applications, frequency synthesizer, frequency multiplier and phase locked loop (PLL) demand

The associate editor coordinating the review of this manuscript and approving it for publication was Yong Chen.

circuits which bring oscillator frequency accurately closest to the target frequency. This essential task is performed by a frequency locked loop which is a vital circuit in RF devices and clock multipliers [9]–[11]. The type-1 PLL, depicted in Fig. 1(a) is composed of phase detector (PD), loop filter (LP) and voltage controlled oscillator (VCO) [12]. The FLL operation is performed in negative feedback loop with phase detector. It is simplest PLL due to single integrator in its control loop and high stability margin, unlike type-2 PLL [13]. However, if there is frequency drift, it cannot achieve zero average steady state phase error. Also, it has locking range constraint, limited disturbance capability and significant reference spur due to persistent ripples on the VCO control line [12], [14]. In analog type-2 PLL, a phase and frequency detector (PFD) acts as analog FLL to bring VCO frequency closest to target frequency [15]–[17]. The PFD circuit compares the f_{ref} and f_{div} to generate up/down signals and tunes VCO frequency closest to the target frequency as shown in Fig. 1(b). Other than digital PFD technique, for the high frequency PLLs a voltage multiplier makes a trick by multiplying f_{ref} and f_{div} signals and getting a phase variation in DC to bring VCO frequency close to target frequency.

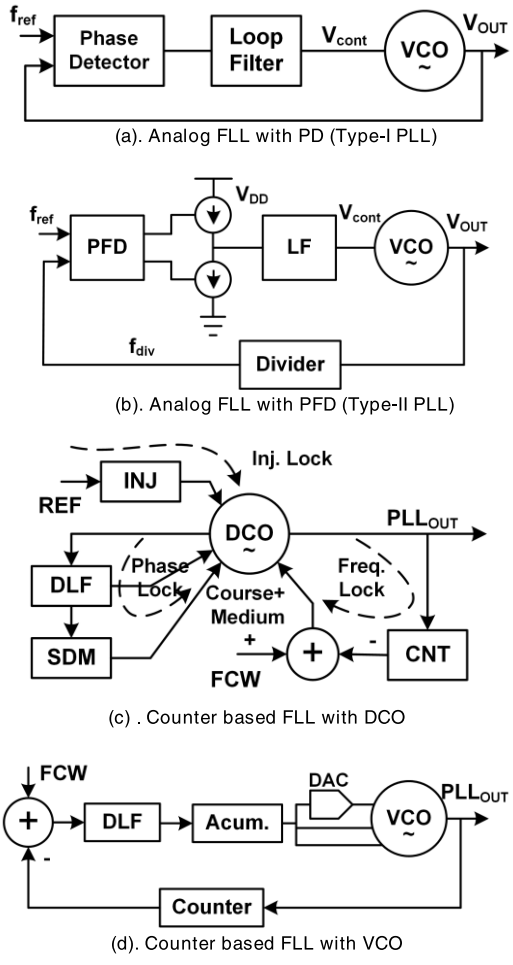


FIGURE 1. Conventional FLL structures in PLL.

These PFD circuits drive charge pump circuitry which cause an increase in area, power and lock time. The charge pump suffers from charge injection and clock feed through. However, type-2 PLL achieves zero average steady-state phase error under both frequency drifts and phase angle jumps, unlike type-1 PLL. Also due to the fast scaling in CMOS technologies, analog FLL circuits suffer from process, voltage and temperature (PVT) variations, loop filter encounters current mismatch, capacitor leakage and limited dynamic range which cause undesired performance in RF applications [18]. To overcome these limitations of PFD, a digital FLL is introduced [19]–[24]. A counter senses VCO/DCO output frequency and then the value is compared with a target frequency control word (FCW) as shown in the Fig. 1(c) and Fig. 1(d). It reduces power consumption by eliminating the charge pump and lock time reduces by introducing coarse and fine tracking strategies. Different oscillator topologies are investigated for improving phase noise (PN) with small area and low power. The single LC-tank oscillators are compact in size but shows inadequate PN. The multi-core VCOs enhance PN and figure-of-merit (FOM) at the cost of additional chip area. Recently, the single-core multi-LC-tank oscillator topologies are reported with compact size and high FOM for mm-wave wireless applications [25], [29].

The digital designs are proven robust to these PVT variations. This brings the idea of all digital FLL design for the wireless applications which meets strict frequency requirements of RF domain [22], [30]. All digital FLL offers significant advantages as compared to analog FLL. Analog FLL requires more area, strict supply voltage requirements, large loop filter capacitors and severe degradation in the performance due to capacitor leakage, current mismatch and PVT variations. Also implementation of state of the art loop calibration algorithms to encounter the PVT variations are not easily possible in analog domain [31]. While the all digital FLL offers advantages like small on chip area, fast settling, reconfigurable loop filter and portability to other process technologies. Current frequency tracking methodologies [19]–[25] use fixed DCO clock cycles for frequency locking closest to the target frequency. The PLL output frequency is measured and its difference from FCW is provided to DCO. The counting duration of DCO output significantly affects the accuracy and the lock time. In prior works, fixed counting duration is used which results large deviation of the locked frequency from the target one. To overcome this limitation, an adaptive FLL is proposed which efficiently adjust the counting mask automatically and significantly improves the locked frequency accuracy. This paper focuses on all-digital frequency loop for BLE applications in IoT devices. The major contributions of proposed design are as follows: (a) An adaptive all digital frequency loop in which DCO clock cycles are counted adaptively in an increasing order as the frequency resolution decreases to achieve DCO fine tuning, (b) DCO gain estimation which is the single bit frequency resolution for PVT variations and frequency-shift keying (FSK) modulation in RF transmitter, (c) Four different configurable

operating modes for various control levels of DCO frequency and (d) Constant current DCO.

The rest of this paper is organized as follows: Section II presents the design of the proposed all-digital frequency-locked loop (ADFLL). The detailed description of the proposed architecture at building block levels is included in Section III; Section IV shows the simulation and experimental results; Finally, the paper is concluded in Section V.

II. PROPOSED ADAPTIVE ALL-DIGITAL FLL DESIGN

An all-digital phase locked loop structure is composed of integer and fractional loops. The fractional loop is typically composed of, digital loop filter (DLF), time-to-digital converter (TDC) and DCO [32]. In integer loop, also known as frequency-locked loop, the DCO coarse tuning is achieved by controlling the coarse (MSB, LSB) capacitor banks. It tunes the free running DCO frequency closest to target channel frequency which is an integer multiple of reference clock. It reduces the frequency locking time and DCO fine tuning range. It operates only once in the beginning when one of the forty BLE frequency channels is selected. When integer loop finishes, then the fractional loop starts its operation. The fractional loop accommodates the fractional part of frequency and aligns the phases of both DCO and reference clocks in the lock state. This loop is always active while ADPLL is operating. In proposed design, before fractional loop, DCO gain is estimated for compensating PVT variations and FSK direct modulation. Numerous techniques for integer loop design are discussed in literature [19], [20]. This paper explores a very simple, reliable adaptive design for all-digital frequency-locked loop in ADPLL applications for BLE transceiver. The binary algorithm is used in a dynamic adaptive way for evaluating binary bit values of MSB and LSB capacitor banks.

A. ADAPTIVE FLL ALGORITHM

Fig. 2 explains the relationship between reference and DCO frequencies. The highly reliable fixed reference clock frequency f_{REF} is slower than that of DCO. Therefore, single reference clock cycle accommodates multiple DCO clocks. If the DCO clock cycles are measured for N_{REF} number of reference clock period T_{REF}, then the total duration, T_M is given in (1) as:

$$T_M = \frac{N_{REF}}{f_{REF}} = N_{REF} T_{REF} \tag{1}$$

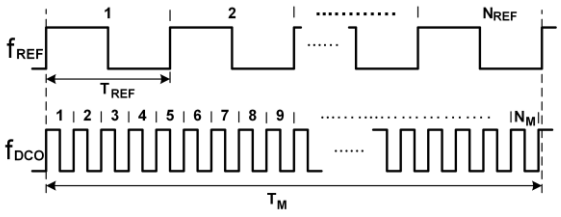


FIGURE 2. Reference frequency and DCO frequency relationship.

If N_M DCO clock cycles are measured in T_M duration, then the DCO frequency is found in (2) as follows:

$$f_{DCO} = \frac{N_M}{T_M} = \frac{N_M}{N_{REF}} f_{REF} \tag{2}$$

Now, the target frequency f_{CH} for a particular BLE channel is already known, then the number of DCO clock cycles, N_C is calculated mathematically as follows in (3):

$$N_C = \frac{f_{CH}}{f_{REF}} N_{REF} \tag{3}$$

The DCO capacitor banks are tuned in such a way that the measured N_M and calculated N_C number of DCO clock cycles are same. When this condition ($N_M \approx N_C$) is achieved then the DCO frequency f_{DCO} is closest to the target channel frequency f_{CH}. In ADPLL design, this goal is achieved in the integer loop before the gain estimation and fine tuning and phase locking in fractional loop. Thus, the design of FFL is very critical in order to achieve an accurate target frequency in an ADPLL.

In this paper, a simple, hardware friendly adaptive FLL design for integer loop is presented. For the evaluation of each bit of coarse capacitor bank, DCO frequency is measured for an adaptive number of reference clock cycles instead of fixed duration. The number of calculated DCO clock cycles are also adaptive with respect to the capacitor bit position. In the proposed design, the adaptive number of reference clock period, $N_{REF}(n)$ is defined as follows in (4):

$$N_{REF}(n) = 2^{N-n} \tag{4}$$

where, N is the total number of bits in the binary capacitor control word (CCW) for MSB and LSB capacitor banks. The n is current bit position which is being evaluated for DCO frequency measurement. Its range is $0 \sim N-1$. The $N_{REF}(n)$ is the function of capacitor bank bit position and its value increases dynamically as n decrements from $N-1$ to *0*. The total duration for DCO cycles count also becomes adaptive and is function of n, defined in (5) as follows:

$$T_M(n) = \frac{2^{N-n}}{f_{REF}} \tag{5}$$

When, N_M is measured for $T_M(n)$ interval for particular bit position n, then the DCO frequency is given by (6) as follows:

$$f_{DCO} = \frac{N_M}{2^{N-n}} f_{REF} \tag{6}$$

The calculated number of reference clocks is now the function of CCW bit position, n and selected frequency channel. It is also adaptive and changes dynamically as the frequency channel and bit position vary. The adaptive number of reference clock cycles, $N_C(n,k)$ are given in (7) as follows:

$$N_C(n,k) = \frac{f_{CH}(k)}{f_{REF}} 2^{N-n} \tag{7}$$

where, $k = 0, 1, 2, 3 \ldots 39$ which corresponds to selected BLE frequency channels CH0$\sim$CH39. The simplified result

of (7) is given as follows in (8):

$$N_C(n,k) = \frac{N_{FCW}(k)}{2^{n-\frac{N}{2}}} \tag{8}$$

The $N_{FCW}(k)$ is the frequency control word as a function of k and is computed by (9) as follows:

$$N_{FCW}(k) = k + N_{CH0}(\frac{M}{D} \times 10^{-6}) \tag{9}$$

Here N_{CH0} is the base frequency magnitude of CH0, M is the DCO frequency multiplier factor and N is the DCO frequency division factor.

Since, the inductor size is very critical in LC-tank based DCO design therefore, for any specific application, the minimum frequency f_{MIN} is limited by the maximum inductance L_{MAX}. For lower frequencies, the inductor size is bigger which results in an increase in area, power consumption and cost. One technique for comparatively reducing inductor size is to design DCO with integer multiple of the required frequency and then divide the frequency with the same integer to get required frequency. In this way the inductor size is reduced. This technique also improves the DCO phase noise. If, M is this multiplying factor then the DCO is running with the frequency as given in (10):

$$f_{DCO} = Mf_{TAR} \tag{10}$$

The DCO running frequency is measured by counting its clock cycles. The counter size is dependent on the frequency and mask time. The DCO frequency is divided by an integer division factor D to reduce the area and power consumption of the counter.

B. DCO GAIN ESTIMATION

After FLL locking, the DCO gain estimation, single bit fine capacitor bank resolution, is determined before the fine tuning in integer loop. The gain estimation is essential for compensating PVT variations and calculating the deviation ratio before the start of direct modulation in BLE transceiver. It is calculated by counting the DCO clock cycles with setting the FINE capacitor back to its maximum and minimum values. The DCO gain, K_{DCO} is computes as follows by the (11):

$$K_{DCO} = \frac{N_{MAX} - N_{MIN}}{2^{N_{FINE}}} \tag{11}$$

where, N_{MAX} and N_{MIN} are the maximum and minimum number of DCO clock cycles when the FINE capacitor bank is set to its minimum and maximum positions respectively and N_{FINE} is the total number of fine capacitor bank bits.

C. LOW POWER DCO DESIGN

The oscillation condition [27] for low power CMOS cross coupled LC-tank DCO is written as follows:

$$g_m \geq \frac{1}{R_P} \tag{12}$$

where, R_P and g_m are the equivalent parallel resistance of the passive section and the equivalent transconductance of active section respectively. The g_m of the NMOS transistors is added to g_m of the PMOS transistors constructively in the CMOS complementary structure. Therefore, compared to NMOS-only or PMOS-only architecture, the power consumption of cross-coupled structure is halved with the same current consumption. In now a day's battery operated devices, the low power consumption and low supply voltage are highly desired. The MOS transistor operation in sub-threshold region is suitable for low power consumption and low supply voltage requirements. The gate to source voltage V_{GS} is less than the threshold value V_{TH} in sub-threshold region. The drain current, I_D in sub-threshold region is described as follows:

$$I_D = \mu_0 C_{ox}(\frac{W}{L})(m-1)U_T^2 e^{(\frac{V_{GS}-V_{TH}}{mU_T})}(1 - e^{\frac{V_{DS}}{U_T}}) \tag{13}$$

where $U_T = KT/q$, K, T, q, μ_0, and C_{ox} are thermal voltage, Boltzman's constant, temperature, electron charge, surface mobility and gate-oxide capacitance respectively. The parameter m represents capacitive coupling between silicon surface and gate. In sub-threshold region, the transconductance is expressed as follows:

$$g_m = \frac{I_D}{mU_T} \tag{14}$$

By selecting larger inductances, the power consumption is minimized. The R_P is calculated as follows:

$$R_p = 2\pi f_0 L Q_L \tag{15}$$

where, f_0 is oscillation frequency, L is inductance value and Q_L is quality factor of inductor. From (12) and (15), the oscillation condition is expressed as follows:

$$g_m \geq \frac{1}{2\pi f_0 L Q_L} \tag{16}$$

Thus, minimum transconductance, $g_{m,min}$ is as follows:

$$g_{m,\min} = \frac{1}{2\pi f_0 L Q_L} \tag{17}$$

According to (17), the oscillation condition is satisfied with larger inductance and smaller g_m in the sub threshold region. This results in less power consumption with lower supply voltage. The tail bias current is $I_{bias} = 2I_D$ and its lower limit for sustainable oscillation is described as follows in (18):

$$I_{bias} = \frac{1}{\pi f_0 L Q_L(\frac{g_m}{I_D})} \tag{18}$$

For the given bias condition in (18), MOS transistors provide high transconductance when operating in the sub-threshold region. The transconductance efficiency (g_m/I_D) is maximum in the sub-threshold region while it is minimum in super-threshold region. The oscillation frequency f_0 of LC-tank DCO is given by the following (19):

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{19}$$

where, C and L are the effective capacitance and inductance respectively. This relation is re-written in more detail as follows in (20):

$$f = \frac{1}{2\pi\sqrt{L_F.(C_F + n\Delta C)}}; \quad (n = 0, 1, \ldots 2^N - 1) \tag{20}$$

where L_F is the fixed inductance including the parasitic inductance and C_F is the fixed capacitance including the parasitic capacitance. The N is the total number of bits and ΔC is the minimum capacitance.

From (20), the oscillation frequency of DCO is approximated as follows:

$$f_0 = f_{MAX} - n\Delta f \tag{21}$$

where

$$f_{MAX} = \frac{1}{2\pi\sqrt{L_F C_F}} \quad \text{and } \Delta f = \pi.\frac{\Delta C}{C_F}.f_{MAX}$$

By using (21), the inductance of the DCO LC-tank is computed as follows in (22):

$$L_F = \frac{2\Delta f}{f_{MAX}^3 \Delta C} \tag{22}$$

For the particular DCO application, f_{MAX} is defined to a fixed value and as a result fixed maximum inductance L_{MAX} is achieved. Hence, C_F defines an upper limit for L_{MAX}. According to (22), with smaller ΔC value, fine frequency step Δf is achieved and it controls DCO quantization noise within entire system. If the ΔC is divided into MSB, LSB and FINE capacitor banks, then (20) is given as follows in (23):

$$f = \frac{1}{2\pi\sqrt{L_F.(C_F + n_{MSB}\Delta C_{MSB} + n_{LSB}\Delta C_{LSB} + n_{FINE}\Delta C_{FINE})}} \tag{23}$$

where;

$$\begin{aligned} n_{MSB}\Delta C_{MSB} &\simeq \Delta C_{TOT} \\ n_{LSB}\Delta C_{LSB} &\simeq 2\Delta C_{MSB}; \quad \Delta C_{LSB} = 0.5fF \\ n_{FINE}\Delta C_{FINE} &\simeq 4\Delta C_{LSB}; \quad \Delta f = 2.4kHz \\ \Delta C_{FINE} &\simeq 16aF \end{aligned}$$

The ΔC_{MSB}, ΔC_{LSB} and ΔC_{FINE} are the unit capacitances for MSB, LSB and FINE capacitor banks respectively for attaining desired frequency resolution.

III. ADAPTIVE ALL-DIGITAL FLL ARCHITECTURE

The detailed architecture of the proposed all-digital FLL is depicted in Fig. 3. The major building blocks includes, all-digital adaptive FLL controller (ADAFLLC), LC-tank DCO and adaptive LDO (ALDO). The detail of each block is discussed in next sub-sections.

A. ALL-DIGITAL ADAPTIVE FLL CONTROLLER

The synthesizable digital circuit design methodologies using behavioral description languages is of great interest due to reusability, simplicity and easy scalability of the circuit

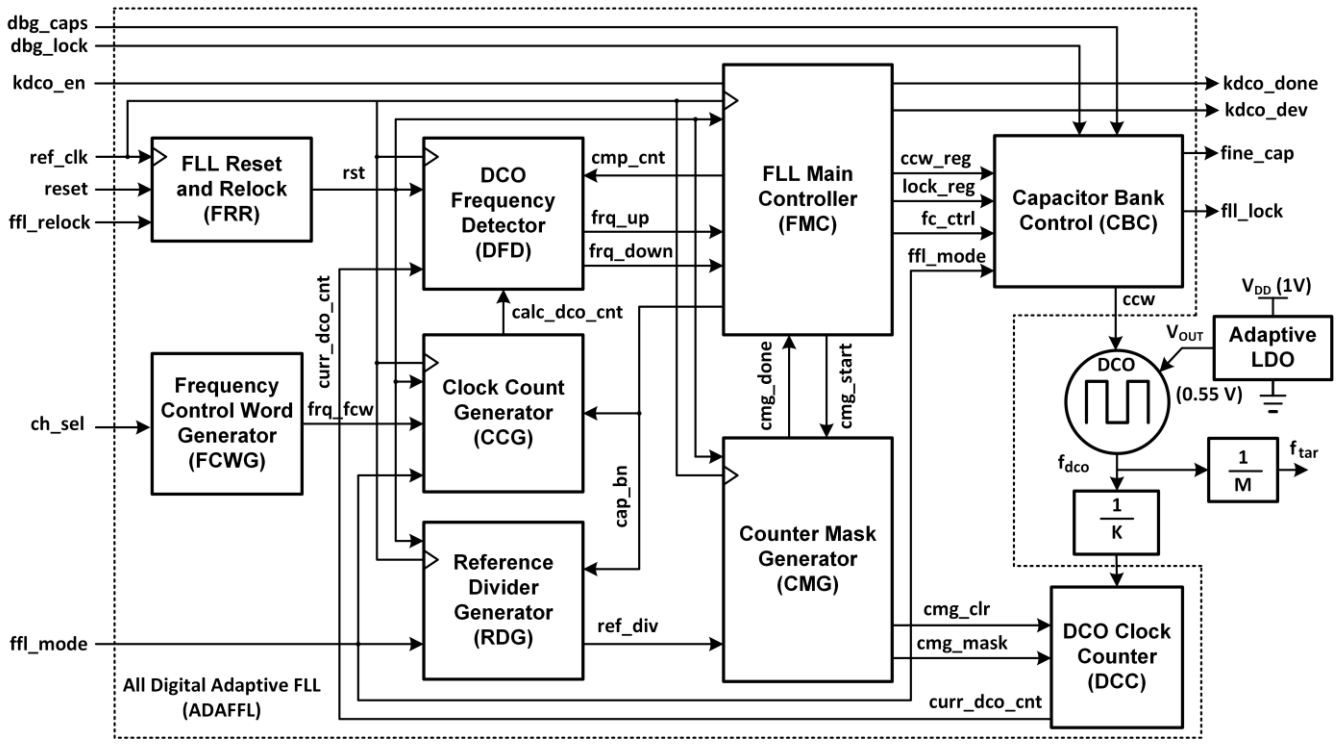


FIGURE 3. All-digital FLL architecture.

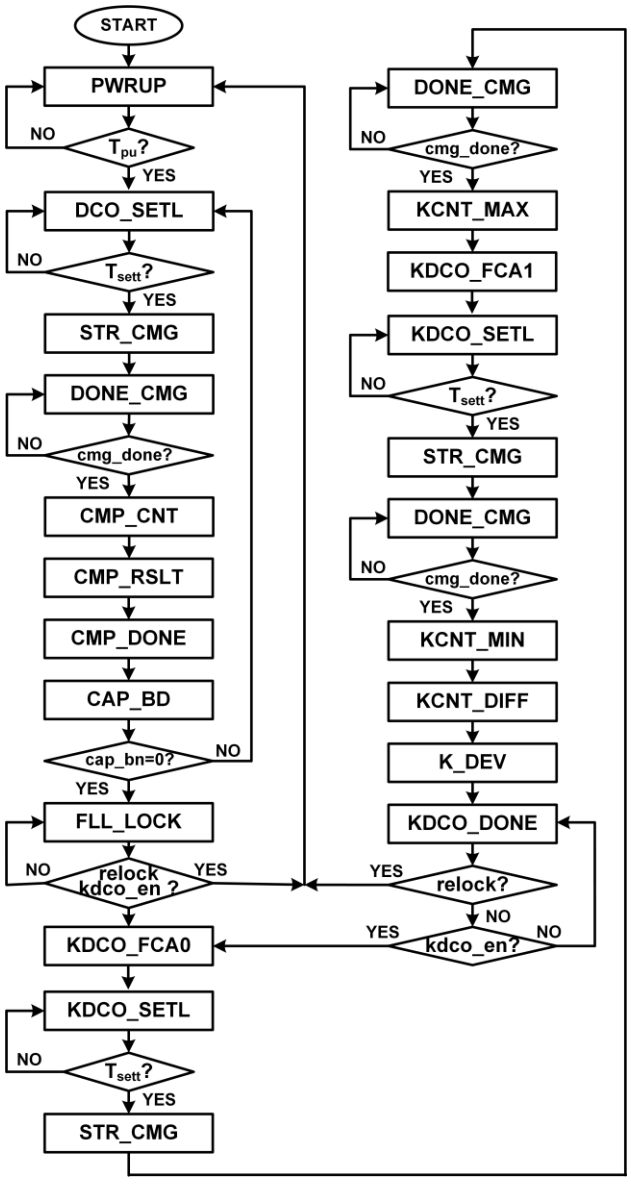


FIGURE 4. FMC finite state machine.

as compared to custom design [21]. Therefore, proposed ADAFLLC is designed with fully synthesizable digital controller and it tunes coarse (MSB, LSB) capacitor banks for target frequency and also performs gain estimation. The FLL main controller (FMC) ensures the operation of each block and generates the exact CCW for selected frequency channel in various modes. After, integer frequency is locked, the DCO gain estimation is computed. The FMC flow diagram is depicted in Fig. 4 while Fig. 5 explains its timing diagram for frequency lock operation. Fig. 6 summarizes the timing diagram for DCO gain estimation. This controller is designed as finite state machine (FSM) control unit and related datapath. On power up, FMC is in PWRUP state and it stays for configurable duration. This state facilitates chip soft start operation, eliminates proposed design's contribution to inrush current and waits for the settling of other analog and digital blocks within the chip. All registers are assigned their default values in reset state. The capacitor control word register ccw_reg is set to its central value 10000_00000_B. After power up, the controller moves to DCO_SETL state. The DCO stables its frequency in DCO_SETL state whenever CCW changes. The FMC enables counter mask generator (CMG) in STR_CMG state and waits for DCO clock cycle counting against current capacitor bit in DONE_SMG state. The CMG, with FSM flow chart and its timing diagram is elaborated in Fig. 7, controls DCO clock counter (DCC) and enables it for specific number of reference clock cycles. It generates the counter mask during which DCC counts DCO clock cycles to measure current frequency. The reference divider generator (RDG) generates reference clock cycle numbers according to (4) as function of current bit position and selected mode. This mask duration, defined in (5) is the function of reference clock frequency, FLL mode and MSB/LSB capacitor bit position, n for which mask is generated. When DCO frequency measurement finishes, the FMC directs DCO frequency detector (DFD) to determine either the oscillator is running faster or slower than the required frequency in CMP_CNT state. In state CMP_RSLT, the DFD compares measured DCO clock cycles *curr_dco_cnt* with the calculated *cal_dco_cnt*, computed by clock count generator (CCG) according to (8) as function of unique frequency control word from frequency control word generator (FCWG) for each BLE channel. The comparison result is available in CMP_DONE state for taking decision about current CCW bit. This bit decision is taken in CAP_BD state. If the DCO is running faster than the required frequency, then it needs to be slowed down by increasing capacitor bank capacitance. For this, DFD asserts *freq_down* high while keeping *freq_up* low. In this case, the current CCW bit remains high. The FMC turns on the next least significant bit high and jumps back to DCO_SETL state for computing the new frequency of DCO after changing capacitance. If the DCO is running slow than the required frequency, the DFD pulls the *freq_up* to high and grounds the *freq_down* signal. In this case, the capacitance needs to decrease in order to increase frequency. The current CCW bit changes from one to zero and next least significant bit is set to one. This process continues till the least significant bit is checked. In CAP_BD state, if all CCW bits are evaluated, then the current DCO frequency becomes approximately equal to the target frequency with minimum fractional error. The CCW is fixed to evaluated value and it is locked in FLL_LOCK state. After FLL lock, FMC determines DCO gain estimation according to (11). The controller sets all the fine capacitor bank bits *fine_cap* to zero in KDCO_FCA0 state and waits for settling for configurable duration in KDCO_SETL state. The CMG is started in STR_CMG and waits for finishing the mask duration for measuring the DCO frequency in DONE_CMG state. The *curr_dco_cnt* gives the maximum value which is saved in *kdco_cnt_max* register in KCNT_MAX state. Similarly, the fine capacitor bank bits are set to high and against this, the minimum counter value,

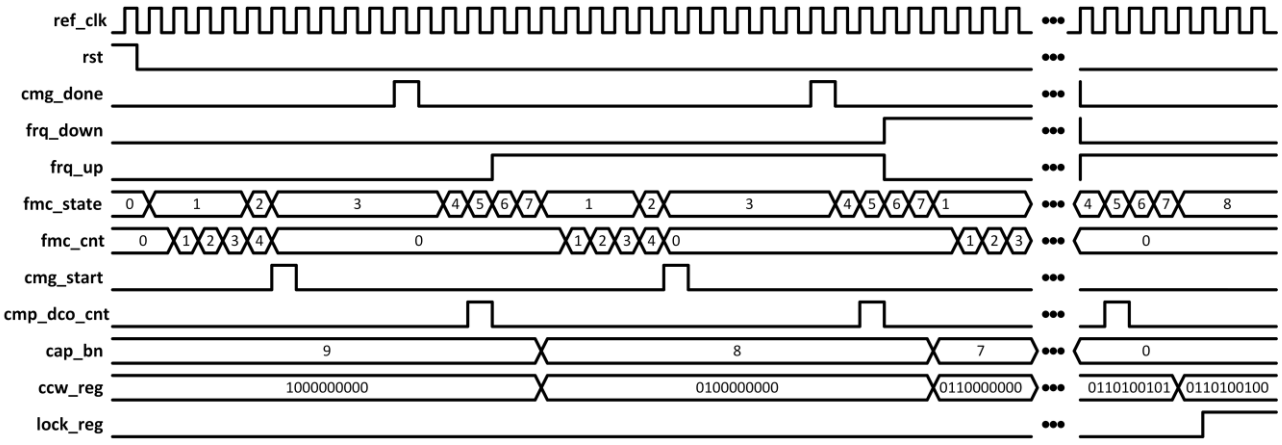


FIGURE 5. FMC timing diagram for frequency lock loop.

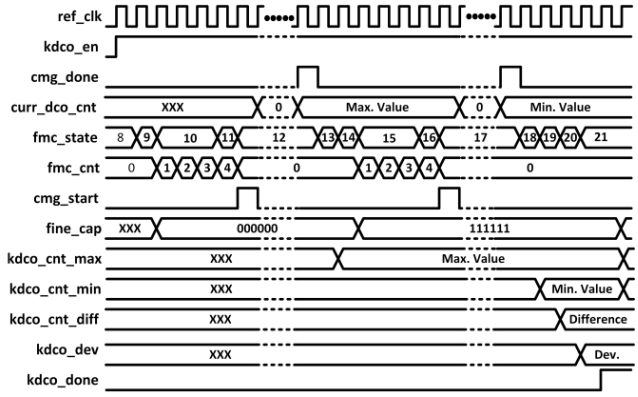


FIGURE 6. FMC timing diagram for gain estimation.

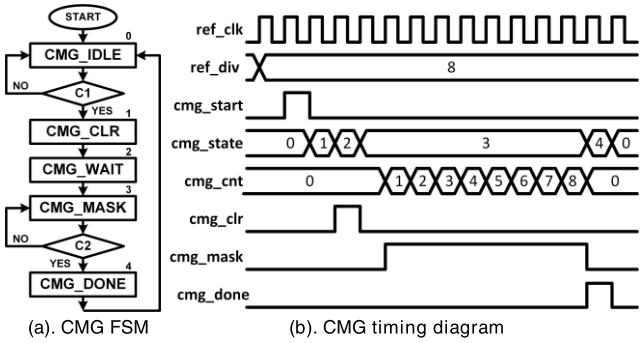


FIGURE 7. CMG finite state machine and timing diagram.

measured as result of same fixed number of reference clock cycles are registered in *kdco_cnt_min* in KCNT_MIN state. The difference *kdco_cnt_diff* of both count values are computed in KCNT_DIFF state and final deviation *kdco_dev* is evaluated in K_DEV state. The DCO gain estimation process is complete and controller announces this in KDCO_DONE state by asserting the *kdco_done* signal high. The controller remains in this state until there is request of computing DCO gain estimation again or repeating the FLL operation.

In the presented FLL design, four configurable operating modes are proposed. These modes control the masking duration for counting DCO clock cycles in various methods. The fully adaptive mode (FAM) is the default mode, in which the counter mask is fully adaptive from MSB to LSB of the capacitor banks. This is the most accurate mode in terms of frequency measurement at the cost of comparatively more locking time. In partial adaptive mode (PAM), the counter mask is adaptive for selectable initial MBS and then become fixed for remaining bits to reduce the lock time. One of the configurable mask is selected and remains fixed during all iterations for capacitor bits in the fixed configurable mode (FCM). In this mode, the locking time depends in the selected mask. In external manual mode (EMM), the capacitor bits and locking signal are directly controlled from external controller for manual debugging and analysis purpose.

B. DIGITALLY CONTROLLED OSCILLATOR (DCO)

The LC-tank DCO is key building block in ADPLL and it consumes most of system power for generating local frequency [1], [25], [31], [33], [35]. Therefore, ultra-low power and ultra-low voltage DCO design significantly reduces system power consumption [36], [37]. The DCO performs digital-to-frequency conversion [32]. The constant current DCO configuration and simplified circuit diagram with MSB, LSB and FINE capacitor banks is shown in Fig. 8 [27]. Since the DCO power consumption is dominant factor in ADPLL in open loop operation, therefore DCO is designed with low power techniques. For minimizing current consumption and relaxing reliability problems, DCO supply is 0.55 V and it is relatively lower than other building blocks. The DCO is designed with ULP process and threshold voltage, V_{TH} is very small (0.18 V∼0.2 V) for this process. The overdrive voltage is 0.1 V. The two transistor can get enough voltage form 0.55 V power supply. The 4-stack transistor (negative gm transistor) can get needed overdrive voltage from 0.55 V power supply. The sigma-delta modulator for dithering and binary to thermometer encoder (B2T) DCO

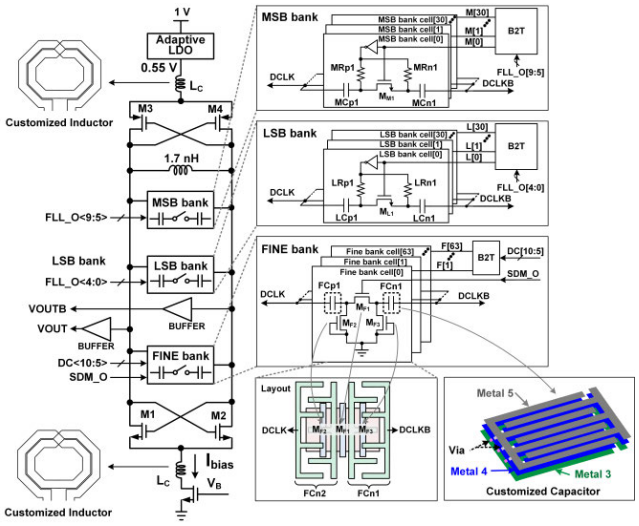


FIGURE 8. DCO design.

digital sub-blocks can operate at 0.55 V supply. The DCO operates and have oscillations with supply voltage from 0.55 V to 1 V. The power consumption will increase if the DCO supply is increased from 0.55 V to 1V. Therefore, the lowest possible supply voltage of 0.55 V is used for minimum power consumption. The 1.2 V devices are used for the presented DCO and transistors reliability is assured for 1.32 V as maximum voltage. Although, peak voltage exceeds than oscillator VDD, it does not increase more than 1.2 V as analyzed from simulation results. Since a larger inductor reduces DCO power consumption, therefore, the main inductor is maximized while the parasitic capacitance is minimized for desired frequency range. The DCO phase noise depends on the frequency resolution, which is limited by the minimum switchable capacitance. For DCO design flexibility and frequency step linearity, the coarse and fine capacitor banks are designed with unit weighted capacitor rather than binary weighted configuration. By optimizing capacitor redundancies, parasitic capacitance is reduced by utilizing flexible number of capacitors in unit weighted structure in comparison with a binary weighted structure. For attaining high linearity and small switchable capacitance, a customized lateral metal capacitor is designed and fabricated, as shown in Fig. 8. Its capacitance is calculated from RC extraction which has 16 aF value approximately. The configurable MSB and LSB capacitor banks are designed with a variable bias switched capacitor. To improve LC- tank Q-factor, metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors are commonly employed instead of MOS capacitors for MSB and LSB capacitor banks. The MOM capacitors are used for designing low cost DCO with improved Q-factor. For minimizing area and increasing capacitor density, these capacitors are stacked from Metal 2 to Metal 5. Because the LSB capacitor bank requires minimum capacitance in the process design kit (PDK) therefore these MOM capacitors are stacked from Metal 3 to Metal 5. The unit capacitor cell is composed of a switch, two capacitors and two blocking resistors as elaborated in Fig. 8. Conventionally, the switch source bias voltage is fixed to zero. However, in case of DCO large swing, switch is not turned off completely in OFF-mode. This causes phase noise degeneration. To overcome this problem, two inverters are utilized as control logic for providing variable biasing. In ON-mode, the switch transistor source voltage is biased at zero while gate voltage is VDD (1V). On the other hand, in OFF-mode, gate and source voltages of switch are biased at zero and about $\mathrm{LDO_{OUT}}$ (0.55V) respectively to ensure complete switch turn off. An ultra-wide width aluminum (Al) pad metal pattern is incorporated to eliminate the parasitic resistance and inductance due to metal routings. This only creates additional capacitance between Al pattern and capacitor banks. There is no stray parasitic capacitance problem due to large distance of about 8.8 μm between Al pattern and substrate. Aluminum pad metal has sufficiently large thickness and no width limitation. All parasitic inductors are tied in parallel with ultra-wide width Al pad metal and via. In this way, parasitic inductors are eliminated effectively. As a result, the DCO is parasitic inductance free and ensures linear frequency steps. As a result, frequency steps are closer to that of measurement and accurate oscillation frequency is achieved without additional cost for Al pad layer. For dithering, one out of 64 cells of FINE capacitor bank is controlled by the first order sigma-delta modulator (SDM). Therefore, SDM dithering effective frequency resolution is 1/16 of the 1-bit frequency resolution of the FINE capacitor bank. In DCO design, there is trade-off between oscillation frequency range and power consumption. The two Lc inductors at top and bottom of DCO are customized design. The inductance of each of these inductors is 3 nH. Each inductor has very small resistance and there is very small voltage drop improving PN by 6 dB at 1-MHz offset. The purpose of these inductors is to improve the phase noise of the DCO. Firstly, two inductors are designed based on EMX simulation and then its quality factor and inductance values are calculated as 15 and 3 nH respectively. The negative gm-cell placement also affects DCO power consumption and frequency range. If all transistor switches are off, the DCO exhibits large parasitic inductance, reduces frequency and decreases current consumption when a negative g_m cell is placed at capacitor banks end side. Similarly, if a negative g_m cell is positioned at inductor end side then the negative g_m cell Q-factor degrades and DCO power dissipation increases. Therefore, for designing low power DCO, the negative g_m cell is located at capacitor banks end side in the proposed FLL.

C. ADAPTIVE LDO

The minimum oscillation and power dissipation of DCO changes with PVT variations. When constant voltage source is used, the DCO draws more current at corner cases due to decrease in g_m. To provide constant current to DCO, an adaptive LDO [27], depicted in Fig. 9 is integrated as DCO driving voltage source. The LDO output voltage automatically changes with PVT variations to keep g_m constant.

The proportional to absolute temperature (PTAT) bandgap reference (BGR) compensates temperature variations and LDO function regulates voltage variation. With PTAT BGR, ALDO ensures constant voltage and current across DCO at corner cases. At corner conditions, constant current keeps DCO g_m constant and reduces DCO power consumption significantly. With ALDO, around 50% power consumption is reduced at the corners.

IV. EXPERIMENTAL RESULTS

The proposed adaptive all-digital FLL is fabricated by using 55 nm 1P6M TSMC CMOS technology. It is part of ADPLL in BLE transceiver for IoT applications. The power supplies for fully synthesizable FLL and DCO are 1 V and 0.55 V respectively. Fig. 10(a) shows the chip microphotograph with 45 μm × 40 μm and 360 μm × 220 μm area of ADAFLLC and DCO respectively with total 0.081 mm^2 area. Fig. 10(b) shows the testing board with fabricated BLE chip for measuring proposed design. Fig. 11 shows lab experimental environment for measuring the performance of FLL and DCO for which spectrum analyzer, signal generator, oscilloscope and power supply are used. Fig. 12 shows the measurement results for integer ADAFLLC operations. The measurement results

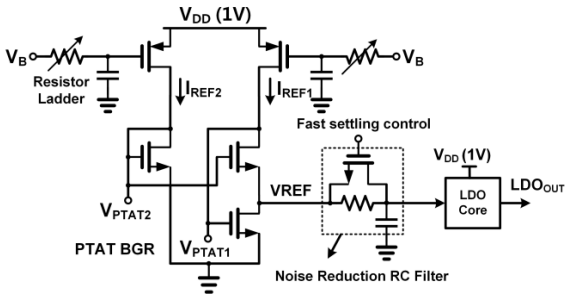
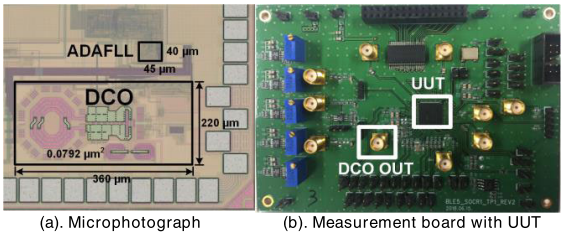


FIGURE 9. Adaptive LDO design.



(a). Microphotograph (b). Measurement board with UUT

FIGURE 10. Chip microphotograph and measurement board.

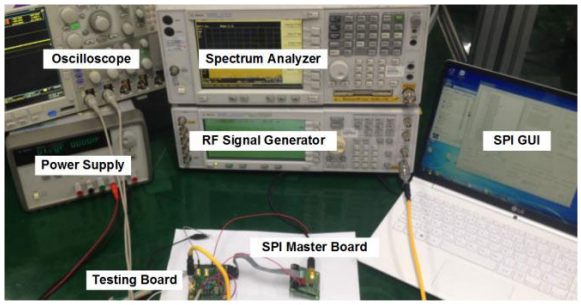
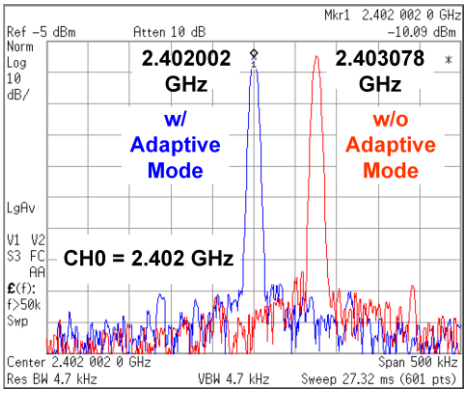
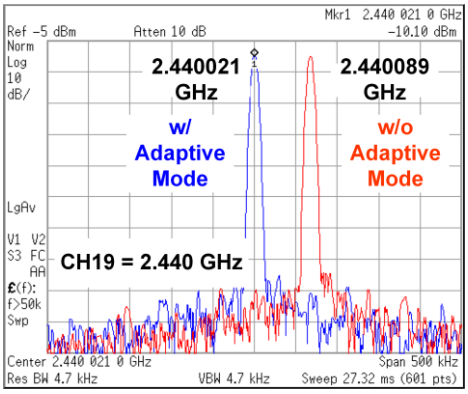


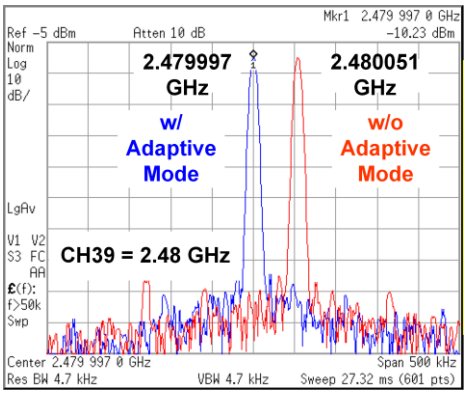
FIGURE 11. Measurement lab setup.



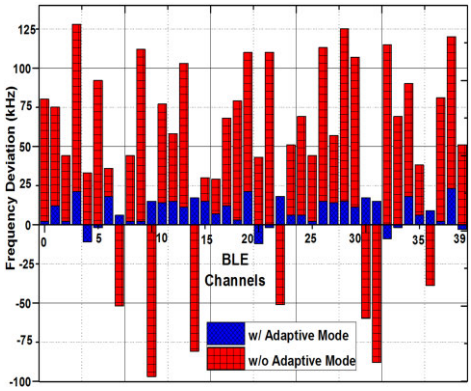
(a). BLE CH0, 2.402 GHz target



(b). BLE CH19, 2.440 GHz target



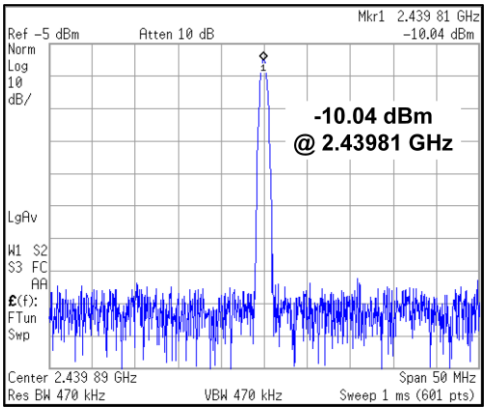
(c). BLE CH39, 2.480 GHz target



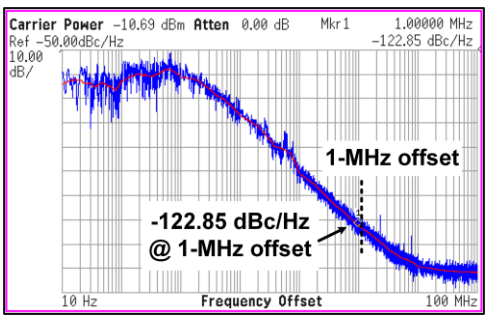
(d). All channels frequency deviation

FIGURE 12. All digital FLL measurement results.

show that the locked frequency for selected channel is more near to the target frequency with proposed adaptive design. In Fig. 12(a), the BLE CH0 target frequency is 2.402 GHz. The frequency deviation from target one is 2 kHz only with adaptive mode while it is 1.078 MHz without adaptive mode. Similarly, for CH19 and CH39, the frequency deviation is much less with proposed FLL in adaptive mode as shown in Fig. 12(b) and Fig. 12(c) respectively. The measurement results for frequency deviation of all forty BLE channels with and without adaptive mode are elaborated in Fig. 12(d). The measurement results prove that the proposed ADAFLLC design is highly effective and lock the integer loop with frequency which is much closer to the target frequency. The frequency deviation is greater in case of without adaptive mode. Fig. 13(a) and (b) show the measured output spectrum and phase noise of DCO respectively. At 1-MHz offset, the measured PN is −122.85 dBc/Hz. The DCO measured performance of PN versus supply voltages and current consumption are plotted in Fig. 14. As shown in Fig. 14, phase noise value, a DCO key characteristic is good compared with that of supply voltage and current consumption. The measurement results for coarse (MSB, LSB), FINE capacitor banks and SDM dithering frequency tuning range are elaborated in Fig. 15. The MSB, LSB, FINE capacitor banks and dithering SDM frequency step are 459 MHz, 27.97 MHz, 4.93 MHz, and 78.24 kHz, respectively. The measured tuning range for DCO is 459 MHz from 2.217 GHz to 2.676 GHz

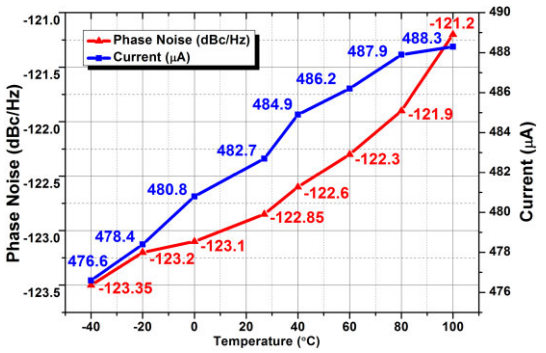


(a). Output spectrum

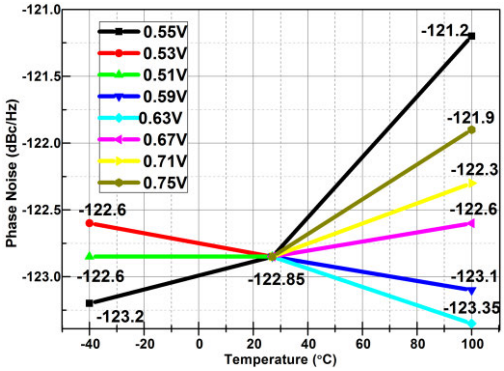


(b). Phase noise @ 1-MHz offset

FIGURE 13. DCO output spectrum and phase noise measurement.



(a). PN Vs. and Temperature



(b) PN vs. supply voltage and temperature

FIGURE 14. DCO measurement results with different conditions.

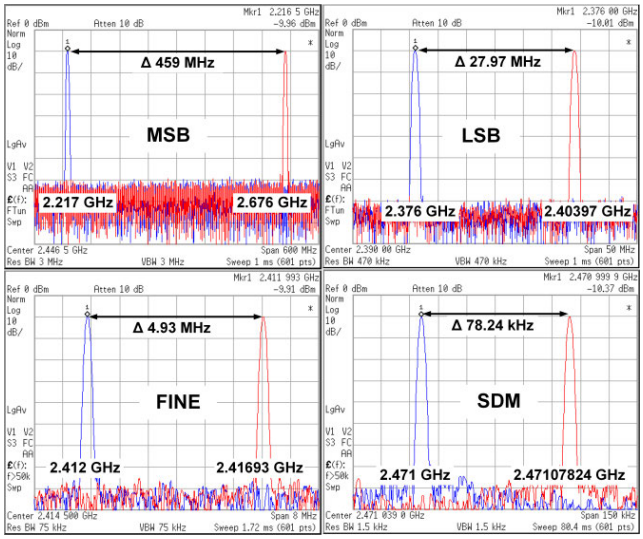


FIGURE 15. Frequency step measurement for MSB, LSB, FINE and SDM.

and it is depicted in Fig. 15 (a). The MSB, LSB, FINE capacitor banks and SDM dithering measured 1-bit resolutions are 14.42 MHz, 870 kHz, 78.21 kHz and 2.41 kHz respectively as depicted in Fig. 16. Table 1 summarizes the performance of fully synthesizable FLL. Its power consumption is 103.32 μW for its full operation. For its implementation in chip, it requires only 1.233 K gates with 1800 μm^2 chip area. The lock time ranges 3.7∼6487 μs and it depends

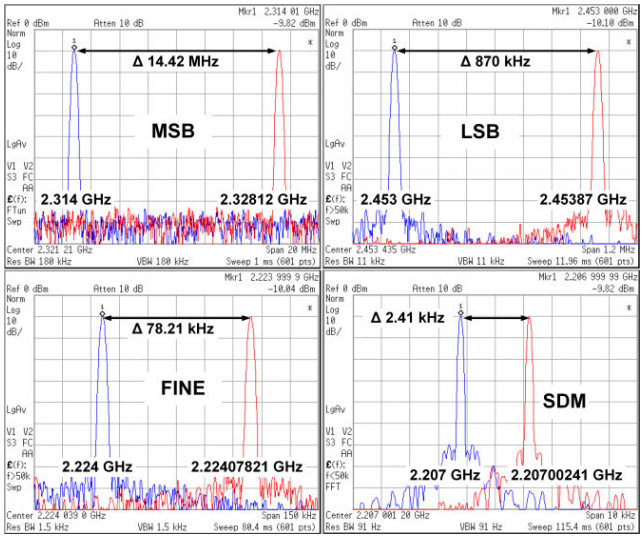


FIGURE 16. 1-bit resolution measurement for MSB, LSB, FINE and SDM.

TABLE 1. ADAFLL performance summary.

Parameter	Value
CMOS technology	55 nm
Occupied Area	1800 μm²
Gate count	1.233 K
Supply voltage	1 V
Current consumption	103.32 μA
Power consumption	103.32 μW
[1]Lock time	3.7~6487 μs

[1]Lock time depends on mode and configured parameters

TABLE 2. DCO performance summary and comparison.

Parameter	Ref. [1]	Ref. [27]	Ref. [31]	This Work
CMOS Process (nm)	40	55	180	55
Supply Voltage (V)	1	0.55	1.8	0.55
Oscillation Frequency (GHz)	2.44	2.44	3.2	2.44
Resolution (kHz)	40	78.13	20	72
Dithering Resolution (kHz)	-	2.44	-	4.8
Frequency Tuning Range (GHz)	2.1~2.7	2.2~2.7	2.8~3.2	2.1~3.05
PN @ 1-MHz Offset (dBc/Hz)	-115.53	-119.05	-114.42	-122.85
P_{DC} (mW)	0.33	0.260	3.8	0.264
Area (mm²)	0.135	0.13	0.35	0.0792
FOM (dBc/Hz)	189.16	193.42	179.32	196.38
FOM_T (dBc/Hz)	196.98	199.12	181.82	208.19

on the selected mode and configured parameters. The DCO performance and comparison with existing designs is listed in Table 2. It needs 0.264 mW power for its full operation. It occupies a very small chip area of 0.0792 mm² when compared with prior works. The PN is −122.85 dBc/Hz. The FOM and total figure of merit (FOM_T) are 196.38 dBc/Hz and 208.19 dBc/Hz respectively confirming its good performance for low voltage and low power applications including

TABLE 3. FLL performance comparison.

Parameter	Ref. [22]	Ref. [25]	Ref. [26]	This Work
CMOS Process	180	90	55	55
FLL Topology	CNT	CNT	CNT	CNT
Oscillator Type	Ring	SRO	DCO	DCO
Frequency Range (GHz)	0.2539 ~1.367	2.36~2.5	2.44	2.1~3.05
Reference Clock (MHz)	19.53	24	32	32
Lock Time (μs)	2.92 μs	20.63	37	3.7~6487
Gain Estimation	No	No	Yes	Yes
Adaptive Algorithm	No	No	No	Yes
Configurable	No	No	No	Yes
Multi-modes	No	No	No	Yes

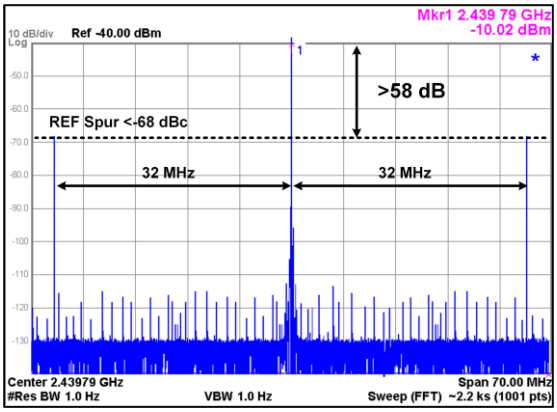


FIGURE 17. Measured reference spur in fractional mode.

BLE. The FOM and FOM_T are evaluated with (24) and (25) respectively [33], [34].

$$FOM = |PN| + 20\log_{10}\left(\frac{f_0}{\Delta f}\right) - 10\log_{10}\left(\frac{P_{DC}}{1wW}\right) \quad (24)$$

$$FOM_T = |PN| + 20\log_{10}\left(\left(\frac{f_0}{\Delta f}\right)\left(\frac{\%FTR}{10}\right)\right) - 10\log_{10}\left(\frac{P_{DC}}{1wW}\right) \quad (25)$$

The FLL performance comparison with the exiting counter based topologies is summarized in Table 3 [22], [25], [26]. Most of previous integer FLL work such as in [22] and [25] used fixed number of clock cycles for each capacitor bank bit evaluation. In contrast, for locking DCO frequency closest to target channel, proposed FLL algorithm adaptively controls capacitor banks with binary algorithm. With decrease in frequency resolution, DCO clock counts for each capacitor bank bit evaluation dynamically increases with the proposed technique for accurate frequency tracking. Additionally, the configurable digital DCO gain estimation is incorporated for compensating PVT variations and finding the BLE frequency deviation. Finally, in the presented work, four configurable operating modes are proposed which control the masking duration for counting DCO clock cycles in various methods. The measured reference super for the fractional mode is less than −68 dBc, as depicted in Fig. 17. The ADLDO measurement and corner simulation results of is plotted in Fig. 18.

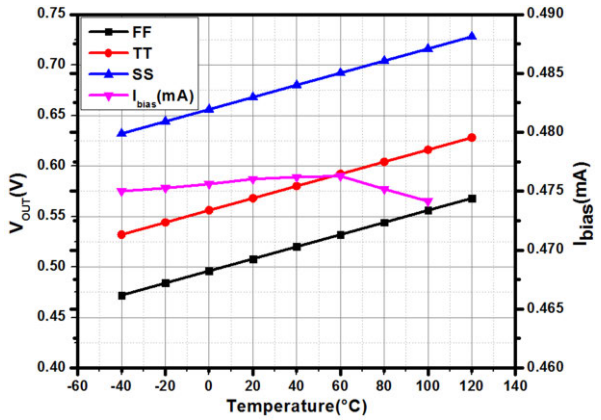
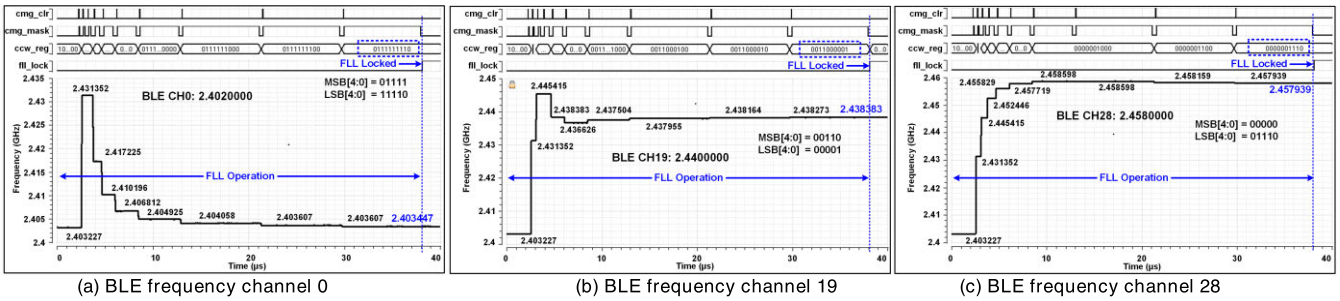


FIGURE 18. Adaptive LDO measurement result and corner simulation.

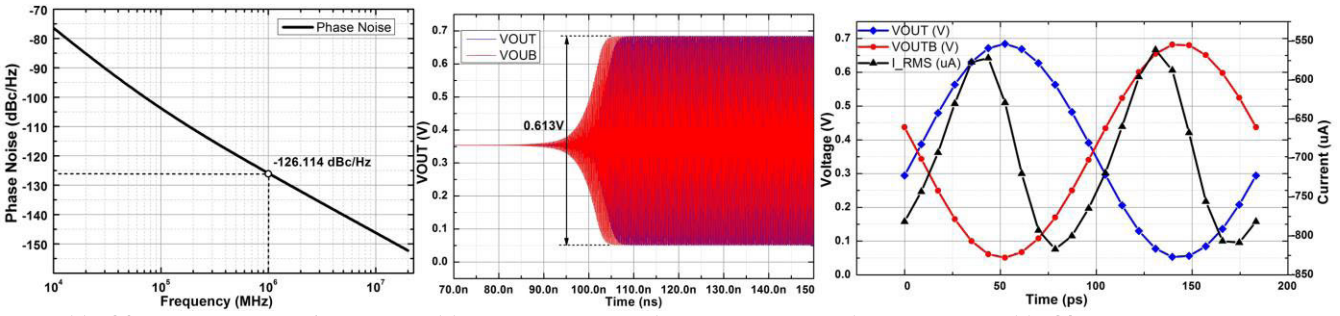
The V_{OUT} increases with the increase in temperature. Without ADLDO, when constant voltage source is used, DCO draws more current due to the increase in g_m. With ADLDO at the corner conditions, this biasing current remains 50% for powering the oscillator. For same g_m with process variation, FF corner requires lower V_{OUT} than TT and SS corner requires less V_{OUT} than TT. With BGR constant current, diode connected MOS determines suitable reference voltages. The MOS transistors threshold voltage changes due to process variation and as a result the reference voltage also changes. The V_{OUT} varies due to trimmed reference voltage and DCO has the same g_m, consumes constant current and dissipates similar power.

The Fig. 19 shows co-simulation for presented integer loop for BLE channels 0, 19 and 28. Fig. 19(a) shows the simulation result for BLE CH0 with 2.402 GHz target frequency. The DCO is tuned to 2.403447 GHz after FLL locking with the deviation of 1.447 MHz. Fig. 19(b) and Fig. 19 (c) show the simulations for channels 19 and 28 in which the locked frequency values are 2.438383 GHz and 2.457939 GHz with 1.617 MHz and 61 kHz frequency deviations respectively. Fig. 20 shows DCO post-payout simulation with 0.55 V power supply and 4.88 GHz oscillation frequency. The phase noise analysis is shown in Fig. 20(a). At 1-MHz offset from the operating frequency, the phase noise is −126.114 dBc/Hz. Fig. 20(b) shows the transient simulation DCO output in which maximum voltage swing is 0.613 V. The output of DCO obtained from periodic steady-state (PSS) analysis is shown in Fig. 20(c). The RMS current consumption of proposed DCO is around 463 μA. Fig. 21 shows the simulated frequency tuning range curves for the DCO. Fig 21 (a) shows DCO frequency tuning range curves based on SP simulation results. For finding frequency tuning range, the SP simulation is run to calculate the imaginary part of admittance (Y11) of 50 Ohm antenna port connected at DCO output. The minimum and maximum frequencies are 2.19 GHz and 2.64 GHz at Y11 zero crossing with tuning range of 450 MHz when capacitor codes are all high and all low respectively for TT corner case as shown in Fig. 21 (a). The transient simulation of MSB capacitor bank change based DCO frequency tuning range is shown in Fig. 21 (b). Since, MSB capacitor bank is for coarse tuning and it controls main



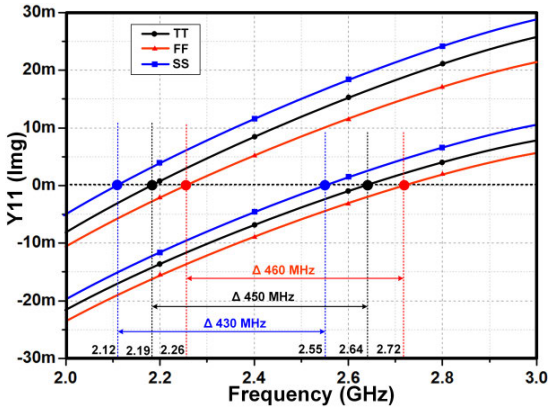
(a) BLE frequency channel 0 (b) BLE frequency channel 19 (c) BLE frequency channel 28

FIGURE 19. All digital FLL settling behavior for selected channels.

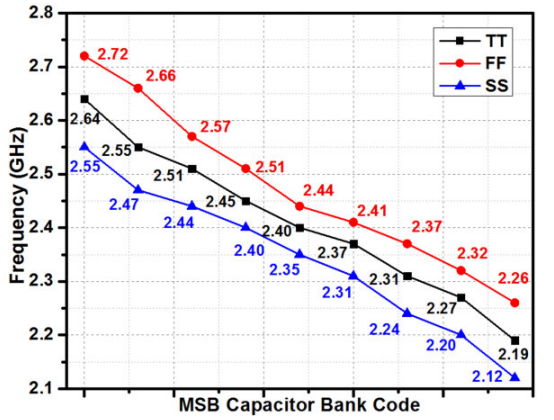


(a) DCO phase noise in dBc/Hz (b) Transient simulation (Voltage swing 0.613 V) (c) PSS simulation

FIGURE 20. DCO simulation analysis.



(a). SP Simulation results for tuning range curves



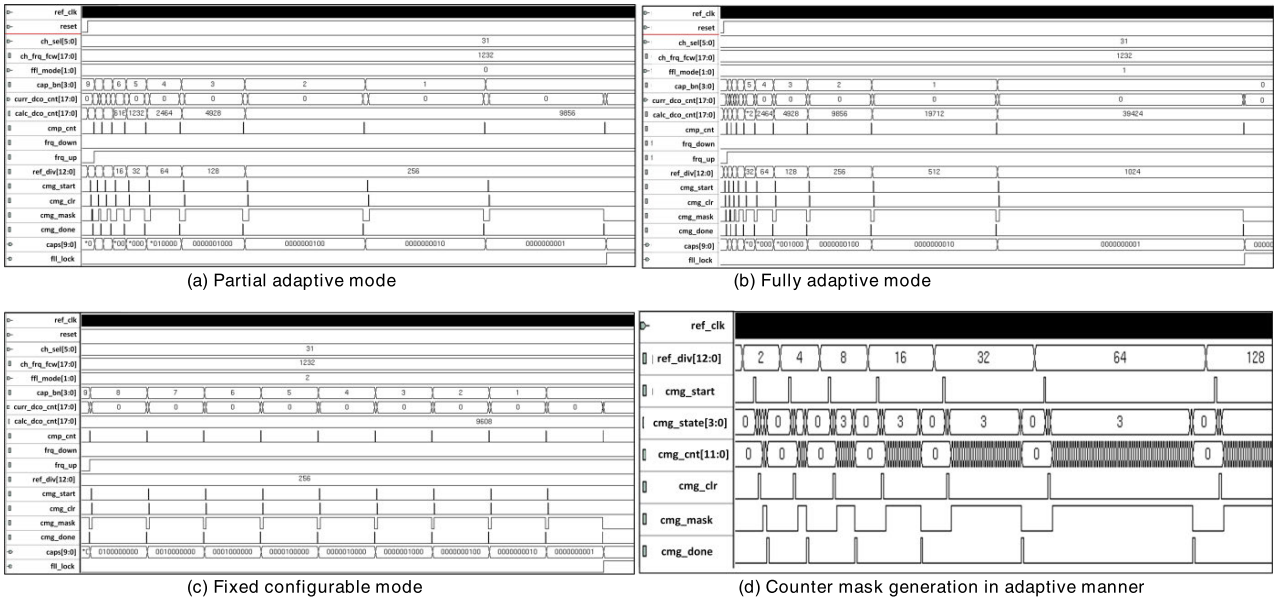
(b). MSB capacitor bank Transient simulation

FIGURE 21. DCO frequency tuning range simulation results.

capacitance, therefore its code is changed from minimum value to its maximum value to get the upper and lower DCO frequency limits respectively. With TT corner case, the transient simulation based DCO tuning range is 450 MHz as shown in Fig. 21(b).The Fig. 22 summarizes ADFLL simulation results for different proposed modes. This is post place and route (P&R) level open loop simulation of ADAFLLC digital part without the DCO in Synopsys® VCS® tool. Fig. 22 (a) shows the PAM simulation in which the *cmg_mask* is adaptive from *cap_bn* 9 to 2 and then become 256 as fixed for remaining bit positions. The CCG also generates *cal_dco_cnt* accordingly. Fig. 22(b) shows the fully adaptive mode simulation results. The *ref_div*, *calc_dco_cnt* and *cmg_mask* adaptively change as *cap_bn* sweeps from MSB to LSB for DCO free running frequency tuning. The fixed configurable mode simulation is elaborated in Fig. 22(c) in which the one of the pre-defined fixed counter mask is generated for all *cap_bn* values against any selected channel. The detailed simulation result for CMG is shown in Fig. 22(d). The adaptive mask generation is elaborated in which the mask time increases exponentially. The counter mask is configurable and adaptive with respect to *cap_bn*. The *cmg_start* is asserted high from FMC which initiates mask generation process. After receiving *cmg_start* signal, CMG first clears the *cmg_cnt* and then generates the mask for configured number of clock cycles according to the algorithm.

V. CONCLUSION

An ultra-low power, adaptive all-digital FLL with gain estimation and constant current DCO for BLE transceiver is presented in this paper. The binary algorithm adaptively controls capacitor banks for locking DCO frequency closest to the target channel. For accurate frequency tracking and tuning, DCO clock counts automatically increase for evaluating each bit of capacitor bank. For compensating PVT variations and finding the BLE frequency deviation, the configurable digital DCO gain estimation is incorporated. The low power



(a) Partial adaptive mode

(b) Fully adaptive mode

(c) Fixed configurable mode

(d) Counter mask generation in adaptive manner

FIGURE 22. All digital FLL simulation results for different proposed operating modes and CMG simulation.

constant current DCO operates in sub-threshold region and its power consumption is minimized by g_m/I_D methodology optimization, constant current source for limiting current in the oscillator core through adaptive LDO and lowering the supply voltage. The ADAFLLC is fully synthesizable, occupies 1800 μm^2 area, utilizes 1.233 K gates, draws 103.32 μA RMS current from 1 V voltage source and dissipates 103.32 μW power. The DCO current consumption is 480 μA from 0.55 V supply at central frequency and has 4.8 kHz frequency resolution. At 1-MHz offset frequency from 2.44 GHz carrier frequency, DCO PN, FoM and FoM$_T$ are -122.85 dBc/Hz, 196.38 dbc/Hz and 208.19 dBc/Hz, respectively. The presented design is integrated in ADPLL. It is fabricated by using 55 nm 1P6M TSMC CMOS technology.

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