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Robustness Improvement of Single-Phase Inverters Under Weak Grid Cases by Adding Grid Current Feedforward in Delay-Based Phase-Locked Loop

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ABSTRACT For inverters, a phase-locked loop (PLL) is usually needed for the grid synchronization. Typically, for the single-phase inverters, the orthogonal-signal-generators based PLLs (e.g., delay-based PLL) can be used. However, if the grid at the point of common coupling (PCC) exhibits a large grid impedance, the inverter may not work well or even be unstable. In order to work satisfactorily in the very weak grid, this study aims to formulate a robust PLL. At first, by modeling the inverter output impedance and considering the frequency coupling effect, the stability of the typical delay-based PLL has been analyzed and the reason for the performance degradation has been explained. Then, based on analyzing the differences of PLL blocks under different PCC conditions, the robust PLL with the grid current feedforward is discussed. Compared with the typical PLL, the improvement of the system behaviors in the weak grid cases is mainly attributed to the extra term on the numerator of output impedance, which is introduced by the current feedforward of the proposed PLL. The selection of control parameters has been emphasized for maintaining the high robustness. At last, selected comparative waveforms have verified that the single-phase inverter can perform well even with the large grid impedance, without the grid impedance estimation.

INDEX TERMS Inverters, phase-locked loops, grid impedance, harmonic distortion, robustness.

I. INTRODUCTION

In the distributed power generation systems (DPGSs), the grid-connected inverter with an *LCL* or *LCL*-Trap filter is the key interface [1], [2]. The filter resonance damping, the current controller, the feedforward of the voltage at the point of common coupling (PCC), and the phase-locked loop (PLL) should be well addressed. For instance, the high-order filter resonance can be solved by many damping methods including the passive damping [3], and the active damping (AD) based on the capacitor current feedback, the delay-based AD [4], [5], the grid current feedback AD [6], [7] and the state feedback AD [8]. For the grid synchronizations, the power-based PLL [9] and orthogonal-signal-generators (OSGs) based PLLs are welcomed in the single-phase system [10], [11]. Besides, the delay-based PLL is widely used for its simple structure.

Note that the above studies on the single-phase control have not seriously considered the non-ideal factors at the PCC. As the PCC is weakened by the large grid impedance [12], the performance must be examined when the grid impedance is considered. As proved by [13], [14], the *LCL* resonance damping, the harmonic resonant controller and the PCC voltage feedforward could all cause the instability due to many reasons, such as the reduction of resonance frequency, the bandwidth reduction and the extra feedback loop related to the PCC feedforward. Thus, for the weak grid applications, the robust or adaptive methods are proposed, e.g., the robust AD in [14]–[16], the robust controllers in [17]–[19], the robust voltage feedforward based on impedance shaping in [20], [21], the adaptive algorithms based on the impedance estimation in [13], [22], [23], and the adaptive feedforward without the grid impedance estimation

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in [24]. As above studies proved, the harmonics at several hundreds of Hz to several kHz (usually, much higher than the PLL bandwidth) can be solved.

However, with the increase of the grid impedance, the system stability is challenged by the PLL. As studied in [23] and [25], the PLL affects the inverter output impedance at the very low frequencies (i.e., from the fundamental frequency to several hundreds of Hz). Hence, for a wide grid impedance variation, harmonics around the PLL bandwidth (i.e., within several hundreds of Hz) can still be aroused [26]. Although an adaptive feedforward is proposed in [23] for enlarging the phase margin (PM), the improvement (only 20° at 400 Hz, much higher than PLL bandwidth) is marginal and the online estimation of the grid impedance is required.

As analyzed, harmonics at the very low frequencies may be triggered due to the phase-locked function (even if the robust AD and controller are used), so that it is required to improve the grid synchronizations [26]. In [27], the power synchronization for the three-phase system is proposed for the weak grid application. Although it is a good candidate for the stability improvement, more in-depth studies shall be necessary. Making revisions to the PLLs is an alternative way for enhancing the stability for the large grid impedance. In [28], [29], the robust design of the three-phase PLL in the weak grid has been discussed. The analysis in [30] recommends the sharp reduction of the PLL bandwidth, which causes the slow transient. In [31] where a very low PLL bandwidth is used (i.e., 18 Hz), an impedance compensator has been proposed to extend the operation range of a three-phase inverter in the weak grid. Only some simulations have been provided, and the core principle is still not explained clearly. Given that a higher bandwidth yields a more desirable system dynamic, it is attractive to find a solution for achieving the desirable bandwidth and the high robustness simultaneously. Despite of the above valuable studies, the robust PLL methods for the single-phase inverter have rarely been found.

Hence, this study proposes a robust PLL approach for the single-phase system with the large grid impedance (e.g., with a short-circuit ratio (SCR) of 3). The main work and contributions are: 1) investigating the system stability based on the inverter output impedance model, through which the reason why the typical PLL cannot assure a stable operation in the case of large grid impedance is explained; 2) proposing an improved PLL, where the grid current feedforward and its design enhance the robustness by increasing the magnitudes and phases of the output impedance within a wide frequency range; 3) providing comparative test results, which can verify that the proposed PLL control works well without the grid impedance estimation and the proposed PLL is suitable for the weak grid application.

Section II briefly introduces the system descriptions and modelings. Section III clarifies the problems of the typical inverter control. Then, the robust PLL is proposed in Section IV where the design is also emphasized. Section V analyses the performances in the default case and in the weak grid cases. Then, simulations and experiments with the proposed single-phase PLL and some existing PLLs are provided in Section VI. At last, Section VII concludes the whole paper.

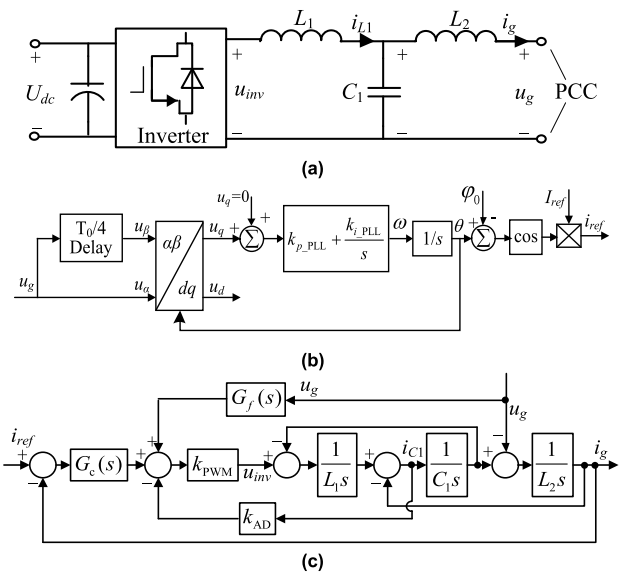

FIGURE 1. Structures of a single-phase grid-connected inverter. (a) LCL filter; (b) delay-based PLL; (c) current control.

II. SYSTEM DESCRIPTIONS AND MODELINGS

A. GRID-CONNECTED INVERTER AND ITS TYPICAL CONTROL

In Fig. 1(a), the *LCL* filter includes an inverter-side inductor L_1, a capacitor C_1, and a grid-side inductor L_2. U_{dc} is the dc-link voltage which can be linked to the renewable energy sources or the output of a front DC-DC converter, u_{inv} is the inverter output voltage, i_{L1} is the inverter-side current, i_g is the grid current, and u_g is the voltage at the PCC. Fig. 1(b) shows the delay-based PLL structure [11], [23], where k_{p_PLL} and k_{i_PLL} denotes the proportional and integral factors of the PI controller, T_0 is the fundamental frequency, φ_0 is the power factor angle (here, 0 for unity power factor), ω is the angular frequency, θ is the phase of PCC voltage u_g, I_{ref} is the grid current amplitude reference generated by the DC-link voltage control or the power control, i_{ref} is the instantaneous grid current reference. Fig. 1(c) depicts the current control used in this study, where $G_c(s)$ is the current controller, $G_f(s)$ is the feedforward factor of PCC voltage, k_{PWM} denotes the gain of PWM inverter (here, for the simplification, $k_{\mathrm{PWM}} = \mathrm{e}^{-sTd}$), and k_{AD} denotes the capacitor current (i_{C1}) feedback factor. Note that the DC-link or power control is ignored, considering that its bandwidth is relatively low compared to the PLL and current control bandwidth.

B. INVERTER OUTPUT IMPEDANCE MODELINGS

The typical impedance model is depicted in Fig. 2(a) [12], where the inverter is seen as a current source paralleled with the output impedance Z_{out} without considering the PLL, and the weak grid is modeled as a voltage source u_s in series with

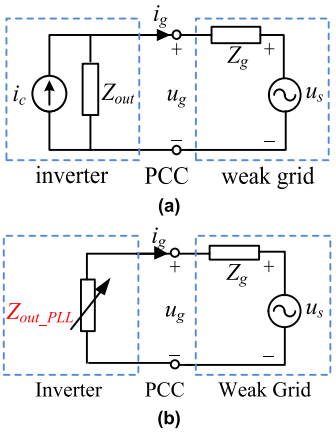

FIGURE 2. Impedance modelings of the grid-connected system. (a) typical model; (b) revised model considering the PLL.

the grid impedance Z_g. Figs. 1(a) and 1(c) tell:

$$\begin{cases} \dfrac{1}{C_1 s} \cdot \left(i_{L1} - i_g\right) = L_2 s \cdot i_g + u_g \\ u_{inv} = L_1 s \cdot i_{L1} + L_2 s \cdot i_g + u_g \\ \dfrac{u_{inv}}{k_{\mathrm{PWM}}} = G_c\left(s\right)\left(i_{ref} - i_g\right) - k_{\mathrm{AD}}\left(i_{L1} - i_g\right) + G_f\left(s\right) u_g \end{cases} \tag{1}$$

Then, i_g is calculated as:

$$i_g = G_{close}\left(s\right) \cdot i_{ref} - Y_{con}\left(s\right) \cdot u_g \tag{2}$$

where, $G_{close}(s)$ and $Y_{con}(s)$ are given by:

$$G_{close}\left(s\right) = \frac{G_c\left(s\right) k_{\mathrm{PWM}}}{L_1 L_2 C_1 s^3 + k_{\mathrm{AD}} k_{\mathrm{PWM}} L_2 C_1 s^2 + \left(L_1 + L_2\right) s + G_c\left(s\right) k_{\mathrm{PWM}}}$$
$$Y_{con}\left(s\right) = \frac{L_1 C_1 s^2 + k_{\mathrm{AD}} k_{\mathrm{PWM}} C_1 s + 1 - G_f\left(s\right) k_{\mathrm{PWM}}}{L_1 L_2 C_1 s^3 + k_{\mathrm{AD}} k_{\mathrm{PWM}} L_2 C_1 s^2 + \left(L_1 + L_2\right) s + G_c\left(s\right) k_{\mathrm{PWM}}} \tag{3}$$

Accordingly, the inverter current control can be simplified as Fig. 3. Then, the output impedance of the inverter system can be defined as:

$$Z_{out}\left(s\right) = \left.\frac{u_g}{-i_g}\right|_{i_{ref}=0} = \frac{1}{Y_{con}\left(s\right)} \tag{4}$$

Based on [18]–[21], the ratio of Z_g and Z_{out} must satisfy the Nyquist Criterion by counting the number of $\pm 180°$ −crossings in the frequency range with gains above 0dB.

Note that i_{ref} is treated as an independent source so that an independent current source occurs in Fig. 2(a). However, i_{ref} is indeed generated by the PLL which relates to u_g. That is to say, it is necessary to take into account the relation between the current reference i_{ref} and u_g, which is expressed as:

$$i_{ref} = T_{PLL}\left(s\right) \cdot u_g \tag{5}$$

where $T_{PLL}(s)$ denotes the PLL transfer function.

Considering the PLL effect, the current control structure of the inverter system changes from Fig. 3 to Fig. 4.

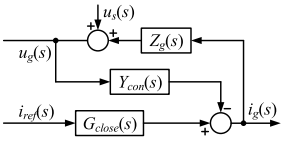

FIGURE 3. Simplified current control structure of the inverter system.

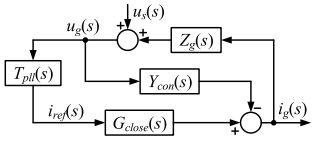

FIGURE 4. Simplified current control structure of the inverter system considering the effect of the PLL.

Hence, by using (1) and (5), the existence of PLL changes the expression of Z_{out} to be:

$$Z_{out\_PLL}\left(s\right) = \frac{u_g}{-i_g} = -\frac{1}{T_{PLL}\left(s\right) G_{close}\left(s\right) - Y_{con}\left(s\right)} \tag{6}$$

In other words, the independent current source in Fig. 2(a) is indeed absent, and the inverter output model should be revised as shown in Fig. 2(b).

C. MODELING OF THE DELAY-BASED PLL CONSIDERING THE FREQUENCY COUPLING EFFECT

For the modeling of Delay-based PLL, as pointed out in [32], in order to be more precise, the relation between the PLL signal u_β and u_α as well as the frequency coupling related to the grid impedance should be considered. Hence, this study follows the derivation method in [32], and the equivalent single-frequency diagram with considering the embedded multi-frequency principle is shown in Fig. 5, wherein s^p and s^n denote $(s + 2j\omega_0)$ and $(s - 2j\omega_0)$, respectively.

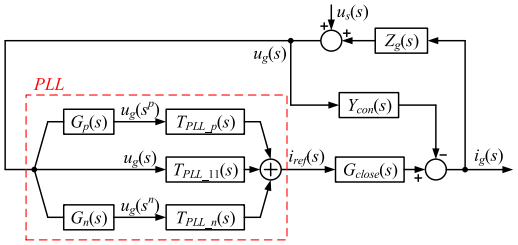

FIGURE 5. Single-frequency control diagram with the embedded multi-frequency principle.

Then, $u_g(s^p)$ and $u_g(s^n)$ are the PCC voltage components at the frequencies of $(s + 2j\omega_0)$ and $(s - 2j\omega_0)$, respectively. $T_{PLL\_11}(s)$, $T_{PLL\_p}(s)$ and $T_{PLL\_n}(s)$ are the transfer functions from $u_g(s)$, $u_g(s^p)$, and $u_g(s^n)$ to $i_g(s)$, respectively.

Following [32], their expressions are given as follows:

$$\begin{cases} T_{PLL\_11}(s) = I_{ref} \cdot 0.25 \\ \cdot \left\{ \begin{array}{l} \left[G_{OSG\_\alpha}(s) + jG_{OSG\_\beta}(s)\right] G_{PLL}(s - j\omega_0)\, e^{-j\varphi_0} \\ + \left[G_{OSG\_\alpha}(s) - jG_{OSG\_\beta}(s)\right] G_{PLL}(s + j\omega_0)\, e^{j\varphi_0} \end{array} \right\} \\ T_{PLL\_p}(s) = I_{ref} \cdot 0.25 \\ \cdot \left[-G_{OSG\_\alpha}(s^p) - jG_{OSG\_\beta}(s^p)\right] G_{PLL}(s + j\omega_0)\, e^{j\varphi_0} \\ T_{PLL\_n}(s) = I_{ref} \cdot 0.25 \\ \cdot \left[-G_{OSG\_\alpha}(s^n) + jG_{OSG\_\beta}(s^n)\right] G_{PLL}(s - j\omega_0)\, e^{-j\varphi_0} \\ G_{PLL}(s) = \dfrac{s \cdot k_{p\_PLL} + k_{i\_PLL}}{s^2 + U_m\left(s \cdot k_{p\_PLL} + k_{i\_PLL}\right)} \end{cases} \quad (7)$$

where, G_{OSG_α} and G_{OSG_β} are the transfer functions of the OSG in the delay-based PLL which are given by:

$$\begin{cases} G_{OSG\_\alpha}(s) = 1 \\ G_{OSG\_\beta}(s) = e^{-\frac{sT_0}{4}} \end{cases} \quad (8)$$

In addition, $G_p(s)$ and $G_n(s)$ in Fig. 5 are the closed-loop transfer functions of $u_g(s)$ to $u_g(s^p)$ and to $u_g(s^n)$:

$$\begin{cases} G_p(s) = \dfrac{u_g(s^p)}{u_g(s)} \\ = \dfrac{Z_g(s^p)\, G_{close}(s^p)\, T_{PLL\_n}(s^p)}{1 - Z_g(s^p) \cdot \left[G_{close}(s^p)\, T_{PLL\_11}(s^p) - Y_{con}(s^p)\right]} \\ G_n(s) = \dfrac{u_g(s^n)}{u_g(s)} \\ = \dfrac{Z_g(s^n)\, G_{close}(s^n)\, T_{PLL\_p}(s^n)}{1 - Z_g(s^n) \cdot \left[G_{close}(s^n)\, T_{PLL\_11}(s^n) - Y_{con}(s^n)\right]} \end{cases} \quad (9)$$

According to the equivalent single-frequency control diagram in Fig. 5, substituting the specific expression of $T_{PLL}(s)$ into (6), the output impedance of the inverter system when considering the frequency coupling effect is (10), as shown at the bottom of this page.

where the subscript FCE is the abbreviation of the frequency coupling effect.

III. INVESTIGATIONS AND PROBLEMS OF TYPICAL CONTROL

In this section, a robust controller which comes from the existing studies will be used, and the instability in the case of high grid impedance will then be analyzed.

A. CONTROLLERS AND PARAMETERS

The system parameters used in this study are given in Table 1. As proved by [21] and [33], reducing $G_f(s)$ is helpful to improve the robustness of the system, while the harmonic resonant controller with phase compensation (HQR-PC) can effectively suppress the low-order current harmonics and improve the phase of the system. Following [21], the feedforward factor $G_f(s)$ is selected as 0.6, and $G_c(s)$ is expressed as:

$$G_c(s) = k_p + k_r \sum_{n=1,3,\ldots}^{n_{\max}} \frac{s\cos(\varphi_n) - n\omega_0 \sin(\varphi_n)}{s^2 + \omega_c s + (n\omega_0)^2} \quad (11)$$

where ω_c represents the bandwidth of the resonant part, k_r/ω_c is the gain at $n\omega_0$, φ_n is the leading angel for each resonant part, and n_{max} is the maximum order of harmonics to be suppressed. By using larger φ_n, the phase at $n\omega_0$ is improved. The design of φ_n can refer to [21] and [33].

For the PI controller in the PLL, its parameters can be selected to achieve a desired bandwidth, by plotting Bode plots of $G_{PLL}(s)$ in (7) with MATLAB tools. Considering the selection of parameters is not the main theme, the detailed plots are not shown. Instead, the parameters are given in Table 1. In order to show the limitation of the typical PLL and the robustness of the proposed method more clearly, the PLL bandwidth is selected to be relatively high (here, about 0.27 kHz in the case of 15 kHz-switching frequency).

In addition, as discussed in [14], for the capacitor-current feedback AD, the large control delay is not beneficial for the resonance damping and AD robustness. Thus, many delay compensation methods have been proposed in the literatures. In this study, the delay compensation is used, and the remaining delay can then be seen approximating to $0.5/f_s$.

To simulate the weak grid with different short-circuit ratios (SCRs), Z_g is regarded as purely inductive and is represented by sL_g for convenience. For a rated power of 5kW, $L_g = 6$ mH

TABLE 1. Parameters of a single-phase TNPC inverter.

Parameter	Symbol	Value	Parameter	Symbol	Value
Rated power of system	P_{rated}	5 kW	Inverter-side inductance	L_1	0.75mH
DC voltage	U_{dc}	760 V	Grid-side inductance	L_2	0.45mH
Grid voltage	U_g U_{gm}	220 V 311 V	Filter capacitance	C_1	6.8 μF
Grid frequency	ω_0	100π rad/s	Switching frequency	f_s	15 kHz
PR current controller	k_p, k_r, ω_c	9, 600, 6	PLL controller	k_{p_PLL} k_{i_PLL}	3 2000
PCC voltage feedforward	$G_f(s)$	0.6	Power factor angle	φ_0	0
AD parameter	k_{AD}	13	Total delay time in k_{PWM}	T_d	$0.5/f_s$

$$Z_{out\_PLL\_FCE}(s) = \frac{u_g}{-i_g} = -\frac{1}{T_{PLL}(s)\, G_{close}(s) - Y_{con}(s)} = -\frac{1}{\left[G_p(s)\, T_{PLL\_p}(s) + G_n(s)\, T_{PLL\_n}(s) + T_{PLL\_11}(s)\right] G_{close}(s) - Y_{con}(s)} \quad (10)$$

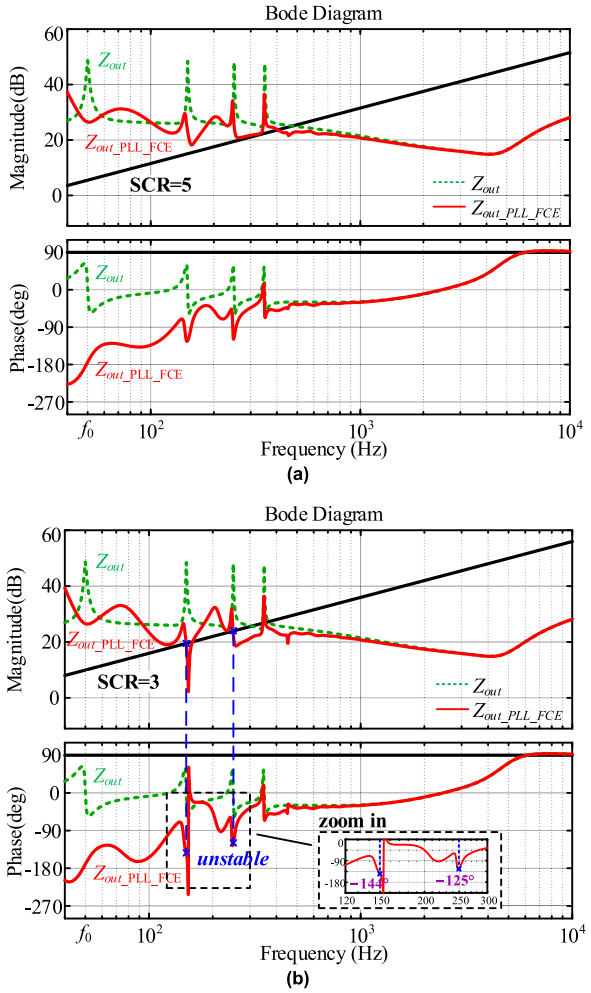

FIGURE 6. Bode plots of inverter output impedance without and with considering the PLL, when a typical robust controller is applied. (a) $L_g = 6$ mH (SCR = 5); (b) $L_g = 10$ mH (SCR = 3).

are used for representing SCR $= 5$. For SCR $= 3$, the value of L_g can be up to 10 mH.

B. INSTABILITY OF PLL FOR THE HIGH GRID IMPEDANCE

At first, the performance is analyzed when ignoring the impact of PLL. With $n_{max} = 7$ in (11) and Table 1, the green curves in Fig. 6(a) and (b) show the magnitude and phase response of (4). Note that this study uses φ_n to make the minimum phase of Z_{out} at $n\omega_0$ to be about $-50°$. It is found that the phases are all in the range between $-90°$ and $90°$ leaving some margins. In other words, the inverter output impedance is "passive" [17]. Even if Z_{out} intersects with Z_g in the magnitude curve at a low frequency, the PM at the crossing frequency is satisfactory (45° for "Z_{out}" in Fig. 6), which proves that the design of the current controller based on [21] is robust. However, such conclusion is not convincing, because the PLL impact is not considered in the low frequency range.

In (6), the PLL impact, i.e., term $T_{\mathrm{PLL}}(s)G_{close}(s)$, can be eased if I_{ref} reduces, as the study in [26] also tells. Thus, in this study, the rated power situation is especially concerned and the value of I_{ref} is I_{rated}, i.e., $1.414P_{rated}/U_g$. Besides, seen from (9) and (10), the characteristics of the output impedance considering the frequency coupling are different for different SCRs. The bode plots of $Z_{out\_PLL\_FCE}$ in (10), i.e., the inverter output impedance under different SCRs are also given in Fig. 6. Unlike the curves for Z_{out}, the existence of PLL can make the phases of inverter output impedance below $-90°$, yielding a "non-passive" feature. In other words, the phase of $Z_g/Z_{out\_PLL\_FCE}$ can cross 180° (i.e., $Z_{out\_PLL\_FCE}$ crosses $-90°$), and the instability can be aroused if the crossing occurs when the gains of $Z_g/Z_{out\_PLL\_FCE}$ above 0dB (i.e., the magnitude curve of Z_g is above $Z_{out\_PLL\_FCE}$). For the case study, when SCR $= 5$, the system can still remain stability. However, as shown in Fig. 6(b), if the grid impedance becomes even larger (e.g., the SCR reduces to 3), $Z_{out\_PLL\_FCE}$ and Z_g have multiple crossings in both the magnitude and phase curves. For SCR $= 3$, the serious instability is yielded because of the crossings at the frequencies close to 150 Hz and 250 Hz.

Note that this study simply uses the current control in Fig. 1(c) for showing the impact institutively. If other robust AD and current controllers are used, the similar phenomenon may be observed because the PLL dominates the behaviors of the inverter system at the very low frequencies [23], [26].

Although reducing the PLL bandwidth can be helpful for the robustness, the degradation of the system dynamic may not be worthwhile. Hence, a robust PLL approach is to be needed for extending the stable operation range without sacrificing the dynamic (i.e., with a high bandwidth).

IV. ROBUST PLL WITH GRID CURRENT FEEDFORWARD AND ITS PARAMETERS DESIGN

Note that the PLL can work well in the default case or with a small grid impedance. Hence, based on analyzing the differences of PLLs under different grid conditions, one way for improving the PLL can be deduced, and the novel robust PLL structure is formulated and discussed hereinafter.

A. ANALYSIS OF PLLS IN DIFFERENT GRID CASES

In the default case with $Z_g = 0$, the input signal u_{g_sample} of the PLL does not contain other components except u_s. On the contrary, in the weak grid cases, u_{g_sample} is the sampled signal of PCC voltage which contains not only u_s but also the voltage across the grid impedance. In other words, the main difference of PLL in the weak grid cases compared to the default case is the addition of $Z_g \cdot i_g$ into the PLL. Hence, it is deduced that the degradation of the system performance closely relates with the additional inductive part feeding into the PLL.

B. PROPOSED PLL WITH GRID CURRENT FEEDFORWARD

This study proposes to use an additional feedforward from i_g with the negative sign to compensate the inherent positive one ($+sL_g \cdot i_g$). The control structure is depicted in Fig. 7 where k_{ff} is the factor of the first-order derivative, and i_{g_sample} is the sampled signal of i_g. With the proposed

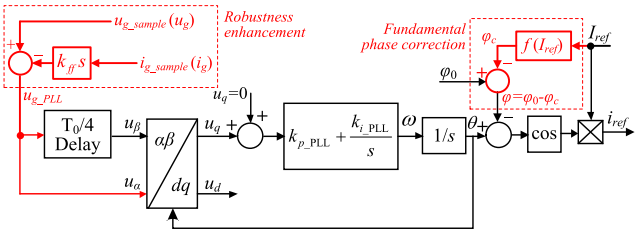

FIGURE 7. Proposed block of robust PLL with the grid current feedforward.

grid current feedforward, the signal used for grid synchronization changes to u_{g_PLL}. Besides, because the PLL input signal for synchronization is no longer the original PCC voltage signal, the correction of the power factor angle is required. Hence, an extra phase correction loop is added. Given that the grid current control can track the amplitude reference I_{ref} precisely (i.e., the amplitude of i_g is equal to I_{ref}), the phase correction is achieved by function $f(I_{ref})$ in Fig. 7.

With the added feedforward of i_g, (2) changes to:

$$i_{ref}(s) = T_{PLL}(s) \cdot \left[u_g(s) - k_{ff} s \cdot i_g(s)\right] \tag{12}$$

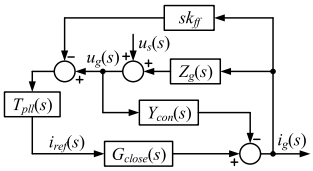

FIGURE 8. Simplified current control structure of the inverter system after adding grid current feedforward to the PLL.

After adding the grid current feedforward to the PLL, the simplified control structure of the inverter system changes from Fig. 4 to Fig. 8.

Furthermore, in the single-frequency modeling with the embedded multi-frequency principle after adding grid current feedforward to the PLL, the voltage reference of the PLL is no longer $u_g(s)$, $u_g(s^p)$ and $u_g(s^n)$ in Fig. 5, but becomes $u_g(s)$, $u_g(s^p)$ and $u_g(s^n)$ subtract the feedforward component at the corresponding frequency separately, that is:

$$\begin{cases} u_{ref\_PLL}(s) = u_g(s) - k_{ff} s \cdot i_g(s) \\ u_{ref\_PLL}(s^p) = u_g(s^p) - k_{ff} s^p \cdot i_g(s^p) \\ u_{ref\_PLL}(s^n) = u_g(s^n) - k_{ff} s^n \cdot i_g(s^n) \end{cases} \tag{13}$$

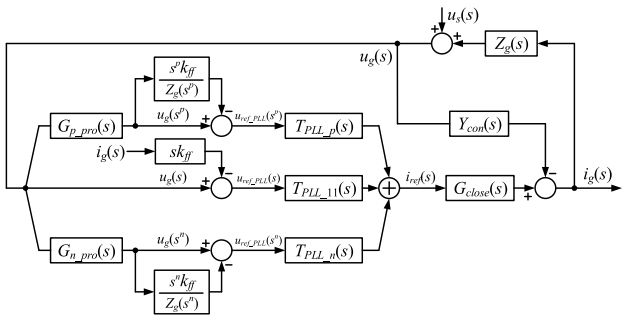

FIGURE 9. Single-frequency control diagram with the embedded multi-frequency principle after adding grid current feedforward to the PLL.

When deriving the small-signal function, the voltage harmonics in u_s at low frequencies can be considered as the disturbances and are thus ignored. Then, $u_g(s^p)$ and $u_g(s^n)$ can be regarded as generated only by $i_g(s^p)$ and $i_g(s^n)$, respectively. Combined with $u_g(s) = i_g(s) * Z_g(s) + u_s(s)$, the following equation can be obtained:

$$i_g(s^p) = \frac{u_g(s^p)}{Z_g(s^p)}, \; i_g(s^n) = \frac{u_g(s^n)}{Z_g(s^n)} \tag{14}$$

Therefore, for the inverter with adding the grid current feedforward to the PLL, its single-frequency control diagram with the embedded multi-frequency principle can be obtained, as shown in Fig. 9. In Fig. 9, $G_{p\_pro}(s)$ and $G_{n\_pro}(s)$ are the closed-loop transfer functions from $u_g(s)$ to $u_g(s^p)$ and from $u_g(s)$ to $u_g(s^n)$, which are expressed as (15), as shown at the bottom of this page.

Then, the inverter output impedance with the proposed PLL is calculated as (16), as shown at the bottom of this page.

C. DESIGN OF GRID CURRENT FEEDFORWARD FACTOR

At first, the phase correction which will be designed later is ignored when designing k_{ff}. In theory, ensuring $k_{ff} = L_g$ is always expected if Z_g varies during the operation. However, in the real-world application, Z_g is changing over the time. In addition, online parameter detection which usually requires complex algorithms is not used here. Therefore, in order to ensure a robust performance in both the default and the weak grid cases, the design should be well treated.

Considering the objective is to make the inverter work well even in the lowest SCR case and the inherent positive feedforward (i.e., $+sL_g \cdot i_g$ in u_g) is be compensated, the basic

$$\begin{cases} G_{p\_pro}(s) = \dfrac{u_g(s^p)}{u_g(s)} = -\dfrac{Z_g(s^p) G_{close}(s^p) T_{PLL\_n}(s^p) s k_{ff} - Z_g(s) Z_g(s^p) G_{close}(s^p) T_{PLL\_n}(s^p)}{Z_g(s)\left[1 + G_{close}(s^p) T_{PLL\_11}(s^p) s^p k_{ff}\right] - Z_g(s) Z_g(s^p)\left[G_{close}(s^p) T_{PLL\_11}(s^p) - Y_{con}(s^p)\right]} \\ G_{n\_pro}(s) = \dfrac{u_g(s^n)}{u_g(s)} = -\dfrac{Z_g(s^n) G_{close}(s^p) T_{PLL\_p}(s^n) s k_{ff} - Z_g(s) Z_g(s^n) G_{close}(s^p) T_{PLL\_p}(s^n)}{Z_g(s)\left[1 + G_{close}(s^p) T_{PLL\_11}(s^n) s^n k_{ff}\right] - Z_g(s) Z_g(s^n)\left[G_{close}(s^p) T_{PLL\_11}(s^n) - Y_{con}(s^n)\right]} \end{cases} \tag{15}$$

$$Z_{out\_PLL\_FCE\_robust}(s) = -\frac{1 + G_{close}(s) T_{PLL\_11}(s) s k_{ff}}{\left[G_{p\_pro}(s)\left(1 - \frac{s^p k_{ff}}{Z_g(s^p)}\right) T_{PLL\_p}(s) + G_{n\_pro}(s)\left(1 - \frac{s^n k_{ff}}{Z_g(s^n)}\right) T_{PLL\_n}(s) + T_{PLL\_11}(s)\right] G_{close}(s) - Y_{con}(s)} \tag{16}$$

guideline for selecting k_{ff} should be:

$$k_{ff} \geq L_{g\_\max} \tag{17}$$

where L_{g_max} represents the maximum value of L_g, i.e., the pure inductive grid impedance corresponding to the minimum SCR. Here, in this study, for making the inverter be robust for SCR ≤ 3, k_{ff} should follow $k_{ff} \geq 0.01$.

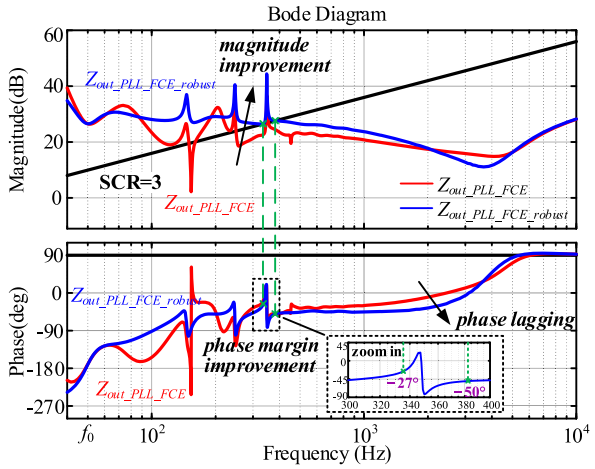

FIGURE 10. Bode plots of different output impedances with $k_{ff} = 0.01$ and SCR = 3.

Fig. 10 shows some Bode plots of different output impedances with $k_{ff} = 0.01$ and SCR $= 3$ to show the changes before and after using the proposed PLL. It is noticed that the proposed PLL can increase the magnitudes and phases of the output impedance in a wide frequency range. Especially, the increase in the magnitude of the proposed output impedance is mainly owing to the extra term introduced on the numerator. As a result, the intersection frequency of output impedance and grid impedance is heightened, which in turn improves the phase margin.

However, seen from Fig. 10, it is emphasized that the addition of the grid current feedforward in the PLL can cause some certain phase laggings at the relatively high frequencies (typically, above twice the PLL bandwidth). Therefore, besides (12), the selection of k_{ff} should also consider such side effect. For details, Fig. 11 depicts some Bode plots of improved $Z_{out\_PLL\_FCE\_robust}$ with different k_{ff}. Although the phases in the range from 1 to 2 kHz are still kept a certain distance from $-90°$, designing too large k_{ff} can affect the performance with a small grid impedance (i.e., in the cases of large SCRs and in the default case when the impedance intersection frequency can be high). As a summary of design, k_{ff} is suggested to be L_{g_max} or a litter larger. Note that the online grid impedance estimation is not needed here.

For the digital implementation, $s \cdot k_{ff}$ is applied to shape the behaviors at low frequencies (far lower than the Nyquist frequency). Hence, the classical backward and 1st high-pass filter (HPF)-based discretization can both be applied, because the implementation hardly causes mismatches with the pure derivative in magnitude and phase curves at low frequencies,

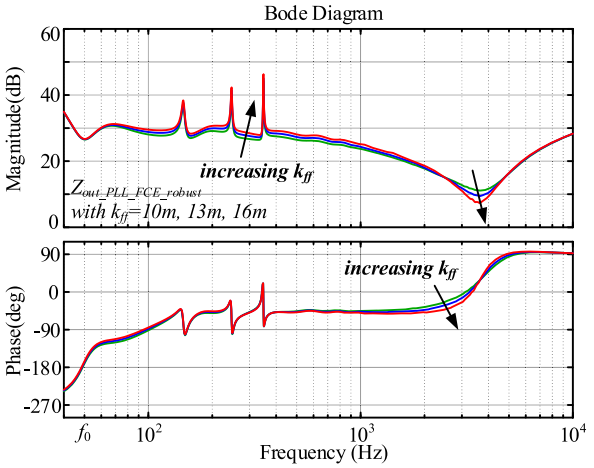

FIGURE 11. Bode plots of improved inverter output impedance with different k_{ff}.

as discussed in [33]. The grid current feedforward is achieved by the backward discretization method in this study.

In addition, the study in [31] did try to apply a similar thought to a three-phase inverter system. The grid current was fed into the PLL by using the proportional factor $j\omega_0 L_g$. Such approach was able to shape the behaviors below ω_0 in the case of using a low PLL bandwidth, while it has little effects at several hundred Hz because of the much lower gains of "$j\omega_0$" than "s". That is to say, the implementation in [31] fails to improve the behaviors above ω_0, which are also very critical for the inverter to work well in the weak grid.

D. DESIGN OF PHASE CORRECTION FUNCTION

For realizing the unity power factor, $f(I_{ref})$ is required. Assuming i_g is synchronized with u_{g_PLL} with the same phase, u_{g_PLL} will lag behind u_g at the fundamental frequency, and the lagging angle φ_c is expressed as:

$$\varphi_c = f(I_{ref}) = \arctan \frac{100\pi k_{ff} I_{ref}}{U_{gm}} \tag{18}$$

Substituting φ_c from φ_0, i.e., using φ in Fig. 7 to replace φ_0 in Fig. 1(b), can then make the phase of i_{ref} be the same with u_g instead of u_{g_PLL}. In addition, for the inverter output impedance with applying the phase correction, the angles in PLL functions, i.e., $T_{PLL\_11}(s)$, $T_{PLL\_p}(s)$, and $T_{PLL\_n}(s)$, need also to be changed accordingly. Note that φ_c is a function of the amplitude reference I_{ref} during the operation. Therefore, the implementation of $f(I_{ref})$ can be achieved through an index table programmed in the DSP. Readers can achieve different power factors by changing φ.

V. PERFORMANCE WITH THE PROPOSED CONTROL

A. STABILITY IN THE DEFAULT CASE

As the impedance-based stability criterion tells, the inverter must work stably when the grid impedance is set to 0. Therefore, the stability and performance with the proposed PLL should be examined at first in the default case. Note that

the proposed control does not change or add any feedbacks into the original current control structure in Fig. 1(c). Hence, the stability and performance with the current control are supposed to be not affected by the proposed feedforward in the PLL. In order to examine the stability, this study uses the closed-loop transfer function of the overall system including the current control and the PLL. Under the condition that the grid impedance is 0, $G_p(s)$, $G_n(s)$, $G_{p\_pro}(s)$, and $G_{n\_pro}(s)$ defined by (9) and (15) will all be equal to 0. Seen from Figs. 5 and 9, the closed-loop transfer functions with the typical control and the proposed control are separately expressed as:

$$\begin{aligned} &G_{closed-loop\_Typical}\big|_{Z_g=0}(s) \\ &= -\frac{1}{Z_{out\_PLL\_FCE}\big|_{Z_g=0}(s)} \\ &= T_{PLL\_11}(s)\,G_{close}(s) - Y_{con}(s) \end{aligned} \tag{19}$$

$$\begin{aligned} &G_{closed-loop\_Proposed}\big|_{Z_g=0}(s) \\ &= -\frac{1}{Z_{out\_PLL\_FCE\_Robust}\big|_{Z_g=0}(s)} \\ &= \frac{T_{PLL\_11}(s)\,G_{close}(s) - Y_{con}(s)}{1 + G_{close}(s)\,T_{PLL\_11}(s)\,sk_{ff}} \end{aligned} \tag{20}$$

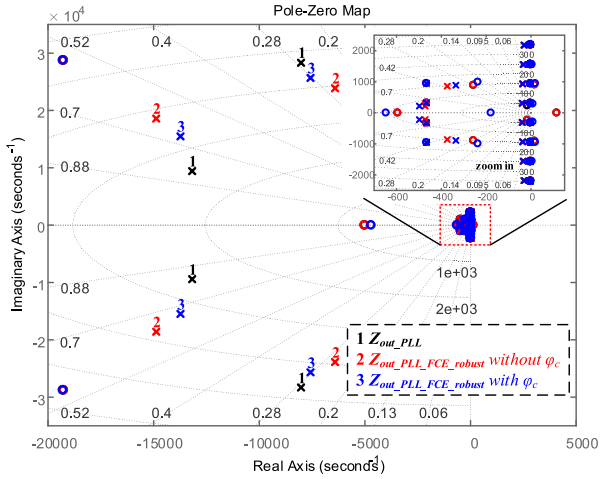

FIGURE 12. Pole-zero maps of inverter output impedances with different PLLs.

Fig. 12 depicts some pole-zero maps of (19) and (20) where Marks 1, 2 and 3 represent the system with the typical control, that with the proposed control without the phase correction, and that with the proposed control with using the phase correction, respectively. First of all, the system is always stable no matter with which control method, because all the poles are located on the left-half plane. Compared with the typical control (Mark 1), the low-frequency poles and zeros with the proposed control (Marks 2 and 3) change slightly, which means the dynamic with the proposed PLL is almost unchanged. Besides, although the differences of high-frequency poles are considerable for different PLLs, damping factors of these high-frequency poles change slightly, which means the high-frequency resonance caused by the *LCL* filter is still well suppressed.

As a summary, the proposed PLL does not affect the stability in the default case without the grid impedance. Then, in the next part, the impedance-based stability criterion is used to evaluate the robustness.

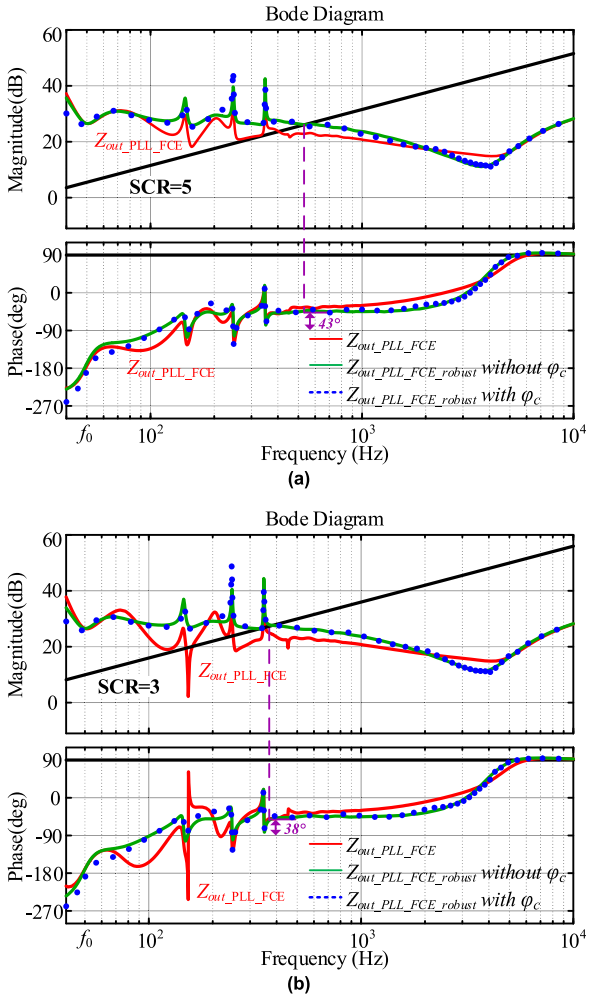

FIGURE 13. Bode plots of different grid impedances and inverter output impedances with different PLLs. (a) L_g = 6 mH (SCR = 5); (b) L_g = 10 mH (SCR = 3).

B. ROBUSTNESS IN THE WEAK GRID CASES

Fig. 13 depicts some plots of the inverter output impedance with the proposed PLL with applying the phase correction. The dashed curves in Fig. 6 for the typical control are shown again for intuitive comparisons. Clearly, the output impedance with the proposed control is heightened. With the proposed PLL, for SCR = 5, the phase at 529 Hz is −47°; for SCR = 3, the phase at the crossing frequency 369 Hz is −52°. In other words, the PMs of the inverter-grid system are always about 40°. A high robustness is achieved. Note that larger k_{ff} can yield a higher improvement, but 0.01 is enough here. Know from the comparisons of Figs. 6 and 13, the proposed PLL can be considered as an extension of the

existing robust controllers, so as to solve serious harmonics and instabilities when the SCR is much lower than 10, while the online grid impedance estimation is not needed.

VI. VERIFICATIONS

A. COMPARISONS WITH THE TYPICAL DELAY-BASED PLL

A single-phase grid-connected inverter has been built in the Saber simulator. The dc-link is connected to a constant voltage source. The grid voltage u_s is 200 V/ 50 Hz simulated by a voltage source. In the simulation, the time step is 200 *ns* and the truncation error is 0.0005.

At first, the waveforms of u_q (which representing the phase error in the PLL) subjected to the sudden drop of grid voltage are shown in Fig. 14. The proposed method with the grid current feedforward works almost the same as the typical delay-based PLL. In other words, the proposed grid current feedforward which is used to improve the robustness does not affect the transient performance of the PLL, which supports the analysis in Part A of Section V.

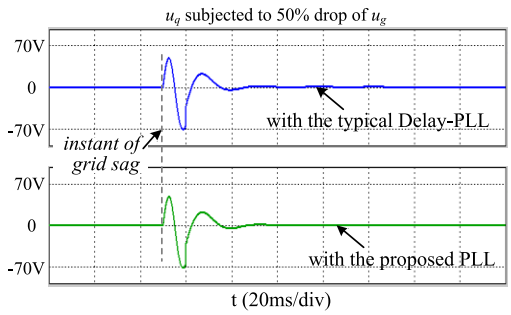

FIGURE 14. Waveforms of u_q with different PLLs.

Then, the simulations are done when the voltage source contains 2% 3rd, 2% 5th and 2% 7th harmonics, i.e., the total harmonic distortion (THD) of u_s is 3.46%. Z_g is simulated by adding an inductor between the PCC and u_s. I_{ref} is set to be I_{rated}. Selected waveforms of the PCC voltage u_g and the grid current i_g with different control for different grid impedance are shown in Fig. 15, while the THD values are provided in Table 2. Note that the oscillations of the PCC voltage shown in Fig. 15(b) is caused by overmodulation. Compared to the typical PLL control, the proposed control can yield much lower THD values no matter how large Z_g is. It is mentioned that the lower THD with the proposed control in the default case ($Z_g = 0$) is owing to the higher magnitudes of the inverter output impedance at low frequencies. The main reason for the lower THD with large L_g is the higher PM value provided by the proposed PLL (as depicted in Fig. 13). In addition, the transient waveforms in Fig. 16 tell that the grid current with the proposed PLL quickly changes with negligible transient oscillations and low distortion, even if a large grid impedance is interfered.

Furthermore, a single-phase T-type neutral point clamped (TNPC) inverter is built in the lab for experiments, by implementing the sampling and the overall control in a DSP TMS320F28335. The capacitance of the upper and lower

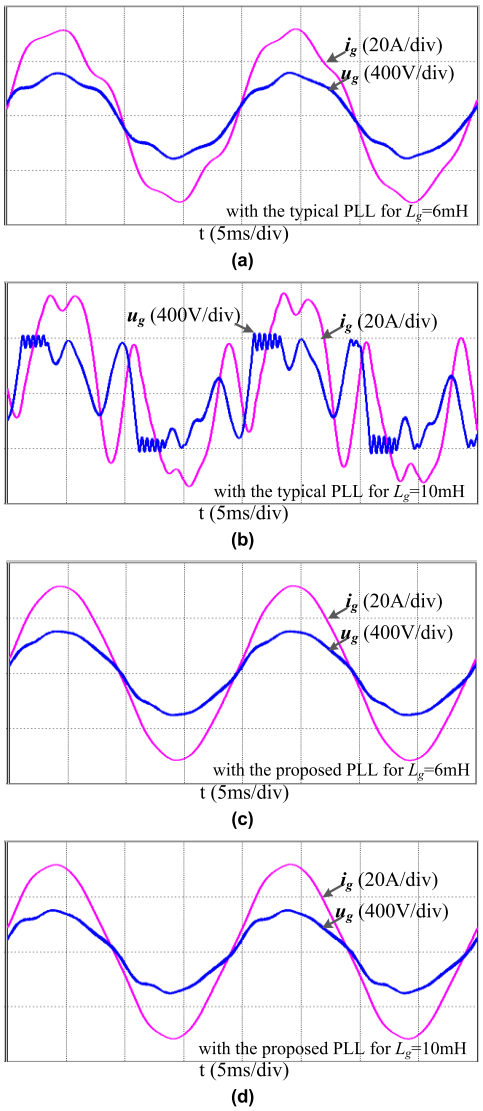

FIGURE 15. Waveforms of PCC voltage and grid current with different PLLs in the weak grid cases. (a) with the typical one for L_g = 6 mH; (b) with the typical one for L_g = 10 mH; (c) with the proposed one for L_g = 6 mH; (d) with the proposed one for L_g = 10 mH.

TABLE 2. THD results with different PLLs for different grid impedance.

THD results		L_g=0	L_g=3 mH	L_g=6 mH	L_g=10 mH
typical	u_g	3.46%	5.29%	6.02%	unstable
control	i_g	2.58%	3.71%	3.83%	unstable
robust	u_g	3.46%	4.60%	5.49%	7.42%
control	i_g	1.49%	1.38%	1.78%	2.52%

half-bridges of the DC-link are both 1.8 mF. As suggested by the simulations, the serious resonance can be aroused in the tests. Therefore, for the sake of safety, all the experiments are carried out under a scale-down condition. The grid voltage and current levels are both 1/4 of those shown in Table 1. The *LCL* parameters are the same as Table 1. Then, for the scale-down inverter, SCR = 5 means L_g = 6 mH, and SCR = 3 represents L_g = 10 mH. The typical Delay-based

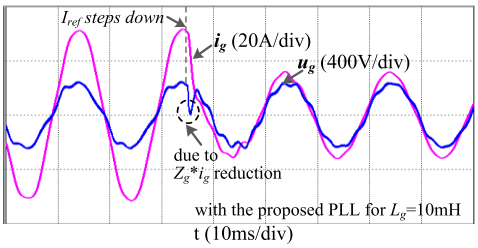

FIGURE 16. Transient waveforms when I_{ref} steps down, with the proposed PLL and a large grid impedance.

PLL and the proposed PLL are then compared for three different grid impedance values, i.e., $L_g \approx 0, 5.5, 11$ mH. The waveforms of grid current and PCC voltage are captured by an oscilloscope ZDS3024. Note that the current is measured through a Hall sensor and "1 V" in the figures means 1 A while the voltage is obtained through a differential probe and "1 V" means 1 V.

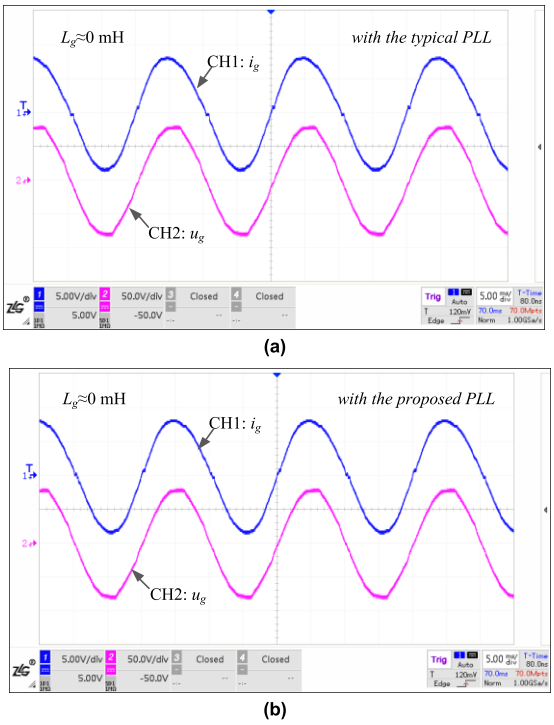

FIGURE 17. Waveforms in the default case with $L_g \approx 0$. (a) with the typical PLL; (b) with the proposed PLL.

Figs. 17, 18, 19 and 20 depict some experimental waveforms when the grid impedance is about 0, 5.5 or 11 mH. From these results, it is summarized as follows:

1) When the grid impedance is set to about 0, the inverter with the proposed PLL performs almost the same as the typical PLL, as depicted in Fig. 17. But, as the detailed grid current spectra in Fig. 18 tell, the current harmonics at the low-order frequencies with the proposed PLL are lower than those with the typical PLL, specially

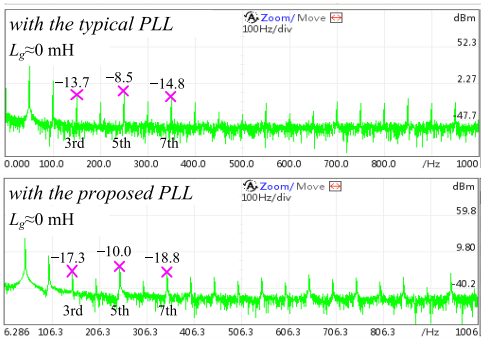

FIGURE 18. Grid current spectra with different PLLs and $L_g \approx 0$ obtained from the oscilloscope.

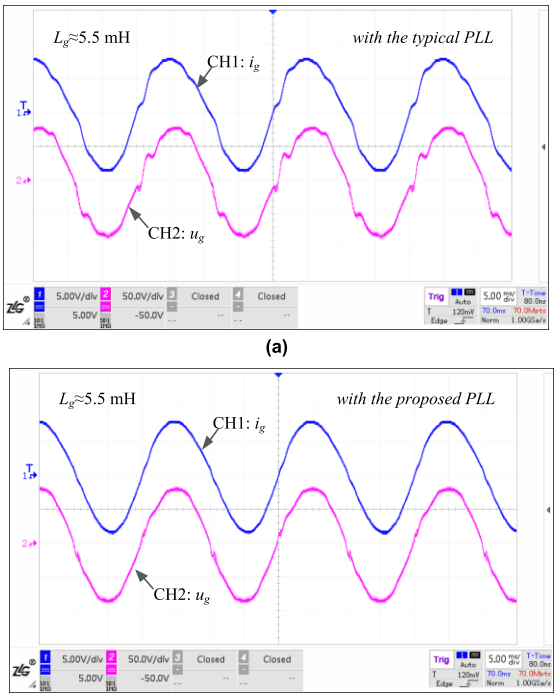

FIGURE 19. Waveforms with $L_g \approx 5.5$ mH. (a) with the typical PLL; (b) with the proposed PLL.

at the 3rd, 5th and 7th frequencies. These test results conform to the simulations and the theoretical analysis.

2) When the grid impedance is set to about 5.5 mH, the two PLLs can both maintain the stability, as shown in Fig. 19. However, the two sub figures in Fig. 19 exhibit a notable difference in the low-order current harmonics, even under the same current controller and parameters. Compared to the proposed PLL (with THD-i_g $\approx$ 2.4%), because of the poorer stability margin with the typical PLL, i_g in Fig. 19(a) is more highly distorted (with THD-i_g over 6%). Then, considering u_g consists of the voltage across L_g, the low-frequency distortion of u_g is yielded in Fig. 19(a).
3) In Fig. 20, once the grid impedance increases to 11 mH (i.e., with SCR $<$ 3), the typical PLL is unable to promise a stable operation of the inverter, while the

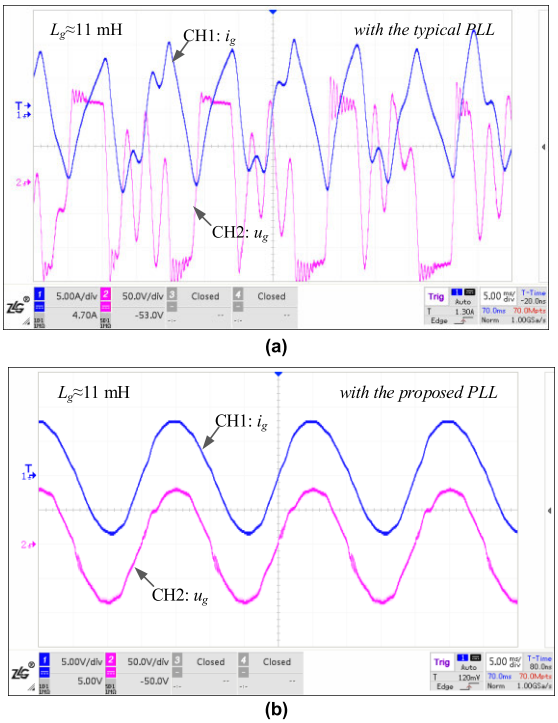

FIGURE 20. Waveforms with $L_g \approx 11$ mH. (a) with the typical PLL; (b) with the proposed PLL.

inverter with the proposed PLL still works stably with only a slight grid current distortion. The proposed grid feedforward-based PLL works well, as expected.

4) As Figs. 17(b), 19(b) and 20(b) tell, the waveforms of i_g with the proposed PLL are almost unchanged. In other words, a high robustness against the variation of L_g is achieved in the practical application. It is mentioned that, compared to u_g in Fig. 19(b), the notable distortion of u_g in Fig. 20(b) is yielded because the term $sL_g \cdot i_g$ can dominate the low-frequency components in u_g with the increase of L_g.

As a conclusion, the limitation of the typical PLL and the effectiveness of the proposed PLL have been verified. It is noticed that i_g in Fig. 18 has a considerable second-order harmonic. This harmonic is produced partly because of the slight imbalance between the two capacitors voltages at the DC-side of the TNPC prototype, where a software-based DC injection is simply used for voltage balancing. Despite of this, the experimental waveforms have demonstrated the superior performances with the proposed method.

B. COMPARISONS WITH OTHER OSG-BASED PLLS

Some simulation results with the existing OSG-based PLLs under the weak grid condition will be provided in order to further show the benefit of the proposed method. Fig. 21 shows the waveforms with single-phase PLLs (including the enhanced phased-locked loop (EPLL) in [10] and the Park-based PLL in [11], [34]) when L_g is set to be 6 mH and 10 mH. Note that the PI parameters in all the PLLs are

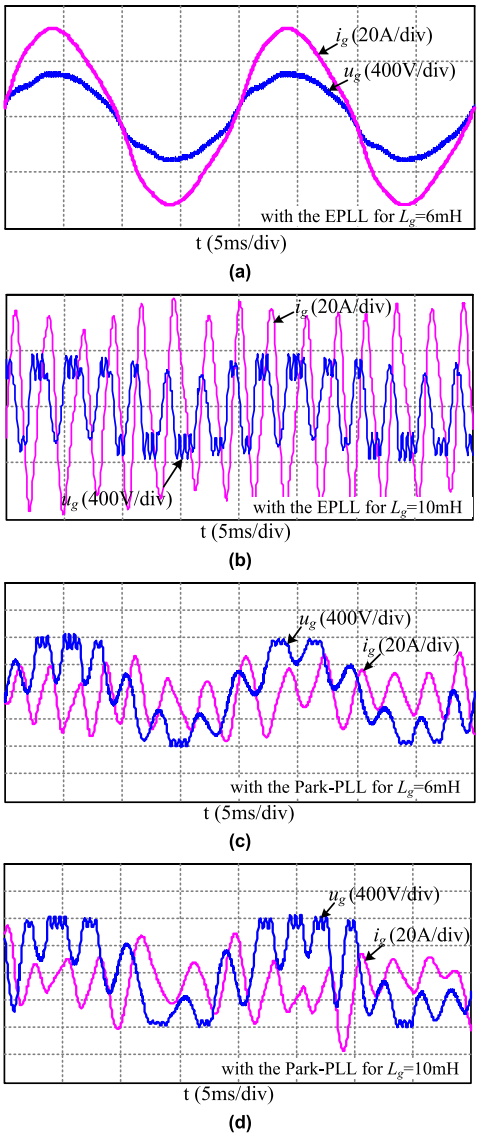

FIGURE 21. Waveforms of PCC voltage and grid current with other types of PLLs in the weak grid cases. (a) with the EPLL for $L_g = 6$ mH; (b) with the EPLL for $L_g = 10$ mH; (c) with the Park-based PLL for $L_g = 6$ mH; (d) with the Park-based PLL for $L_g = 10$ mH.

kept the same as those used in Fig. 15. Seen from the results, the EPLL is robust if the grid impedance is not very high. But larger L_g still yields the serious instability. Even worse, the Park-based PLL cannot work well even if L_g is not high.

VII. CONCLUSION

For the grid-connected inverter, the PLL has a non-negligible interaction with the grid impedance. In this study, the delay-based PLL is taken as the benchmark. The major conclusions are as follows:

1) With ignoring the PLL, the impedance-based criterion tells that the inverter works satisfactorily in the weak grid cases. However, if the grid impedance is large, the inaccurate impedance model with ignoring the PLL can fail to predict the robustness. Taking into account

the PLL is necessary for analyzing the behaviors within twice the PLL bandwidth.

2) The voltage across the grid impedance which is injected into the grid synchronization signal shall be responsible for the large amount of harmonics and instability.
3) The robust delay-based PLL proposed in this paper can increase the magnitude of the output impedance. Then, the intersection frequency of output impedance and grid impedance is heightened, which in turn improves the phase margin.
4) By analyzing the closed-loop poles, the proposed PLL is proved to have almost no adverse effect to the stability and dynamic in the default case (with small or negligible grid impedance). Besides, because of the improved magnitudes at the low frequencies, the current low-order harmonics with the proposed PLL are much lower than the typical PLL in the default case.
5) Because of the improved phase margins with the proposed PLL and its robust design, the inverter works satisfactorily for the grid impedance varying. The grid current quality can exhibit a high robustness even if the SCR goes down to 3 or even lower.

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