

Received April 15, 2020, accepted May 7, 2020, date of publication May 19, 2020, date of current version June 30, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2995726

# Negative Conductance Modeling and Stability Analysis of High-Frequency Oscillation Based on Cascode GaN Circuits

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This work was supported by the Fundamental Research Funds for the Central Universities under Grant 2019YJS166.

**ABSTRACT** GaN devices are developed rapidly in recent years, which makes it possible to produce power electronic converters with higher efficiency and higher power density. However, with the circuit parasitic parameters, large di/dt and dv/dt caused by the GaN devices' extremely fast switching can easily lead to voltage and current oscillations. This problem affects circuit stabilities and increases the difficulty of application with GaN devices. In this paper, oscillation problems will be explained by oscillator theory and an oscillation suppression method will be introduced. All the researches here are based on Cascode GaN devices. Considering all circuit parasitic parameters, negative conductance models of the GaN devices in the switching-on and switching-off process have been established according to oscillation mechanism analysis. And stability criteria of the GaN-based circuit have been derived which can well predict that whether the oscillations will happen and how will the oscillations last. Besides, the suppression method that placing a ferrite bead in power loop in series has been introduced based on the established model. Selection method is provided quantitatively and suppression effect can be calculated. All the achievements of this research have been verified by simulations and experiments.

**INDEX TERMS** GaN, stability criteria, modeling, high-frequency oscillation, oscillation suppression.

## I. INTRODUCTION

In recent years, the wide bandgap semiconductor devices such as Gallium Nitride (GaN) HEMT and Silicon Carbide (SiC) MOSFET are booming. They can work at high switching frequency and help power electronics devices achieve high efficiency as well as high power density [1]–[5]. Compared with SiC MOSFET, GaN devices have relatively lower rated voltage and are more suitable for low voltage applications. Besides, GaN devices have two other characteristics including smaller conduction resistance and junction capacitance, leading to lower conduction loss and higher frequency [6]. According to the manufacturing technology, GaN devices can be divided into Cascode type and Enhanced mode (E-mode) type. Both have been studied a lot and put into applications. With the Cascode GaN devices, Virginia Tech University has developed a 2kW Buck converter (operation frequency is 600kHz and the peak efficiency is 99%) and a

600W Boost converter (operation frequency is 5MHz and the efficiency is higher than 98% at any operating point) [7], [8]. The objects of this paper are Cascode GaN devices.

If switching frequency is increased to MHz level in the GaN based application, the di/dt and dv/dt will be 3000A/ $\mu$ s and 80~100V/ns even higher. With the influence of parasitic parameters in the circuit, there will be switching waveforms oscillation which may last in the whole high frequency period or be divergent [9]. Fig.1 shows the oscillating waveforms of drain-source voltage ( $v_{DS}$ ) and drain current ( $i_d$ ) in a dual pulse test (DPT) circuit. When oscillations happen, the high voltage and current stresses will affect devices reliability. Besides, power loss will be increased which makes the device temperature higher. If the oscillations are sustained or even divergent, the circuit will be unstable even damaged.

For Cascode GaN devices, the general relationship between oscillation and partial circuit parameters can be obtained by switching process analysis and simulation [10]–[12]. In further oscillation mechanism researches, the methods can be divided into three categories. They are

The associate editor coordinating the review of this manuscript and approving it for publication was Poki Chen<sup>1</sup>.

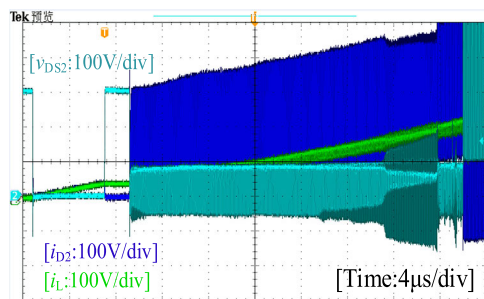


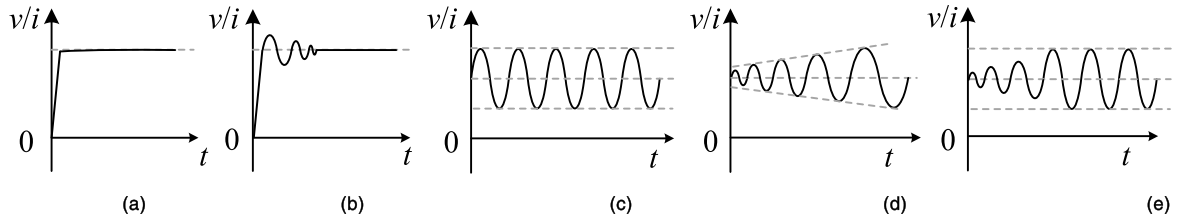
FIGURE 1. Experimental oscillation waveforms in DPT circuit.

based on circuit theory [13]–[18], control theory [20]–[22] and oscillator theory [23]–[25] respectively. Researches in [13]–[17] analyze the current and voltage oscillation process with equivalent circuit and formula of electric parameters. Oscillation waveforms are detailed illustrated but it is complicated to quantitatively calculate the oscillation conditions. Research in [18] uses the second-order circuit theory to analyze the cause of oscillation. In this method, the devices are assumed as fully on or off to be considered as a resistance or capacitor. But in fact, some oscillations happen when the devices are in the variable resistance region, where the driving voltage exceeds the threshold but is not high enough to make the device fully switched on. Considering this point, the applications of control theory and oscillator theory are more comprehensive and accurate. Control theory is a common method for stability analysis of converters [19]. In [20], sustained oscillation during the devices' switching-off process has been studied by small signal model based on the E-mode GaN devices. Loop feedback system is established and zero-pole map is used to analyze the circuit stability. Reference in [21] studies the oscillation problem of E-mode GaN devices caused by the active device's mistaken switching-on during its switching-off process. A feedback system model is established to analyze the change of active device's driving voltage. Then judge the convergence of the driving voltage to analyze the circuit stability. The research method of [22] is the same as that of [21]. But the studied oscillation is during the active device's switching-on process and the model is based on Cascode GaN devices. The internal structure of Cascode device is considered but it is ignored that the internal structure is changed under different driving voltage. References [23]–[25] belong to the third categories. In [23], sustained oscillation of E-mode GaN devices is analyzed by modeling. In this model, driving resistance is set to zero to make the most serious oscillation. Barkhausen criteria are used to judge whether the circuit meets the oscillation conditions but how the oscillation last can't be determined. The researches in [24], [25] are based on SiC MOSFET and negative resistance oscillator theory is used to analyze the switching-off oscillation. The studied oscillation is caused by the active device's mistaken switching-on. The model only considers the active device and take the passive device as short circuit. Besides, no parasitic parameter is

taken into account. In this paper, the oscillation problem of Cascode GaN-based circuit will be analyzed with negative resistance oscillator theory. Different oscillation mechanisms from [24], [25] are studied. Effect of the passive device to circuit stability is focused on both in active device's switching on and off process. The established model considers the interaction between two devices and includes both the active and passive devices. Besides, all the parasitic parameters are included.

To solve oscillation problems, the suppression methods are divided into active methods and passive methods in this paper. The active suppression methods mean impeding the oscillation's appearance by controlling stray parameters [26]–[28]. Stray parameters include the internal adapter capacitance of the device, the parasitic inductance and capacitance of PCB, the parasitic inductance of driving circuit and power circuit, etc. For Cascode GaN devices, stack-die package structure with low parasitic inductance [29] and internal capacitance matching [14] control the device parameters. But these methods are difficult to realize in device application. As for the circuit parameters, using kelvin packaged devices [30] and vertical structure layout [31] can reduce the parasitic inductance in the circuit, leading to lower switching peak value of voltage and reduced possibility of oscillation. But the reduction is constrained by many factors. Besides, [32] mentions reducing the switching speed and [30] mentions negative voltage switching-off. But these will sacrifice the high-speed capability of GaN devices and add extra power supplies. Since the active methods have limitations, passive methods which mean adding suppressors into circuit should be used for some already happening oscillations. References [21] and [33] introduce the design method of RC snubber circuit added in the driving circuit and main power circuit respectively. A patent of Transphorm Company introduces an oscillation suppression method which is taking the ferrite bead (with impedance of dozens of ohms at 100MHz) as driving resistance [34]. Switching speed will be decreased to some degree and the literature doesn't tell the boundary conditions of the oscillators' parameters. What's more, there are also some literatures which mention the method of adding a ferrite bead in the power loop [18], [22]. However, though these literatures introduce this method, they give no detailed selection method of the ferrite bead or quantitative calculation of the suppression effect. In this research, the method of adding a ferrite bead in the power loop will be further studied. Based on the established model and stability criterion, the detailed selection method is introduced and the suppression effect can be calculated.

In this paper, responses of GaN devices' switching process are classified into five kinds, as shown as Fig.2. Fig.2(c) and Fig.2(d) cannot exist stably in the actual circuit and will eventually be transformed into high frequency continuous oscillation which is Fig.2(e). Compared with Fig.2(b), the oscillations in Fig.2(e) will have more serious impact. Therefore, the latter one is focused on in the following analysis.



**FIGURE 2.** Classification of oscillations. (a) No oscillation. (b) Self-extinguishing oscillation. (c) Continuous oscillation. (d) Divergent oscillation. (e) High frequency continuous oscillation.

Based on the above introduction, this research applies oscillator theory into the circuit stability analysis of Cascode GaN-based circuit and provides a methodology about the application. According to comparison between two existing oscillator theory, negative resistance oscillator theory is selected. Then based on the oscillation mechanism analysis, the stages to be modeled in the switching on and off processes are determined. With the proper equivalent circuit, negative conductance models of Cascode GaN devices are established and stability criteria for the models are derived. These make it possible to predict whether continuous oscillations will happen in a Cascode GaN-based circuit, which is helpful to reduce the probability of oscillation problems during the circuit design. The established model considers the interaction of two devices in one bridge arm and all the parasitic parameters. With this methodology, both the switching-on and switching-off process are analyzed. And the influence of significant parameters on the circuit stability can be reflected. As for oscillation suppression, this paper analyses the passive method of series ferrite bead in the power loop based on the established model. The detailed selection criteria of the ferrite bead are introduced with calculation. The circuit stability with the series ferrite bead can be determined by the proposed stability criteria.

This paper is divided into six part. Part II introduces the applicability of oscillator theory in this study and the key points in application. Part III establishes the negative conductance oscillation model of Cascode GaN devices in the switching-on and switching-off process. Part IV verifies the oscillation model by calculation and experimental results. Part V analyses the suppression method which is verified by calculation and experimental verifications. Part VI concludes the whole research.

## II. OSCILLATOR THEORY APPLICATION METHOD

Originally, oscillator theories and stability criteria are used to design the oscillators which can produce stable oscillation waveforms. But these can also be used to avoid oscillations.

There are two oscillator theories, feedback oscillator theory and negative resistance oscillator theory [35]. In this paper, the latter is selected to analysis oscillation problem of Cascode GaN devices. Here are the reasons. Firstly, a feedback system needs to be constructed when using the feedback oscillator theory. But the model of the negative resistance

oscillator theory can be obtained just by simplification based on proper equivalent circuit diagram with no requirement of the feedback system construction. Secondly, feedback oscillation theory cannot predict how the oscillation continues alone. The control theory is also needed to accomplish the circuit stability analysis, leading to an increased complexity. Besides, the negative conductance model can be extended to complex circuits more easily by block calculation, combination and superposition. But with the feedback oscillation theory, a full recalculation is required if the circuit changes.

In this part, the application method of the negative resistance theory in GaN devices' oscillation analysis is introduced.

To use this theory, the switching stages to be analyzed should be selected first, which determines the equivalent circuit diagram. The following analysis is based on the dual pulse test (DPT) circuit shown as Fig.3. Papers [24], [25] study the sustained oscillation caused by mistaken switching on of the active device in switching-off process. However, besides this oscillation mechanism, sustained oscillations can also happen because of the passive device's mistaken switching on both in the switching on and off processes. Therefore, the effect of the passive device to circuit stability is focused on in this research, supposing the active device's  $v_{gs}$  is normal. With the large  $dv/dt$  and  $di/dt$  when switching, there are displacement current and induced voltage under the influence of the internal junction capacitance  $C_{GD}$  and common source inductor  $L_{CS}$ . Then, displacement current and inductive voltage will have coupling effect on  $T_1$ 's junction capacitance  $C_{GS}$ , leading to the changing of  $v_{gs}$ . When the  $v_{gs}$  is higher than the threshold voltage  $v_{th}$ ,  $T_1$  is switched on mistakenly, resulting in a change in the impedance relationship of the circuit. Fig.4 shows the main waveforms during switching process of  $T_2$ . The switching stages to be modeled are  $[t_4 \sim t_6]$  in switching on process and  $[t_9 \sim t_{11}]$  in switching off process.

In the two switching stages, GaN devices can be considered as the active components in the circuit which provide energy consumed by the other passive components. If the provided is equivalent to the consumed, the circuit will experience high frequency continuous oscillation. The active component can be regarded as a negative resistance device. Take it as a two-port network connected with two branches. One branch is to the active part, called the terminating matching network.

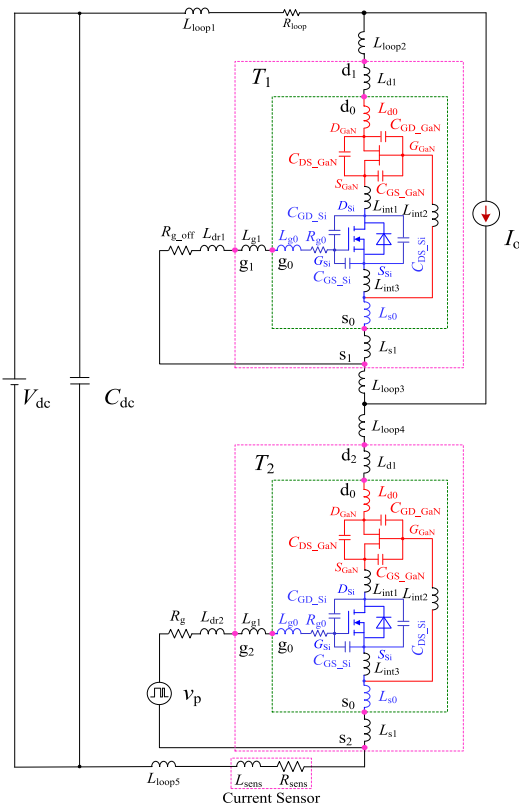


FIGURE 3. Dual pulse test (DPT) circuit based on Cascode GaN devices.

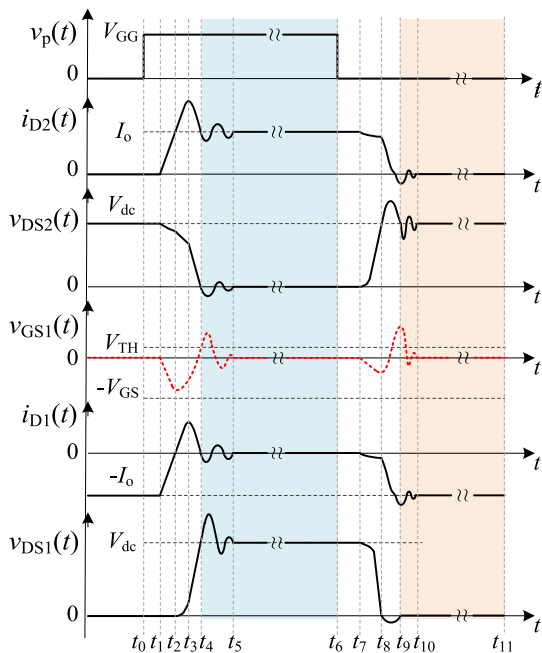


FIGURE 4. Main waveforms during switching process of T<sub>2</sub>.

The other is to the passive part, called load-matching network. For simplicity of calculation, express the two branches' impedance as admittance and a negative conductance model is formed as this way, as shown as in Fig. 5.

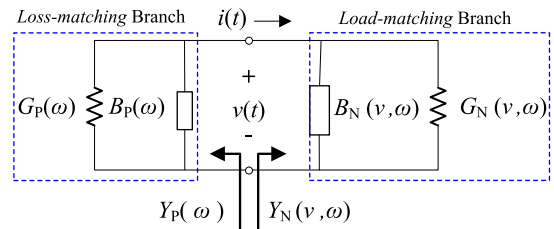


FIGURE 5. The negative conductance model.

In this model, the negative resistance device is represented by the voltage amplitude and frequency function, as shown in equation (1):

$$Y_N(v, \omega) = G_N(v, \omega) + jB_N(v, \omega) \quad (1)$$

where  $v$  is the amplitude of the current  $v(t)$  and  $\omega$  is the angular frequency. Other passive devices in the circuit can be equivalent as shown in equation (2).

$$Y_P(\omega) = G_P(\omega) + jB_P(\omega) \quad (2)$$

According to the negative conductance model, the type of the oscillation waveforms can be predicted by  $G_N(v, \omega)$  and  $G_P(\omega)$  which are the real parts of  $Y_N(v, \omega)$  and  $Y_P(\omega)$ . So the oscillation criteria of the oscillator circuit are shown as follows:

(1) if  $G_P(\omega) + G_N(v, \omega) > 0$ , which means the circular conductance around the oscillation frequency  $\omega$  is a positive value and thus consumes energy, the oscillation will be self-extinguishing.

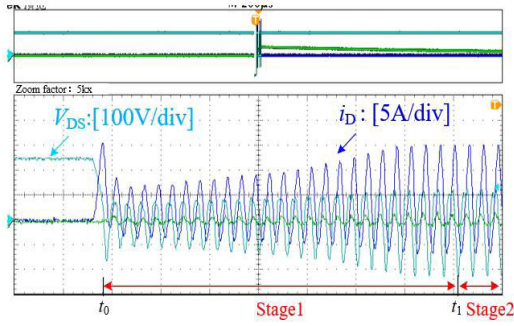
(2) if  $G_P(\omega_0) + G_N(v_0, \omega_0) = 0$  and  $B_P(\omega_0) + B_N(v_0, \omega_0) = 0$ , which means there is no conductance or electrical admittance in the negative conductance model with the certain voltage  $v_0$  and frequency  $\omega_0$ , the circuit will have constant amplitude oscillation. The voltage  $v_0$  and frequency  $\omega_0$  won't change and can be calculated by the two equations.

(3) if  $G_P(\omega) + G_N(v, \omega) < 0$ , which means the circular conductance around the oscillation frequency  $\omega$  is negative value and thus provide energy, the oscillation will be divergent.

Besides, according to Fig. 6, the oscillation waveforms of GaN based circuit are divided into two stages. Waveforms in stage 1 are compared to divergent oscillation while the waveforms in stage 2 are compared to constant amplitude oscillation. In the actual circuit, it is impossible to make the oscillation diverge indefinitely. The divergent oscillation will turn into the constant amplitude oscillation in the end because of the non-linearity of GaN devices. Therefore, the analysis of oscillation should be focused on the stage 1.

### III. NEGATIVE CONDUCTANCE MODELING

In this part, the negative conductance modeling method for the DPT circuit with Cascode GaN devices are introduced in details.



**FIGURE 6.** Oscillation waveforms in DPT circuit when input voltage is 250V.

### A. SWITCHING-ON PROCESS

Based on switching stage  $[t_4 \sim t_6]$ , four assumptions are raised as follows: a) the active device has been switched on, regarded as on-resistance  $R_{ds\_on}$ . Its drain and source parasitic inductors are strung into the power loop. b) the input voltage source  $V_{dc}$  and the input side capacitance  $C_{dc}$  are short-circuited. The inductance current is equivalent to the current source and opened. c) when the passive device is switched on by mistake, the channel is opened and there is channel current flowing from the source electrode to the drain electrode. The channel current can be represented by the product of  $v_{gs}$  and  $g_m$ .  $g_m$  is the GaN device's transconductance coefficient. d) the coaxial shunt is strung into the power loop.

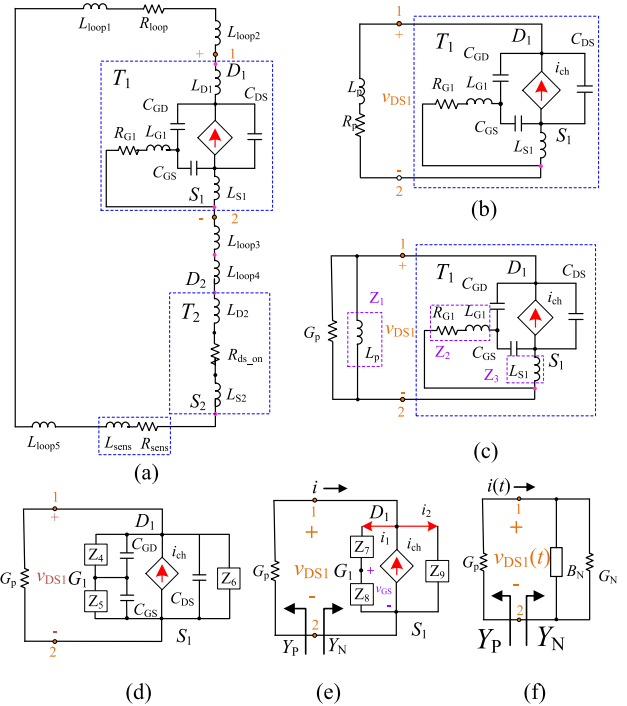
According to the above assumptions, the equivalent circuit Fig. 7(a) is obtained. In this diagram,  $L_{S1}$  is a common source inductor, which exists in both the driving loop and the power loop. Take the passive device as the main research object. Keep other parameters unchanged. String the drain inductor  $L_{D1}$  into the power loop, and get the loop inductance and resistance expressed as:  $L_p = L_{loop1} + L_{loop2} + L_{loop3} + L_{loop4} + L_{loop5} + L_{D1} + L_{D2} + L_{S2} + L_{sens}$ ,  $R_p = R_{ds\_on} + R_{loop} + R_{sens}$ . Fig. 7(a) is simplified to Fig. 7(b). The blue dotted line box represents an active device branch  $T_1$ ;  $R_p$  and  $L_p$  represent passive branches; active and passive branches are connected by ports 1-2. Because the mechanism of  $L_{D1}$  on the oscillation is the same with the inductance outside  $T_1$  and the value of  $L_{D1}$  is small, the equivalence is reasonable and the voltage between the new nodes 1 and 2 is still considered as  $v_{DS1}$ .

Based on Fig.7(b), detailed steps to construct negative conductance model are as follows:

a) change  $R_p$  and  $L_p$  into parallel connection in admittance form. Supposing that  $\omega L_p \gg R_p$ , Fig.7(c) can be obtained. The specific transformation is shown as follows.

$$Y_P = \frac{1}{R_p + j\omega L_p} = \frac{R_p}{R_p^2 + (\omega L_p)^2} - \frac{j\omega L_p}{R_p^2 + (\omega L_p)^2} = \frac{R_p}{R_p^2 + (\omega L_p)^2} + \frac{1}{j\omega L_p} = G_p + \frac{1}{j\omega L_p} \quad (3)$$

b)  $R_{G1}$  has a damping effect on the driving waveform but has no significant effect on the voltage and current oscillation. So  $R_{G1}$  is ignored here. Simplify the circuit by changing



**FIGURE 7.** Circuit diagram simplification during switching-on in the oscillation modeling. (a) Process 1. (b) Process 2. (c) Process 3. (d) Process 4. (e) Process 5. (f) Process 6.

the branches of Y-type joints into  $\Delta$ -type joints, shown as Fig. 7(d). The equivalent transformation formulas are shown as equations (4) and (5).

$$\begin{cases} Z_1 = j\omega L_{G1} \\ Z_2 = j\omega L_{S1} \\ Z_3 = j\omega L_p \\ Z_\Sigma = Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 \end{cases} \quad (4)$$

$$\begin{cases} Z_4 = \frac{Z_\Sigma}{Z_2} = Z_1 + Z_3 + \frac{Z_1 Z_3}{Z_2} \\ Z_5 = \frac{Z_\Sigma}{Z_3} = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3} \\ Z_6 = \frac{Z_\Sigma}{Z_1} = Z_2 + Z_3 + \frac{Z_2 Z_3}{Z_1} \end{cases} \quad (5)$$

c) with the circuit further simplified, Fig.7 (e) can be obtained. The transformation formulas are as follows.

$$\begin{cases} X_1 = \frac{1}{j\omega C_{GD}} \\ X_2 = \frac{1}{j\omega C_{GS}} \\ X_3 = \frac{1}{j\omega C_{DS}} \end{cases}, \quad \begin{cases} Z_7 = \frac{Z_4 \cdot X_1}{Z_4 + X_1} \\ Z_8 = \frac{Z_5 \cdot X_2}{Z_5 + X_2} \\ Z_9 = \frac{Z_6 \cdot X_3}{Z_6 + X_3} \end{cases} \quad (6)$$

Based on Fig. 7 (e), calculate the admittance in the right side of the port 1-2. Its terminal voltage is  $v_{DS1}$  and loop current is  $i$ . When the channel of  $T_1$  is open, part of the inductance current reverse flow in the channel. The channel current is controlled by  $v_{GS1}$ .  $g_{m1}$  represents transconductance coefficient of  $T_1$ . Write Kirchoff's current equation

for the endpoint “D1” as (7).

$$\begin{cases} i_{ch} = g_{m1} \cdot v_{GS1} = g_{m1} \cdot \frac{Z_8}{Z_7 + Z_8} v_{DS1} \\ -i + \frac{v_{DS1}}{Z_7 + Z_8} + \frac{v_{DS1}}{Z_9} - g_{m1} \cdot \frac{Z_8}{Z_7 + Z_8} v_{DS1} = 0 \end{cases} \quad (7)$$

Then, the expression of  $Y_N$  can be obtained as equation (8). Fig.7(f) is the established negative conductance model.

$$\begin{aligned} Y_N &= \frac{i}{v_{DS1}} = \frac{1}{Z_7 + Z_8} + \frac{1}{Z_9} - g_{m1} \cdot \frac{Z_8}{Z_7 + Z_8} \\ &= \frac{Z_9 + Z_7 + Z_8 - g_{m1} \cdot Z_8 Z_9}{(Z_7 + Z_8) \cdot Z_9} \\ &\quad - g_{m1} \cdot \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_A})(\omega C_{DS} - \frac{1}{\omega L_A})} \\ &= \frac{1}{(\omega C_{GD} - \frac{1}{\omega L_{S1}})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} + \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_p})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} \\ &\quad + \frac{j(\frac{1}{(\omega C_{DS} - \frac{1}{\omega L_{G1}})} + \frac{1}{(\omega C_{GD} - \frac{1}{\omega L_{S1}})} + \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_p}})}{(\omega C_{GD} - \frac{1}{\omega L_{S1}})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} + \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_p})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} \end{aligned} \quad (8)$$

where  $L_A = L_p \cdot L_{G1} + L_p \cdot L_{S1} + L_{G1} \cdot L_{S1}$

### B. SWITCHING-OFF PROCESS

Based on switching stage  $[t_9 \sim t_{11}]$ , assumptions of the switching-off process are as follows: a) the active device has been switched off, regarded as output capacitance  $C_{oss}$ . Its drain and source parasitic inductors are strung into the power loop. b) the input voltage source  $V_{dc}$  and the input side capacitance  $C_{dc}$  are short-circuited. The inductance current is equivalent to the current source and opened. c) when the passive device is switched on by mistake, the channel is opened and there is channel current flowing from the source electrode to the drain electrode. The channel current can be represented by the product of  $v_{gs}$  and  $g_m$ .  $g_m$  is the GaN device’s transconductance coefficient. d) the coaxial shunt is strung into the power loop. Based on these, the simplified circuit is shown as Fig.8(a).

Similarly, make the parasitic parameters in the power loop combined into  $L_{p1}$  and  $R_{p1}$ .  $L_{p1} = L_{loop1} + L_{loop2} + L_{loop3} + L_{loop4} + L_{loop5} + L_{D1} + L_{D2} + L_{S2} + L_{sens}$ ;  $R_{p1} = R_{loop} + R_{sens}$ . Then simplify the circuit into Fig.8(b).

In Fig.8(b), the blue dotted line box represents the passive device. Turn the left side of port 1-2 into a paralleled admittance expression. Since  $(\omega L_{p1} - 1/\omega C_{oss}) \gg R_{p1}$ , equivalent circuit Fig.8(c) can be obtained. The detailed transformation formulas are as follows.

$$\begin{aligned} Y_p &= \frac{1}{R_{p1} + j(\omega L_{p1} - 1/\omega C_{oss})} \\ &= \frac{R_{p1}}{R_{p1}^2 + (\omega L_{p1} - 1/\omega C_{oss})^2} + \frac{-j(\omega L_{p1} - 1/\omega C_{oss})}{R_{p1}^2 + (\omega L_{p1} - 1/\omega C_{oss})^2} \end{aligned}$$

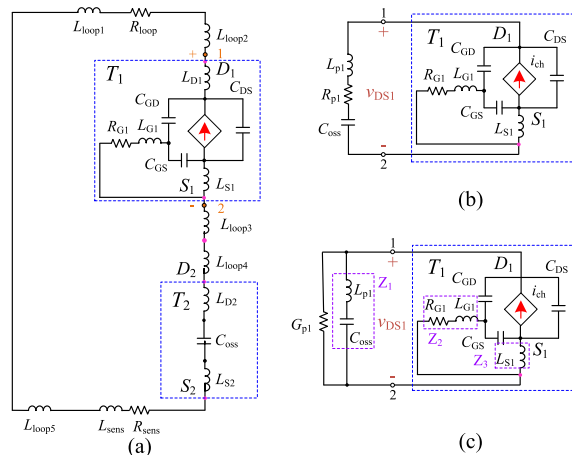


FIGURE 8. Circuit diagram simplification during switching off in the oscillation modeling. (a) Process 1. (b) Process 2. (c) Process 3.

$$\begin{aligned} &= \frac{R_{p1}}{R_{p1}^2 + (\omega L_{p1} - 1/\omega C_{oss})^2} + \frac{1}{j(\omega L_{p1} - 1/\omega C_{oss})} \\ &= G_{p1} + jB_{p1} \end{aligned} \quad (9)$$

Obviously, Fig.8(c) is similar with Fig.7(c). Therefore, further calculations of the circular admittance around port 1-2 are similar. The expression of  $Y_N$  is raised as equation (10).

$$\begin{aligned} Y_N &= -g_{m1} \cdot \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_p})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} \\ &= \frac{1}{(\omega C_{GD} - \frac{1}{\omega L_{S1}})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} + \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_p})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} \\ &\quad + \frac{j(\frac{1}{(\omega C_{DS} - \frac{1}{\omega L_{G1}})} + \frac{1}{(\omega C_{GD} - \frac{1}{\omega L_{S1}})} + \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_p}})}{(\omega C_{GD} - \frac{1}{\omega L_{S1}})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} + \frac{1}{(\omega C_{GS} - \frac{1}{\omega L_p})(\omega C_{DS} - \frac{1}{\omega L_{G1}})} \end{aligned} \quad (10)$$

where  $Z_A = \omega^2 L_{G1} L_{S1} + \omega^2 L_{S1} L_{p1} + \omega^2 L_{G1} L_{p1} - \frac{L_{G1}}{C_{oss}} - \frac{L_{S1}}{C_{oss}}$ .

### IV. THEORETICAL ANALYSIS AND EXPERIMENT

In this section, the negative conductance model and stability criteria are put into used in a DPT circuit with Cascode GaN devices TPH3205WS. The accuracy of the above analysis is verified by the comparison of theoretical calculation and experimental results.

Regard Fig.7(f) as the negative conductance model, stability of the GaN based circuit can be analyzed by the negative resistance theory. Firstly, the oscillation frequency  $f_0$  of the circuit can be obtained by solving  $B_{loop} = B_p + B_N = 0$ . Secondly, take  $f_0$  into the loop conductance  $G_{loop} = (G_p + G_N)$  to analyze the polarity of the loop conductors. If  $G_{loop}$  is less than 0, the divergence oscillation will occur. If  $G_{loop}$  is equal to 0, equal amplitude oscillation will occur. If  $G_{loop}$  of loop conductance is greater than 0, oscillation will be self-extinguished.

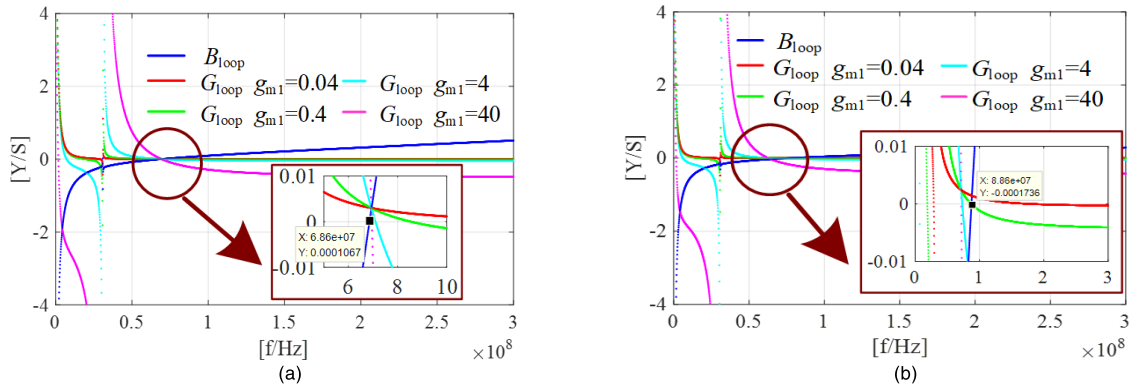


FIGURE 9. Loop admittance curves of TPH3205WS with different input voltage during switching-on process. (a)  $V_{in} = 100V$ . (b)  $V_{in} = 250V$ .

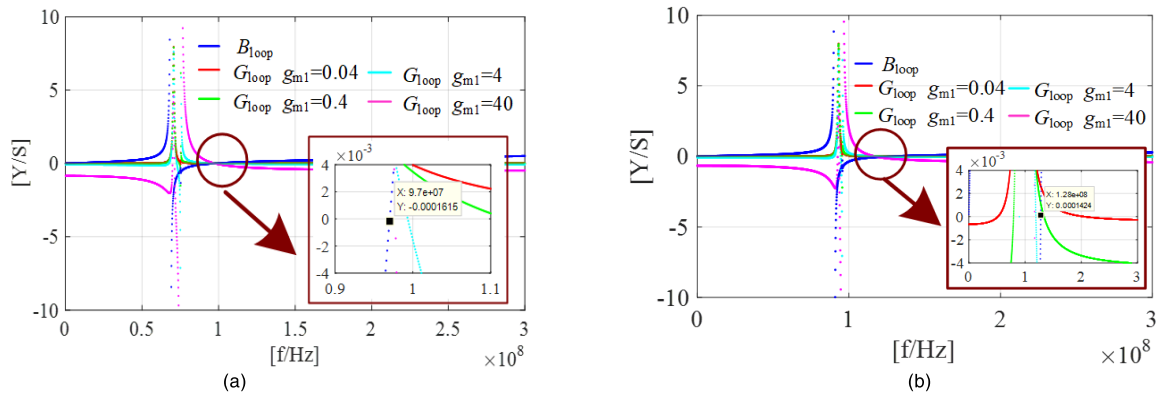


FIGURE 10. Loop admittance curves of TPH3205WS with different input voltage during switching-off process. (a)  $V_{in} = 100V$ . (b)  $V_{in} = 250V$ .

$g_{m1}$  in formula (8) and (10) is the cross-guide coefficient, which represents the slope of the transfer characteristic curve, as shown in formula (11). The opening degree of passive device can be represented by  $g_{m1}$ . For the convenience of analysis, make  $g_{m1}$  as 0.004-40, where the peak voltage of the passive device is below 5V.

$$g_{m1} = \frac{\Delta i_{D1}}{\Delta v_{GS1}} \quad (11)$$

Table 1 is the model parameter values of TPH3205WS-based circuit, in which the parasitic inductance parameters are extracted by Q3D software.

TABLE 1. Model parameter values of TPH3205WS.

Parameter	Value	Parameter	Value
$L_{G1}$	10.7nH	$L_p$	17.7nH
$L_{S1}$	1.19nH	$R_p$	0.177Ω
$g_{m1}$	0.04~40S	/	/

Table 2 shows the capacitance value of TPH3205WS at different voltage levels. Though the voltage on the device is changing continuously, the capacitance value changes little

when the  $v_{DS}$  is higher than 50V. So the capacitance values are considered constant during the switching process.

TABLE 2. Capacitance values of TPH3205WS with different input voltages.

Voltage Capacitor	50V	100V	200V	250V	300V	400V
$C_{oss}$ (pF)	430	287	215	165	150	137
$C_{GD}$ (pF)	29.4	28.1	25.8	24.7	23.9	23.2
$C_{GS}$ (pF)	2205.6	2206.9	2209.2	2210.3	2211.1	2211.8
$C_{DS}$ (pF)	400.6	258.9	189.2	140.3	126.1	113.8

Substitute the data in the above tables into the loop admittance equations of GaN device during the switching process. Larger  $v_{GS1}$  leads to greater channel conduction and  $g_{m1}$  will also be larger. The circuit stability is analyzed by comparing the circuit conductance polarity under different  $g_{m1}$  values at the same voltage level. Fig.9 shows the loop admittance curve of TPH3205WS under 100V and 250V during the switching on process, and Fig.10 shows the loop admittance curve of TPH3205WS under 100V and 250V during the switching off process.

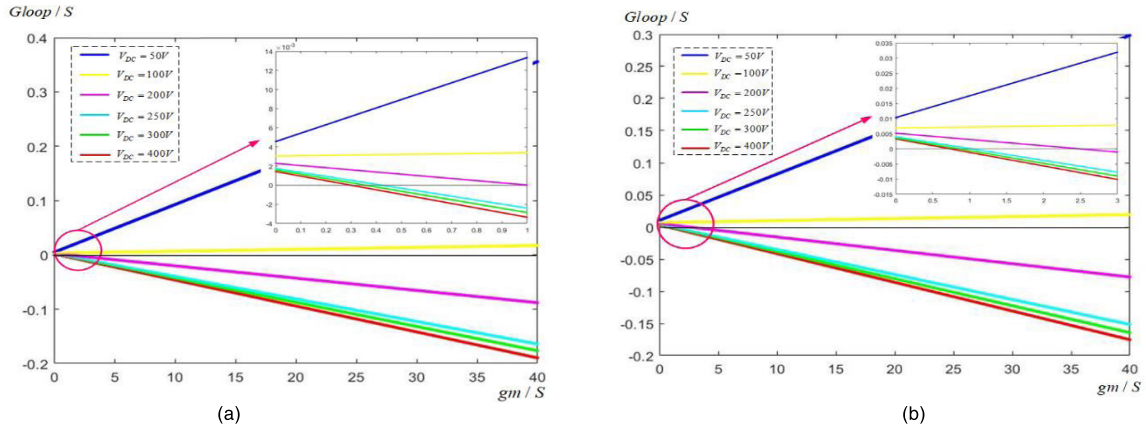


FIGURE 11. The relationship between  $G_{loop}$  and  $g_m$  under different voltages. (a) Switching-on process; (b) Switching-off process.

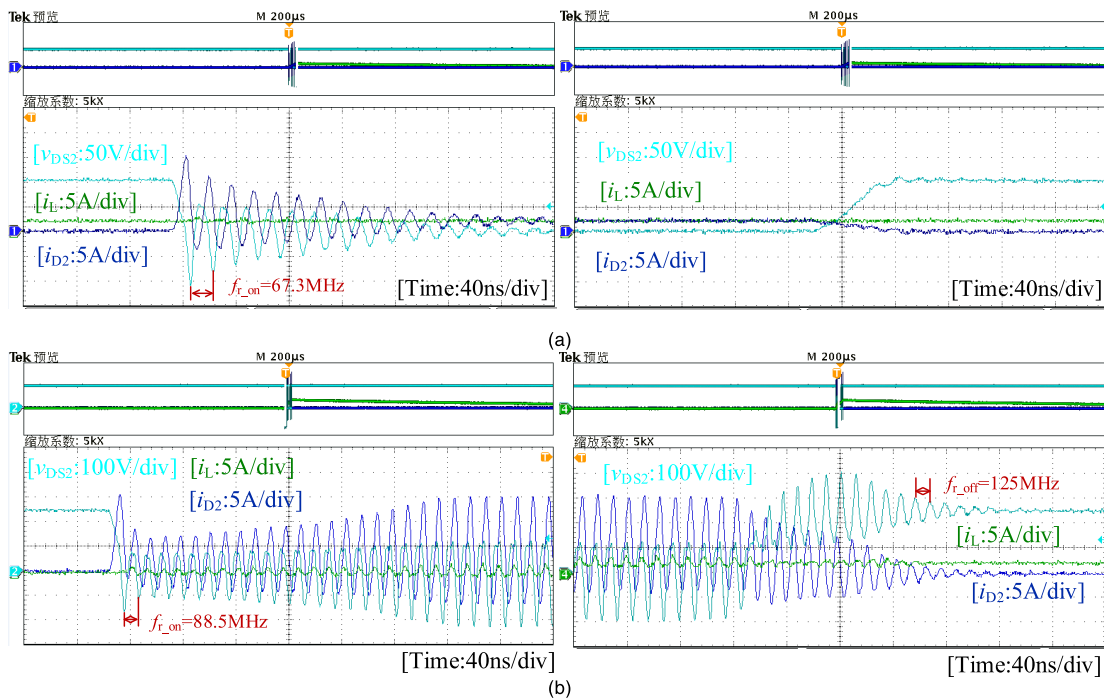


FIGURE 12. Experimental waveforms of GaN devices (TPH3205WS) in the DPT circuit. (a) Switching-on at  $V_{in} = 100V$ . (b) Switching-off at  $V_{in} = 100V$ . (c) Switching-on at  $V_{in} = 250V$ . (d) Switching-off at  $V_{in} = 250V$ .

In Fig.9 and Fig.10, the oscillation frequency under different  $V_{in}$  is showed by the intersection of  $B_{loop}$  and  $Y = 0$ . According to the above simulation waveforms, under 100V, there is  $G_{loop} > 0$  regardless of the value of  $g_{m1}$ . So the GaN based circuit won't have divergent oscillation even though the passive device is switched on mistakenly. Under 250V, when  $g_{m1} = 0.04$ ,  $G_{loop} > 0$  and the circuit won't have divergent oscillation. But when  $g_{m1} = 4 \sim 40$ , there is  $G_{loop} < 0$  and divergent oscillation will happen.

Fig.11 summarizes the relationship curves between  $G_{loop}$  and  $g_m$  under different voltage levels. The curves in Fig. 11(a) and Fig.11(b) are calculated by the established negative conductance models in switching-on and switching-off process respectively. The law of the influence of voltage change on the stability of GaN-based circuit can be showed here. With

a certain oscillation frequency  $\omega$  (calculated by  $B_{loop} = 0$ ),  $G_{loop}$  has a linear relationship with  $g_m$ . At low voltages ( $V_{DC} = 50/100V$ ), there is no positive  $g_m$  value which makes  $G_{loop}$  equal to 0. So the GaN based circuit won't have sustained oscillation. As the voltage increases, the  $g_m$  value which makes  $G_{loop}$  equal to 0 is decreased.  $g_m$  represents the degree of device activation, which is determined by  $v_{gs}$ . Around the gate threshold voltage ( $V_{th}$ ), higher  $v_{gs}$  leads to larger  $g_m$ . Therefore, for the passive devices, if small  $g_m$  can make  $G_{loop}$  equal to or even less than 0, small disturbance of  $v_{gs}$  will cause constant amplitude or divergent oscillations. So, the higher the voltage is, the more likely the circuit will continue to oscillate and the more unstable the circuit will be.

Fig.12 shows the switching waveforms of the active device under 100V and 250V, representing the low and medium



voltage conditions respectively. According to the waveforms, it can be seen that: under 100V, the switching process has self-extinguished oscillations; under 250V, the switching on process has high frequency continuous oscillation but the switching off process has self-extinguished oscillations. Besides, the oscillation frequency of the switching on process under 100V is 67.3MHz. The oscillation frequency of the switching on process under 250V is 88.5MHz while that of switching off process is 125MHz. The experiment results are corresponding with theoretical analysis and verify the accuracy and validity of the negative conductance model.

### V. OSCILLATION SUPPRESSION METHOD

In this part, a passive suppression method of adding a ferrite bead in power loop is introduced based on the established negative conductance model. This method works by increasing  $G_P$  (conductance of the passive devices in circuit) when oscillation occurs. According to the stability analysis, with the increased  $G_P$ , the loop conductance  $G_{loop}$  will be higher at the oscillation frequency, leading to reduced possibility of continuous oscillation and increased stability margin. Suppression effect of this method is verified by theoretical calculation and experiments. Besides, how to select the appropriate ferrite bead is shown in details.

Fig. 13 shows the position of the added ferrite bead in negative conductance model. Under normal working conditions, the impedance value of ferrite bead is very small. But if the oscillation occurs, the ferrite bead will provide a large impedance, which works like a damper to make the oscillation attenuate quickly. When the frequency is between 50MHz and 150MHz (the oscillation frequency range of TPH3205WS obtained in part IV), most ferrite beads have an inductive reactance besides a resistance. Therefore, a series of variable resistance and inductance is taken used to represent the ferrite bead in this paper. Equation (12) shows the impedance value of ferrite bead. With the ferrite bead added, the passive devices' conductance  $G_P$  is changed into  $G'_p$ , expressed by equation (13).

$$Z_{bead} = \sqrt{R_{bead}^2 + (\omega L_{bead})^2} \quad (12)$$

$$G'_p = \frac{(R_p + R_{bead})}{(R_p + R_{bead})^2 + (\omega(L_p + L_{bead}))^2} \quad (13)$$

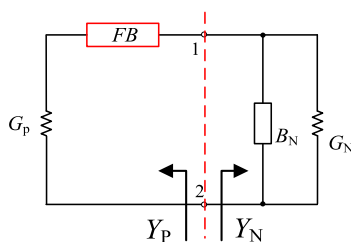


FIGURE 13. Schematic diagram of adding the ferrite bead.

When selecting the ferrite bead, two basic requirements should be satisfied first: a) the DC current through the ferrite

bead should be lower than its rated value; b) it's better to select the type with lower DC impedance value to avoid extra power loss. Then, suppose  $\omega$  unchanged and calculate the  $R_{bead}$  and  $L_{bead}$  that maximize  $G'_p$  at this oscillation frequency. Obviously,  $G'_p$  increases as  $L_{bead}$  decreases. So make  $L_{bead}$  equal to 0 in equation (13) and derive  $G'_p$  with respect to  $R_{bead}$ , shown as equation (14). When the derivative is 0,  $R_{bead}$  is expressed as equation (15). With the calculated optimal values, the range of impedance parameters that the ferrite bead should have at the oscillation frequency can be roughly determined. Finally, select the type that makes  $G'_p$  closest to the maximum value among the ferrite beads available in the market.

$$\frac{dG'_p}{dR_{bead}} = \frac{(\omega L_p)^2 - (R_p + R_{bead})^2}{((R_p + R_{bead})^2 + (\omega L_p)^2)^2} \quad (14)$$

$$R_{bead} = \omega L_p - R_p \quad (15)$$

Since the DC current values which the ferrite beads in the market can withstand are generally not large, this method is actually applicable to low DC current state. Therefore, to be verified, this method is applied to a low-power synchronous Boost converter shown as Fig.14. Both the output voltage and load are according to the application requirements. The converter contains output current and voltage sampling. But in order to eliminate the influence of the feedback system oscillation, experiments in this part are carried out under the open-loop condition. The switching condition difference between DCM and CCM is the current value when the device is switched on. According to Part II and III, the oscillation analysis method and the negative conductance modeling for DCM are similar with CCM. Therefore, only the

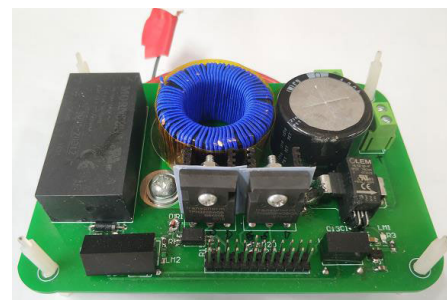


FIGURE 14. Synchronous Boost converter based on TPH3205WS.

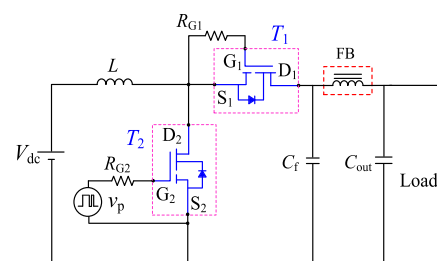


FIGURE 15. Simplify circuit of synchronous Boost converter with a ferrite bead.

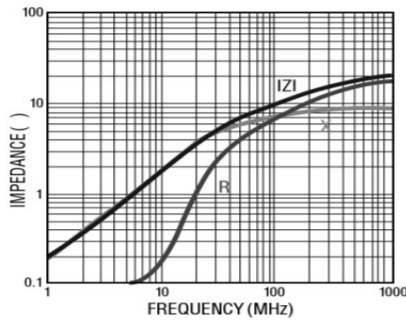


FIGURE 16. Electrical specification of MH2029-100Y.

calculation and experiment in CCM are introduced here. During the open-loop experiment, sustained oscillation happens in switching-on process when the switching voltage increases to 150V. Extracting the loop parasitic parameters with Q3D,  $L_{G1}$  is equal to 12.18nH,  $L_P$  is equal to 33.78nH,  $R_P$  is equal to 0.39Ω.  $C_{GD}$ ,  $C_{GS}$  and  $C_{DS}$  can be obtained by the capacitance-voltage curve. Fig.17(a) shows the loop admittances under 150V obtained by equation (3) and (8) and the calculated oscillation frequency is 57.5MHz. To suppress the sustained oscillation, ferrite bead MH2029-100Y is selected according to the above selection method and the

added position is shown as Fig.15. When selecting the ferrite bead, firstly, according to the converter design, the maximum DC current that the ferrite bead will flow through is 2.2A. Therefore, the types with rated current values less than 2.2A are excluded. Then, substitute the circuit parameters of the synchronous Boost converter into formula (14) and (15). It can be calculated that the ideal values of  $R_{bead}$  and  $L_{bead}$  which maximize  $G'_p$  are 11.8Ω and 0nH around oscillation frequency 57.5MHz. Therefore, the parameter range of the ferrite bead can be roughly determined according to the ideal values. Substitute the values of the eligible ferrite beads in the range into formula (13). Considering that MH2029-100Y can make  $G'_p$  closet to maximum and has lower DC impedance which lead to lower additional power loss, MH2029-100Y is chosen in this paper. The electrical specification of MH2029-100Y is shown as Fig.16. With the added ferrite bead, it's can be seen from Fig.17(b) that the conductance polarity with similar  $g_{m1} = 0.4$  at  $f_{on} = 57.5$ MHz changes from negative value into the positive value, making sustained oscillations probability decreased. Fig.18 shows the inductance current  $i_L$  and  $v_{DS2}$  in experiment. The oscillation frequency is basically consistent with the calculated result. And the sustained oscillation is indeed suppressed into self-extinguishing by this method.

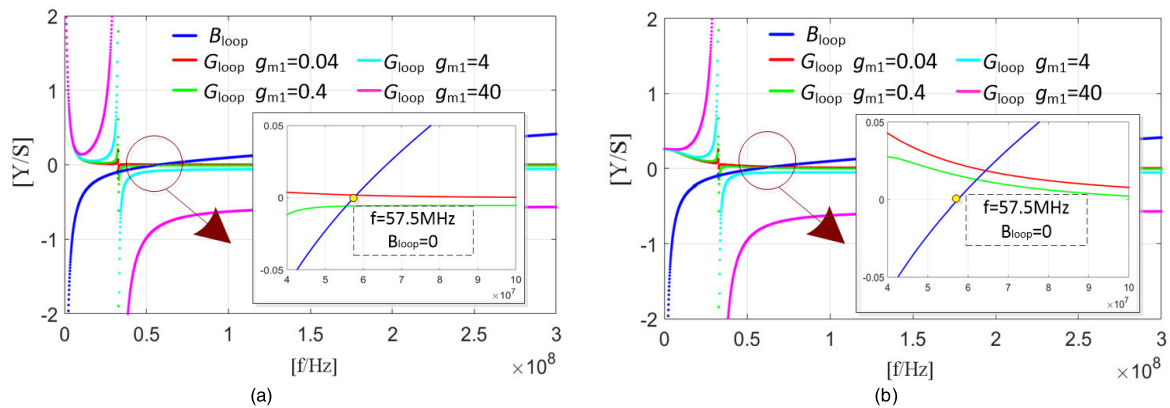


FIGURE 17. Loop admittance curves with 150V voltage stress. (a) Without ferrite bead. (b) With a ferrite bead.

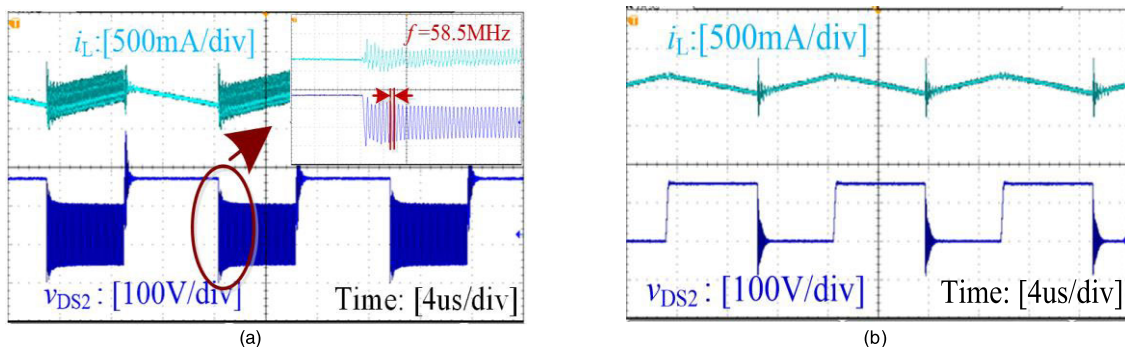


FIGURE 18. Experimental waveforms of TPH3205 in the synchronous Boost converter. (a) Without ferrite bead. (b) With a ferrite bead.

## VI. CONCLUSION

Based on Cascode GaN devices, switching oscillation problems and circuit stability have been studied in this paper. High operating frequency of GaN devices leads to large  $dv/dt$  and  $di/dt$  during switching process. With the influence of parasitic parameters in the circuit, oscillation will happen easily. In order to judge oscillation conditions, negative resistance oscillator theory is used to establish an oscillation model and stability criteria are put forward. Modeling process is based on oscillation mechanism analysis, considering the interaction of two devices in one bridge arm and all the parasitic parameters. The established model can reflect the influence of  $g_m$ ,  $v_{ds}$  and parasitic loop parameters on the circuit stability well. Besides, according to the model and stability analysis, a ferrite bead is chosen to be connected into the power loop to suppress oscillation. The suppression mechanism and selection method of the ferrite bead are introduced quantitatively. All the theoretical analyses have been verified by calculations and experimental results. The oscillation model and stability criteria can accurately predict whether there will be oscillations in the circuit and how the oscillations will last. The selected ferrite bead is proved to be effective in an actual Cascode GaN-based converter. What's more, the developed methodology can be extended to a wider range of applications because the key steps and considerations in the modeling process are similar. And the calculation in ferrite bead selection can also be considered as a design idea of optimal suppressor, which can break through the selecting limitations of ferrite bead. All these achievements can help the applicator to avoid the oscillation phenomenon of the converter at the level of circuit design.

## REFERENCES

- [1] E. A. Jones, F. Wang, and B. Ozpineci, "Application-based review of GaN HFETs," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Oct. 2014, pp. 24–29.
- [2] *Application Note*. Accessed: Oct. 31, 2019. [Online]. Available: <http://www.transphormusa.com/>
- [3] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.
- [4] T. J. Flack, B. N. Pushpakaran, and S. B. Bayne, "GaN technology for power electronic applications: A review," *J. Electron. Mater.*, vol. 45, no. 6, pp. 2673–2682, Mar. 2016.
- [5] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.
- [6] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency Gallium-Nitride-Based point of load converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2008–2015, Apr. 2014.
- [7] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.
- [8] X. Huang, Z. Liu, F. C. Lee, and Q. Li, "Characterization and enhancement of high-voltage cascode GaN devices," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 270–277, Feb. 2015.
- [9] F. Zhao, Y. Li, Q. Tang, and L. Wang, "Analysis of oscillation in bridge structure based on GaN devices and ferrite bead suppression method," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Oct. 2017, pp. 391–398.
- [10] N. Galanos, J. Popovic, J. A. Ferreira, and M. Gerber, "Influence of the magnetic's parasitic capacitance in the switching of high-voltage cascode GaN HEMT," in *Proc. 9th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2016, pp. 1–6.
- [11] N. Hari, T. Logan, and R. McMahon, "Design considerations for 600 V GaN cascode based half-bridge converter systems for utility based applications," in *Proc. 8th IET Int. Conf. Power Electron., Mach. Drives (PEMD)*, Apr. 2016, pp. 1–6.
- [12] A. J. Sellers, C. Tine, R. L. Kini, M. R. Hontz, R. Khanna, A. N. Lemmon, A. Shahabi, and C. New, "Effects of parasitic inductance on performance of 600-V GaN devices," in *Proc. IEEE Electric Ship Technol. Symp. (ESTS)*, Aug. 2017, pp. 50–55.
- [13] S. Ishiwaki, T. Iwaki, Y. Sugihara, K. Nanamori, and M. Yamamoto, "Analysis of false turn-on phenomenon of GaN HEMT with parasitic inductances for propose novel design method focusing on peak gate voltage," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Oct. 2017, pp. 1395–1401.
- [14] X. Huang, W. Du, F. C. Lee, Q. Li, and W. Zhang, "Avoiding divergent oscillation of a cascode GaN device under high-current turn-off condition," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 593–601, Jan. 2017.
- [15] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014.
- [16] Z. Zhang, B. Guo, and F. Wang, "Evaluation of switching loss contributed by parasitic ringing for fast switching wide band-gap devices," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9082–9094, Sep. 2019.
- [17] J. Chen, Q. Luo, J. Huang, Q. He, and X. Du, "A complete switching analytical model of low-voltage eGaN HEMTs and its application in loss analysis," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1615–1625, Feb. 2020.
- [18] T. Liu, Y. Zhou, Y. Feng, T. T. Y. Wong, and Z. John Shen, "Experimental and modeling comparison of different damping techniques to suppress switching oscillations of SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 7024–7031.
- [19] P. Pan, W. Chen, L. Shu, H. Mu, K. Zhang, M. Zhu, and F. Deng, "An impedance-based stability assessment methodology for DC distribution power system with multivoltage levels," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4033–4047, Apr. 2020.
- [20] K. Wang, X. Yang, L. Wang, and P. Jain, "Instability analysis and oscillation suppression of enhancement-mode GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1585–1596, Feb. 2018.
- [21] J. Chen, Q. Luo, J. Huang, Q. He, P. Sun, and X. Du, "Analysis and design of an RC snubber circuit to suppress false triggering oscillation for GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2690–2704, Mar. 2020.
- [22] T. Zhu, F. Zhuo, F. Zhao, F. Wang, and T. Zhao, "Quantitative model-based false turn-on evaluation and suppression for cascode GaN devices in half-bridge applications," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10166–10179, Oct. 2019.
- [23] R. Matsumoto, K. Umetani, and E. Hiraki, "Optimization of the balance between the gate-drain capacitance and the common source inductance for preventing the oscillatory false triggering of fast switching GaN-FETs," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Cincinnati, OH, USA, Oct. 2017, pp. 405–412.
- [24] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half-bridge circuits switched with wide band-gap transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2380–2392, May 2014.
- [25] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability considerations for silicon carbide field-effect transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4453–4459, Oct. 2013.
- [26] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017.
- [27] A. B. Jorgensen, S. Beczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jorgensen, and S. Munk-Nielsen, "A fast-switching integrated full-bridge power module based on GaN eHEMT devices," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2494–2504, Mar. 2019.
- [28] X. Zhao, C.-W. Chen, J.-S. Lai, and O. Yu, "Circuit design considerations for reducing parasitic effects on GaN-based 1-MHz high-power-density high-step-up/down isolated resonant converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 695–705, Jun. 2019.

[29] W. Zhang, X. Huang, Z. Liu, F. C. Lee, S. She, W. Du, and Q. Li, "A new package of high-voltage cascode gallium nitride device for megahertz operation," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1344–1353, Feb. 2016.

[30] Z. Xu, W. Zhang, F. Xu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Investigation of 600 V GaN HEMTs for high efficiency and high temperature applications," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Fort Worth, TX, USA, Mar. 2014, pp. 131–136.

[31] X. Zhang, Z. Shen, N. Haryani, D. Boroyevich, and R. Burgos, "Ultra-low inductance vertical phase leg design with EMI noise propagation control for enhancement mode GaN transistors," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Long Beach, CA, USA, Mar. 2016, pp. 1561–1568.

[32] A. Lidow, J. Strydom, M. de Rooij, and Y. Ma, *GaN Transistors for Efficient Power Conversion*, 1st ed. El Segundo, CA, USA: Power Conversion, 2012.

[33] K. Yatsugi, K. Nomura, and Y. Hattori, "Analytical technique for designing an RC snubber circuit for ringing suppression in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4736–4745, Jun. 2018.

[34] Z. Wang, Y. Wu, and J. Honea, "Switching circuits having ferrite beads," U.S. Patent 0222 640 A1, Transphorm Inc., Apr. 3, 2017.

[35] G. Gonzalez, *Foundations of Oscillator Circuit Design*. Norwood, MA, USA: Artech House, 2007.



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