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A 17.6-nW 35.7-ppm/°C Temperature Coefficient All-SVT-MOSFET Subthreshold Voltage Reference in Standard 0.18-μm N-Well CMOS

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ABSTRACT This paper presents a low-power, low-voltage, and low-temperature-coefficient (TC) MOSFET-only subthreshold voltage reference circuit based on a standard 0.18-μm n-well CMOS process. The circuit consists of two novel current generators and an I/V conversion circuit with temperature compensation. Under the control of a proposed pMOS-bulk-driven (PBD) temperature compensation circuit, two pMOSFETs operating in a linear region act as resistors with different TCs and can be used for PTAT and CTAT current generation. Owing to the PBD technique and the subthreshold operating method, these two current generators and the I/V conversion circuit can operate at low voltage. The proposed reference circuit is realized with only standard V_{TH} (SVT) MOS devices. The measurement results show that it can operate at a minimum supply voltage of 0.5 V. The line sensitivity is 0.09% for supply voltages between 0.5 and 1.8 V. The PSRR measured at 100 Hz is 51.8 dB. A measurement of 20 samples indicates that the average TC is 35.7 ppm/°C across a temperature range of −40 to 85 °C. The proposed circuit consumes 17.6 nW from a 0.5-V power supply and occupies an active area of 0.0092 mm^2.

INDEX TERMS pMOS-bulk-driven, temperature compensation, line regulation, subthreshold, nanowatt, voltage reference.

I. INTRODUCTION

In the future, billions of smart devices with sensing and processing capabilities will be connected to the Internet with the continuous development of Internet of Things (IoT). Devices with the above-described functions are called IoT nodes and will preferably be energy efficient, miniaturized, have a long life cycle, and be low cost [1]–[3]. In this scenario, low voltage digital-assisted system-on-chips (SoCs) with MOSFETs operating in the subthreshold region are very attractive. These benefit from a low supply voltage, and the power consumption can be reduced for digital circuits. However, the situation is not the same in analog circuit design. Analog circuits with a lower supply voltage may consume much more power and chip area to achieve competitive noise performance and linearity. More-over, MOS transistors biased in the subthreshold region are more sensitive to variations in the process, voltage, and temperature (PVT) [4]. Therefore, it is challenging but urgently needed to develop suitable techniques for low-supply analog circuits.

As one of the key analog circuits, the voltage reference generator is widely used in various applications to generate a DC voltage that is insensitive to PVT variations. Conven-tional bandgap references (BGRs) require relatively high supply voltages (> V_{BE}+ V_{DS}) and consume significant power (at the μW level) [5], [6], where V_{BE} is the base-emitter voltage of the parasitic vertical bipolar junction transistor (BJT), and V_{DS} is the drain-source saturation voltage of a MOSFET. This cannot satisfy the requirement of low-voltage applications. Moreover, a survey of the literature reveals that resistor compensation schemes are typically utilized to realize low-temperature-coefficient (TC) voltage references (VRs) [6]–[11]. However, the usage of resistors can increase the chip area, cost, and noise coupled from the substrate [12]. From the research on the temperature characteristics of MOSFETs in [13], it was found that the gate-source voltage of a MOSFET with a fixed drain current bias can decrease with temperature.

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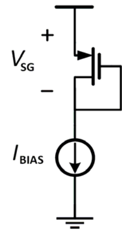

FIGURE 1. Diode-connected p-channel MOSFET.

Several prior works reduced the supply voltage by using V_{GS} of a diode-connected MOSFET to replace the high V_{BE} of a BJT. A MOSFET-only subthreshold VR with no amplifiers was presented in [14]. It can operate with a minimum supply voltage of 0.45 V and achieves superior line sensitivity by using a special twin-well CMOS process. The subthreshold VR circuit in [15] can operate with a 0.25-V supply voltage. Owing to the usage of an additional low-voltage comparator and charge-pump circuit, the circuit consumes considerable power. The structure in [16] with stacked pMOS transistors reduces the quiescent current of the circuit but does not leave enough headroom for a supply voltage reduction. To achieve low power, small area, and low supply, the two-transistor VR in [17] avoids amplifiers, saturated devices, and resistors, but has both a native device and thick oxide device. This needs trimming to address the process sensitivity of the TC and output voltage. The subthreshold VRs presented in [18] and [19] use switched-capacitor circuits for quiescent current reduc-tion. However, the operating temperature range is restricted owing to the leakage current of the switches [20].

This paper presents a novel all-MOSFET VR generator realized in standard 0.18-μm n-well CMOS. It incorporates both the pMOS-bulk-driven (PBD) temperature compensation technique and the subthreshold operating method, leveraging each other's strength to achieve low TC and low power under a low supply. Two current sources with opposite TCs are generated by controlling the bulk of the pMOS transistor with different temperature compensation circuits. A low-TC output voltage is finally obtained after an I/V conversion with further temperature compensation. Different from [14], the proposed VR with PBD technique does not require any bulk-driven nMOS transistors and can be realized in a standard n-well CMOS process. This paper begins by describing the detailed circuit design of the proposed VR generator in Section II. Design considerations are provided in Section III. Measured results are summar-ized and compared with those of previous works in Section IV. Finally, conclusions are given in Section V.

II. CIRCUIT ARCHITECTURE

Fig. 1 shows the operation of a pMOS transistor in a weak inversion region. The model assumes that 1) the channel in the MOSFET is so long that the horizontal and vertical electric fields are approximately independent and the channel-length modulation effect is negligible, and 2) the source-drain voltage of the pMOSFET is sufficiently higher than the thermal voltage at room temperature. Under these requirements, the I-V characteristic of a pMOS transistor operating in a weak inversion region can be described as [21]

$$I_D = KI_0 \exp\left(\frac{|V_{GS}| - |V_{THP}|}{\eta V_T}\right) \times \left[1 - \exp\left(-\frac{|V_{DS}|}{V_T}\right)\right] \tag{1}$$

$$I_0 = \mu_p C_{OX} (\eta - 1) V_T^2 \tag{2}$$

For $|V_{DS}| > 0.1$ V, the drain current I_D is almost indepen-dent from $|V_{DS}|$ and can be approximately given by [9]

$$I_D = KI_0 \exp\left(\frac{|V_{GS}| - |V_{THP}|}{\eta V_T}\right) \tag{3}$$

where I_0 is called the pre-exponential factor, K is the aspect ratio (W/L) of the pMOSFET, μ_p is the carrier mobility, C_{OX} is the gate-oxide capacitance per area, $V_T(= kT/q)$ is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and V_{THP} is the threshold voltage of a pMOSFET. η is the subthreshold slope factor.

From (3), the gate-source voltage of the MOSFET for a given drain current can be described as

$$|V_{GS}| = \eta V_T \ln \frac{I_D}{KI_0} + |V_{THP}| \tag{4}$$

In this equation, the threshold voltage of the MOSFET can be described as [22]

$$|V_{THP}| = -\frac{kT}{q} \ln \frac{P_{D,\,poly}}{N_A} + \frac{2\sqrt{kTN_A\varepsilon_{si} \ln \frac{N_A}{n_i}} - Q'_{SS}}{C_{OX}} \tag{5}$$

where $P_{D,poly}$ is the doping concentration of acceptor atoms in the P+ poly gate, and N_A is the doping concentration of acceptor atoms in the substrate. n_i are the intrinsic carriers, ε_{si} is the relative dielectric constant of silicon, and Q'_{SS} stands for the constant of the surface-state charge.

As described in [23], we can substitute (5) in (4) and take the derivative of $|V_{GS}|$ with respect to T. The TC of $|V_{GS}|$ can be approximately written as

$$\begin{aligned}\frac{\partial |V_{GS}|}{\partial T} &\approx \eta \frac{k}{q} \ln \frac{I_D}{KI_0} - \frac{k}{q} \ln \frac{P_{D,\,poly}}{N_A} \\ &= -\frac{k}{q} \ln \frac{P_{D,\,poly}(KI_0)^\eta}{N_A(I_D)^\eta}\end{aligned} \tag{6}$$

which indicates that $|V_{GS}|$ decreases with an increase in temperature. In general, $P_{D,poly}$ is much greater than N_A.

Fig. 2 shows the simulated variation of $V_{SG,\,M1}$ vs. temperature at different bias currents. When the drain current is at a nanoampere level, the change rate of V_{SG} with temperature is almost invariable if the drain current experiences a slight change. Therefore, two currents at the nanoampere level that are proportional-to-absolute temperature (PTAT) and complementary-to-absolute temperature (CTAT), respectively, are generated with the temperature performance of the resistance of the pMOSFET controlled by the bulk-driven technique.

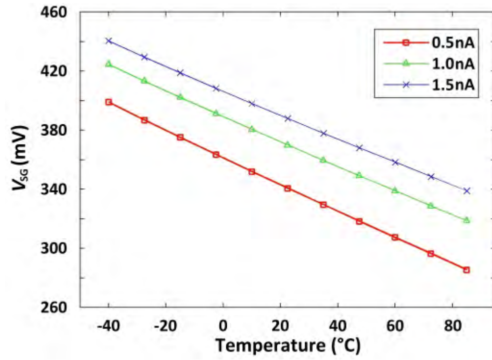

FIGURE 2. Simulation results of variation in $V_{SG,M1}$ with temperature at different bias currents.

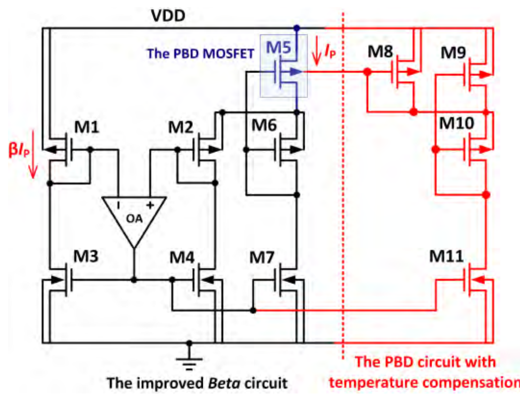

FIGURE 3. Proposed PTAT current generator.

A. PTAT CURRENT GENERATOR

The *Beta* multiplier is a simple bias-current generator [14], [22]. It can achieve relatively good line sensitivity under a standard supply voltage. However, its temperature coeffi-cient is insufficient. The line sensitivity can also deteriorate under low supply voltages because the generated current by the MOSFET in the subthreshold region varies with its V_{DS}. Fig. 3 shows the proposed PTAT current generator. We use a self-cascode pMOS transistor to replace the resistor in the *Beta* circuit. According to [24], it can achieve small area and is appropriate for low voltage design. A PBD circuit with temperature compensation is proposed as shown in Fig. 3. It can bias the bulk of M5 for threshold voltage reduction. Moreover, the thermal slope of the PTAT drain current of M5 can also be easily adjusted by this circuit.

In Fig.3, the resistance of M5 in linear region can be expressed as [14]

$$R_{M5} = \frac{1}{\mu_P C_{OX} K_5 \left(\left|V_{GS,\,M5}\right| - \left|V_{TH,\,M5}\right|\right)} \tag{7}$$

where V_{GS} is the gate-source voltage. The drain current of M5 can be written as

$$I_P = \mu_p C_{OX} K_5 (V_{SG,\,M5} - \left|V_{TH,\,M5}\right|) V_{SD,\,M5} \tag{8}$$

The threshold voltage V_{TH} is an important parameter that is sensitive to temperature variations. It increases as the temperature decreases owing to Fermi-level and bandgap energy shifts. V_{TH} has a linear relationship with the temperature over a wide range of temperatures for long-channel devices. According to [25], if we take body effect into consideration, the expression of V_{TH} can be given by

$$\begin{aligned} V_{TH} &= V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right) \\ &\approx V_{TH0} + (\eta - 1)\, V_{SB} \end{aligned} \tag{9}$$

where V_{TH0} is the threshold voltage without the body effect, γ is the body-effect constant, and V_{SB} is the source-bulk voltage of a MOSFET. Therefore, we have

$$\left|V_{TH,\,M5}\right| \approx \left|V_{TH0,\,M5}\right| + (\eta - 1) V_{BS,\,M5} \tag{10}$$

In Fig. 3, $V_{SB,M5}$ can be expressed as

$$V_{BS,\,M5} = V_{SG,\,M10} - V_{SG,\,M9} \tag{11}$$
$$V_{SG,\,M5} = V_{SG,M1} - V_{SG,\,M2} + V_{SG,\,M6} \tag{12}$$
$$V_{SD,M5} = V_{SG,M1} - V_{SG,M2} \tag{13}$$

From (5) and (9), regardless of the V_{SB}, we have

$$V_{TH} = V_{TH0} \tag{14}$$
$$\frac{\partial\left|V_{TH0}\right|}{\partial T} \approx -\frac{k}{q}\ln\frac{P_{D,\,poly}}{N_A} \tag{15}$$

To determine the current variation of M5 with temperature, we differentiate (8) with respect to T and obtain

$$\begin{aligned} \frac{\partial I_P}{\partial T} = C_{OX} K_5 \Bigg[&\underbrace{a_1 \mu_p V_{SD,\,M5}}_{x_1} + \underbrace{b_1 \mu_p \left(V_{SG,\,M5} - \left|V_{TH,\,M5}\right|\right)}_{y_1} \\ &+ \underbrace{c_1\left(V_{SG,\,M5} - \left|V_{TH,\,M5}\right|\right) V_{SD,\,M5}}_{z_1} \Bigg] \end{aligned} \tag{16}$$

To generate a current with a positive TC, $[x_1 + y_1 + z_1]$ in (16) is expected to be greater than zero. It can be observed that the thermal slope of I_P is a function of parameters that are marked using a_1, b_1, and c_1. From (4), (8), and (9), we can express a_1 and b_1, respectively, as bellow.

$$\begin{aligned} a_1 &= \frac{d\left(V_{SG,\,M5} - \left|V_{TH,\,M5}\right|\right)}{dT} \\ &\approx \frac{\partial\left(V_{SG,M1} - V_{SG,\,M2}\right)}{\partial T} + \frac{\partial V_{SG,\,M6}}{\partial T} \\ &\quad - \frac{\partial\left[\left|V_{TH0,\,M5}\right| + (\eta - 1)\left(V_{SG,\,M10} - V_{SG,\,M9}\right)\right]}{\partial T} \\ &\approx \eta\frac{k}{q}\ln\left(\frac{K_1}{K_2}\right) - \frac{k}{q}\ln\frac{P_{D,\,poly}(K_6 I_0)^\eta}{N_A (I_{D6})^\eta} \\ &\quad + \frac{k}{q}\ln\frac{P_{D,\,poly}}{N_A} - (\eta - 1)\,\eta\frac{k}{q}\ln\left(\frac{K_{10}}{K_9}\right) \end{aligned} \tag{17}$$

$$b_1 = \frac{dV_{SD,\,M5}}{dT} = \eta\frac{k}{q}\ln\left(\frac{K_1}{K_2}\right) \tag{18}$$

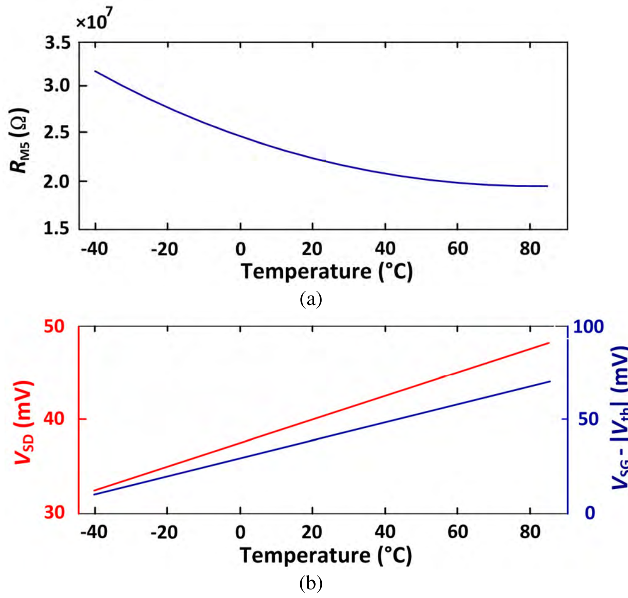

FIGURE 4. Simulation results of M5 in Fig. 3: (a) resistance variation of M5 with temperature, and (b) variations of $V_{SD,M5}$ and $V_{SG,\,M5} - |V_{TH,M5}|$ with temperature.

According to the temperature dependency of the carrier mobility described in [7], [13] and [21], c_1 can be given by

$$c_1 = \frac{d\mu_p}{dT} = -m\mu_{p0}\frac{T_0^m}{T^{m+1}} \tag{19}$$

where T_0 is the room temperature. The value of m is about 1.5 for an ordinary MOSFET.

In (17), we provide an appropriate overdrive voltage for M5, and we can have

$$V_{SG,\,M5} - \left|V_{TH,\,M5}\right| > V_{SD,\,M5} > 0 \tag{20}$$

We also make $K_6 \ll 1$ and ensure that

$$\frac{k}{q}\ln\frac{P_{D,\,poly}(K_6 I_0)^\eta}{N_A (I_{D6})^\eta} < \frac{k}{q}\ln\frac{P_{D,\,poly}}{N_A} \tag{21}$$

For (17) and (18), if we provide appropriate aspect ratios for K_1, K_2, K_9, and K_{10}, we can get

$$a_1 > 0 \tag{22}$$

$$b_1 > 0 \tag{23}$$

Since c_1 is a negligibly small value, we can change (16) to

$$x_1 + y_1 > 0 \tag{24}$$

From (24), it is found that the current flowing through M5 will increase with temperature. Simulations were performed on M5 under a supply voltage of 0.5 V over a temperature range of −40 to 85 °C. The simulation results are shown in Fig. 4. It is indicated that the resistance of M5 in Fig. 3 decreases with an increase in temperature. The variations in $V_{SD,M5}$ and $V_{SG,\,M5}$-$|V_{TH,M5}|$ with temp-erature can also match the above theoretical analysis.

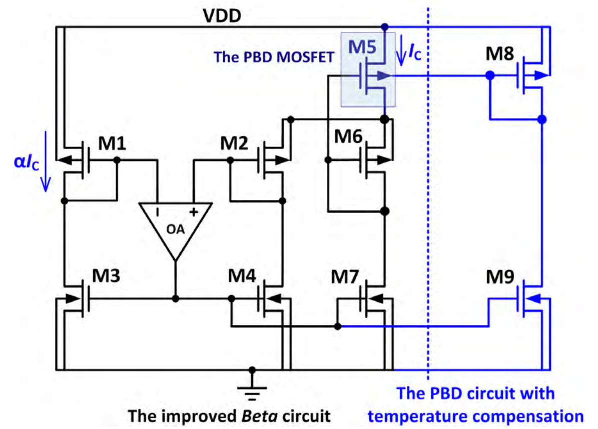

FIGURE 5. Proposed CTAT current generator.

B. CTAT CURRENT GENERATOR

Fig. 5 shows the proposed CTAT current generator. Its difference from the generator in Fig. 3 is the PBD circuit with CTAT temperature compensation. The drain current, gate-source voltage and substrate voltage of transistor M5 in Fig. 5 can be given by

$$I_C = \mu_p C_{OX} K_5 (V_{SG,\,M5} - \left|V_{TH,\,M5}\right|) V_{SD,\,M5} \tag{25}$$

$$V_{SG,\,M5} = V_{SG,\,M1} - V_{SG,\,M2} + V_{SG,\,M6} \tag{26}$$

$$V_{BS,\,M5} = -V_{SG,\,M8} \tag{27}$$

From (9), we get

$$\left|V_{TH,\,M5}\right| \approx \left|V_{TH0,\,M5}\right| + (1-\eta)V_{SG,M8} \tag{28}$$

To determine the current variation of M5 in Fig. 5 with temperature, we differentiate I_C in (25) with respect to T and obtain

$$\frac{\partial I_C}{\partial T} = C_{OX}K_5\Bigg[\underbrace{a_2\mu_p V_{SD,\,M5}}_{x_2} + \underbrace{b_2\mu_p(V_{SG,\,M5} - \left|V_{TH,\,M5}\right|)}_{y_2} + \underbrace{c_2(V_{SG,\,M5} - \left|V_{TH,\,M5}\right|)V_{SD,\,M5}}_{z_2}\Bigg] \tag{29}$$

In a similar manner as that in (16), $[x_2 + y_2 + z_2]$ in (29) is expected to be less than zero to obtain a current with a negative TC. The thermal slope of I_C can be described as a function of parameters that are marked using a_2, b_2, and c_2. c_2 is same as c_1 in (19) and we express a_2 and b_2 as follows:

$$\begin{aligned} a_2 &= \frac{d(V_{SG,\,M5} - \left|V_{TH,\,M5}\right|)}{dT} \\ &\approx \frac{\partial\left(V_{SG,M1} - V_{SG,\,M2}\right)}{\partial T} + \frac{\partial V_{SG,\,M6}}{\partial T} \\ &\quad - \frac{\partial\left[\left|V_{TH0,\,M5}\right| - (\eta-1)V_{SG,\,M8}\right]}{\partial T} \\ &\approx \eta\frac{k}{q}\ln\left(\frac{K_6K_1}{K_8K_2}\right) + \frac{k}{q}\ln\frac{P_{D,\,poly}}{N_A} \end{aligned}$$

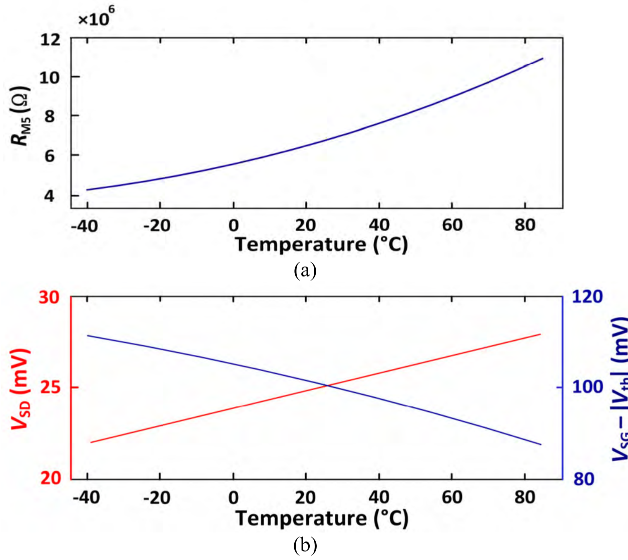

FIGURE 6. Simulation results of M5 in Fig. 5: (a) resistance variation of M5 with temperature, and (b) variations of $V_{SD,M5}$ and $V_{SG,\,M5}-|V_{TH,M5}|$ with temperature.

$$-\eta\frac{k}{q}\ln\frac{P_{D,\,poly}(K_8I_0)^\eta}{N_A(I_{D8})^\eta} \tag{30}$$

$$b_2=\frac{dV_{SD,\,M5}}{dT}=\eta\frac{k}{q}\ln\left(\frac{K_1}{K_2}\right) \tag{31}$$

In the process used, η is about 1.60 for pMOSFETs. We can set an appropriate K_8 to ensure

$$\eta\frac{k}{q}\ln\frac{P_{D,\,poly}(K_8I_0)^\eta}{N_A(I_{D8})^\eta}-\frac{k}{q}\ln\frac{P_{D,\,poly}}{N_A}>0 \tag{32}$$

For (30), if we provide appropriate aspect ratios for K_1, K_2, K_6, and K_8, we can get

$$\frac{K_8K_2}{K_6K_1}<1 \tag{33}$$

$$a_2<0 \tag{34}$$

We provide the overdrive voltage for M5 below:

$$V_{SG,\,M5}-\left|V_{TH,\,M5}\right|\gg V_{SD,\,M5} \tag{35}$$

Since c_2 is same as c_1, we see from (19) that it is a small value. From (28), (29), and (34), if we provide appropriate K_8, K_6, K_2, and K_1 to make

$$|a_2|\gg b_2 \tag{36}$$

then, we can get

$$x_2+y_2+z_2<0 \tag{37}$$

From (37), it is found that the current flowing through M5 in Fig. 7 decreases with an increase in temperature. Simulations are also performed to M5 under a supply voltage of 0.5 V over a temperature range of −40 to 85 °C. The simulation results are shown in Fig. 6. It is indicated that the resistance of M5 in Fig. 5 increases with temperature. The variations in $V_{SD,M5}$ and $V_{SG,M5}-|V_{TH,M5}|$ with temperature can also match the theoretical analysis.

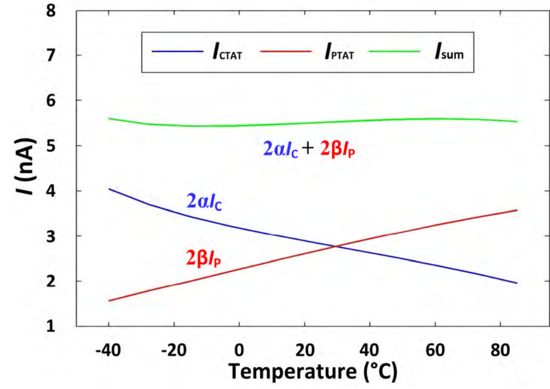

FIGURE 7. Simulated variations of generated currents.

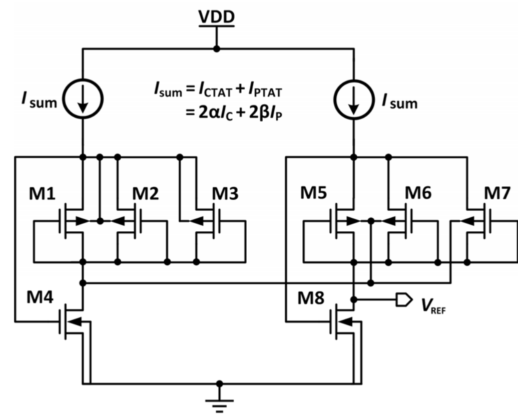

FIGURE 8. I/V conversion circuit with temperature compensation.

C. I/V CONVERSION CIRCUIT WITH TEMPERATURE COMPENSATION

The proposed VR is expected to generate a reference voltage that is almost independent of the temperature. Although we can obtain a low TC current, as shown in Fig. 7, with a combination of the proposed PTAT and CTAT current generators, it is still not possible to directly achieve an expected low-TC reference voltage with this generated current flowing through an active resistance device. Thus, we present an I/V conversion circuit as shown in Fig. 8. It can compensate the variation in the output voltage with temperature. Different from that in [14], the PBD technique enables it operate in a standard n-well CMOS. Moreover, necessary effort was made on matching these two branches in Fig. 8, aiming to reduce the output error caused by process variation as possible.

All of these MOS devices are in the subthreshold region so they can operate at low voltage. From Fig. 8, V_B and V_{SB} for M5, M6, and M7 can be given by

$$V_B=V_{GS,\,M4}-\left|V_{GS,\,M1}\right| \tag{38}$$

$$V_{BS}=V_{GS,\,M4}-V_{GS,\,M8}-\left|V_{GS,\,M1}\right| \tag{39}$$

Using (4), (9), and (39) and assuming that η is a constant value in the process used, the output voltage V_{REF} can be

approximately written as

$$\begin{aligned} V_{\mathrm{REF}} &= V_{\mathrm{GS,\,M8}} - \left|V_{\mathrm{GS,\,M5}}\right| \\ &\approx V_{\mathrm{TH,\,M8}} - \left|V_{\mathrm{TH,\,M5}}\right| + \eta V_{\mathrm{T}} \ln\left(\frac{3\mu_{\mathrm{p}}K_5}{\mu_{\mathrm{n}}K_8}\right) \\ &\approx V_{\mathrm{TH0,\,M8}} - \left|V_{\mathrm{TH0,\,M5}}\right| + \eta V_{\mathrm{T}} \ln\left(\frac{3\mu_{\mathrm{p}}K_5}{\mu_{\mathrm{n}}K_8}\right) \\ &\quad + \gamma\left(\sqrt{2\Phi_{\mathrm{F}} + V_{\mathrm{GS,\,M8}} - V_{\mathrm{GS,\,M4}} + \left|V_{\mathrm{GS,\,M1}}\right|} \right. \\ &\quad \left. - \sqrt{2\Phi_{\mathrm{F}}}\right) \end{aligned} \tag{40}$$

By setting the same W/L and current for M4, and M8, and making $V_{\mathrm{SG4}} = V_{\mathrm{SG8}}$, we have

$$\begin{aligned} V_{\mathrm{REF}} = V_{\mathrm{TH0,\,M8}} - \left|V_{\mathrm{TH0,\,M5}}\right| + \eta V_{\mathrm{T}} \ln\left(\frac{3\mu_{\mathrm{p}}K_5}{\mu_{\mathrm{n}}K_8}\right) \\ + \gamma\left(\sqrt{2\Phi_{\mathrm{F}} + \left|V_{\mathrm{GS,\,M1}}\right|} - \sqrt{2\Phi_{\mathrm{F}}}\right) \end{aligned} \tag{41}$$

Roughly, assuming that $3\mu_{\mathrm{p}} = \mu_{\mathrm{n}}$ and $V_{\mathrm{TH0,M8}} = |V_{\mathrm{TH0,M5}}|$, (41) can be approximated as

$$V_{\mathrm{REF}} \approx (\eta - 1)\left|V_{\mathrm{GS,\,M1}}\right| + \eta V_{\mathrm{T}} \ln\left(\frac{K_5}{K_8}\right) \tag{42}$$

Differentiating (42) with respect to temperature, we can have

$$\begin{aligned} \frac{\partial V_{\mathrm{REF}}}{\partial T} &= (\eta - 1)\frac{\partial\left|V_{\mathrm{GS,\,M1}}\right|}{\partial T} + \eta\frac{k}{q}\ln\left(\frac{K_5}{K_8}\right) \\ &= (\eta - 1)\,\phi + \eta\frac{k}{q}\ln\left(\frac{K_5}{K_8}\right) \end{aligned} \tag{43}$$

where ϕ is the first-order slope of $V_{\mathrm{TH,\,M1}}$, equivalent to -8.67×10^{-4}V/°C. Because M1 is designed with a large aspect ratio, the first-order slope of $|V_{\mathrm{GS,M1}}|$ is smaller than ô. Solving for $\partial V_{\mathrm{REF}}/\partial V_{\mathrm{T}} = 0$, we arrive at the expression

$$K_5 = K_8 \exp\left(\frac{q}{k}\frac{1-\eta}{\eta}\phi\right) \tag{44}$$

According to (44), the aspect ratios of M5 and M8 in Fig. 8 can be determined for temperature compensation.

III. DESIGN CONSIDERATIONS

A. CONSIDERATIONS OF SIZE FOR SEVERAL KEY DEVICES

Fig. 9 shows the entire circuit of this subthreshold voltage reference. In Table 1, the parameters of the used process and the aspect ratios for all of these MOS devices in this proposed voltage reference circuit are provided.

TABLE 1. Parameters of process and sizes for all components in proposed circuit.

Name	W/L, μm/μm
M1/M3	0.22/10
M2	4/10
M4	0.51/10
M5	6/10
M6	12/10 = (6/10)×2
M20	18/10 = (6/10)×3
M23	0.35/10
M24/M28	2/10
M27	32/10 = (8/10)×4
M7/M13	4/10
M8/M10	6/10
M9/M11	4/10
M12/M14	6/10
M15/M17	4/10
M16/M18	6/10
M19/M21	4/10
M31/M37	1/10
M35/M38	12/10
M29/M33	12/10
M22/M25/M26	0.22/10
M36/M39/M40	12/10
M30/M32/M34	48/10 = (12/10)×4
$\mu_{\mathrm{n}}C_{\mathrm{OX}}$	251.1 μA/V^2
$\mu_{\mathrm{p}}C_{\mathrm{OX}}$	83.2 μA/V^2
$V_{\mathrm{TH0,\,PMOS}}$	-402 mV
$V_{\mathrm{TH0,\,NMOS}}$	390 mV

1) The operational amplifier (OA) is realized without a tail current. The structure selected for these two OAs can accommodate the low-supply-voltage requirement. The structure is also expected to achieve enough gain and a low offset. The area $W \times L$ of the devices in these OAs can affect the matching performance. Since long-channel devices have relatively low threshold voltages, we design all these MOS devices with L_{MAX}. The input offset of the OA is reduced as much as possible by using long-channel devices and matching these two branches.
2) M3 and M22 in Fig. 9 operate in the triode region. They are expected to act as resistors with opposite TCs. The channel length is inversely proportional to the threshold voltage and directly proportional to the impedance. M3 and M22 are both designed with an aspect ratio of $W_{\mathrm{MIN}}/L_{\mathrm{MAX}}$ to accommodate a low supply voltage and low current. At room temperature, the drain current of M22 is 2 nA, while the corresponding current of M3 is 3.5 nA. The channel widths of M4 and M23 in Fig. 9 are carefully determined for a better temperature compensation effect on the generated currents.
3) For the output stage circuit, temperature compensation is realized by introducing the difference between two temperature-dependent variables, $V_{\mathrm{GS,M30}}$ and $V_{\mathrm{GS,M31}}$, into the bulk of M36. The presented I/V conversion circuit consists of two current summation circuits. They are not strictly symmetrical. The value of $V_{\mathrm{BS,M36}}$ should not be too small in order to avoid turning on the bulk-source junction. The width of M30 is four times that of M36. The pMOS device in each branch has been split to three devices with same aspect ratio in parallel for matching optimization, output error reduction and to achieve better TC. Taking mismatch and process variation into consideration, 1000-times Monte Carlo simulation results show that about 3 ppm/°C TC improvement can be achieved by splitting these two pMOS devices in Fig. 8.

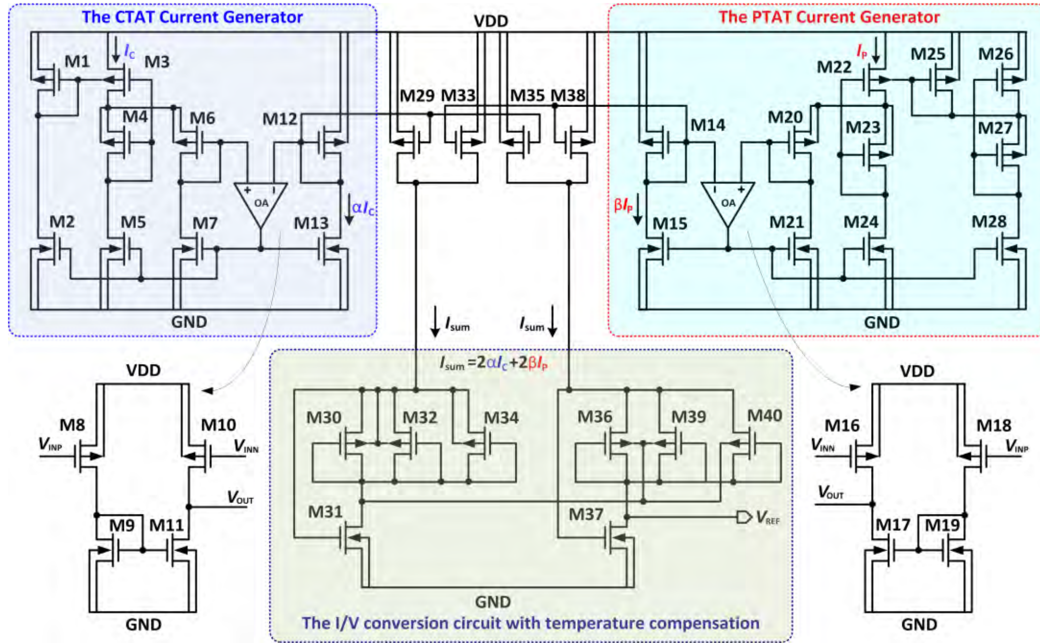

FIGURE 9. Circuit of proposed subthreshold voltage reference.

B. MINIMUM SUPPLY VOLTAGE

In the proposed voltage reference circuit, except for M3 and M22, which operate in the triode region, all the other devices are operated in the subthreshold region. The supply voltage should not only keep all these transistors in the sub-threshold region but also ensure that the I_D of these transistors is almost irrelevant to their V_{DS}. The V_{DS} of each MOS transistor operating in the subthreshold region should be greater than 0.1 V. Hence, we have

$$\begin{aligned} V_{DD,\,min} = \max\{&0.1\text{ V} + |V_{GS,\,M19}|,\, 0.1\text{ V} + |V_{GS,\,M14}|,\\ &0.1\text{ V} + |V_{GS,\,M22}|,\, 0.1\text{ V} + |V_{GS,\,M26}|,\\ &0.1\text{ V} + |V_{GS,\,M31}|,\, 0.1\text{ V} + |V_{GS,\,M37}|,\\ &0.1\text{ V} + |V_{GS,\,M12}|,\, 0.1\text{ V} + |V_{GS,\,M9}|,\\ &0.1\text{ V} + |V_{GS,\,M1}|,\, 0.1\text{ V} + |V_{GS,\,M3}|,\\ &0.1\text{ V} + |V_{GS,\,M20}| + |V_{DS,\,M22}|,\\ &0.1\text{ V} + |V_{GS,\,M25}| + |V_{GS,\,M27}|,\\ &0.1\text{ V} + |V_{GS,\,M6}| + |V_{DS,\,M3}|\} \end{aligned} \tag{45}$$

The 13 items in the brackets of (45) represent the 13 branches of this proposed subthreshold reference.

The source-gate voltage of M22, $V_{SG,\,M22}$, should be larger than its $|V_{TH}|$ to make it operate in the triode region. Owing to the superposition of $V_{DS,M28}$ and $|V_{GS,M27}|$, the V_{BS} of M22 is not low enough, and $|V_{TH,M22}|$ stays at a relatively high value. Since a large $|V_{GS,M22}|$ is needed to make M22 operate in a triode region, the branch constructed with M22, M23, and M24 mainly restricts the supply-voltage reduction. The simulated value of $|V_{TH,M22}|$ is 350 mV. The V_{DS} of M24, which operates in the subthreshold region, is about 0.1 V.

Therefore, the required minimum supply voltage is 450 mV. Since the threshold voltage can vary with temperature, a supply voltage no less than 500 mV is applied conservatively in our design.

C. SENSITIVITY TO SUPPLY-VOLTAGE VARIATIONS

To determine how the fluctuation of the power supply affects the subthreshold voltage reference, we start with (41). It shows that the relationship between the output voltage and the variation in the power supply depends mainly on $V_{GS,M1}$ in Fig. 8. According to (4), we can get

$$|V_{GS,\,M1}| = |V_{TH,\,M1}| + \eta V_T \ln\left[\frac{I_{sum}/3}{\mu_p C_{OX}(\eta-1)K_1 V_T^2}\right] \tag{46}$$

$$\begin{aligned} \frac{\partial |V_{GS,\,M1}|}{\partial V_{DD}} &= \eta V_T \frac{\mu_p C_{OX}(\eta-1)K_1 V_T^2}{I_{sum}/3}\frac{\partial I_{sum}}{\partial V_{DD}}\\ &\quad\times \frac{1}{3\mu_p C_{OX}(\eta-1)K_1 V_T^2}\\ &= \frac{\eta V_T}{I_{sum}}\frac{\partial I_{sum}}{\partial V_{DD}} \end{aligned} \tag{47}$$

Then, we evaluate the sensitivity of this proposed VR to the supply voltage by taking the derivative of V_{REF} in (41) with respect to V_{DD} and substituting (47) into it. Thus, we have

$$\begin{aligned} \frac{\partial V_{REF}}{\partial V_{DD}} &= \gamma \frac{\frac{\partial |V_{GS,\,M1}|}{\partial V_{DD}}}{2\sqrt{2\Phi_F + |V_{GS,\,M1}|}}\\ &= \frac{\gamma}{I_{sum}} \frac{\eta V_T \frac{\partial I_{sum}}{\partial V_{DD}}}{2\sqrt{2\Phi_F + |V_{GS,\,M1}|}} \end{aligned} \tag{48}$$

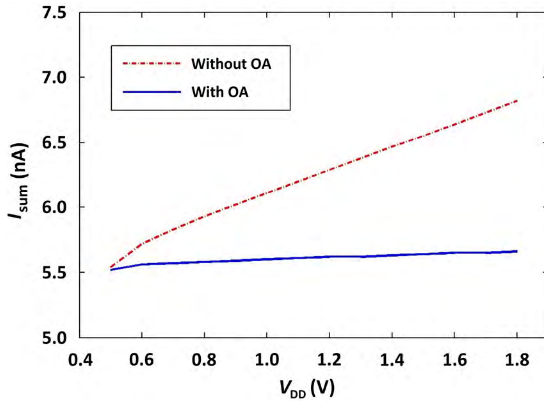

FIGURE 10. Simulated current variations of I_{sum} in Fig. 9 with V_{DD}.

From (48), the proposed voltage reference will be more robust against the fluctuation in V_{DD} if the currents flowing into the I/V conversion circuit are insensitive to it. Actually, *Beta* circuits usually have good line sensitivities. Since the proposed circuit operates in the subthreshold region and its line sensitivity can deteriorate under a nanoampere current, we use two simple operational amplifiers in the presented current generators to increase the robustness of the generated currents against the fluctuation in V_{DD}. Fig. 10 shows the simulated current variations of I_{sum} in Fig. 9 when the supply voltage ranges from 0.5 V to 1.8 V. It can be found that the current variation is significantly reduced after using these two operational amplifiers.

D. SENSITIVITY TO PROCESS VARIATIONS

As shown in (42) and (43), the reference voltage and its TC are both η-dependent. η depends on the gate oxide and depletion layer capacitances, so it is determined by the process [26]. The values of η almost vary equally for same type MOSFETs with certain sizes. In [14], two nMOSFETs are connected in series, and the process variation is mainly reduced by changing the threshold voltage of the bulk-driven nMOSFET. This structure can only be used in a special twin-well CMOS process.

In order to reduce the process manufacturing cost and improve the applicability of the proposed circuit, bulk-driven pMOSFETs are used instead of bulk-driven nMOSFETs in the proposed VR. Special twin-well process is no longer needed as we only use pMOSFETs with different bulk voltages. Fig. 9 shows that the reference voltage of the proposed VR is associated with the threshold voltages of M36 and M37, where M36 is a bulk-driven pMOSFET and M37 is a nMOSFET. With their connection shown in Fig. 9, the size of M36 differs greatly from that of M37. Hence, there will be slightly different changes in their threshold voltages with process variations due to different variations of η for M36 and M37. Since the I/V conversion output stage utilizes two types of MOS devices for temperature compensation, its robustness against process variation is degraded to some extent.

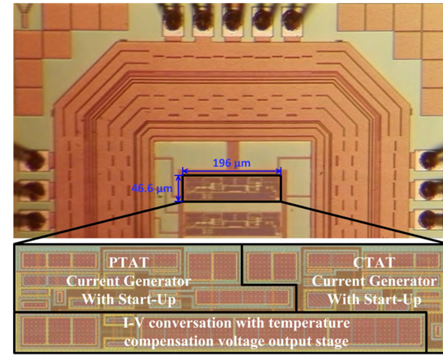

FIGURE 11. Die photograph and layout topology of proposed voltage reference. Notice that two cores are shown.

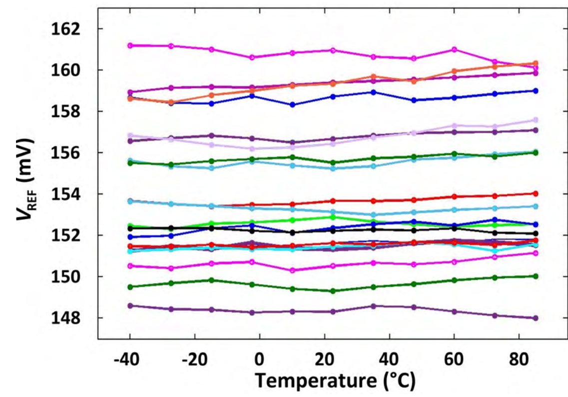

FIGURE 12. V_{REF} vs. temperature at 0.5-V supply voltage for 20 samples.

IV. MEASUREMENT RESULTS

The proposed subthreshold voltage reference is implement-ed in a standard 0.18-μm CMOS process. A microphoto-graph of the fabricated chip is shown in Fig. 11. The occupied active area for a single chip is 196 μm × 46.6 μm. The post-layout simulation shows that the TC of this proposed VR is 26.7 ppm/°C at a 0.5-V supply voltage. Twenty chips of the proposed VR were measured. These measured output reference voltages were in the range of 148 mV to 161 mV, as shown in Fig. 12. With the temperature ranging from -40 to 85 °C, the minimum and maximum output variations of these measured chips with a 0.5-V supply were 0.4 mV and 0.9 mV, respectively, which means that the TC ranges from 21 ppm/°C to 86 ppm/°C. Fig. 13 shows the TC distribution of 20 tested samples. The average TC of the output reference voltage is 35.7 ppm/°C.

The average reference voltage of a randomly selected chip measured at 0.5-V supply voltage is 151.91 mV over the temperature range from −40 to 85 °C. This chip was also measured under different supply voltages. Fig. 14 shows the power supply current of the proposed VR vs. the temperature under different supply voltages. Since the threshold voltage of MOSFET decreases with temperature, the current of the reference under a constant supply voltage increases with temperature. Operated at a 0.5-V supply voltage, the measured

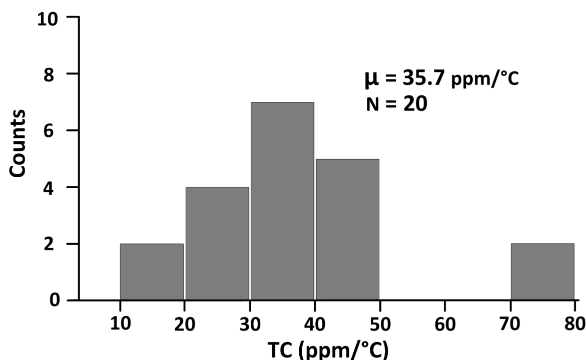

FIGURE 13. Distribution of the measured TC for 20 samples.

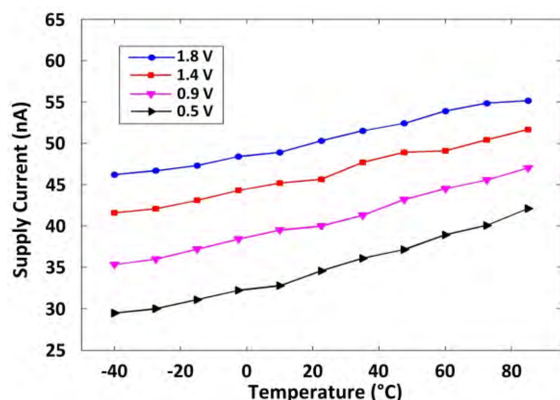

FIGURE 14. Power supply current vs. temperature at different supply voltages.

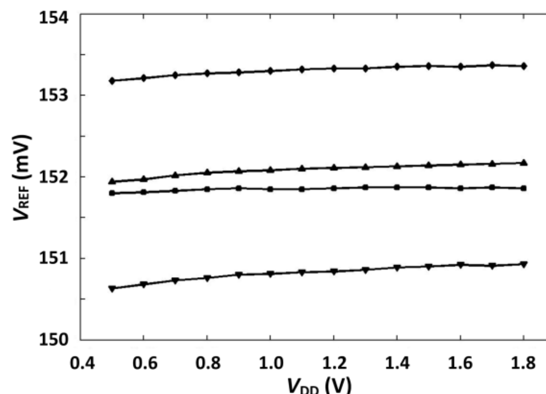

FIGURE 15. Measured V_{REF} at different supply voltages.

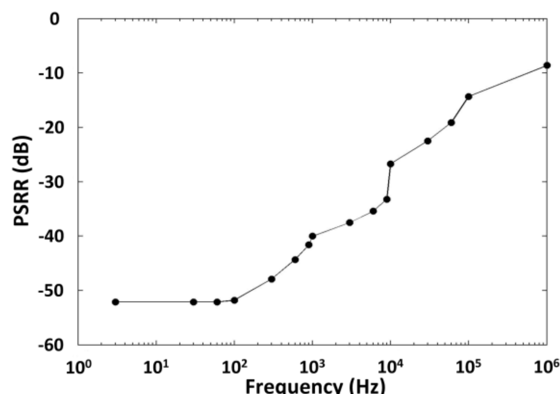

FIGURE 16. Measured PSRR of presented voltage reference at 0.5-V supply voltage.

current varies from 28.2 nA to 37.6 nA when the temperature ranges from −40 to 85 °C. The power dissipation of the presented voltage reference circuit with a 0.5-V supply voltage is 17.6 nW at room temperature. It varies from 13.6 nW to 19.7 nW when the temperature ranges from −40 to 85 °C. The supply current also increases slightly with the supply voltage. At room temperature, the supply current increases from 35.2 nA to 48.3 nA when the input voltage ranges from 0.5 V to 1.8 V. When the temperature is 85 °C, the measured supply current at $V_{DD} = 0.5$ V is 41.3 nA, while it is 55.1 nA at $V_{DD} = 1.8$ V. Fig. 15 shows the measured V_{REF} of four randomly selected samples vs. the power supply at room temperature. With the supply voltages ranging from 0.5 V to 1.8 V, the measured line sensitivities are 0.1%, 0.086%, 0.03%, and 0.15%, respectively. The average line sensitivity of this voltage reference is 0.09%. As shown in Fig. 16, the PSRR is −51.8 dB at 100 Hz, while it is −40.1 dB at 1 kHz.

The performance of this proposed voltage reference is summarized and compared with those of previous works in Table 2. Owing to the proposed temperature compensation technique, the proposed VR achieves a much lower TC than in [4], [14], [17], [18], and [26]–[29]. To avoid deterioration in the temperature characteristic of the output reference, it does not use any additional circuit for trimming its process variation. It should be mentioned that the proposed VR does not use a resistor, capacitor, BJT, or special active devices. It is realized with only standard V_{TH} (SVT) MOSFETs in standard n-well CMOS process and occupies the smallest area compared to all of the competitors except [17], [27] and [29] in Table 2, while featuring robustness against supply variations. The simple operational amplifier without a tail current source that we used does not obviously increase the circuit complexity and power dissipation. The proposed VR circuit consumes less current than most of the other designs in Table 2. Implemented in a twin-well CMOS process, the design reported in [14] achieves better line sensitivity and consumes less power. The presented circuit with pMOS-bulk-driven technology does not require the twin-well CMOS process. Since it is an all-SVT-MOSFET voltage reference and no special device is utilized, if the model library provided is accurate, it is also very promising to perform well in other standard 0.18-μm CMOS process.

According to [27] and [28], we also use FoM (Figure-of-Merit) to evaluate the main performance parameters of a voltage reference. It can be expressed as

$$\text{FoM} = \frac{(T_{MAX} - T_{MIN})^2}{\text{TC} \times \text{Power} \times \text{Area}} \times 10^{-18} \tag{49}$$

It has been multiplied by 10^{-18} for easy description and comparison. $T_{MAX} - T_{MIN}$ is the operating temperature range of the VR. Since the threshold voltages of MOS devices

TABLE 2. Comparison to state-of-the-art subthreshold VR circuits.

Parameter	This work	[4] TCAS-II'17	[5] TCAS-II'18	[9] TVLSI'18	[14] TCAS-I'16	[17] JSSC'12	[18] ISSCC'15	[20] TCAS-I'18	[26] JSSC'13	[27] TCAS-I'17	[28] TCAS-II'19	[29] TCAS-II'19
Process, μm	0.18	0.18	0.18	0.18	0.18	0.18	0.13	0.18	0.18	0.18	0.13	0.18
Temp., °C	-40–85	-40–130	-40–125	-40–125	-40–85	-20–80	0–80	-45–120	-40–120	0–120	0–85	-40–125
TC, ppm/°C	35.7	84.5	23.5	33.7	59.4	54.1–176.4	75	28	114	72.4	81.5	89.83
Supply voltage, V	0.5–1.8	0.4–1.8	0.6–2.0	0.9–2	0.45–1.8	0.5–3.6	0.5–1.5	0.55–1.8	0.7–1.8	0.45–3.3	0.3–1.2	0.4–1.8
V_{REF}, mV	151.91	212.4	218.3	411.86	118.41	326.8–330	498	460	548	256.6	306.8	151
PSRR, dB @ 100 Hz	-51.8	-40	NA	-44	-50.3	-49	-40	-62	-56	-43.9	-29	> -55
Line sensitivity	0.09%	NA	0.4%	0.06%	0.033%	0.044%	2%	0.059%	NA	0.43%	11.7%	0.23%
Supply current, nA	35.2 @ 0.5 V	480 @ 0.4 V	51 @ 0.6 V	94 @ 0.9 V	34.7 @ 0.45 V	0.011 @ 0.5 V	64 @ 0.5 V	83 @ 0.55 V	75 @ 0.7 V	0.33 @ 0.45 V	9156 @ 0.45 V	2.5 @ 0.4 V
Area, mm^2	0.0092	0.09	0.075	0.11	0.0132	0.001425	0.0264	0.061	0.0246	0.002	0.014	0.005
FOM, °C^3/W×mm^2	2.70	0.020	0.51	0.087	1.28	7233.10	0.10	0.35	0.17	669.68	0.0015	60.61
Trimming	NA	NA	NA	NA	Yes	Yes	Yes	Yes	NA	Yes	NA	Yes
Special requirements	NA	Resistor	HV IO device & resistor	Resistor & BJT	Twin-well	Native & thick oxide devices	Resistor & BJT	Resistor & BJT	BJT	High V_{TH} devices	Diodes, resistor & capacitor	Native & IO devices

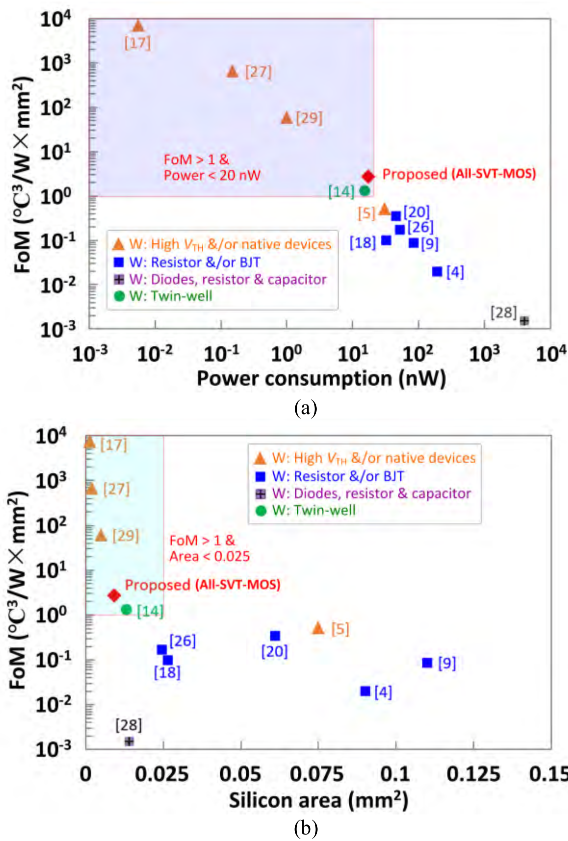

FIGURE 17. FoM comparison with prior works with respect to (a) power and (b) silicon area.

in this used process vary greatly with temperature, especially at high temperature, the temperature performance of the proposed VR deteriorates when the temperature is over 85 °C. Fig. 17 shows the comparison between the proposed all-SVT-MOS VR with published low power subthreshold voltage references. It has been shown that the proposed VR features very competitive FoM. Although [17], [27], and [29] present higher FoMs, [17] and [29] use both native and thick oxide devices, and [27] utilize both standard and high V_{TH} devices.

V. CONCLUSION

This paper presented a pMOS-bulk-driven temperature compensation technique for a subthreshold voltage reference. Using novel PTAT and CTAT current generators and an I/V conversion circuit with temperature compensation, a voltage reference was implemented with only SVT-MOS devices in a standard 0.18-μm n-well CMOS process. The measurement results showed that the circuit achieves low TC with low power and a miniaturized chip area. The measured results have indicated that a competitive line sensitivity and PSRR were achieved. The circuit is suitable for applications that require low power and small size.

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