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Ultra Miniature $1850 \mu\text{m}^2$ Ring Oscillator Based Temperature Sensor

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ABSTRACT Temperature sensing is a necessity in semiconductor products, in order to monitor die behavior and avoid thermal runaway, while achieving high performance. Integrated sensors are used to monitor and regulate numerous hot spots across the die to prevent reliability issues. As the hot spots are in the most congested areas of the chip, it is also desirable for the sensors to have a very small sensing element which can be placed close to the hot-spot. The sensors are also used to monitor the coldest parts of the chip to determine the required Vdd level. These functions require the sensors to be very compact as well as low energy. A ring oscillator based temperature sensor is presented in TSMCs 65nm node, with an area of $1850 \mu\text{m}^2$. This sensor has a novel structure which is similar to a bandgap reference, with the BJT devices replaced by scaled ring oscillators. The sensor exhibits a 3-sigma inaccuracy of $\pm 1^\circ\text{C}$ near the throttle point, for hot-spot sensing, and $\pm 2.5^\circ\text{C}$ over the -10°C to 110°C range. The power supply rejection is $2.4^\circ\text{C}/\text{V}$. The sensor consumes 0.94nJ per $10 \mu\text{s}$ conversion and achieves a resolution FOM of $96\text{pJ}\cdot\text{K}^2$.

INDEX TERMS Low power, ring oscillators, sub-threshold design, MOS temperature sensors.

I. INTRODUCTION

Thermal sensors are used to measure and regulate the temperature in nearly every computer system and integrated circuit (IC). The hot-spots in CPUs are identified by multiple thermal sensors spread across the die [1], [2]. When one of these hot-spots approaches the reliability limit the sensor indicates a warning to the Power Management Unit (PMU) or the Package Control Unit (PCU) of the chip, which causes the IC to reduce its frequency, a command referred to as throttling [3]–[5]. If the chip continues to heat up, there is an additional catastrophic temperature indicator, usually $15\text{--}20^\circ\text{C}$ above the throttle point at which the platform shuts down [3]. At low operating voltages the IC frequency can observe an inverse temperature dependence, which causes the operating frequency to be lowered as the temperature drops [2]. As such, the sensors are also used to determine the coldest parts of the CPU, in order to determine the required Vdd level to maintain frequency and avoid under spec performance [5]. The sensors are also used to determine fan regulation of the entire system [6]. The accuracy of the sensor is thus linked to the power/performance of the chip.

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In addition, as multiple hot-spots and cold-spots need to be measured, there can be many sensors spread across the die (as many as 40) [2]. It is thus highly desirable that the sensors be compact ($< 0.02 \text{ mm}^2$) [1] and low energy. The thermal time constant of CPU's is $\sim 1\text{--}10\text{ms}$ [2], so the sensors should have a sensing speed $> 1\text{kS}/\text{sec}$. If the sensors are faster, then they can be duty-cycled to save further power. During deep-sleep states, the sensors can be turned off to save power. Upon reawakening, a fast reading ($10\text{--}20 \mu\text{s}$) is required to determine the required supply level [2]. This initial reading is not required to be highly accurate, since some guard band can be added to the initial Vdd level to compensate. Vdd can be lowered subsequently without interfering with operation, once the sensor provides a better reading or average of several readings. The specifications of compact sensors in a CPU is $\pm 3^\circ\text{C}$ at the throttle point and $\pm 5^\circ\text{C}$ across the rest of the range. Since part of the inaccuracy is associated with the testing and calibration, it is recommended that the Si accuracy be $\pm 1^\circ\text{C}$ at throttle and $\pm 3^\circ\text{C}$ over the range [2]. There are several mechanisms available to sense temperature [7], the most established in products being the parasitic PNP bipolar junction transistor (BJT) found in the CMOS process. The PNP sensor, and its variants are based upon summing proportional to absolute temperature (PTAT)

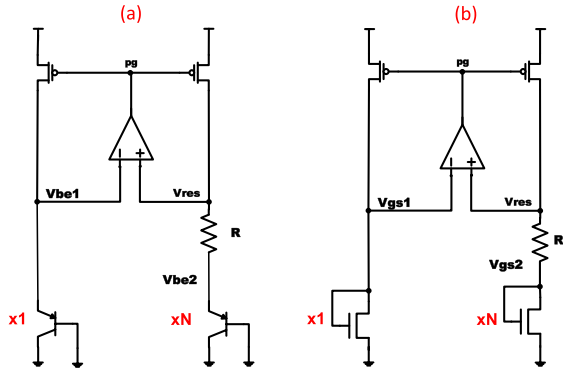


FIGURE 1. (a) BJT based bandgap reference and (b) MOS based biasing circuit.

and complementary to absolute temperature (CTAT) nodes in a bandgap reference circuit to create a reference voltage, V_{ref} [8]. The CTAT or PTAT nodes are then compared to V_{ref} using an analog-to-digital converter. Resistors are also a good alternative to PNP-based sensors, although the sensing elements tend to be larger [9], [10]. MOS based sensors, which utilize the temperature dependence of the threshold voltage, V_{th} , have also been reported and these can be both small and very fast [11]–[14]. Another type of sensor is Thermal Diffusivity (TD) which can achieve high accuracy, without calibration [15]. In this paper, we present a compact $1850\mu\text{m}^2$ ring-oscillator based sensor, which exhibits a 0.94 nJ/conv. energy and a conversion speed of $10\mu\text{s}$.

II. RING OSCILLATOR BASED SENSOR CIRCUIT DESIGN

A conventional bandgap reference (BGREF) current generator is shown in Fig. 1a. Since the two BJT’s are sized differently, the ΔV_{be} voltage will appear across the resistor [8] and the current will obey (1)

$$I = \frac{\Delta V_{be}}{R} = \left(\frac{KT}{qR}\right) \ln(N) \tag{1}$$

where KT/q is the thermal constant, R is the resistance and N is the BJT ratio. In Fig. 1b, the BJT’s are replaced with diode connected NMOS devices in subthreshold, and the ΔV_{gs} voltage will appear across the resistor, and the current will obey (2)

$$I = \frac{\Delta V_{vg}}{R} = \left(\frac{KT}{qR}\right) \ln(N) \tag{2}$$

If the transistors are in strong inversion, the circuit in Fig. 1b will obey (3).

$$I = \frac{2}{\mu C_{ox} \frac{W}{L} R^2} \left(1 - \frac{1}{\sqrt{N}}\right) \tag{3}$$

The MOS reference circuit can also have the smaller transistor operating in strong or moderate inversion, while the larger device operates in sub-threshold, although the equations in this case become more complex.

In a conventional bandgap-based thermal sensor, an accurate Analog-to-Digital-Converter (ADC) is required to

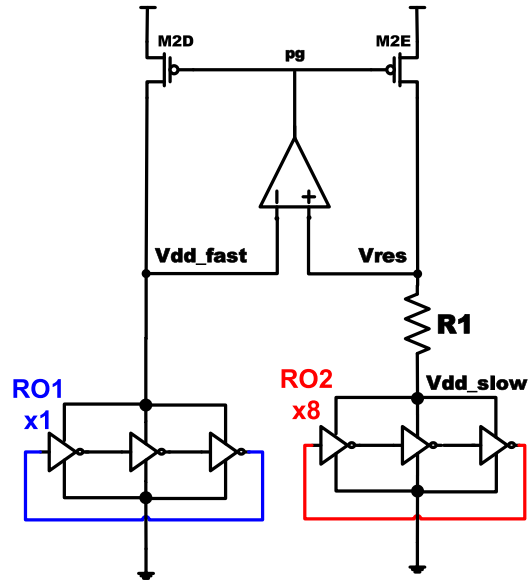


FIGURE 2. Sensor concept: The BJT devices in the bandgap reference are replaced with ring oscillators.

digitize the PTAT or CTAT voltages [1] [2]. In addition, the parasitic PNP used in BJT-based sensors are very large devices in modern CMOS processes. The advantage of a ring-oscillator sensor is that the temperature dependent frequency just needs to be input into a counter to yield a digital code, which is output after a known period, thus avoiding the need for an ADC. Ring oscillators or other delay-based sensors, such as [11], can allow very fast conversion times at relatively high resolution and low power. They can also be designed to be relatively compact. However, ring-oscillators are highly sensitive to the supply voltage as well which can make power supply rejection a difficult problem to solve using digital means alone. In this design, it is proposed to replace the conventional BJTs or subthreshold MOS with ring oscillators (RO), as shown in Fig. 2. This topology combines the compact size and high resolution aspect of ring oscillator sensors with the analog regulation of bandgap-based sensors. RO1 and RO2 are similar oscillators, but RO2 was instantiated 8 times in parallel by shorting the input and output nodes of 8 identical oscillators. The feedback loop regulates the supply voltages of the ring oscillators, V_{dd_fast} and V_{dd_slow} in a similar manner as the bandgap references in Fig. 1 regulated V_{be} or V_{gs} of the BJTs or MOSs respectively. The current in each of oscillators can be expressed as (4):

$$I = C \cdot V \cdot F \tag{4}$$

or as (5):

$$F = \frac{I}{C \cdot V} \tag{5}$$

where F is the frequency of operation, C is the total capacitance in the oscillator and V is the oscillation amplitude.

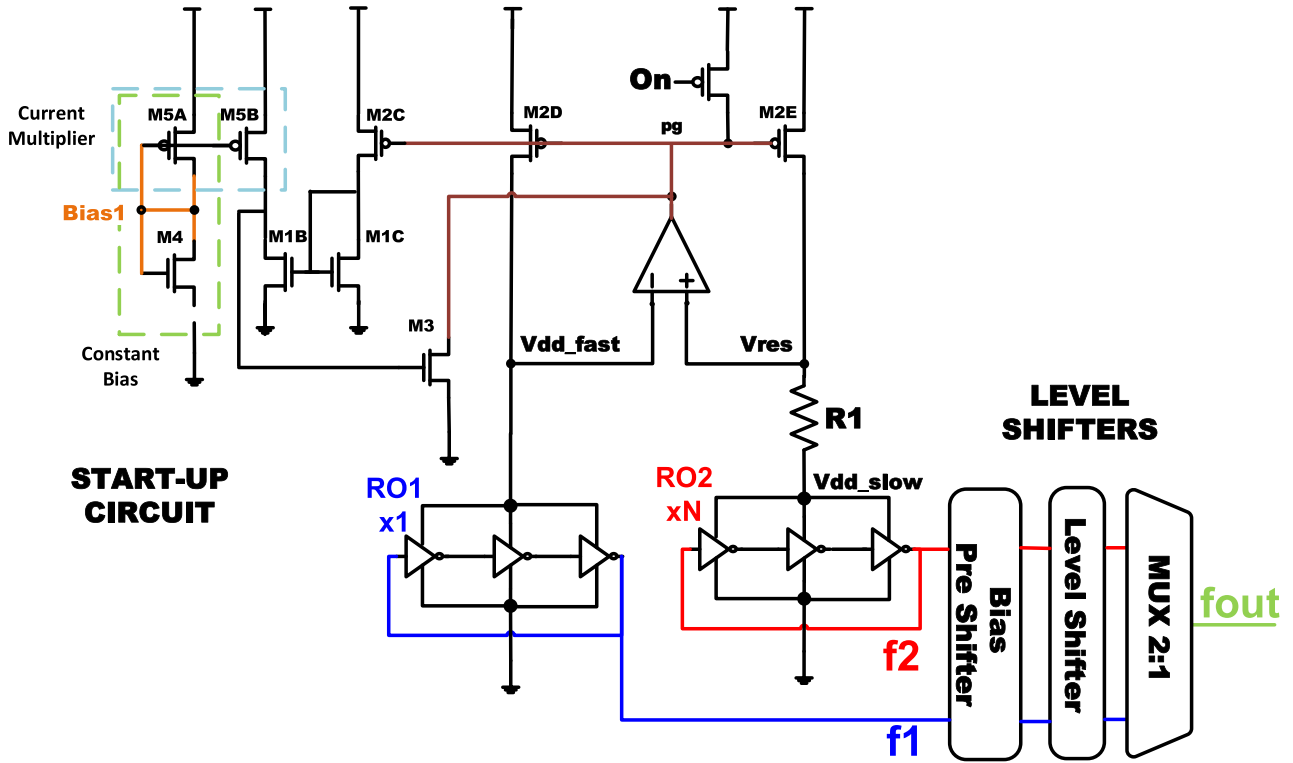


FIGURE 3. Sensor block diagram.

The amplifier forces the nodes V_{dd_fast} and V_{res} to an equal voltage, thereby yielding (6):

$$V_{res} = V_{dd_fast} \tag{6}$$

which results in the relationship (7) for V_{dd_slow} .

$$V_{dd_slow} = V_{dd_fast} - I \cdot R \tag{7}$$

During steady-state operation, the current is relatively low (in the μA range), so the oscillators toggle close to V_{th} . As the temperature rises, the amplitude is lowered, due to the CTAT nature of V_{th} , which increases the operating frequency. In addition, the current exhibits a PTAT nature, similar to its BJT counterpart (Fig. 1a), which further increases the operating frequency. Both effects are close to linear, resulting in a nearly linear frequency rise with temperature. The currents in the two oscillators are equal and provided by the two current sources in Fig. 2 which are controlled by the feedback loop. Since the capacitance of RO2 is $8\times$ larger, its operating frequency is much slower than RO1. However, it also has a slightly lower amplitude of operation, which slightly increases the frequency, so the ratio between frequencies is approximately $5.5\times$. The sensor in Fig.2 behaves very similarly to the MOS based BGREF of Fig. 1b. The V_{dd_fast} and V_{dd_slow} nodes are close to the V_{th} voltage. The difference in the oscillators V_{dd} voltages appears across the resistor R1 as in (7). However, because of the toggling of the oscillators, some switching noise appears at these nodes.

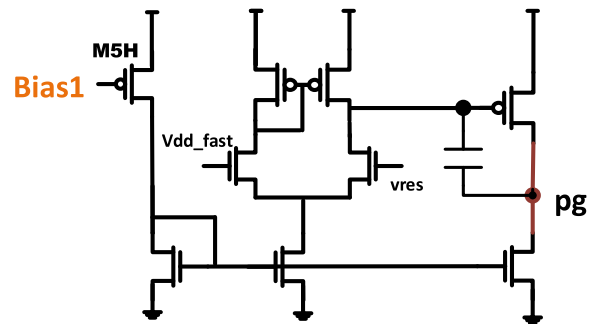


FIGURE 4. Two stage miller amplifier.

In order to mitigate these effects, decoupling capacitors were placed at nodes V_{dd_fast} (100fF to V_{ss}), V_{dd_slow} (50fF to V_{ss}) and PG (200fF to V_{dd}).

Fig. 3 shows the top-level schematic of the sensor. This includes the sensing core with the two oscillators, as well the feedback loop regulating them. There is a start-up circuit which ensures that the circuit reaches the correct operating point. Since the oscillators operate near V_{th} , level shifters are used to raise f_1 and f_2 to CMOS levels. Additional biases are required to enable the level shifting operation.

Conventional BGREF circuits, similar to Fig. 1, are usually started up by injecting a current into the circuit. This current, which may be dependent upon PVT effects, can place the circuit into its correct operating state. Usually the startup circuit

consists of a feedback loop, which allows it to turn off automatically after powerup. BJT's currents obey an exponential dependence on V_{be} ; thus, even if very high start-up currents are injected initially, the BJT's will clamp the V_{be} voltage, and the circuit will settle to its correct operating point. However, the oscillators shown in Fig. 2 have a linear voltage dependence on current, as expressed in (4). Thus, the voltage drop across the oscillator is essentially unconstrained, and must be carefully controlled during startup. If the start-up currents are too high, it could lead to the node PG being clamped to V_{ss} and the RO supplies reaching V_{dd} . In most conventional BGREFs, there are two stable states: the correct operating state, and a zero-current state. The RO based circuit has an additional stable state whereby there is too much current and regulation is lost. This is a dangerous unknown, making the startup problem more complex than conventional BGREFs.

The startup circuit is shown in Fig. 3. The startup mechanism is based upon the assertion of the node PG to the supply voltage, and the oscillator nodes to the ground using dedicated MOS switches. This closes the current sources, and ensures the oscillators are not running, thus avoiding the situation where the circuit starts at very high currents. The startup consists of a low current bias created by two stacked diode-connected transistors (M4 and M5A), which provide a stable PTAT branch of current. Once this branch is turned on, at the start of the operation, the current is copied (with a multiplying factor) to M5B, pulling the gate of M3 high. This leads to the drop of node PG, opening the current sources. The current sources allow the charging of internal nodes, and place the amplifier in its working region, near the equilibrium governed by the exact temperature and supply voltage of the system. Likewise, the oscillators begin their oscillation, stabilizing at their native frequency, governed by the number of oscillators, current in the branch, and process variation. Once current is flowing in the system, it is mirrored to M2C, where it is copied to M1B through M1C, leading to the lowering of the gate of M3, thereby closing the startup circuit.

Similar to the BGREF circuits described in Fig. 1, an amplifier is in the heart of the system, holding the nodes V_{dd_fast} and V_{res} at equilibrium. In order to allow high PSR (power supply rejection) a relatively high DC gain is required. As such the amplifier was chosen to be a two stage Miller amplifier as shown in Fig. 4 with a nominal gain of 75dB. Since the amplifier is a critical block in the system, it was chosen to be biased by the always-on startup bias circuit, Bias1, and not self-biased from the node PG. While self-biasing is an elegant and resource saving option, it carries the risk of interfering with the startup mechanism. The amplifier is an integral part of the startup mechanism, taking over from the startup circuit once the nodes of the circuit are charged to their steady state voltages. Taking the bias from PG rather than Bias1 (Fig. 3) risked the circuit waking up in the high current mode in some of the corners.

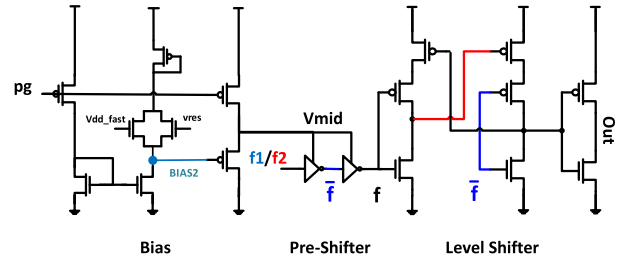


FIGURE 5. Level shifter and accompanying biasing circuit.

The amplitudes of the RO supplies are close to V_{th} , and thus the frequency outputs need to be level shifted to CMOS levels. Connecting the oscillator directly to a standard level shifter input produces a varactor effect which can degrade the PSR. This is because at the CMOS gates C_{gs} is highly V_{dd} dependent and will affect the oscillator current and frequency according to (5). Thus, any change or noise in the supply is translated into error in temperature. According to simulations this could cause a PSR of over $30^\circ\text{C}/\text{V}$. To counteract this effect, the Bias2 voltage was implemented, which is V_{dd} independent, as shown in Fig. 5. The bias is created using a replica of the amplifier circuit which biases a current branch along with the V_{dd} -independent PG bias. The supply voltage V_{mid} obeys the following equation:

$$V_{mid} = Avg(V_{res}, V_{dd_fast}) - V_{gsn} + V_{gsp} \quad (8)$$

Thus V_{mid} is very close to the voltages of the RO supplies and can be used to supply buffers which isolate the RO frequencies f_1 and f_2 from the level shifter inputs, as shown in Fig. 5. The replica had to be implemented, since the tail current bias of the amplifier was insufficient, since its overall bias was V_{dd} -dependent for reasons mentioned earlier.

A counter block (not shown) was connected to the level shifter output, in which the oscillator's frequency was compared to a reference frequency. An adjustable counter allowed different settings of integration time, effectively enabling an averaging of several consecutive measurements if needed. Integrating the frequency over an extended period reduces the influence of noise of both the RO's and the external reference.

III. SIMULATED AND MEASURED RESULTS

Figure 6 and 7 show the simulated oscillator frequencies vs. temperature for the slow and fast oscillators respectively at different process corners. Since the circuit obeys equations (4)-(7), there is not much difference between the corners compared to a standard ring oscillator. We suspect that much of the frequency shift across corners is associated with the resistance of R_1 across corners.

The results of transient Monte Carlo (MC) simulations of the slow and fast frequencies are shown in Fig. 8 and Fig. 9 for the TT corner. The steady-state frequency is plotted against temperature. It is observed that both curves are nearly linear with temperature with the slow oscillator having a sensitivity of $0.4\text{MHz}/^\circ\text{C}$, while the sensitivity of the fast oscillator is $1.45\text{MHz}/^\circ\text{C}$. The observed spread in frequency is caused by

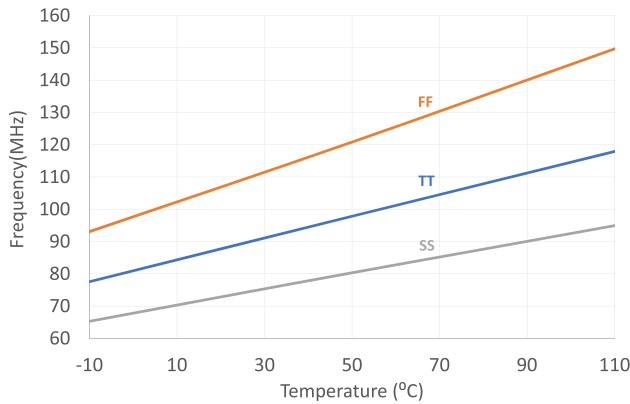


FIGURE 6. Simulated slow frequency vs. temperature across corners.

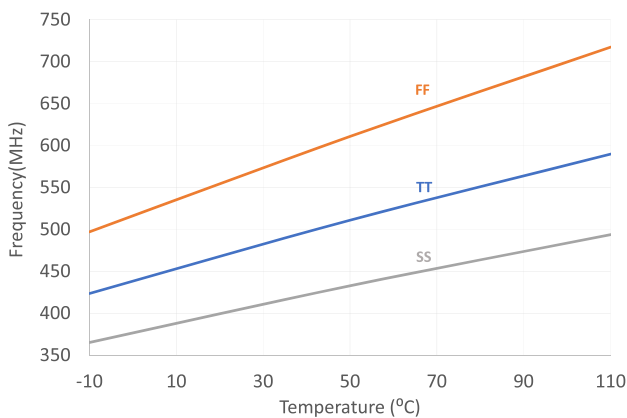


FIGURE 7. Simulated fast frequency vs. temperature across corners.

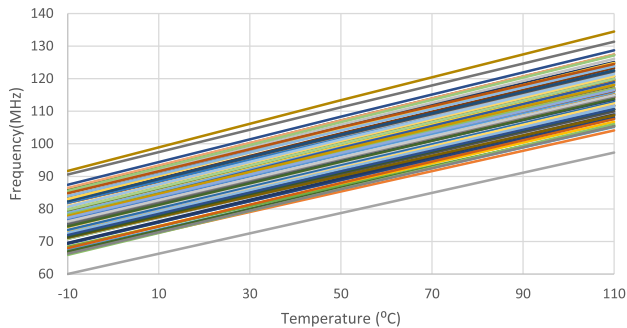


FIGURE 8. Monte Carlo simulation of the slow frequency vs temperature (100 splits).

random variation, including a combination of branch current, amplifier offsets and the V_{th} of devices in the oscillators themselves. These qualities apply directly to the resulting variations in output frequency of the oscillators.

Fig. 10 shows an internal oscillating node of the slow oscillator plotted against time, along with the simulated V_{th} voltage under nominal conditions. It is observed that the peak voltage of oscillation is close to V_{th} indicating that the slow oscillator operates in the subthreshold condition. The fast oscillator will have a larger peak-to-peak voltage, and the

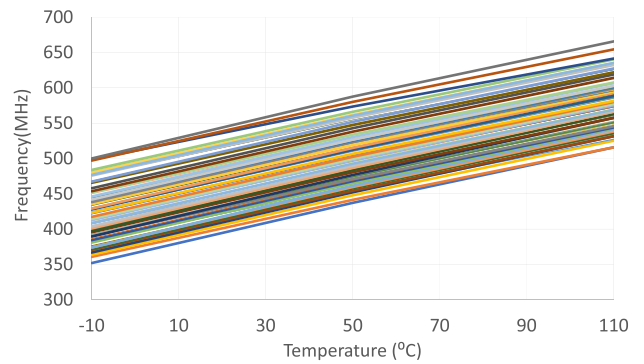


FIGURE 9. Monte Carlo simulation of the fast frequency vs temperature (100 splits).

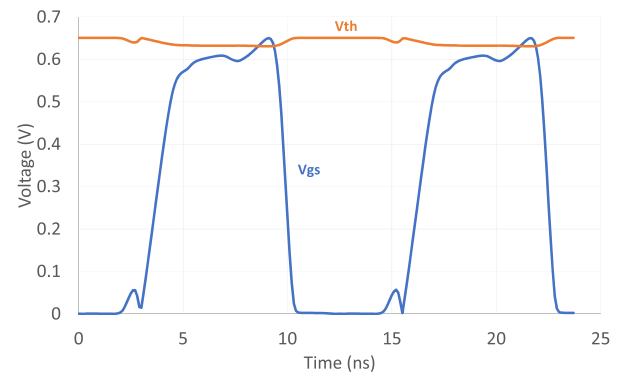


FIGURE 10. Simulation of an oscillator internal node (V_{gs}) and the threshold voltage (V_{th}) in the slow oscillator.

transistors may enter strong or moderate inversion during parts of the cycle.

A test chip of the sensor was designed and fabricated in TSMC's 65nm node. The sensor's area is $1850\mu\text{m}^2$, not including the counter which was shared among 8 sensors. The area of a 12-bit counter in this technology is $170\mu\text{m}^2$. The packaged chip was coupled to an aluminum heat sink with a graphite thermal pad. Measurements were made with the chip and custom test board in a Votsch VT 7004 Test Chamber. The chips' performance was validated and characterized through the standard temperature range of -10°C through 110°C . An external 100MHz reference clock was provided and the chip's temperature was monitored using a PT100 temperature probe embedded into the aluminum heat sink and monitored using a 4 terminal sensing setup. The PT100 resistive thermal sensor, shaped as a 300mm long rod, was calibrated by the manufacturer such that it provides an accuracy of 20mK. It was placed through an opening in the oven into the heat sink such that its position in the heat sink was very close to the chip (within 1mm). The opening was blocked from the outside by a seal which prevented the heat from escaping. During the chip's measurement, the PT100 was sampled several times to determine the temperature, and to ensure the temperature at the chip was stable. The experimental setup is shown in Fig. 11. A total of 35 sensors, over 5 dies, were

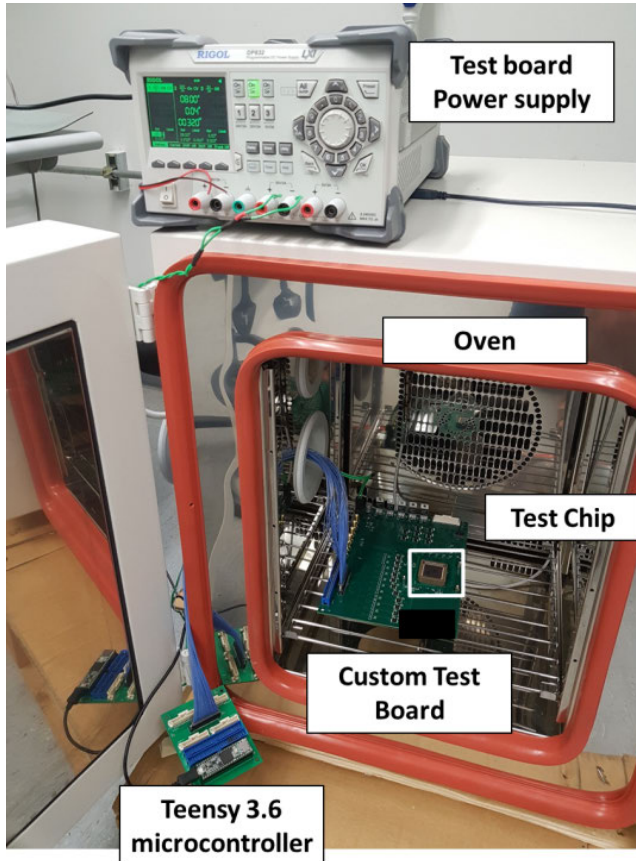


FIGURE 11. Experimental setup for the sensor measurement. The custom test board is in the oven, while the Teensy microcontroller sends instructions to the board. A PT100 probe is embedded in the heat sink on the board(not shown).

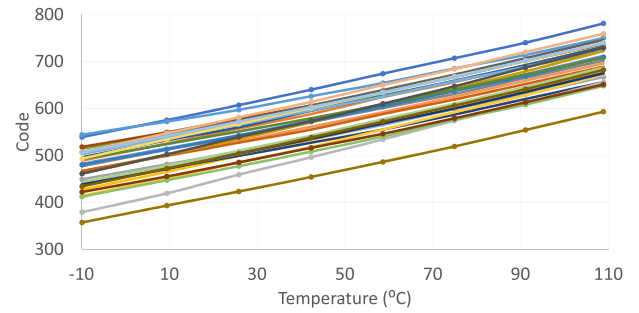


FIGURE 13. Measured sensor code vs temperature for the slow oscillator for 35 sensors.

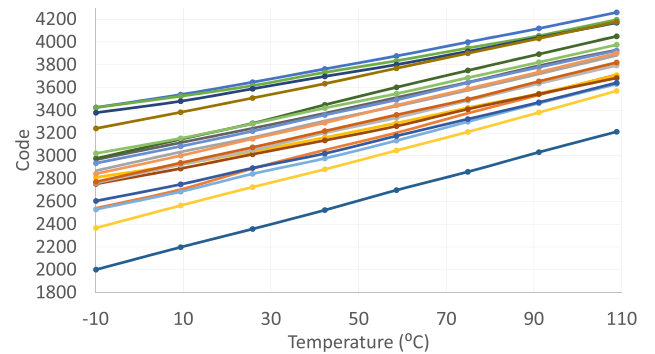


FIGURE 14. Measured sensor code vs temperature for the fast oscillator for 35 sensors.

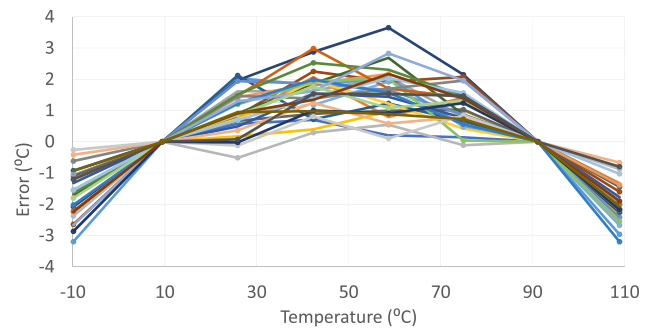


FIGURE 15. Measured error vs. temperature for 2 pt Calibration For the slow oscillator.

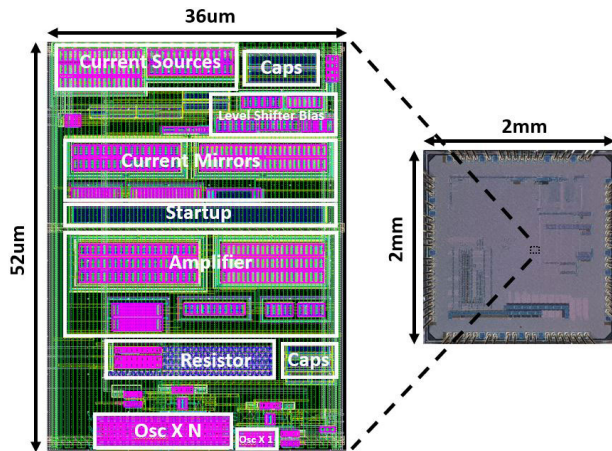


FIGURE 12. Sensor layout visualized over silicon die micrograph.

measured in order to evaluate the statistical performance of the sensor. A die photo and the sensor’s layout are shown in Fig. 12.

The measured output codes of the counters vs. temperature are shown in Fig. 13 and Fig. 14 for the slow and fast codes

respectively. Both frequencies behave approximately linearly as a function of temperature, similar to the simulated results. The fast oscillator was found to be more sensitive to noise and variation and thus less accurate due to the smaller overall oscillator size and low capacitive load on the oscillator nodes. The results hereafter are thus based upon the slow oscillator’s performance.

Fig. 15 shows the measured sensor error vs. temperature for 2-point calibration for 35 sensors. The curvature of the sensor is apparent from this figure. This curvature can be nulled by applying a 2nd order polynomial fix as is done in the prior-art [9], [10]. In a production environment, the curvature would be measured across several hundred units and then applied to the rest of the lot (millions). Applying the 2nd order

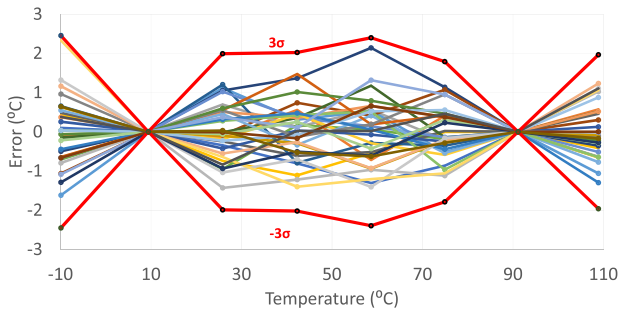
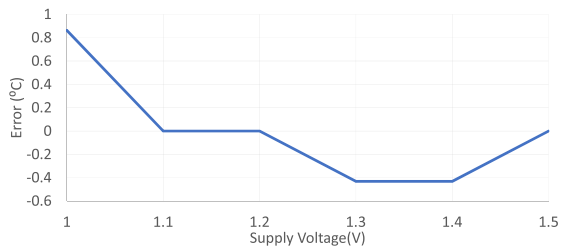
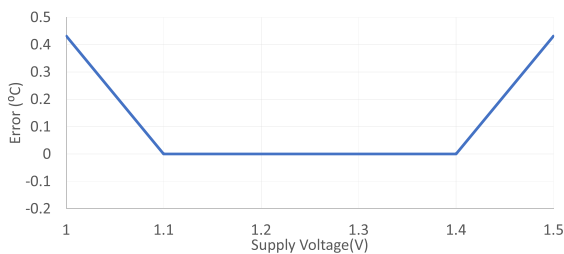


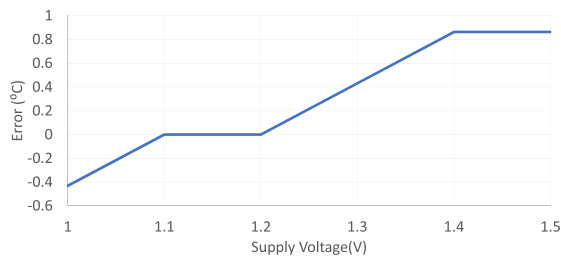
FIGURE 16. Measured error vs. temperature with 2 pt. calibration for the slow oscillator with systematic curvature correction.



(a)



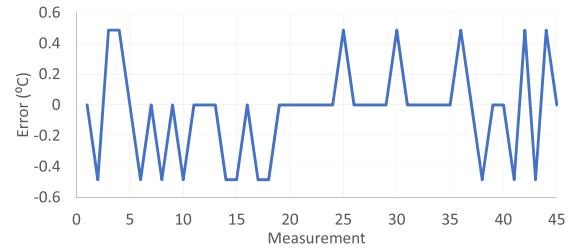
(b)



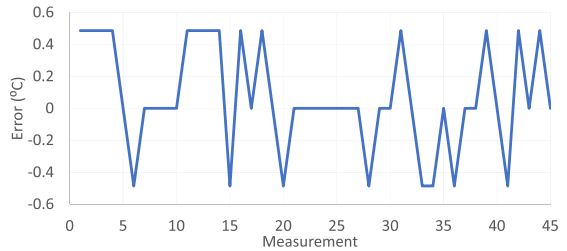
(c)

FIGURE 17. Measured error vs supply voltage at (a) -10°C , (b) 42°C , (c) 110°C .

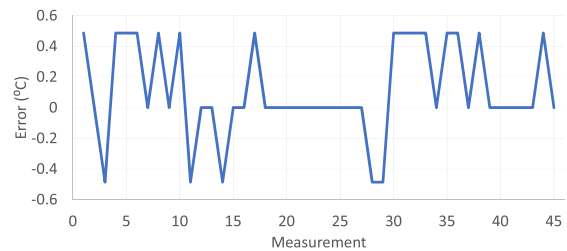
curvature correction yields Fig. 16, which exhibits approximately a 50% reduction in error at the center of the spectrum. The measured 3-sigma error is $\pm 2.5^{\circ}\text{C}$ over the range, which is within the required specification for CPUs [2]. Note, that the calibration points used are typical for products [2]. Usually the lower temperature would be used for wafer level testing, while the higher temperature would be the maximum temperature of operation, at which point the sensor would indicate that the chip should throttle.



(a)



(b)



(c)

FIGURE 18. Measured error for repeated measurements at (a) -10°C , (b) 42°C , (c) 110°C .

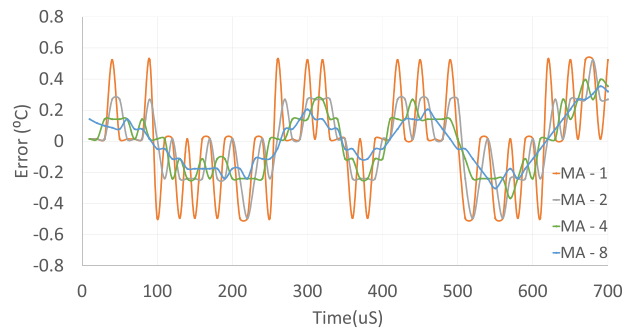


FIGURE 19. Measured error vs. moving average (MA) for consecutive measurements.

The circuits resilience to changes in the supply voltage is shown in Fig. 17. The measured sensor code error relative to the nominal voltage (1.2V) is plotted for several temperatures. The worst case PSR error is $2.4^{\circ}\text{C}/\text{V}$. By measuring a sensor continuously over time, the noise behavior of a typical sensor can be evaluated. This is shown in Fig. 18 for a repeated measurements at different temperatures. It is observed that the sensor toggles between ± 1 LSB, which is 400mK in this case. In products it is possible to take a fast initial measurement, and then improve the resolution by

TABLE 1. Comparison to the prior art.

Reference		1	2	16	15	14	17	11	12,13	10	9
Source/Year	This Work	JSSC 13'	JSSC 15'	ESSCIRC 18'	JSSC 17'	SSCL 18'	ISSCC 18'	JSSC-16'	JSSC 12'	SSCL 19'	JSSC 18'
Technology [nm]	65	22	14	65	40	28- FDSOI	22	65	90	65	65
Type	MOS	PNP	PNP	PNP	TD	MOS	PNP+MOS	MOS	MOS	Res	Res
Range ($^{\circ}\text{C}$)	-10/100	-10/100	0/100	-10/110	-40/125	-5/85	-30/120	0/100	20/130	-50/105	-40/110
Total Area (μm^2)	1850	6100	8700	3000	1650	1000 (11,482 ^b)	4300	4000	3750	5800(6700 ^c)	10,000
Total Area (F^2)	4.4E+05	1.3E+07	4.4E+07	7.1E+05	1.0E+06	1.3E+06	8.9E+06	9.5E+05	4.6E+05	1.6E+06	2.4E+06
Sensing Element Area (μm^2)	160	1040	1200	510	240	225	-	-	-	1720	-
Supply Voltage (V)	1.2	1.35	1.35	1.3	1.05	0.9	1	1	1.3	0.85	1.1
Current [μA]	78	1030	822	86	2500	62 (684 ^b)	50	154	700.0	38.2	11.6
Conversion time [ms]	0.01	0.7	0.02	4.1	1	0.036	0.03	0.022	0.1	1	0.08
Energy (nJ/conv.)	0.94	973	22	458	2625	2 (22)	1.5	3.388	91	32.5	0.9
Relative Inaccuracy (%) [*]	3.25 ^a	2.7	3.3	2.2 ^a	1.7 ^a	3.4 ^a	1.4 ^a	1.8 ^a	1.1	0.21 ^a	1.4
RMS Resolution [mK]	320	250	500	130	360	760	580	300	200	2.8	150
Trim	2	2	2	2	0	1	1	2	2	2	2
Resolution FOM [$\text{nJ}\cdot\text{K}^2$]	0.096	61	6.1	7.7	320	1.2	0.54	0.3	3.6	2.50E-04	0.02
Power Supply Rejection ($^{\circ}\text{C}/\text{V}$)	2.4			3-14		1.9	~ 1.9	34	-	0.22	3

^{*} Relative Inaccuracy defined as peak-to-peak-inaccuracy * 100/Range [7]

^{**} Only sensors which have a complete sensor (sensing element + readout) were included. Sensors requiring external elements such as a precision references were not placed in this table.

^a - These sensors require linearization or curvature correction to obtain the relative inaccuracy quoted

^b [14] has an area of 11,482 μm^2 and current of 684 μA , including readout + 11 sensing elements. The area of 1000 μm^2 and current of 62 μA is achieved by averaging the overall area/current by the amount of sensing elements.

^c - Area of 6700 includes the estimated area of the bias circuit and counter

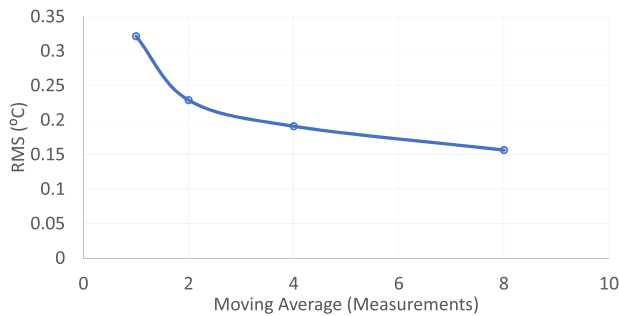


FIGURE 20. RMS error vs moving average.

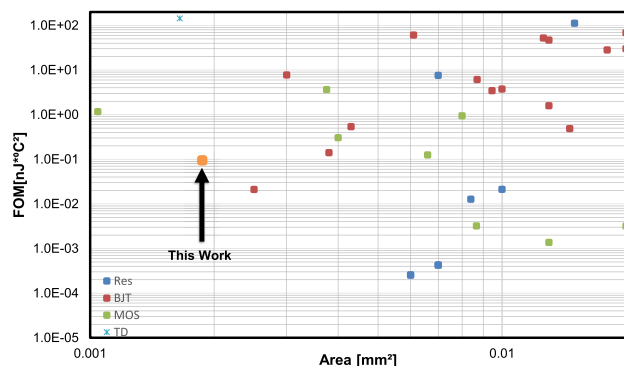


FIGURE 21. Area vs FOM compared to the prior-art.

taking a moving average (MA) of subsequent measurements [2]. This is shown in Fig. 19 for moving averages of 2,4, and 8 measurements. Fig. 20 exhibits the RMS resolution of the sensor vs. MA, which shows that the error is reduced for higher MA.

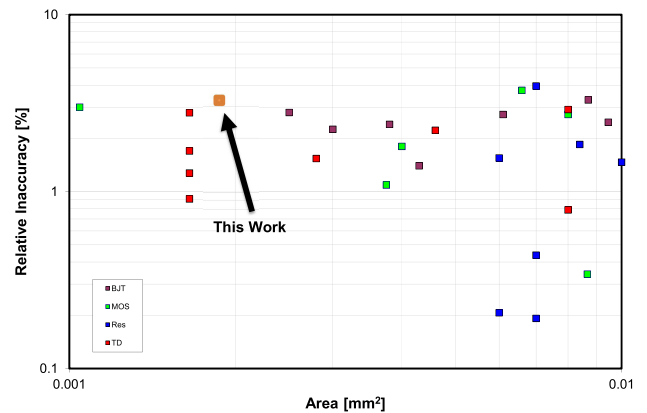


FIGURE 22. Area vs Relative Inaccuracy compared to the prior-art.

IV. DISCUSSION AND CONCLUSIONS

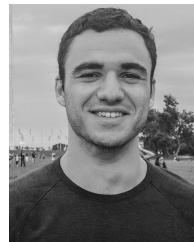
Figures 21 and 22 show graphical comparisons of the sensor's resolution FOM and accuracy vs. area respectively (borrowed with permission from [7]). A comparison of the sensor's performance to recent small sensors is presented in Table 1. The sensor is compared to small sensors which can meet the CPU specification ($< 0.02\text{mm}^2$ [2]). This sensor is one of the smallest and fastest sensors reported. Its accuracy and resolution are comparable to most other small sensors and meet the CPU specification. The conversion energy is one of the lowest amongst the small sensors. It is also possible to use the ring-oscillator and level shifter as remote sensing elements by extending two analog wires from the rest of the readout circuit. Since the hot-spot areas are very congested, this enables the readout circuit to be positioned at a more remote location, with only the sensing element at the hot-

spot. Among the sensors shown in Table 1, this sensor has the smallest such sensing element. The achieved resolution FOM of the sensor is among the best for sensors smaller than $5000\mu\text{m}^2$, since the conversion time is very fast ($10\mu\text{s}$). This conversion time may enable a quick temperature reading when the chip exits deep sleep states. It can also be used to duty-cycle the temperature readings to save power. We are planning to add offset cancellation circuitry to this design in future revisions. This could facilitate higher accuracy while potentially saving area.

A sensor is shown which uses ring-oscillators instead of BJT's in a bandgap-like circuit structure. A nearly linear temperature dependent frequency is observed. The sensor benefits from the compact area, low power, and high-resolution characteristics of a digital circuit. It also exhibits relative process independence and power supply rejection of an analog circuit. The sensor excels both in size, $1850\mu\text{m}^2$, and conversion time, $10\mu\text{s}$. It achieves a resolution FOM of 96pJ-K^2 , which is highly competitive among the compact sensors. These features make the sensor attractive for dense thermal monitoring in IC products.

REFERENCES

- [1] J. S. Shor and K. Luria, "Miniaturized BJT-based thermal sensor for microprocessors in 32- and 22-nm technologies," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2860–2867, Nov. 2013.
- [2] T. Oshita, J. Shor, D. E. Duarte, A. Kornfeld, and D. Zilberman, "Compact BJT-based thermal sensor for processor applications in a 14 nm tri-gate CMOS process," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 799–807, Mar. 2015.
- [3] D. E. Duarte, G. Geannopoulos, U. Mughal, K. L. Wong, and G. Taylor, "Temperature sensor design in a high volume manufacturing 65nm CMOS digital process," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, 2007, pp. 221–224.
- [4] D. Brooks and M. Martonosi, "Dynamic thermal management for high-performance microprocessors," in *Proc. HPCA 7th Int. Symp. High-Perform. Comput. Archit.*, Nuevo Leon, Mexico, Jan. 2001, pp. 171–182.
- [5] E. Rotem, A. Naveh, A. Ananthakrishnan, E. Weissmann, and D. Rajwan, "Power-management architecture of the intel microarchitecture code-named sandy bridge," *IEEE Micro*, vol. 32, no. 2, pp. 20–27, Mar. 2012.
- [6] E. Rotem, R. Ginosar, A. Mendelson, and U. C. Weiser, "Power and thermal constraints of modern system-on-a-chip computer," in *Proc. 19th Int. Workshop Thermal Investigations ICs Syst. (THERMINIC)*, Berlin, Germany, Sep. 2013, pp. 141–146.
- [7] K. A. A. Makinwa. *Temperature Sensor Performance Survey*. Accessed: Feb. 2020. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls
- [8] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001, pp. 377–404.
- [9] A. Mordakhay and J. Shor, "Miniaturized, 0.01mm^2 , resistor-based thermal sensor with an energy consumption of 0.9 nJ and a conversion time of $80\mu\text{s}$ for processor applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2958–2969, Oct. 2018.
- [10] Y. Lee, W. Choi, T. Kim, S. Song, K. A. A. Makinwa, and Y. Chae, "A $5800\text{-}\mu\text{m}^2$ resistor-based temperature sensor with a one-point trimmed inaccuracy of $\pm 1.2^\circ\text{C}$ (3σ) from -50°C to 105°C in 65-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 67–70, Sep. 2019.
- [11] T. Anand, K. A. A. Makinwa, and P. K. Hanumolu, "A VCO based highly digital temperature sensor with $0.034^\circ\text{C}/\text{mV}$ supply sensitivity," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2651–2663, Nov. 2016.
- [12] K. Luria and J. Shor, "Miniaturized CMOS thermal sensor array for temperature gradient measurement in microprocessors," in *Proc. IEEE Int. Symp. Circuits Syst.*, Paris, France, May/June. 2010, pp. 1855–1858.
- [13] M. Yuffe, M. Mehalel, E. Knoll, J. Shor, T. Kurts, E. Altschuler, E. Fayneh, K. Luria, and M. Zelikson, "A fully integrated multi-CPU, processor graphics, and memory controller 32-nm processor," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 194–205, Jan. 2012.
- [14] M. Cochet, B. Keller, S. Clerc, F. Abouzeid, A. Cathelin, J.-L. Autran, P. Roche, and B. Nikolic, "A $225\mu\text{m}^2$ probe single-point calibration digital temperature sensor using body-bias adjustment in 28 nm FD-SOI CMOS," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 1, pp. 14–17, Jan. 2018.
- [15] U. Sonmez, F. Sebastiano, and K. A. A. Makinwa, "Compact thermal-diffusivity-based temperature sensors in 40-nm CMOS for SoC thermal monitoring," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 834–843, Mar. 2017.
- [16] O. Bass and J. Shor, "Ultra-miniature 0.003mm^2 PNP-based thermal sensor for CPU thermal monitoring," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2018, pp. 334–337.
- [17] C.-Y. Lu, S. Ravikumar, A. D. Sali, M. Eberlein, and H.-J. Lee, "An 8b subthreshold hybrid thermal sensor with $\pm 1.07^\circ\text{C}$ inaccuracy and single-element remote-sensing technique in 22nm FinFET," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2018, pp. 318–320.



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