IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 31, 2020, accepted April 17, 2020, date of publication May 11, 2020, date of current version May 27, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2991742

Practical Analytical Model of Adjustable Speed Drive for Tolerance Ability Evaluation of Transient Low Voltage Disturbance

Z. XU, Qianwen Guo, L. LUAN, AND K. ZHOU
Electric Power Test Research Institute, Guangzhou Power Supply Bureau Company, Ltd., Guangzhou 510410, China
Corresponding author: Qianwen Guo (996354022@qq.com)

This work was supported by the Science and Technology Project of China Southern Power Grid Company, Ltd., under Grant GZHKJXM20170141.

ABSTRACT The failure of adjustable speed drive (ASD), which is sensitive to transient low voltage disturbance such as voltage sag and short duration interruption, will bring considerable loss to industrial users. Evaluating the disturbance tolerance ability of adjustable speed drives is the key to improve its tolerance. The voltage tolerance curve (VTC) is a tool to quantify the tolerance of voltage sag sensitive equipment including adjustable speed drives. However, the traditional test strategy for obtaining this curve is time-consuming and may introduce errors caused by the performance deterioration of the tested equipment. This paper proposes an analytical model of adjustable speed drive based on its response mechanism analysis to voltage sags. The model constructs a group of practical formulas for calculating the knee point of the voltage tolerance curve. The knee point can be used to quickly estimate the contour of the curve. This model can help engineers to conduct a first-cut assessment of the sag tolerance for drives to select equipment or design planning. Experimental tests are carried out to verify the effectiveness of the proposed method. Moreover, an application of the results is presented to improve the traditional test strategy.

INDEX TERMS Voltage sag, short-duration interruption, adjustable speed drive, voltage tolerance curve, analytical model.

I. INTRODUCTION

Adjustable speed drives (ASD) are widely used in industrial processes [1]. Transient low voltage disturbances, such as voltage sags and short duration interruptions, have more significant impacts on high-end manufacturing users [2]–[7]. ASD affected by this kind of disturbance will force the industrial process to be interrupted and cause huge loss to users [8]–[10]. Therefore, it is of practical significance to adopt a reasonable method to evaluate the low voltage tolerance ability of ASD to assist the design and selection of equipment.

The voltage tolerance curve (VTC), which is derived from the computer and information industry immune curves CBEMA and ITIC, is a common tool to quantify the transient low-voltage disturbance tolerance of sensitive equipment [11]. VTC is often obtained by experimental tests [12]–[15]. Thus, IEEE has recommended some standard test methods, including the top-down, the left-right, and the box-in test strategies [16]. These methods can meet the basic requirements for obtaining the VTC of different kinds of sensitive equipment but lack pertinence, additionally, their testing efficiency is insufficient for certain types of equipment. The binary test method improves the efficiency of testing in small step sizes [17]. However, it is still a tentative test strategy. For ASDs, various test conditions such as sag types and load levels need to be considered, and the interval among each test is longer than other kinds of voltage-sensitive equipment, such as AC contactor (ACC), programmable logical controller (PLC), and personal computer (PC). These factors lead to a long test cycle, causing inconvenient evaluations and vulnerable equipment. Therefore, more convenient methods need to be proposed for evaluating the VTC of ASD.

For ACC and PLC, some researchers have used the working principle of equipment to guide VTC testing [14], [15], [18]. In [15], based on the analytical model of ACC,

The associate editor coordinating the review of this manuscript and approving it for publication was Jason Gu.

the researchers gave a method to quickly estimate the contour of VTC, which can effectively guide the testing work of VTC. Thus, studying the response mechanism of ASD to transient low-voltage disturbances can also be helpful to improve the test strategy of VTC. The influence of different control methods on ASD sag tolerance is discussed in [19]. The research results show that the common control strategies have a limited impact on equipment tolerance, which provides a reference for the factors that need to be considered in the model construction. In [20]–[22], the triggering mechanism of low voltage and overcurrent protection of ASD affected by voltage sag is studied, but it is not effectively combined with the VTC test scheme to further form a practical mathematical model. Thus, the response mechanism of ASD to voltage sags needs to be further characterized and used to guide the assessment.

To solve the above problems, this paper proposes a method to calculate the knee point of VTC for improving the efficiency of the ASD test strategy. The discharge time of the ASD capacitor under typical load conditions is obtained through testing. Based on the working principle of the rectifier, the mechanism of device trigger voltage and over current protection under different sag types are discussed. Furthermore, a practical model for judging the contour of VTC under each test condition is derived. Based on the working principle of ASD, the trigger conditions of protection under different voltage sag types are discussed. Furthermore, another practical model for calculating VTC knee points under each test condition is derived to complete the estimation of VTC contours. The effectiveness of the proposed scheme was verified by experiments. Moreover, the application of the results obtained by the method in optimizing the traditional VTC test scheme is described.

II. TRADITIONAL METHOD AND PROBLEMS

As ASDs are three-phase equipment, the influence of the voltage sag type needs to be considered. To facilitate the test, the Type I, Type II.A2, and Type III voltage sags in IEEE 1668 are usually used as test conditions, as shown in Fig. 13 in Appendix D. For each voltage sag type, there is a corresponding group of VTC under different working conditions to characterize ASD tolerance. Thus, a complete characterization of the voltage sag tolerance capability of an ASD requires multiple tests.

For each case mentioned above, VTC is obtained by the test strategies recommended by [16]. Fig. 1 illustrate the strategies mentioned in [16]. The details of these strategies are given in Appendix E.

As mentioned above, these test strategies are tentative, which contacts a lot of unnecessary test steps. In fact, the shape of VTC for ASD is approximately rectangular. Thus, to find the knee point of VTC as shown in Fig. 1 can

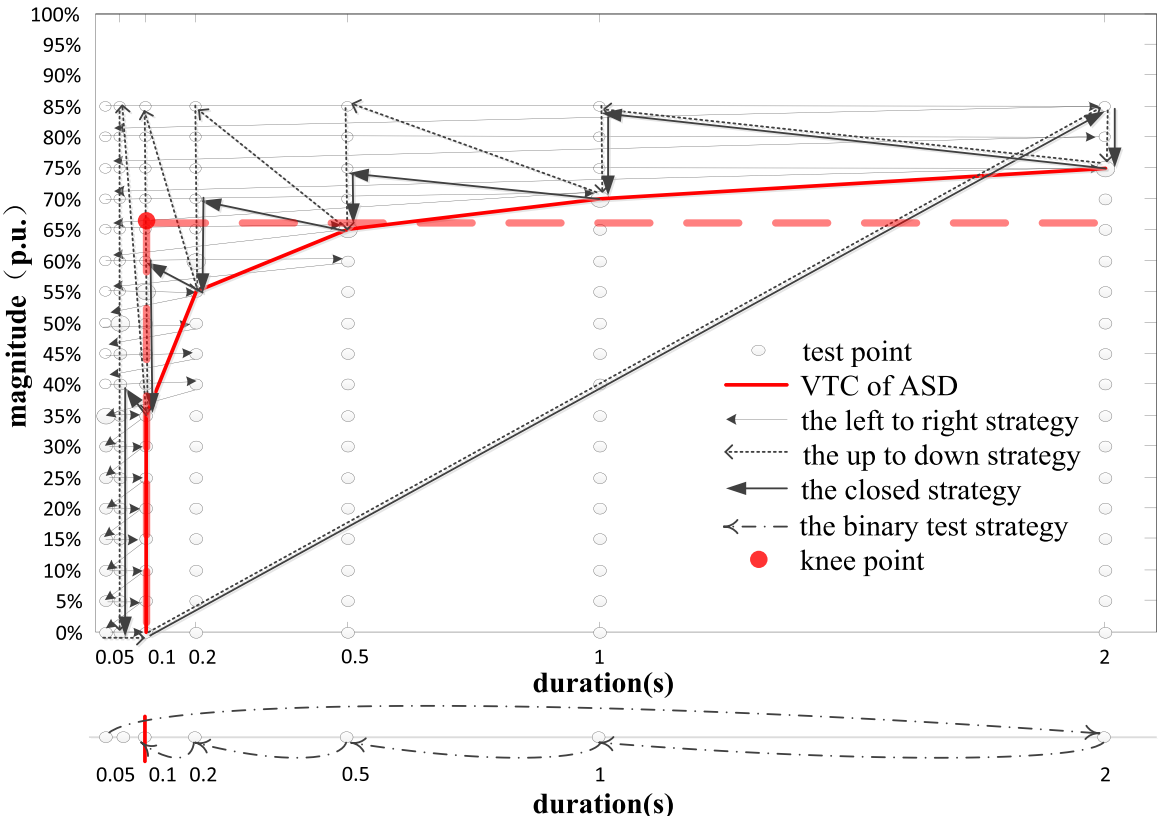


FIGURE 1. Schematic diagram of traditional test strategies.

obtain the contours of it, which can be used as a basis for first-cut assessment. A flow chart is given in the appendix to better illustrate the work of this paper.

III. BASIC WORKING PRINCIPLE OF ASD AND THE MIAN IDEA OF THE PROPOSED METHOD

This section introduces the basic working principle of ASD and further points out the idea to solve the problem mentioned above.

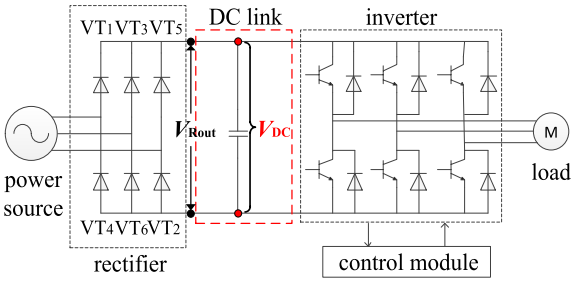


FIGURE 2. Structure of ASD.

As shown in Fig. 2, ASD consists of a rectifier, DC-link, and inverter. The orderly operation of each diode of the rectifier and transistor of the inverter makes the energy dissipation of DC-link balanced and ensures the normal operation of ASD. The mechanism of ASD fault caused by voltage sag is that it breaks the conduction sequence of diodes and makes DC-link energy imbalance. This will trigger the low voltage and other protections of DC-link causing transistor locking.

For example, when ASD suffering a symmetrical low voltage event, the diodes of the rectifier will fail to conduct, making the output voltage of rectifier V_{Rout}, as shown in Fig. 2, lower than the voltage of the capacitor/DC link V_{DC}. Thus, the capacitor will continue to discharge, causing V_{DC} to drop continuously. When V_{DC} is below the protection set value V_{DCth}, ASD will trip. For an asymmetrical low voltage event, the conduction of the rectifier diode is more complicated. The waveform of V_{Rout} is no longer approximated by a DC voltage. Thus, the relationship between the protection set value and the input voltage of ASD is difficult to characterize.

For calculating the VTC knee point of ASD, describing the relationship between the protection set value and the input voltage of ASD mathematically and properly is critical. This paper considers the two most common protection types, low voltage protection and over current protection. Both protection set values can be converted to low voltage thresholds. To simplify the analysis of asymmetric sags, this paper selects the typical voltage sags of Type I, Type II.2A, and Type III that are commonly used in VTC testing. This also makes the model easy to verify and used to modify the test strategy to address the problem mentioned above.

The following will first give the entire analysis model to establish the overall concept. Later, detailed analysis and derivation will be given out.

IV. THE PROPOSED ANALYTICAL MODEL

This section introduces the analytical model to calculate the knee point under each type of voltage sag. The model consists of several practice formulas, which can be used to assess directly. Only the discharge duration $T_{3\mathrm{th}}$ of the capacitor needs to be tested by using a short duration interruption generated by the programmable power source under different typical load power P_{L}.

A. SYMMETRICAL VOLTAGE SAG-TYPE III

1) The critical duration (the duration from the occurrence of the sag to the protection action) of the low voltage protection is $T_{3\mathrm{th}}$, which is the horizontal coordinates of the knee point.

$T_{3\mathrm{th}}$ is the discharge time of the DC-link capacitor, which is the key factor to measure the low voltage tolerance ability of ASD. Considering the constant power load, it can be determined by (10).

$$T_{3\mathrm{th}} = \frac{C}{2P_{\mathrm{L}}}(V_{\mathrm{DCn}}^2 - V_{\mathrm{DCth}}^2) \tag{1}$$

It can be seen that for a certain low voltage protection setting value of certain equipment, the discharge time is only determined by the load power P_{L}. Thus, $T_{3\mathrm{th}}$ can be obtained by experimental tests under typical load power.

2) Using (2) to calculate the critical voltage $V_{3\mathrm{th-V}}$ of the low voltage protection neglecting the overlapping phenomenon.

$$V_{3\text{th-V}} = \frac{V_{\mathrm{DCth}}}{2.34} \tag{2}$$

where V_{DCth} is the setting value of DC-link's low voltage protection.

3) The critical voltage $V_{3\mathrm{th-I}}$ of the overcurrent protection can be calculated as follows

$$V_{3\text{th-I}} = \frac{V_{\mathrm{DCn}} - \Delta i_{\max}\sqrt{L/C}}{2.34} \tag{3}$$

where $\Delta i_{\max} = I_{\mathrm{DCth}} - I_{\mathrm{DCn}}$, I_{DCth} is the overcurrent protection threshold, I_{DCn} is the current of DC-link underrated condition, V_{DCn} is the voltage of DC link underrated condition, L is the inductance value of ASD, and C is the capacitance of ASD. The derivation of equation (3) can be found in Appendix B.

Thus, the critical voltage of this case is $V_{3\mathrm{th}} = \max(V_{3\mathrm{th-V}}, V_{3\mathrm{th-I}})$, which is the vertical coordinates of the knee point.

B. SINGLE PHASE VOLTAGE SAG-TYPE I

Without considering the lack of phase protection, ASD is usually immune to single-phase voltage sag. Thus, here just giving formula to quickly determine whether ASD will fail.

Using (4) to calculate the feature time T_x

$$T_x = T_{\mathrm{pul}}(0.5 + \frac{1}{\pi}\arcsin\frac{V_{\mathrm{DCth}}}{V_{\mathrm{LP}}}) \tag{4}$$

where T_{pul} is the cycle of the line-to-line voltage waveform, which is 10 ms in a 50 Hz power frequency system, V_{LP} is the peak value of the line to line voltage.

As explained in Section V-B, if (5) is true, ASD is immune to voltage sag. Otherwise, further test needs to be conducted to obtain VTC.

$$T_{3th} > T_x \tag{5}$$

C. TWO-PHASE VOLTAGE SAG-TYPE II-2A

1) The critical duration, in this case, can also be evaluated by T_{3th}.

2) The minimum magnitude of two-phase voltage sags that ASD can pass-through be calculated by (6).

$$V_{2th\text{-}V} = \frac{V_{sLP} - |V_{nP}\sin(\alpha + 2\pi/3)|}{V_{nP}\sin\alpha} \cdot V_{nP}, \quad \alpha \in [\frac{2\pi}{3}, \frac{5\pi}{6}] \tag{6}$$

where α is a calculate angle, the details will be given in Section V-C, V_{sLP} is line to line voltage which contains a non sag phase (normal phase), V_{nP} is the nominal value of the phase voltage. α can be obtained by solving (7), and V_{sLP} can be obtained by solving (8) and (9). The details can be found in Section V-C.

$$\frac{V_n\sqrt{6} - V_{sLP}}{V_n\sqrt{6} - V_{LP}\sin 5\pi/6} = \frac{\alpha - 2\pi/3}{5\pi/6 - 2\pi/3} \tag{7}$$

$$V_{sLP} = \frac{\sqrt{6}}{2.34}\sqrt{\frac{2P_L\Delta T}{C} + V_{DCth}^2} \tag{8}$$

$$\begin{cases} \theta = \dfrac{2\pi}{3} \cdot \dfrac{V_{DCth}}{V_{DCn}} \\ \Delta T = K(1 - \dfrac{\theta}{\pi})T_{pul} \end{cases} \tag{9}$$

where V_n is the nominal phase voltage, K is the time error correction coefficient, which is used for flexible correction of model error, generally 0.8 - 0.9.

3) The critical voltage V_{2th-I} decided by the overcurrent protection can get in a similar way of V_{2th-V}, but V_{sLP} needs to be calculated by (10).

$$V_{sLP} = \frac{V_{DCn} - \Delta i_{max}\sqrt{L/C}}{2.34} \cdot \sqrt{6} \tag{10}$$

The critical voltage under this case is $V_{2th} = \max(V_{2th-V}, V_{2th-I})$.

V. DEVELOPMENT OF THE MODEL

This section gives a detailed analysis and derivation process of the above models.

A. SYMMETRICAL VOLTAGE SAG-TYPE III

For the case of symmetrical voltage sag, the rectifier still keeps working in a three-phase operation mode. Thus, the output ripple of DC-link is relatively small and can be ignored. This means the critical voltage, in this case, can be obtained by (2). To reduce the interference of uncertain factors in test results and obtain a proper value of V_{DCth}, the following steps can be carried out. Substitute nameplate parameter C, P_L, V_{DCn} and test parameter T_{3th} into (1) to calculate the estimated value of V_{DCth}. The mean value of the estimated value and the nameplate value of V_{DCth} is taken as the correction value of this parameter.

B. SINGLE PHASE VOLTAGE SAG-TYPE I

Assume that the sag occurs in phase A, the magnitude of the line voltage V_{AB} and V_{CA} will be decreased, as shown in Fig. 3. When V_{AB} and V_{CA} are below the voltage of DC-link V_{DC}, according to Fig. 2, VT1 and VT4 would be closed and the rectifier would work in single-phase mode. The waveform of the DC link is shown in Fig. 3. Thus, the key rule for judging whether ASD can pass through the single-phase sags is as follow:

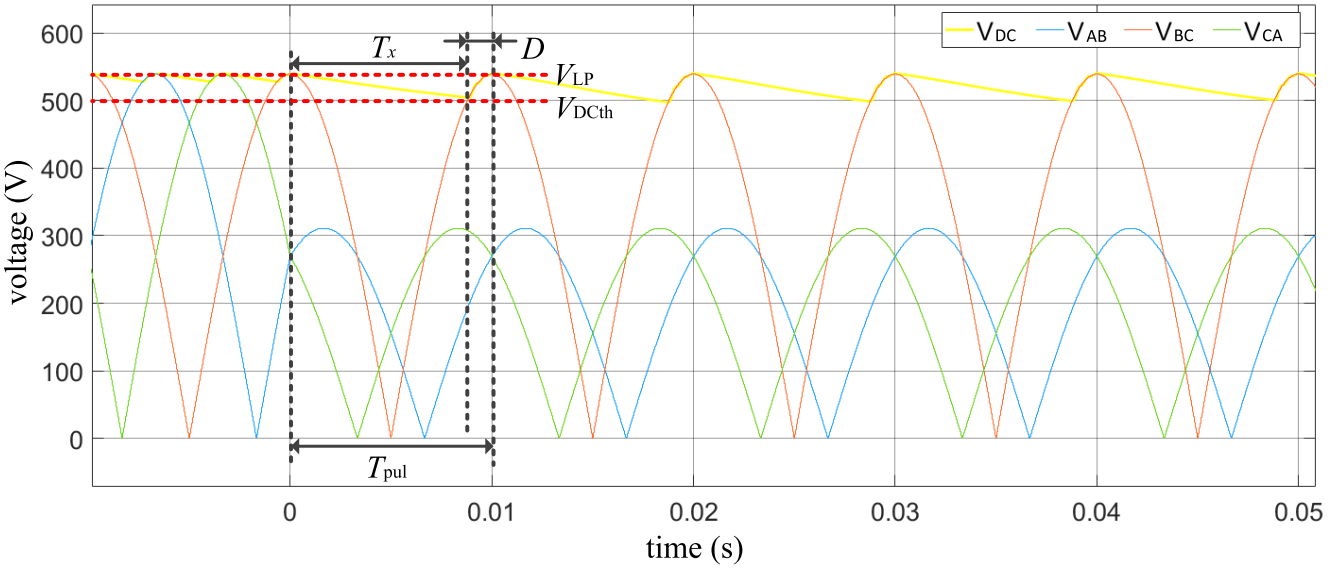


FIGURE 3. DC voltage waveform under single-phase sag.

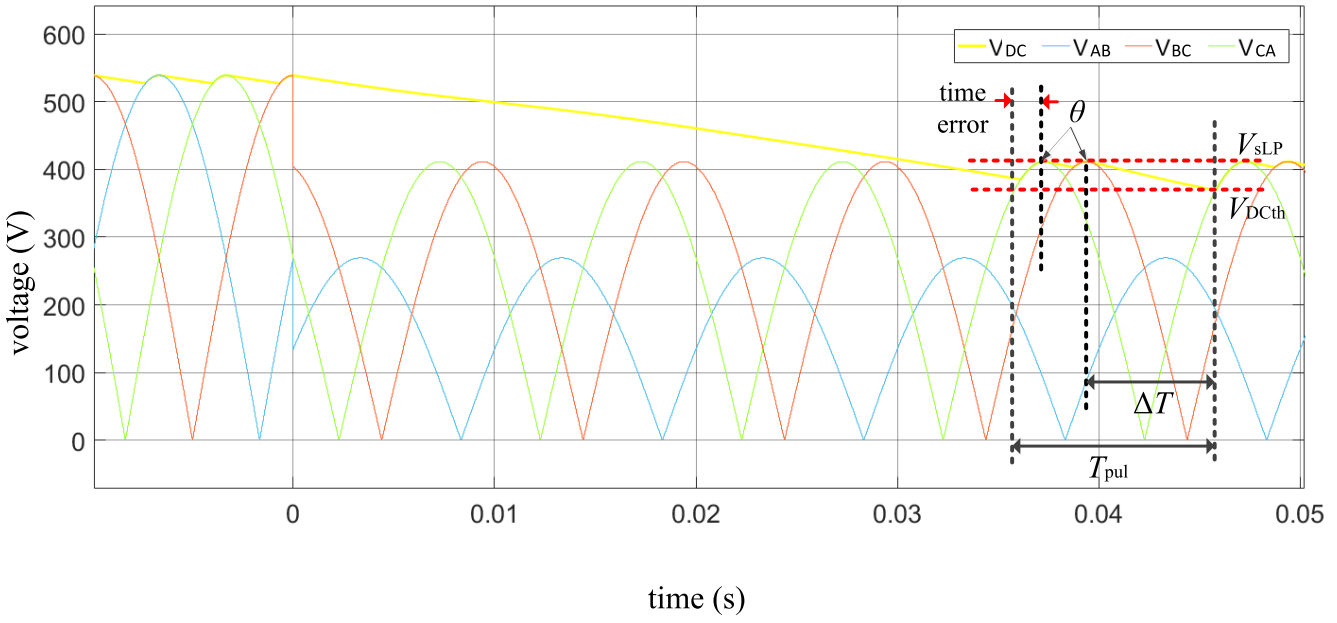


FIGURE 4. DC voltage waveform under two-phase sag.

If $V_{DC} < V_{DCth}$ happens during the discharge period between the peak of V_{BC}, ASD would be failed.

In a cycle of the waveform pulse of V_{BC}, if the discharge time of the capacitor without protection is T_x and the charging time is D, the following expression can be obtained based on the geometric analysis.

$$\phi = \arcsin \frac{V_{DCmin}}{V_{LP}} \tag{11}$$

$$D = \frac{T_{pul}}{2} - \frac{\phi}{\pi} T_{pul} \tag{12}$$

$$T_x = T_{pul} - D \tag{13}$$

Considering $V_{DCmin} = V_{DCth}$, the expression of T_x, which is (4), under the critical failed condition can be obtained by (11)-(13). According to Fig. 3, if $T_{3th} > T_x$, then $V_{DCmin} > V_{DCth}$ is also established, which means that the DC voltage cannot fall below the protection threshold within the discharge time. Thus, ASD can pass through the sag.

As the rectifier works in single-phase mode in this case, there is no significant overcurrent phenomenon at the voltage recovery stage. For this operation mode, the overcurrent protection value is mainly set from the perspective of heating. The setting time of the protection is long, which is beyond the definition of voltage sag. Therefore, the single-phase sag will not trigger the overcurrent protection.

C. TWO-PHASE VOLTAGE SAG-TYPE II-2A

Assuming that phase A, B occurs voltage sags, the magnitude of all line voltage is decreased, where the magnitude of V_{AB} is lowest among them. As shown in Fig. 4, the capacitor charging is mainly completed by V_{CA} and V_{CB}. As the voltage magnitude decreases, the phase difference of the two pulses, which are the waveform of V_{CA} and V_{CB} in a cycle, decreases, and the proportion of the charging period in a cycle decreases gradually. Thus, in the analysis of ASDs' tolerance time (the critical duration), the charging period can be ignored, and T_{3th} can be regarded as the critical duration.

Fig.4 shows the waveform relationship at the critical stage of ASD failure. The voltage ripple of the DC side under two-phase sag is large, which needs to be concerned. In a cycle T_{pul} of the ripple, V_{sLP} is a key parameter to characterize the ripple and it is also an intermediate quantity to obtain V_{2th-V} as shown in (6). Based on V_{DCth}, V_{sLP} can be obtained by solving (8), and the key is to obtain the time difference ΔT.

As the voltage sag magnitude (phase voltage) changing from 1 p.u. to 0 p.u., the phase angle difference θ between V_{BC} and V_{CA} will change from $2\pi/3$ to 0°. Thus, the value of θ corresponding to V_{DCth} can be solved by the first expression of (9). Based on the geometric relationship in Fig. 4, ΔT can be obtained by the second expression of (9), where the coefficient K is used to correct the time error in the model.

Another important intermediate quantity in (6) is α. Fig. 5 shows the voltage waveforms of one sag phase (eg. Phase A) and one non sag phase (eg. Phase C). This figure is used to illustrate the relationship between V_{sLP} and V_{2th-V}. The waveform of V_{CA} is the difference between V_A and V_C. Taking a cycle after zero crossings as an example, as the voltage magnitude of phase A V_A change from nominal to 0, the horizontal ordinate value of the peak of the line voltage V_{CA} changes from 120° to 150°. Thus, the calculated angle α can be obtained by (7).

The difference between the peak value of line voltage V_{sLP} and V_C at the corresponding angle is the value of V_A at that angle. The ratio of V_A to the rated value at the corresponding angle is the unit value of the sag, which is also the characteristic magnitude of a sag event, such as (6).

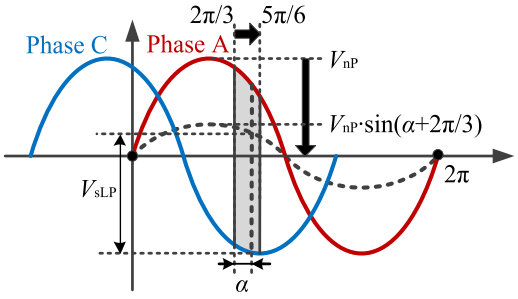


FIGURE 5. Schematic diagram of the relationship between line voltage and phase voltage.

Compared with V_{2th-V}, the main difference in obtaining V_{2th-I} lies in the way of determining V_{sLP}, such as (10). The process of deriving and analyzing the relationship between line voltage and phase voltage is similar to the above.

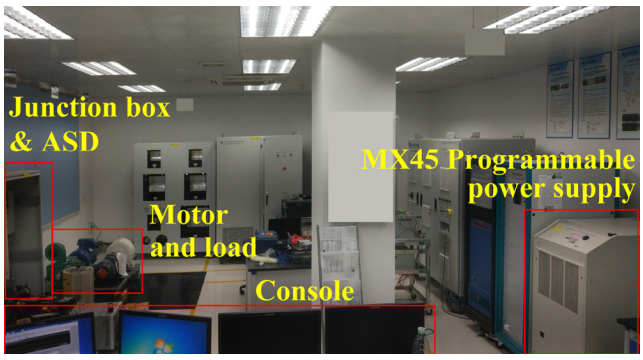
VI. LABORATORY TEST VERIFICATION

The laboratory test is lunched in this section to verify the effectiveness of the proposed method.

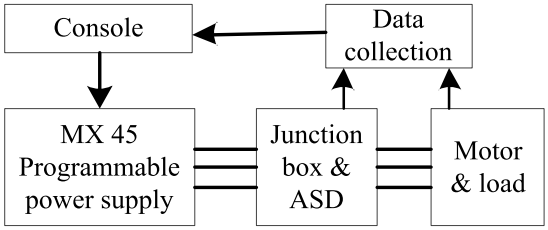
A. EXPERIMENTAL INFORMATION

1) TEST PLATFORM

The experimental platform and circuit diagram are shown in Fig. 6.



(a)



(b)

FIGURE 6. VTC test platform, (a) test environment, (b) test circuit.

The setting of related parameters is shown in Table 1.

2) TEST PROCEDURE

(1) Complete the construction of the test platform and check the wiring to ensure it can work normally.

(2) Set the parameter of ASD and start it. Then switch on the load according to preset requirements.

TABLE 1. Parameter settings.

Type of data	Parameter settings	
Load condition	load power (kW)	10
	load level (%)	80&100
Parameters of ASD	inductance (mH)	1
	capacitor (μF)	1600
	low voltage protection threshold V_{DCth} (V)	400
	overcurrent protection threshold I_{DCth} (A)	123
	rated phase voltage (V) and frequency (Hz)	220&50
Test condition	test sag type and setting method	As described in Section 2.
	step of the magnitude	$0.01V_n$
	step of the duration	1ms
	the longest duration	1s
	capacitor discharge time under various load conditions T_{3th} (ms)	100%=>12.619 80%=>14.326

(3) Select the voltage sag type and use the box-in strategy recommended by IEEE1668 for testing. The detail steps are as follows. First, set the magnitude of voltage to 0%. Then, increase the duration of the sag until ASD fails and record the duration. After that, set the duration to the maximum value and reduce the voltage magnitude in steps from the rated value to determine the critical tripping voltage of the ASD. Reduce the duration in steps and repeat the above operation until the ASD no longer trips. Note that the interval between each test should be about 10s to make the motor speed return to the normal state.

(4) After completing the test under all working conditions and all sag types, record and arrange the amplitude and duration information corresponding to the critical trip point of ASD obtained by the test, and draw the VTC by Matlab software.

B. RESULTS

1) SINGLE PHASE VOLTAGE SAG-TYPE I

According to the experimental results, the tested ASD will not fail at the most serious situation in Table 1. This means it can pass-through single-phase voltage sag without triggering protection.

For the analytical model, based on the parameters in Table 1, the feature time T_x can be calculated by (4), which is 7.663ms. Thus, T_x is smaller than both the critical duration T_{3th} = 12.619ms at the 100% load condition and T_{3th} = 14.326ms at the 80% load condition. Thus, it can pass through the single-phase voltage sag events, which is coincide with the experimental results.

2) TWO-PHASE VOLTAGE SAG-TYPE II-2A

VTCs obtained by the experiment and the analytical model is shown in Fig. 7. The coordinates of the knee points obtained by the analytical model under the 100% load level conditions and 80% load level conditions are (12.619ms, 0.783p.u.) and

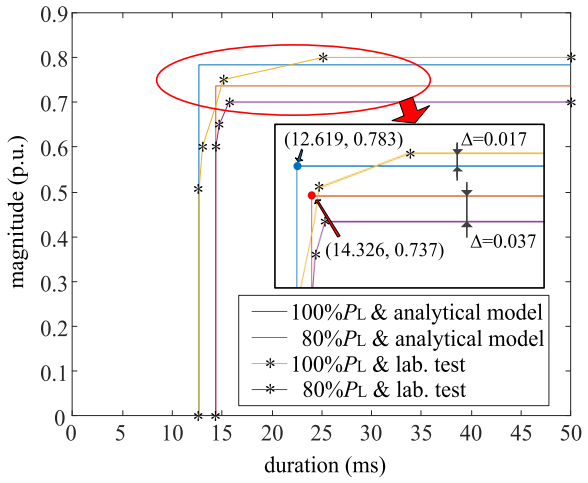


FIGURE 7. VTC obtained by the analytical model and experimental results under two-phase voltage sags (Type II.2A).

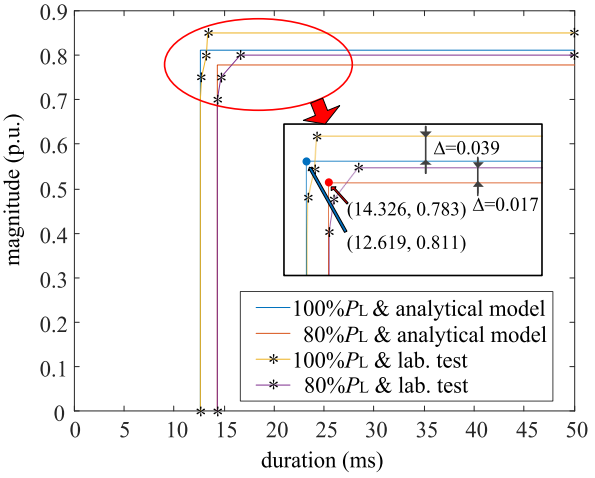


FIGURE 8. VTC obtained by the analytical model and experimental results under symmetrical voltage sags (Type III).

(14.326ms, 0.737p.u.) separately. The difference between the magnitude value of the curves horizontal section is 0.017 and 0.037 under the above two load conditions. The standard deviations based on the experimental results are 2.215% and 5.286%.

3) SYMMETRICAL VOLTAGE SAG-TYPE III

VTCs obtained under symmetrical voltage sags are shown in Fig. 8. The coordinates of the knee points obtained by the analytical model under the 100% load level conditions and 80% load level conditions are (12.619ms, 0.811p.u.) and (14.326ms, 0.783p.u.) separately. The difference between the magnitude value of the curves horizontal section is 0.039 and 0.017 under the above two load conditions. The standard deviations based on the experimental results are 4.588% and 2.125%.

Based on the results above, VTCs obtained by the analytical model are basically coincide with those obtained by experimental results. So, the proposed method is helpful to give a first-cut judgment for experts and engineers.

VII. APPLICATION

A. TEST STRATEGY

In addition to the above applications, the results can be further used to improve the laboratory test efficiency. Based on the knee point calculated by the model, VTC can be quickly obtained by test, as shown in Fig. 9.

The improved test strategy is as follows:

1) Step 1: Complete the experimental platform construction and parameter setting;

2) Step 2: Generate a voltage sag with the longest duration and the magnitude which has the same value of the knee points' ordinate. According to the preset magnitude step size, the value is set up and down, as shown in Fig. 9, to generate voltage sag until the equipment fails. This is the upper boundary of VTC;

3) Step 3: Set the magnitude value is 0 p.u. and the duration of the sag which has the same value of knee points' abscissa, and increase the duration until the tested equipment is failed. Record the position of this point. Increase the magnitude and repeat the above operation until the magnitude is equal to the upper boundary;

4) Connect all critical points to get VTC.

B. PERFORMANCE COMPARISON

The proposed scheme is compared with the commonly used box-in test scheme in IEEE 1668. The number of test steps required to obtain the above VTC underrated condition of ASD is shown in Table 2. VTC under Type II-2A, which can be found in Appendix C, has been chosen as an example to show the test results.

TABLE 2. Methods comparison.

	Number of steps		
	Type I	Type II-2A	Type III
Box-in test strategy	50	163	97
Proposed test strategy	1	40	52

According to Table 2, the proposed test strategy can reduce the number of test steps significantly, especially for the case of Type I. In this case, because a group of diodes is in a normal working state, the charge and discharge cycle of the capacitor can be maintained at original voltage magnitude. This allows despite the large ripple, it does not cause an overcurrent that will cause the device to trip when the voltage is restored. Therefore, it is only necessary to consider T_{3th} which reflects the discharge time of the capacitor. This saves a lot of time for testing. As for the other two types, the calculated knee points can roughly reflect the curve position and provide guidance for the test. Thus, it can effectively improve the test efficiency and solve the problems in the test of ASD VTC.

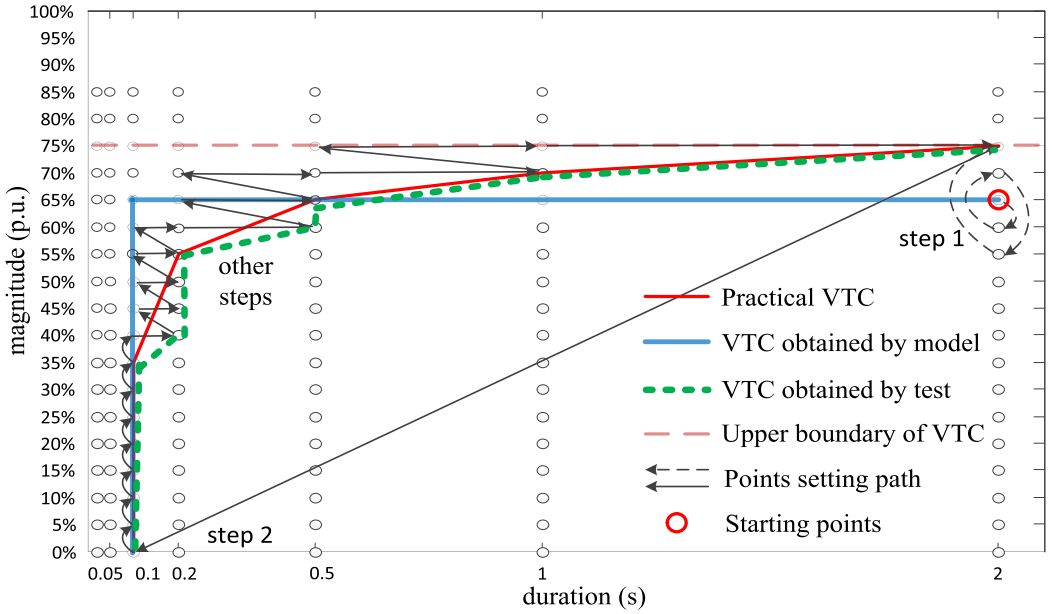


FIGURE 9. Proposed VTC test strategy.

VIII. CONCLUSION

This paper presents an analytical model for calculating the knee point of the voltage tolerance curve of adjustable speed drive. This point can characterize the contour of the curve and give a first-cut judgment for experts or engineers to select equipment from the voltage tolerance angle. The main conclusions are summarized as follows:

1) Based on the measured parameters of DC inductance, capacitance value and capacitance discharge time under the certain load condition of the tested equipment, the knee point can be calculated by the proposed analytical model to describe the contour of the voltage tolerance curve.

2) The relative deviation between the evaluation results of the proposed method and the experimental test results are within 5%, which demonstrates the effectiveness of this method.

3) In addition, to give a first-cut judgment for experts to select equipment, the results of the method can be also used to improve the test efficiency for VTC.

4) The proposed method can be also improved in terms of model accuracy. Based on the work of this paper, related voltage sag sensitivity indicators of ASD can be further designed for user voltage sag failure probability assessment, sensitive user modeling, etc.

APPENDIX A

A flow chart is given below to illustrate the work of this paper more clearly.

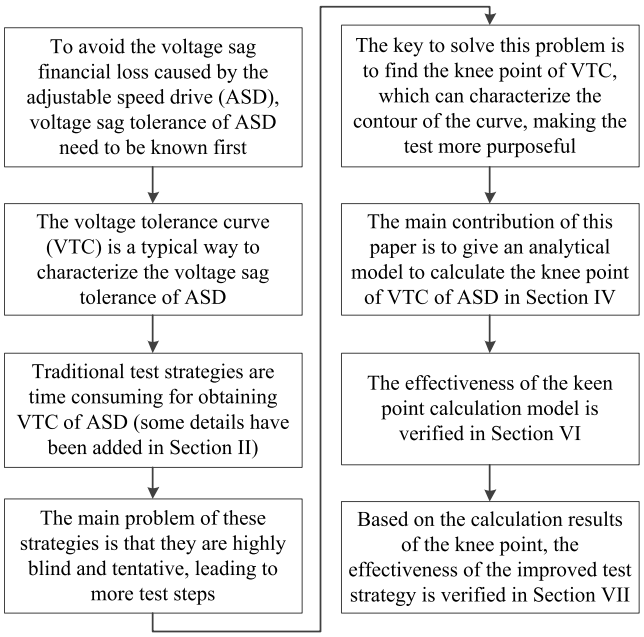


FIGURE 10. Research work and contribution of this article.

APPENDIX B

The derivation of (3) considers the following transient processes. At the moment of voltage recovery, due to the motor inertia, the current of the load circuit (including the inverter and motor) cannot respond in time, so it can be disconnected in the equivalent circuit, as shown in Fig. 11. The voltage and current of the DC link mainly depend on L and C.

Assume that in this moment dt, the current change amount di/dt is Δi and the voltage change amount dv/dt is Δv, then the current change amount of L, noted as v_{L}, and the voltage change amount of C noted as i_{C}, are as follows.

$$\begin{aligned} L \cdot \Delta i &= v_L \\ C \cdot \Delta v &= i_C \end{aligned} \tag{14}$$

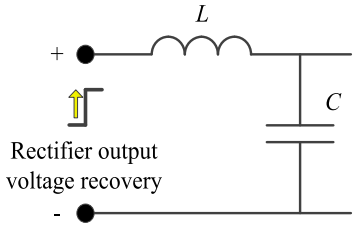


FIGURE 11. Equivalent circuit of the DC link at the moment of voltage recovery.

At this moment, the voltage and current changes of L and C are mutually coupled, i.e. $v_L = \Delta v$ and $i_C = \Delta i$, this can also be understood from the perspective of energy conservation. Thus, the following relationship exists.

$$L \cdot \Delta i^2 = C \cdot \Delta v^2 \tag{15}$$

where the voltage change amount Δv of ASD suffered by voltage sag with a critical magnitude which would trigger overcurrent protection can be written as $V_{DCn} - V_{DCth-I}$. Thus, (15) can be further written as

$$\Delta i_{max}^2 \frac{L}{C} = (V_{DCn} - V_{DCth-I})^2 \tag{16}$$

where V_{DCth-I} is the critical DC link voltage that will trigger over current protection. The above formula can be rewritten as

$$V_{DCth\text{-}I} = V_{DCn} - \Delta i_{max}\sqrt{L/C} \tag{17}$$

According to (2), the relationship between V_{3th-I} and V_{DCth-I} is as follows

$$V_{3th-I} = \frac{V_{DCth-I}}{2.34} \tag{18}$$

Thus, (3) can be obtained.

The derivation process of formula (10) is similar to this.

APPENDIX C

According to Fig. 12, the upper boundary of equipment's VTC can be obtained first by the spiral test strategy shown in Fig. 9. Then, the left boundary of VTC can be found easily which is almost consistent with VTC obtained by the model. Later, the deviation point between the two VTC on the left boundary can be quickly obtained. After that, a box-in strategy from the left side to the right side can be used to finish the test.

APPENDIX D

Voltage-sag test vectors used in this paper are mentioned in Fig. 13. In this paper, Type I represents the single-phase voltage sag, Type II.2A represents the two-phase voltage sag, and Type III is the symmetrical voltage sag. The rules are as follows: (a) For Type I, the magnitude of non-voltage sag phase remains at the rated level, and the magnitude of the phase affected by the sag coincides with the sag magnitude; (b) For Type II.2A, the magnitude of non-voltage sag phase remains at the rated level, and the magnitude of the two phases

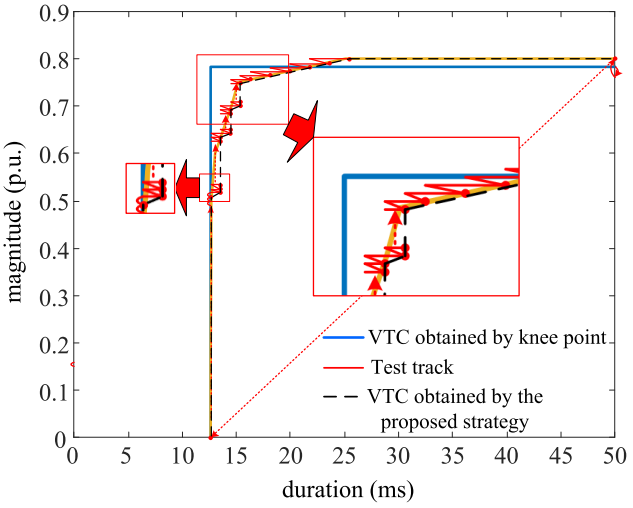


FIGURE 12. VTC obtained by the proposed strategy under two-phase voltage sags (Type II.2A).

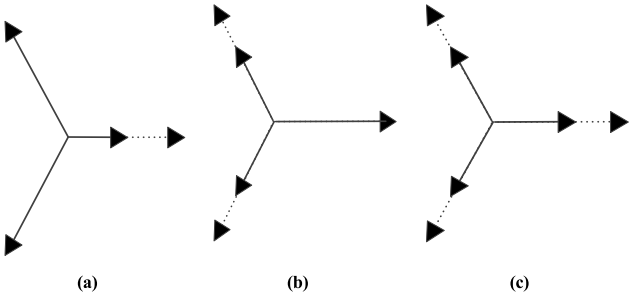


FIGURE 13. Voltage-sag test vectors [16], (a) Single-phase sag (Type I), (b) Two-phase sag (Type II.A2), (c) Three-phase sag (Type III).

affected by the sag coincides with the sag magnitude; (c) For Type III, the magnitude of the all phases affected by the sag coincides with the sag magnitude.

APPENDIX E

The test strategies mentioned in Section II are described as follows: (a) For top-down strategy, it involves holding the sag duration constant while the magnitude of the sag voltage is stepped down in intervals from the maximum magnitude (defined by the test plan) until the minimum magnitude (also defined by the test plan) is reached or the equipment under test (EUT) trips. At that point, the sag duration is decreased to its next scheduled value, and the magnitude steps are repeated at that duration. This magnitude down-stepping within a duration loop continues until all scheduled duration are exhausted; (b) The left-right method is similar to the top-down strategy, but it holds the sag magnitude constant while the duration of the sag is changed; (c) The box-in strategy is also similar to the top-down strategy, the sag duration is held steady while the magnitude is incrementally decreased. However, once a trip point is determined during a loop, the duration is decreased to the next value and the magnitude is increased by the magnitude interval from the value of the trip point. This process continues until all steps in the final duration

loop are completed; (d) The binary test strategy finds the critical failure point by continuously shrinking the magnitude/duration interval. When the test results at the end of the interval are different, it means that the critical failure point is in the interval. In fact, the dichotomy has a fixed number of test steps in each loop, sometimes it is not as efficient as the box-in strategy.

REFERENCES

[1] H. Li and R. S. Curiac, "Designing more efficient large industrial induction motors by utilizing the advantages of adjustable-speed drives," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 1805–1809, Sep. 2010.
[2] C. Behera, G. H. Reddy, P. Chakrapani, A. K. Goswami, C. P. Gupta, and G. K. Singh, "Assessment of equipment trip probability due to voltage sags based on fuzzy possibility distribution function," *IEEE Access*, vol. 6, pp. 76889–76899, 2018.
[3] A. Parreno Torres, P. Roncero-Sanchez, J. Vazquez, F. J. Lopez-Alcolea, and E. J. Molina-Martinez, "A discrete-time control method for fast transient voltage-sag compensation in DVR," *IEEE Access*, vol. 7, pp. 170564–170577, 2019.
[4] S. Arias-Guzman, O. A. Ruiz-Guzman, L. F. Garcia-Arias, M. Jaramillo-Gonzales, P. D. Cardona-Orozco, A. J. Ustariz-Farfan, E. A. Cano-Plata, and A. F. Salazar-Jimenez, "Analysis of voltage sag severity case study in an industrial circuit," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 15–21, Jan. 2017.
[5] A. C. Finch, "A cement Plant's experience in investigating power sags leads to a reduction in kiln outages by utilizing power hardening methods," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4435–4441, Sep. 2016.
[6] J. C. Cebrian, J. V. Milanovic, and N. Kagan, "Probabilistic assessment of financial losses in distribution network due to fault-induced process interruptions considering process immunity time," *IEEE Trans. Power Del.*, vol. 30, no. 3, pp. 1478–1486, Jun. 2015.
[7] A. K. Goswami, C. P. Gupta, and G. K. Singh, "Voltage sag assessment in a large chemical industry," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 1739–1746, Sep. 2012.
[8] Y. Xu, W. Lu, K. Wang, C. Li, and W. Aslam, "Sensitivity of low-voltage variable-frequency devices to voltage sags," *IEEE Access*, vol. 7, pp. 2068–2079, 2019.
[9] K. Lee, T. Jahns, D. W. Novotny, T. A. Lipo, W. E. Berkopec, and V. Blasko, "Impact of inductor placement on the performance of adjustable-speed drives under input voltage unbalance and sag conditions," *IEEE Trans. Ind. Appl.*, vol. 42, no. 5, pp. 1230–1240, Sep. 2006.
[10] K. Pietilainen, L. Harnefors, A. Petersson, and H.-P. Nee, "DC-link stabilization and voltage sag ride-through of inverter drives," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1261–1268, Jun. 2006.
[11] *IEEE Recommended Practice for Evaluating Electric Power System Compatibility With Electronic Process Equipment*, Standard 1346-1998(R2004), 2004.
[12] S. Z. Djokic, K. Stockman, J. V. Milanovic, J. J. M. Desmet, and R. Belmans, "Sensitivity of AC adjustable speed drives to voltage sags and short interruptions," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 494–505, Jan. 2005.
[13] S. Ouyang, L. Liu, P. Liu, and X. Li, "Test and analysis on sensitivity of low-voltage releases to voltage sags," *IET Gener., Transmiss. Distrib.*, vol. 9, no. 16, pp. 2664–2671, Dec. 2015.
[14] Y. Xu, Y. Wu, M. Zhang, and S. Xu, "Sensitivity of programmable logic controllers to voltage sags," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 2–10, Feb. 2019.
[15] X. Xiao, H. He, and Y. Wang, "Analytical model of AC contactors for studying response mechanism to multi-dimensional voltage sag characteristics and its novel applications," *IET Gener., Transmiss. Distrib.*, vol. 13, no. 17, pp. 3910–3920, Sep. 2019.
[16] *IEEE Recommended Practice for Voltage Sag and Short Interruption Ride-Through Testing for End-Use Electrical Equipment Rated Less than 1000 V*, Standard IEEE Std 1668-2017 (Revision of IEEE Std 1668-2014), 2017.
[17] Z.-Y. Ma, Z. Xu, W.-X. Mo, Q.-W. Guo, H.-J. Wang, K. Zhou, Y. Wang, and L.-Y. Gui, "A new method for sensitive single-phase equipment testing to voltage sag," in *Proc. 18th Int. Conf. Harmon. Qual. Power (ICHQP)*, May 2018, pp. 1–6.
[18] N. A. Ismail, L. M. Kasim, N. F. Mokhtar, T. S. T. Yaakub, and H. Mokhlis, "Digital analysis and development of ride-through capability of AC contactor with respect to voltage sag characteristics," in *Proc. 2nd Int. Conf. Comput. Autom. Eng. (ICCAE)*, Feb. 2010, pp. 26–28.
[19] S. C. Vegunta, J. V. Milanović, and S. Ž. Djokić, "Modelling of V–Hz and vector controlled ASDs in PSCAD/EMTDC for voltage sag studies," *Electric Power Syst. Res.*, vol. 80, no. 1, pp. 1–8, Jan. 2010.
[20] M. H. J. Bollen, *Understanding Power Quality Problem: Voltage Sag and Interruption*. New York, NY, USA: IEEE Press, 2000.
[21] S. Tao, S. Tang, and C. Chen, "Experimental research on adjustable speed drivers tolerance to voltage sags and quantitative method—Part I: Mechanism analysis and test method," *Trans. China Electrotech. Soc.*, vol. 34, no. 6, pp. 1273–1281, Mar. 2019.
[22] S. Tang, S. Tao, and Y. Liu, "Experimental research on adjustable speed drivers tolerance to voltage sags and quantitative method—Part II: Experiment and quantification method," *Trans. China Electrotech. Soc.*, vol. 34, no. 10, pp. 2207–2215, May 2019.

Z. XU received the M.S. degree from Chongqing University, Chongqing, China, in 2010. He is currently a Senior Engineer with the Electric Power Test Research Institute, Guangzhou Power Supply Bureau Company, Ltd., Guangzhou, China. His research interest includes power quality and its application.

Qianwen Guo received the M.S. degree from the Huazhong University of Science and Technology, Hubei, China, in 2015. She is currently an Engineer with the Electric Power Test Research Institute, Guangzhou Power Supply Bureau Company, Ltd., Guangzhou, China. Her research interest includes power quality management.

L. LUAN received the M.S. degree from Xi'an Jiaotong University, Shanxi, China, in 2008. She is currently an Engineer with the Electric Power Test Research Institute, Guangzhou Power Supply Bureau Company, Ltd., Guangzhou, China. Her research interests include power quality and electricity market.

K. ZHOU received the M.S. degree from Chongqing University, Chongqing, China, in 2016. He is currently an Engineer with the Electric Power Test Research Institute, Guangzhou Power Supply Bureau Company, Ltd., Guangzhou, China. His research interests include power quality and customized power technology.