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Modeling and Stability Analysis of a Smart Transformer-Fed Grid

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ABSTRACT The interaction of the smart transformer (ST) with the grid-converter-based distributed energy resources (DERs) could trigger instability. Recent research efforts have been made to study the stability issues caused by the resonances (e.g. LC or LCL filter resonances of DERs) in ST LV side grid. This paper studies the impact of the grid synchronization of the grid-converter-based DER on the stability of the ST as well as the grid. The equivalent admittance of the grid converter considering the effect of synchronous reference frame phase-locked loop (SRF-PLL) is developed and merged with the ST voltage control. Based on the generalized Nyquist criterion, the stability analysis of a ST-fed grid is carried out, showing that the PLL bandwidth is a key factor that determines the system stability. To address the stability issue, a stabilization method based on virtual impedance is proposed and can be seamlessly integrated with the ST voltage control. Simulation and experimental results are provided to validate the effectiveness of the analysis and the proposed control strategy.

INDEX TERMS Solid-state transformer, smart transformer, stability, grid synchronization, phase-locked loop.

I. INTRODUCTION

The smart transformer (ST) is a solid-state transformer adopted as intelligent substation with control and communication functionalities. The ST has a three-stage structure as shown in Fig. 1, including medium voltage (MV) converter stage, dc/dc converter stage, and low voltage (LV) converter stage. The MV converter is able to work with medium voltage level (e.g., 10 kV). It regulates the power/current absorption from the MV grid and deliver active power demanded from the loads in the LV grid. The dc/dc stage interfaces the two dc links, transferring the power from the MV to the LV side and regulating the voltage of the LV dc-link. For the LV converter, it controls the voltage waveforms of the LV grid (e.g., 0.4 kV) to be sinusoidal and balanced independent from the load dynamics. Depending on the loading capability, the power rating of smart transformers can range from several hundreds KVA to several MVA [1]–[4].

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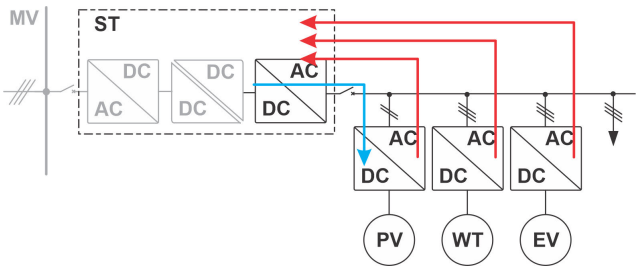

FIGURE 1. Interactions between ST and DERs in a ST-fed microgrid.

Compared to the conventional distribution transformer, the ST offers connection to hybrid grid and is able to significantly improve the demand response balance while keeping a reasonable energy cost [5]. The ST could help solving system-level challenges, however it represents challenges itself. One of the main challenges of the ST comes from its LV grid: the ST-fed LV grid is likely to suffer from stability issues due to the interacting with grid converter-based distributed energy resources (DERs) [6]–[8]. Being affected by

the control dynamics and the filter resonances, the instability is characterized by harmonic oscillations, typically ranging from hundreds of hertz to kilohertz [7], [9]. In [6], [7], the effects of the filter resonances on the stability of ST-fed grid have been studied and the stabilization methods based on active damping techniques were proposed to address those issues. Nevertheless, the influences of the grid synchronization on the ST-fed grid stability has seldom been investigated.

In the conventional distribution grid, the effects of the three-phase grid synchronization have already drawn wide attentions. The research starts with the input admittance model of grid converters considering the phase-locked loop (PLL) [10]. It is found a negative damping has been introduced by the PLL, which tends to compromise the stability of the grid converters under the weak grid conditions. To well study the impact of PLL on system stability, later research efforts have been put on the equivalent impedance models of grid converter served by PLL in both dq and $\alpha\beta$ frames [11], [12]. Moreover, a unified impedance model was proposed for better evaluation of the dynamic influences of PLL [13], where the mathematical relations between the models in dq and $\alpha\beta$ frames have been revealed. It is shown that the two different models have the identical stability implications. In recent literature, the impact of PLL on the transient stability has been further investigated. In [14], the impedance model of the PLL-synchronized converter has been extended in dq frame for the stability analysis under the case of large perturbation. In [15], the design-oriented transient stability analysis of PLL-synchronized converter has been studied during the grid faults conditions. From these previous researches, it is seen that an asymmetric frame model could be obtained since the phase detection is realized through the q-axis channel of the PLL. In particular, a PLL with high bandwidth could further decreases the negative real part of the q-axis impedance and therefore can destabilize the system stability in the distribution grid [10], [12]–[14]. For this reason, the bandwidth of the PLL of grid converters in the distribution grids has to be limited with the concern of system stability.

In contrast, this paper investigates the stability issues of a ST-fed grid considering the effect of PLL. Different from the conventional distribution grid, the ST LV grid is supported by the ST LV side converter instead of power transformer. This imposes new potentials regarding grid stabilization: since the grid impedance is characterized by the ST LV converter, it can be modified by means of the ST voltage control and its control parameters. More specifically, the idea is to design an appropriate voltage control to reshape the grid impedance, so that the interactions between the grid impedance and the PLL-synchronized converter can be modified. With appropriate control and parameters, the ST LV converter can stabilize all local converters equipped with PLLs. Comparing to the conventional distribution grids, the reshaping of the equivalent impedance is expected to be an indispensable service provided to all the PLL-synchronized converters. In addition, it can avoid complex design of the PLLs of the local converters.

As reported in [13], asymmetrical cross couplings between d- and q-axis of the overall system can be introduced due to the PLL. For this reason, a multi-input multi-output (MIMO) dynamic model of the LV ST-fed considering the effect of PLL of the connected converters will be developed in this paper. The MIMO model can better reveal the characteristics of an asymmetric system (e.g., system in dq frame). For the stability assessment, the generalized Nyquist criterion has to be used for the MIMO model. Based on the stability analysis, a stabilization method based on the virtual impedance will be proposed to address the stability issue caused by the PLL.

The rest of this paper is organized as follows: The system configuration and the fundamental voltage control structure of the ST LV side converter are presented in Section II. To include the effect of grid synchronization, the equivalent admittance of a grid-converter-based DER with a synchronous reference frame PLL (SRF-PLL) has been developed in Section III. The stability of the ST voltage control with the equivalent admittance of DER is then assessed by using the generalized Nyquist criterion, which is given in Section IV. In this section, the influences of different PLL bandwidth on the stability of the ST-fed grid have been discussed and a stabilization method based on the virtual impedance has been proposed. Simulation and experimental results are given in Section V to verify the effectiveness of the proposed strategy. Conclusions are drawn in Section VI.

II. SYSTEM CONFIGURATION

The system configuration and control scheme of a ST LV side converter is shown in Fig. 2a, where L_f and C_f are the inductor and capacitor of the LC filter; Z_L represents the equivalent line impedance connecting to the point of common coupling (PCC). The grid-converter-based DERs and AC loads can be connected to the PCC. The ST LV converter controls the voltage waveform of the LV grid. In most cases, the ST generates sinusoidal and balanced three-phase voltage at the PCC independently from the connected DERs and loads. In addition, grid services like overload control and reverse power flow control can be implemented to exploit the hosting capability [16], [17]. In this paper, the fundamental voltage control of the ST LV converter is considered for the modeling and stability analysis.

In literature, multiple feedback loop control strategies have been commonly employed for voltage control due to its ease of implementation and good performance [18], [19]. To achieve overcurrent protection, the inductor current feedback scheme is adopted for the ST LV side control in this paper. For the sake of simplicity, the zero-sequence component was not considered in this paper. Therefore, the detailed voltage control as well as its one line block diagram is shown in Fig. 2b. $\mathbf{G_{o,v}}$ and $\mathbf{G_{i,i}}$ are the transfer function matrices of the outer-loop and inner-loop controllers, where PI controllers can be utilized to control the ST capacitor voltage and the inductor current in $dq(0)$ frame. $\mathbf{G_d}$ represents the

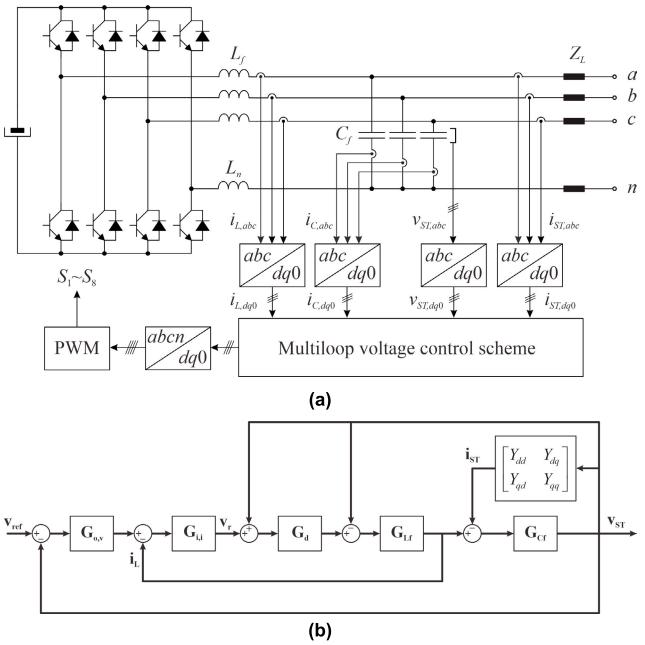

FIGURE 2. System configuration of ST LV side converter: (a) voltage control scheme and (b) one line block diagram of ST LV control.

equivalent delay imposed by the computation and PWM, $\mathbf{G_{Lf}}$ and $\mathbf{G_{Cf}}$ are the transfer function matrices of the filter inductor L_f and capacitor C_f, respectively.

Considering the effects of the LV side grid, the equivalent admittance matrix of the LV grid in dq frame can be defined by $\mathbf{Y_{eq}}$ and coupled in the block diagram as shown in Fig. 2b. In this way, the impact of the grid converters connected to the LV grid on the ST voltage control can be well studied. The open-loop MIMO transfer function matrix of the ST LV converter and its control can be obtained by

$$\mathbf{G_{op}} = \mathbf{G_d G_{o,v} G_{i,i} G_{Lf}} \cdot [\mathbf{G_{Lf}}(\mathbf{I} - \mathbf{G_d}) + \mathbf{Y_{eq}} + \mathbf{G_{Cf}^{-1}} + \mathbf{G_d G_{i,i} G_{Lf}}(\mathbf{Y_{eq}} + \mathbf{G_{Cf}^{-1}})]^{-1} \quad (1)$$

From control point of view, it is easily to design a stable ST LV control system in case of constant impedance load. However, the control dynamics of $\mathbf{Y_{eq}}$ have to be taken into account due to the increasing penetration of grid-converter-based DERs in the LV grid. The detailed model of $\mathbf{Y_{eq}}$ including one grid converter is given in the next section. In particular, the effect of the grid synchronization will be considered.

III. EQUIVALENT ADMITTANCE OF DER WITH THE EFFECTS OF GRID SYNCHRONIZATION

The control strategy applied to the grid converter consists mainly of two cascaded loops. Commonly, there is a current loop, which regulates the injected current, and an outer loop which controls the dc-link voltage as well as the injected power [20]. Since the dynamic of the outer loop is much slower than that of the inner loop as well as the PLL, the outer loop can be neglected for the following modeling and analysis. A simplified system configuration of a grid converter is shown in Fig. 3a. The current control system is implemented in dq frame and a synchronous reference frame phase-locked loop (SRF-PLL, shown in Fig. 3b) is employed for grid synchronization. The detailed current control is presented in Fig. 3c, where G_{cc} is the transfer function of the current controller. In this paper, PI controllers are used for current regulation.

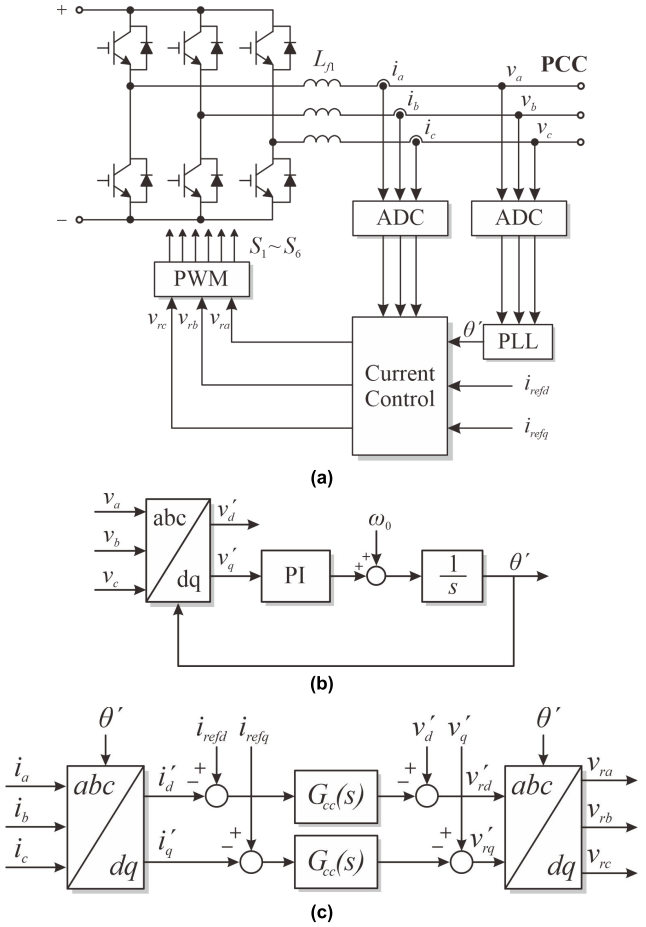

FIGURE 3. System configuration of DER grid converter: (a) system configuration, (b) SRF-PLL, and (c) current control system in dq frame.

Given the three-phase PCC voltage $[v_a, v_b, v_c]^T$, the average mode of the inverter in abc frame is

$$L_{f1}\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = G_d \begin{bmatrix} v_{ra} \\ v_{rb} \\ v_{rc} \end{bmatrix} - \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (2)$$

where L_{f1} is the output filter of the grid inverter, $[v_{ra}, v_{rb}, v_{rc}]^T$ are the voltage references of the grid converter, and G_d represents the delay caused by computation and PWM. Using an ideal transform (with actual phase angle θ_0 from ST), the dq frame average model in s-domain is given by

$$\begin{bmatrix} L_{f1}s & -\omega L_{f1} \\ \omega L_{f1} & L_{f1}s \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} G_d(s) & 0 \\ 0 & G_d(s) \end{bmatrix}\begin{bmatrix} v_{rd} \\ v_{rq} \end{bmatrix} - \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (3)$$

Noting that all of the d and q components in (3) are obtained by applying the ideal Park transform $\mathbf{T}(\theta_0)$, namely these components are directly oriented with the actual PCC voltage, and thus do not rely on the effect of PLL.

According to the control scheme shown in Fig. 3c, the perturbation equation of current control can be written by

$$\begin{bmatrix} \Delta v'_{rd} \\ \Delta v'_{rq} \end{bmatrix} = -\begin{bmatrix} G_{cc}(s) & 0 \\ 0 & G_{cc}(s) \end{bmatrix}\begin{bmatrix} \Delta i'_d \\ \Delta i'_q \end{bmatrix} + \begin{bmatrix} G_{cc}(s) & 0 \\ 0 & G_{cc}(s) \end{bmatrix}\begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} \Delta v'_d \\ \Delta v'_q \end{bmatrix} \quad (4)$$

where $[\Delta i_{refd}, \Delta i_{refq}]^T$ and $[\Delta i'_d, \Delta i'_q]^T$ are the perturbations of the current references and grid current in dq frame, $[\Delta v'_{rd}, \Delta v'_{rq}]^T$ and $[\Delta v'_d, \Delta v'_q]^T$ are the perturbations of the voltage references and grid voltage in dq frame. Here, the superscript $(\cdot)'$ denotes the corresponding components are obtained by applying $\mathbf{T}(\theta')$ using the detected phase angle θ' from the PLL. This indicates the PLL dynamic would have an impact on these control variables.

To decouple the PLL effects, the modeling procedures with small-angle approximation presented in [21] can be applied to the variables which correspond to the Park transform and its inverse. Then, the small-signal equations of the above-mentioned variables can be represented by

$$\begin{bmatrix} \Delta v'_d \\ \Delta v'_q \end{bmatrix} = \begin{bmatrix} 1 & V_q G_{PLL}(s) \\ 0 & 1 - V_d G_{PLL}(s) \end{bmatrix}\begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} \Delta i'_d \\ \Delta i'_q \end{bmatrix} = \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} + \begin{bmatrix} 0 & I_q G_{PLL}(s) \\ 0 & -I_d G_{PLL}(s) \end{bmatrix}\begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} \Delta v'_{rd} \\ \Delta v'_{rq} \end{bmatrix} = \begin{bmatrix} \Delta v_{rd} \\ \Delta v_{rq} \end{bmatrix} + \begin{bmatrix} 0 & V_{rq} G_{PLL}(s) \\ 0 & -V_{rd} G_{PLL}(s) \end{bmatrix}\begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \quad (7)$$

where V_d and V_q are the dc quantities of the grid voltage, I_d and I_q are the dc quantities of the grid current, and V_{rd} and V_{rq} are the dc quantities of the voltage reference, in dq frame. $G_{PLL}(s)$ is the closed-loop transfer function of the SRF-PLL, which is

$$G_{PLL}(s) = \frac{V_d k_{pPLL} s + V_d k_{iPLL}}{s^2 + V_d k_{pPLL} s + V_d k_{iPLL}} \quad (8)$$

where k_{pPLL} and k_{iPLL} are the proportional and integral gains of the PI controller of the SRF-PLL.

By substituting (5)-(7) into (4), one can get the small-signal model of the grid converter, which is

$$\begin{aligned} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} &= \mathbf{Y_{eq}}\begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \mathbf{I_{eq}}\begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} \\ &= \begin{bmatrix} Y_{dd}(s) & Y_{dq}(s) \\ Y_{qd}(s) & Y_{qq}(s) \end{bmatrix}\begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \\ &\quad + \begin{bmatrix} I_{dd}(s) & I_{dq}(s) \\ I_{qd}(s) & I_{qq}(s) \end{bmatrix}\begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} \end{aligned} \quad (9)$$

The detailed expressions of the matrix elements of (9) are given in the Appendix. Here, the matrix $\mathbf{Y_{eq}}$ in the first term of the model is the equivalent admittance of the grid converter considering both synchronization and control.

By substituting (9) to (1), the impact of grid converter with the effect of synchronization on the ST LV converter can be investigated.

IV. STABILITY ANALYSIS OF A ST-FED GRID CONSIDERING GRID SYNCHRONIZATION

This section studies the stability issue of a ST-fed grid when considering the effects of PLL. A stabilization method based on the virtual impedance is proposed to address the issue.

A. IMPACT OF PLL-BASED SYNCHRONIZATION

To investigate the stability regarding the impact of grid synchronization, the equivalent admittance $\mathbf{Y_{eq}}$ developed in Section III has been substituted to open-loop transfer function matrix of the ST LV converter (1). The system parameters listed in Table 1 are used for the stability analysis. In the analysis, the proportional and integral gains of the PI controller of the SRF-PLL have been changed, so that different PLL bandwidth can be obtained. The impact on the system stability can be studied by using the generalized Nyquist criterion.

TABLE 1. System parameters.

Symbol	Quantity	Value
S_n	nominal power rating	4 kVA
V_n	phase-to-neutral voltage (rms)	230 V
Z_L	equivalent line impedance	$0.5 + j0.94\ \Omega$
f_s	switching frequency	10 kHz
f_c	sampling frequency	20 kHz
L_f	filter inductance of ST	5.03 mH
C_f	filter capacitance of ST	1.5 μF
L_{f1}	filter inductance of DER converter	5.03 mH
k_{pv}	proportional gain of ST outer loop	1.05
k_{iv}	integral gain of ST outer loop	50
k_{pi}	proportional gain of ST inner loop	2.25
k_{ii}	integral gain of ST inner loop	75
k_{pc}	proportional gain of DER current control	7.5
k_{ic}	integral gain of DER current control	250
k_{pPLL}	proportional gain of DER PLL case 1: bandwidth (BW) = 20 Hz case 2: bandwidth (BW) = 200 Hz	case 1: 92 case 2: 920
k_{iPLL}	integral gain of DER PLL case 1: bandwidth (BW) = 20 Hz case 2: bandwidth (BW) = 200 Hz	case 1: 4223 case 2: 423327

For the asymmetric MIMO system, the system stability can be analyzed using the eigenvalues of the characteristic loci [22], [23]. Based on the open-loop transfer function matrix of the ST LV converter, the eigenvalues of the characteristic loci can be defined by [23]

$$\lambda_{1,2}(s) = \frac{G_{op,dd}(s) + G_{op,qq}(s)}{2} \pm \sqrt{\left[\frac{G_{op,dd}(s) - G_{op,qq}(s)}{2}\right]^2 - G_{op,dq}(s)G_{op,qd}(s)} \quad (10)$$

where $G_{op,dd}, G_{op,dq}, G_{op,qd}, G_{op,qq}$ are the dd, dq, dq, qq elements of the open-loop transfer function matrix $\mathbf{G_{op}}$. In case

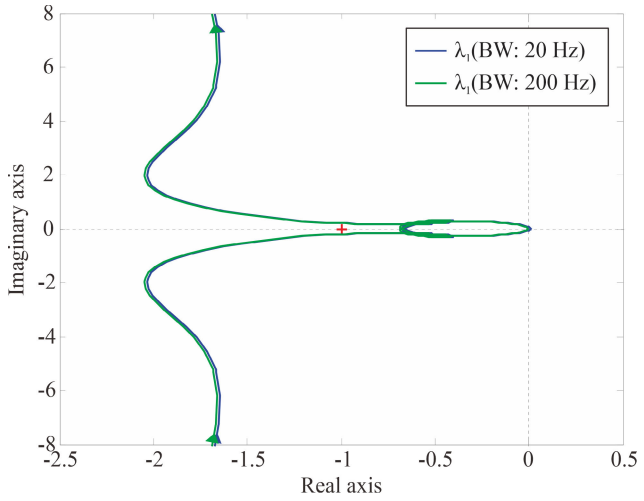

FIGURE 4. Stability analysis of a ST-fed grid considering the effects of PLL: (a) Nyquist diagram of λ_1 and (b) Nyquist diagram of λ_2.

the eigenvalues fulfill the Nyquist criterion, the system is asymptotically stable [23].

The Nyquist diagrams of the two eigenvalues λ_1 and λ_2 with different PLL bandwidths are plotted in Fig. 4a and Fig. 4b, respectively. The PLL bandwidths of the grid converter of DER are 20 Hz and 200 Hz in the two case studies. In Fig. 4a, it can be seen that the Nyquist diagrams of λ_1 with different PLL bandwidths are overlapping and there is no encirclement of the critical point $(-1, j0)$. This indicates λ_1 is insensitive to the PLL bandwidth and it does not suffer from stability issue. In Fig. 4b, the Nyquist diagrams of λ_2 have different stability conditions, when using different PLL bandwidths. When a PLL with 20 Hz bandwidth is used, as plotted by the blue curve, the Nyquist diagram has no encirclement of $(-1, j0)$, showing the system is stable. On the other hand, when a faster PLL with 200 Hz bandwidth is used, the Nyquist diagram plotted by the green curve has

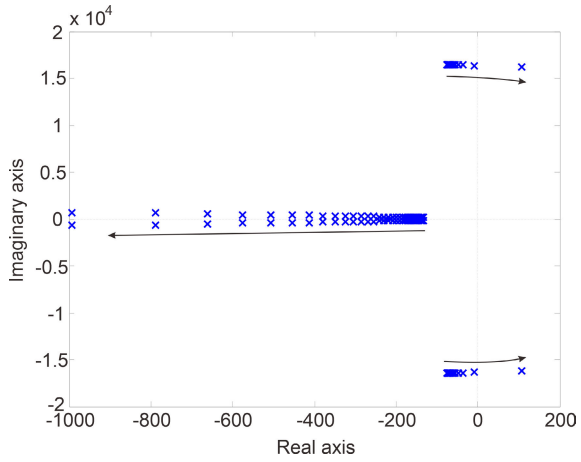

FIGURE 5. Root locus of the dominant poles of the qq element of the closed-loop transfer function matrix.

two clockwise encirclement of $(-1, j0)$, indicating the system with a faster PLL presents unstable behavior.

To better show the impact of PLL on system stability, the root locus of the dominant poles of the *qq* element of the closed-loop transfer function matrix is presented in Fig. 5. In this root locus, the PLL bandwidth increases from 20 Hz to 200 Hz. It can be seen that a pair of poles gradually shift from the left half plane to the right half, when increasing the PLL bandwidth. Since the poles locate at the high-frequency range, it is expected that the unstable behavior would be represented by the high-frequency oscillations.

B. STABILIZED METHOD USING VIRTUAL IMPEDANCE

From Fig. 5, it can be seen the poles of the *qq* element lacks of damping when high bandwidth PLL is applied to the grid converter of DER. With this consideration, one intuitive way is to selectively enhance the system damping by using virtual impedance. For a ST-fed grid, one promising way is to implement the virtual impedance in the ST voltage control. In this way, the ST LV converter can reshape the equivalent grid impedance so that enhance the system damping for all the connected grid converters.

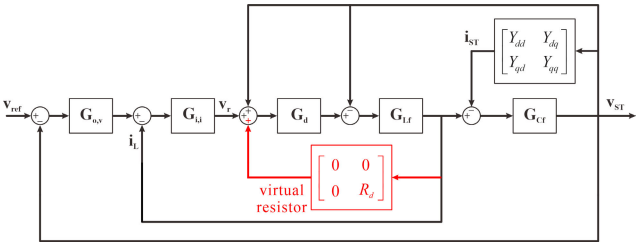

FIGURE 6. Schematic of the proposed ST voltage control with virtual impedance.

To achieve the target, a voltage control with the virtual impedance on its *q*-axis has been proposed in this paper. The control schematic is shown in Fig. 6, where a virtual resistor has been added and highlighted in red. The updated open-loop

MIMO transfer function matrix of the ST LV converter and its control is given as follows

$$\mathbf{G_{op}} = \mathbf{G_d G_{o,v} G_{i,i} G_{Lf}} \cdot [\mathbf{G_{Lf}(I - G_d)} + \mathbf{Y_{eq}} + \mathbf{G_{Cf}^{-1}} + \mathbf{G_d G_{Lf}(G_{i,i} - G_{VR})} \cdot (\mathbf{Y_{eq}} + \mathbf{G_{Cf}^{-1}})]^{-1} \quad (11)$$

where $\mathbf{G_{VR}}$ is the transfer function matrix of the virtual impedance.

It can be observed that the voltage control in d-axis remain the same, since the virtual resistor in d-axis is zero. For this reason, the major feature of λ_1 can be preserved since it mainly depends on the control in d-axis. The Nyquist diagram again does not have any encirclement of $(-1, j0)$. Nevertheless, for the Nyquist diagram of λ_2 will be largely altered by tuning the introduced virtual resistance, and so does the system stability.

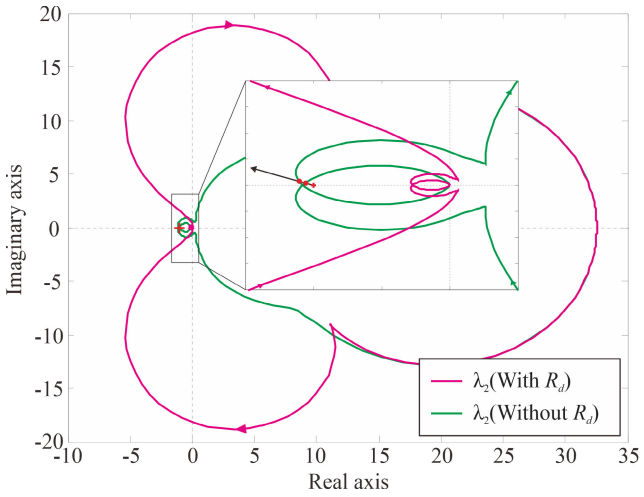

FIGURE 7. Nyquist diagrams of λ_2 when PLL bandwidth is 200 Hz: green curve - using the conventional ST voltage control, magenta curve - using the proposed ST voltage control.

To show the effectiveness, the Nyquist diagram of λ_2 with the proposed voltage control strategy (magenta curve) is presented in Fig. 7. For comparison, the Nyquist diagram of λ_2 with the conventional control (green curve) is shown in the same figure. For both cases, a PLL with 200 Hz bandwidth has been employed by the grid converter of DER. It can be seen that the Nyquist diagram plotted by the green curve has two clockwise encirclement of $(-1, j0)$, indicating the original system is unstable. When applying a 2 Ω virtual resistor to the proposed ST voltage control, the Nyquist diagram plotted by the magenta curve has no encirclement of the critical point any more, showing the system becomes stable. The q-axis equivalent impedance of the ST LV converter is also modified due to the virtual resistor. The Bode diagrams of the equivalent impedances with/without the virtual resistor are given in Fig. 8. It can be seen both the magnitude and the phase of the equivalent impedance have been reshaped when the virtual resistor being applied.

The value of the virtual resistance can be tuned based on the root locus of the dominant poles of the qq element

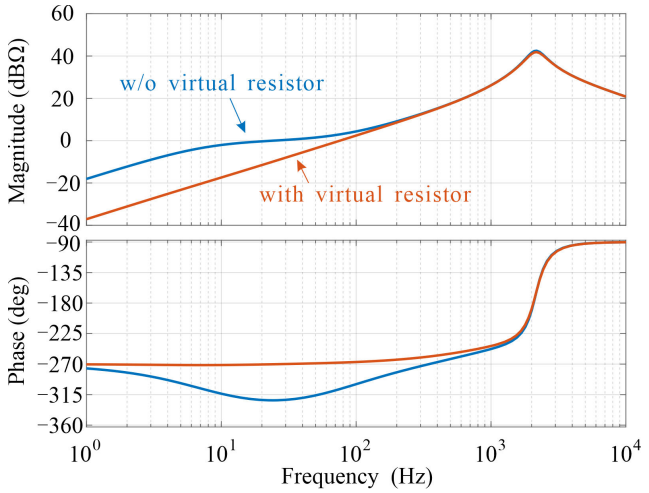

FIGURE 8. Bode diagrams of the q-axis equivalent impedances of the ST LV converter: blue curve - without the virtual resistor R_d, red curve – with the virtual resistor R_d.

of the closed-loop transfer function matrix of the proposed voltage control in Fig. 9a. In this case, the based value of 2 Ω is selected since it can maintain a minimum phase margin of 30°. When the virtual resistance increases from 0 to 1 p.u. (based value is 2 Ω). It can be observed that a pair of poles move from the right half plane to the left, with the increasing of the virtual resistance R_d. Nevertheless, the virtual resistor on q-axis could introduce the asymmetric effect to the PCC voltage. More importantly, seen from the zoomed figure of Fig. 9b (the highlighted gray area), some poles will shift towards the imaginary axis when a larger virtual resistance is used. This indicates the minimum phase margin of the system could be reduced when the virtual resistance further increases. For this reason, a trade-off must be made considering the characteristics of all dominant poles. With the aid of the Robust Control Toolbox™ of MATLAB/ Simulink, R_d of [0.75 p.u., 1.3 p.u.] is recommended to obtain a minimum phase margin of 30°.

V. SIMULATION AND EXPERIMENTAL RESULTS

For the validation, both simulation and experiments are carried out in a 2-bus ST-fed grid, where a grid converter is connected to the terminal of the ST LV converter. The current control scheme in Fig. 3 is used for the grid converter, and the voltage control schemes in Fig. 2 and Fig. 6 are used for the ST LV converter. The system parameters given in Table 1 are used for both simulation and experiments.

A. SIMULATION RESULTS

Two case studies are simulated by using the MATLAB/ Simulink with the aid of the PLECS toolbox. Firstly, the effect of the SRF-PLL on the system stability is studied. In Fig. 10a, the system is initially stable where the PLL bandwidth is 20 Hz. At $t = 0.5$s, the bandwidth of the PLL jumps from

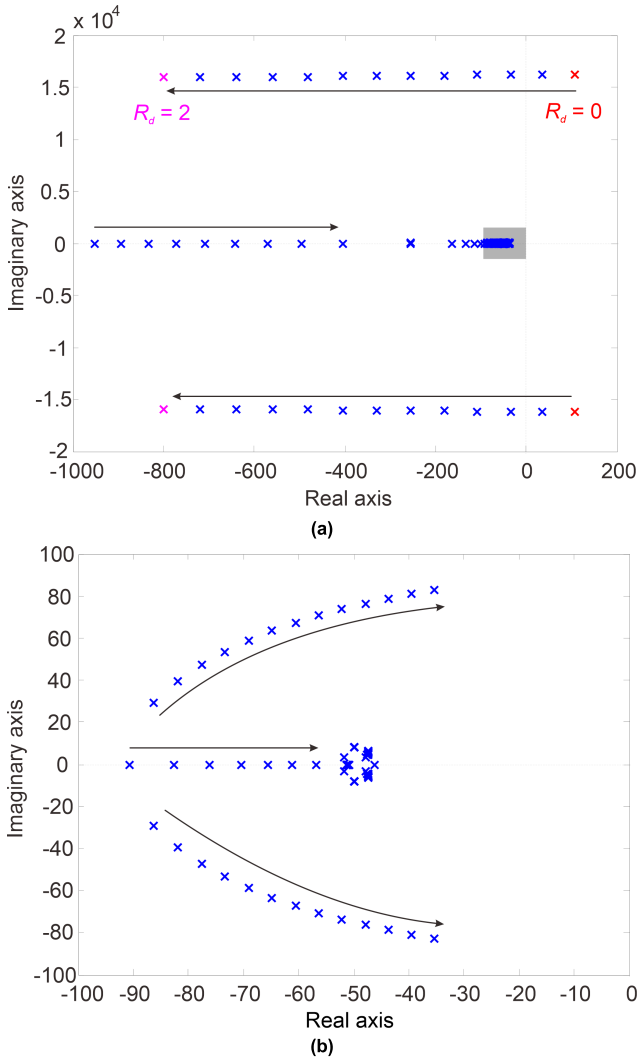

FIGURE 9. Root locus of the dominant poles of the *qq* element of the closed-loop transfer function matrix using the proposed voltage control: (a) Root locus when increasing R_d and (b) zoomed root locus for the gray area in Fig. 8a.

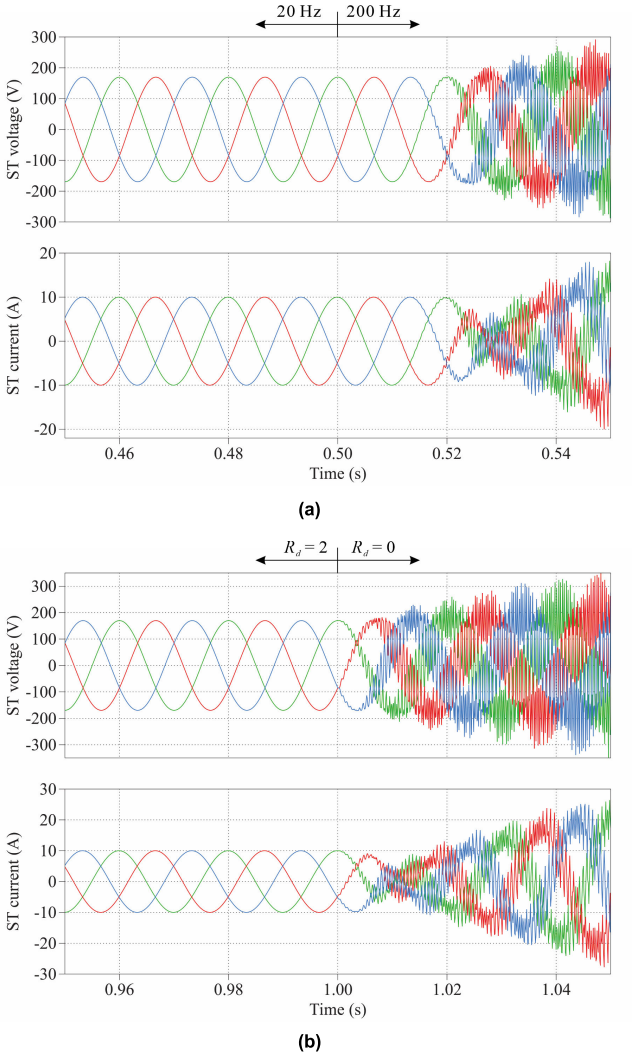

FIGURE 10. Simulation results of ST voltage and current under different scenarios: (a) PLL bandwidth jump, from 20 Hz to 200 Hz and (b) with/without the virtual resistor.

20 Hz to 200 Hz, it can be seen that both the ST voltage and current begin to oscillate when a higher BW is applied.

Then, the effectiveness of the proposed voltage control is shown in Fig. 10b, where the 200 Hz BW PLL is utilized. The virtual resistor of 2 Ω has been used in the very beginning and been removed since $t = 1$s. It is seen that the system can maintain stability even a high bandwidth PLL is used, when the virtual impedance has been plugged in. The system turns to be unstable as soon as the virtual resistor being removed.

B. EXPERIMENTAL RESULTS

To better validate theoretical analysis and effectiveness of control strategies, an experimental setup consisting of two commercial inverters has been developed in the laboratory. The system configuration is presented in Fig. 11: two Danfoss FC302 inverters are used, one for the ST LV converter and the other for the grid converter of DER. A dSPACE 1006 is used to achieve the control strategies as well as signal processing in real-time.

Fig. 12a shows the experimental results when the bandwidth of PLL changes. In the beginning, the ST-fed grid is running under stable conditions according to the waveforms of the PCC voltage, the DER current, and the PLL phase angle. At the moment (that indicated by the dashed line), the bandwidth of the PLL increases from 20 Hz to 150 Hz, the PCC voltage, the DER current and the PLL phase angle start to oscillate, showing the overall grid becomes unstable.

In order to stabilize the grid, a virtual resistor of 2 Ω has been plugged into the *q*-axis of the proposed voltage control at the dashed line of Fig. 12b. The green curve represents the signal of turn on/off the virtual resistor: low level - off, high level - on. Seen from Fig. 12b, all the waveforms including the PCC voltage, the DER current, and the PLL phase angle gradually stop oscillation after the virtual resistor being

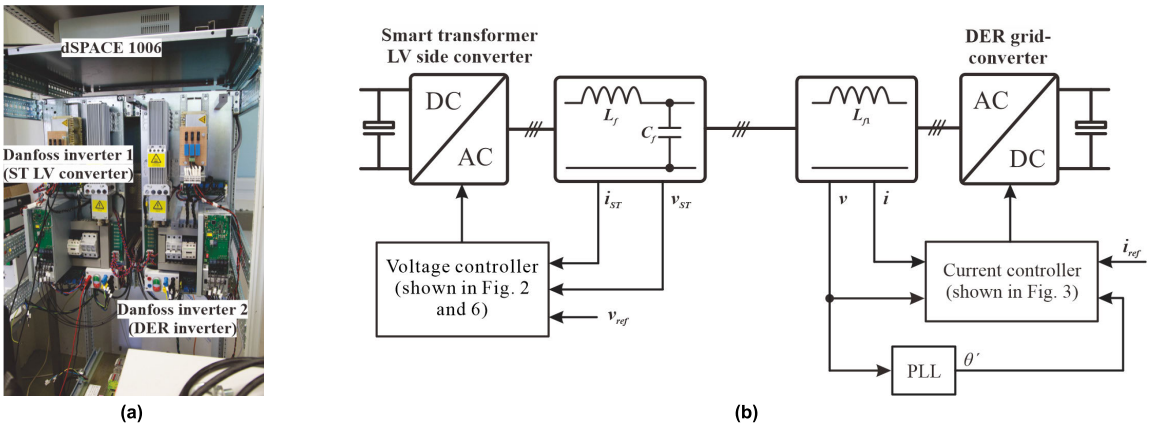

FIGURE 11. Laboratory setup: (a) photo and (b) configuration and control schematics.

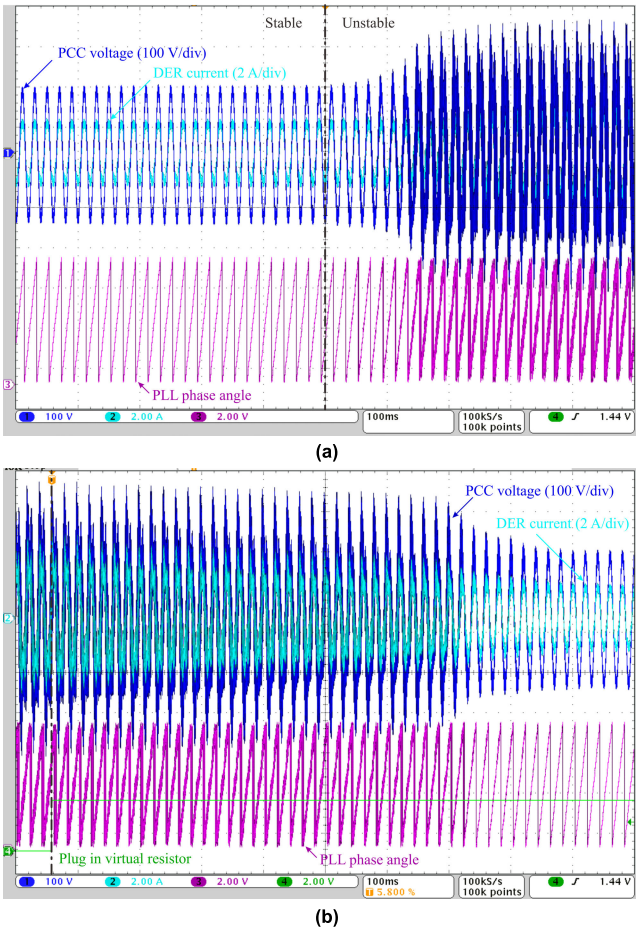

FIGURE 12. Experimental waveforms of the PCC voltage (blue), the DER current (aquamarine), and the PLL phase angle (magenta) under different conditions (time: 100 ms/div): (a) increasing of the PLL bandwidth and (b) plug in the virtual resistor.

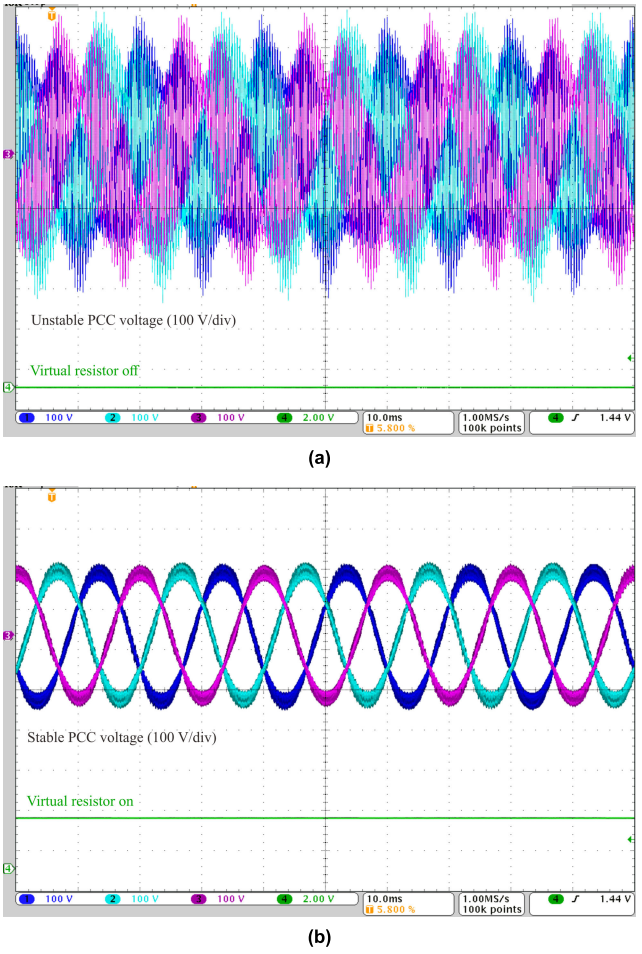

FIGURE 13. Experimental waveforms of the zoomed three-phase PCC voltage (time: 10 ms/div): (a) unstable case (without virtual resistor) and (b) stable case (with virtual resistor).

turned on, showing that the overall grid becomes stable. The zoomed PCC voltage waveforms before and after the virtual resistor being plugged in, are shown in Fig. 13a and Fig. 13b, respectively.

VI. CONCLUSION

This paper studies the modeling of a ST-fed grid and the effect of PLL-based synchronization on the system stability. Likewise conventional distribution grid, higher bandwidth

PLL is more likely to incur harmonic instability in a ST-fed grid, due to the insufficient damping ratio in the qq-axis. However, this does not imply a lower bandwidth PLL would not incur any stability issue. In fact, a low bandwidth PLL could cause other kinds of instability as reported in [24]–[26], like low-frequency oscillation and voltage collapse.

For the medium- or high-frequency oscillation, caused by the high bandwidth PLL, it can be alleviated by using appropriate voltage control of the ST. A stabilization method based on the virtual impedance is proposed and can be seamlessly implemented in the voltage control of ST LV converter. This method can effectively address the stability issues caused by the high bandwidth PLL of local grid converters. Simulation and experimental results are given to verify the effectiveness of the analysis as well as the stabilization method.

APPENDIX

The detailed expressions of the matrix elements of (9) is given in the followings.

The admittance matrix $\mathbf{Y_{eq}}$ can be rewritten by

$$\mathbf{Y_{eq}} = \begin{bmatrix} Y_{dd}(s) & Y_{dq}(s) \\ Y_{qd}(s) & Y_{qq}(s) \end{bmatrix} = \begin{bmatrix} Y_{dd}(s) & Y'_{dq}(s) + \Theta_d(s) \\ Y_{qd}(s) & Y'_{qq}(s) + \Theta_q(s) \end{bmatrix} \tag{12}$$

where $\Theta_d(s)$ and $\Theta_q(s)$ are the equivalent admittance terms related to the effect of PLL. For (12), one can have

$$\begin{aligned} Y_{dd}(s) &= Y'_{qq}(s) = \frac{G_c(s)G_d(s) + L_{f1}s}{(G_c(s)G_d(s) + L_{f1}s)^2 + (L_{f1}\omega)^2} \\ Y'_{dq}(s) &= -Y_{qd}(s) = \frac{L_{f1}\omega}{(G_c(s)G_d(s) + L_{f1}s)^2 + (L_{f1}\omega)^2} \end{aligned} \tag{13}$$

$$\begin{aligned} \Theta_d(s) &= \frac{L_{f1}\omega G_d(s) G_{PLL}(s)}{(G_c(s)G_d(s) + L_{f1}s)^2 + (L_{f1}\omega)^2} \\ &\quad \cdot (G_{cc}(s)I_d + V_{rd}) \\ \Theta_q(s) &= \frac{G_d^2(s) G_{PLL}(s)(G_{cc}(s)G_d(s) + L_{f1}s)}{(G_c(s)G_d(s) + L_{f1}s)^2 + (L_{f1}\omega)^2} \\ &\quad \cdot (G_{cc}(s)I_d + V_{rd}) \end{aligned} \tag{14}$$

The detailed expressions of current matrix elements are

$$\begin{aligned} I_{dd}(s) &= I_{qq}(s) = \frac{G_c(s)G_d(s)(G_c(s)G_d(s) + L_{f1}s)}{(G_c(s)G_d(s) + L_{f1}s)^2 + (L_{f1}\omega)^2} \\ I_{dq}(s) &= -I_{qd}(s) = \frac{G_c(s)G_d(s)L_{f1}\omega}{(G_c(s)G_d(s) + L_{f1}s)^2 + (L_{f1}\omega)^2} \end{aligned} \tag{15}$$

REFERENCES

[1] (2020). *LV_ENGINE Project*. [Online]. Available: https://www.spenergynetworks.co.uk/pages/lv_engine.aspx
[2] C. Kumar, R. Zhu, G. Buticchi, and M. Liserre, "Sizing and SOC management of a Smart-Transformer-Based energy storage system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6709–6718, Aug. 2018.
[3] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in Today's and future distribution grids," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 317–326, Jan. 2019.
[4] A. Kazerooni, G. De Carne, M. Eves, J. Yu, and M. Langwasser, "Technical requirements and challenges for grid applications of Smart Transformers," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, Nuremberg, Germany, May 2019, pp. 1–5.
[5] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z.-X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Ind. Electron. Mag.*, vol. 10, no. 2, pp. 46–58, Jun. 2016.
[6] Z.-X. Zou, G. Buticchi, and M. Liserre, "Analysis and stabilization of a smart transformer-fed grid," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1325–1335, Feb. 2018.
[7] Z.-X. Zou, G. Buticchi, and M. Liserre, "Grid identification and adaptive voltage control in a smart transformer-fed grid," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2327–2338, Mar. 2019.
[8] F. Cecati, M. Andresen, R. Zhu, Z. Zou, and M. Liserre, "Robustness analysis of voltage control strategies of smart transformer," in *Proc. IECON 44th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2018, pp. 5566–5573.
[9] X. Wang and F. Blaabjerg, "Harmonic stability in power electronic-based power systems: Concept, modeling, and analysis," *IEEE Trans. Smart Grid*, vol. 10, no. 3, pp. 2858–2870, May 2019.
[10] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323–3334, Dec. 2007.
[11] M. Cespedes and J. Sun, "Impedance modeling and analysis of grid-connected voltage-source converters," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1254–1261, Mar. 2014.
[12] B. Wen, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Analysis of D-Q small-signal impedance of grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 675–687, Jan. 2016.
[13] X. Wang, L. Harnefors, and F. Blaabjerg, "Unified impedance model of grid-connected voltage-source converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1775–1787, Feb. 2018.
[14] Z.-X. Zou and M. Liserre, "Modeling phase-locked loop-based synchronization in grid-interfaced converters," *IEEE Trans. Energy Convers.*, vol. 35, no. 1, pp. 394–404, Mar. 2020.
[15] H. Wu and X. Wang, "Design-oriented transient stability analysis of PLL-synchronized voltage-source converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3573–3589, Apr. 2020.
[16] Z.-X. Zou, G. De Carne, G. Buticchi, and M. Liserre, "Smart transformer-fed variable frequency distribution grid," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 749–759, Jan. 2018.
[17] G. De Carne, G. Buticchi, Z. Zou, and M. Liserre, "Reverse power flow control in a ST-fed distribution grid," *IEEE Trans. Smart Grid*, vol. 9, no. 4, pp. 3811–3819, Jul. 2018.
[18] N. M. Abdel-Rahim and J. E. Quaicoe, "Analysis and design of a multiple feedback loop control strategy for single-phase voltage-source UPS inverters," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 532–541, Jul. 1996.
[19] P. Chiang Loh, M. J. Newman, D. N. Zmood, and D. G. Holmes, "A comparative analysis of multiloop voltage regulation strategies for single and three-phase UPS systems," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1176–1185, Sep. 2003.
[20] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
[21] Z.-X. Zou, R. Rosso, and M. Liserre, "Modeling of the phase detector of a synchronous-reference-frame phase-locked loop based on second-order approximation," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, May 31, 2019, doi: 10.1109/JESTPE.2019.2920309.
[22] J. M. Maciejowski, *Multivariable Feedback Design*. Reading, MA, USA: Addison-Wesley, 1989.
[23] L. Harnefors, "Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2239–2248, Aug. 2007.
[24] Z. Zou, G. Buticchi, M. Liserre, A. M. Kettner, and M. Paolone, "Voltage stability analysis using a complete model of grid-connected voltage-source converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2016, pp. 1–8.
[25] L. Fan, "Modeling Type-4 wind in weak grids," *IEEE Trans. Sustain. Energy*, vol. 10, no. 2, pp. 853–864, Apr. 2019.
[26] L. Huang, H. Xin, Z. Li, P. Ju, H. Yuan, Z. Lan, and Z. Wang, "Grid-synchronization stability analysis and loop shaping for PLL-based power converters with different reactive power control," *IEEE Trans. Smart Grid*, vol. 11, no. 1, pp. 501–516, Jan. 2020.

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