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A Diode-Enhanced Scheme for Giant Magnetoresistance Amplification and Reconfigurable Logic

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ABSTRACT Magnetoresistance (MR) effects have been intensively investigated and widely recognized as an effective path for realizing information sensing, storage, and processing. In particular, giant MR (GMR) effect discovered in ferromagnetic/nonmagnetic multilayers or junctions exhibits high magnetic-field sensitivity and has been successfully applied in magnetic sensors and hard disk drive (HDD) read heads. However, the relatively small MR ratio becomes the Achilles' Heel for its further application in high-reliability electronic systems. In this paper, we propose a scheme to amplify the GMR effect of a multilayer strip by utilizing the nonlinear transport property of a diode. MR ratio up to 6947% is obtained with a magnetic field as small as 50 Oe. A theoretical model is established to describe the amplification behavior and various factors influencing MR ratio are experimentally analyzed. Based on this scheme, reliable logic functions have been carried out, which can be reconfigured by changing the working current. Our work can be extended to enhance the MR effect of any two-terminal MR device and has the potential to build emerging high-performance computing systems.

INDEX TERMS Diode-enhanced, giant magnetoresistance, magnetic multilayers, reconfigurable logic, spintronics.

I. INTRODUCTION

Magnetoresistance (MR) effects [1] have shown unprecedented vitalities in information sensing, storage, and processing by providing advantages of non-volatility, high speed, and high density. A number of applications based on MR effect have been proposed, such as sensors for magnetic field, current or angle [2]–[7], hard disk drive (HDD) read heads [8], magnetic random-access memory (MRAM) [9]–[12], and in-memory computation systems [13]–[18], many of which have been developed into commercial products. Meanwhile, the emerging information technologies, such as high-performance computing, Artificial Intelligence (AI), and Internet of Things (IoT), put forward higher demands from different hierarchies. Large MR ratio and high magnetic-field sensitivity are two crucial orientations of performance improvements. However, spin-dependent MR effects, for example, giant MR (GMR) [19]–[22] and its counterpart tunneling MR (TMR) [23]–[25], suffer from the MR ratio bottleneck. Further optimization requires more sophisticated structures and more restrict nanofabrication process. Although the traditional MR effects based on electrons and holes in semiconductor materials, such as Si and InSb [26]–[30], exhibit large MR in simple structures, their MR ratios are negligible in modest magnetic field. In addition, their large characteristic resistivity also limits

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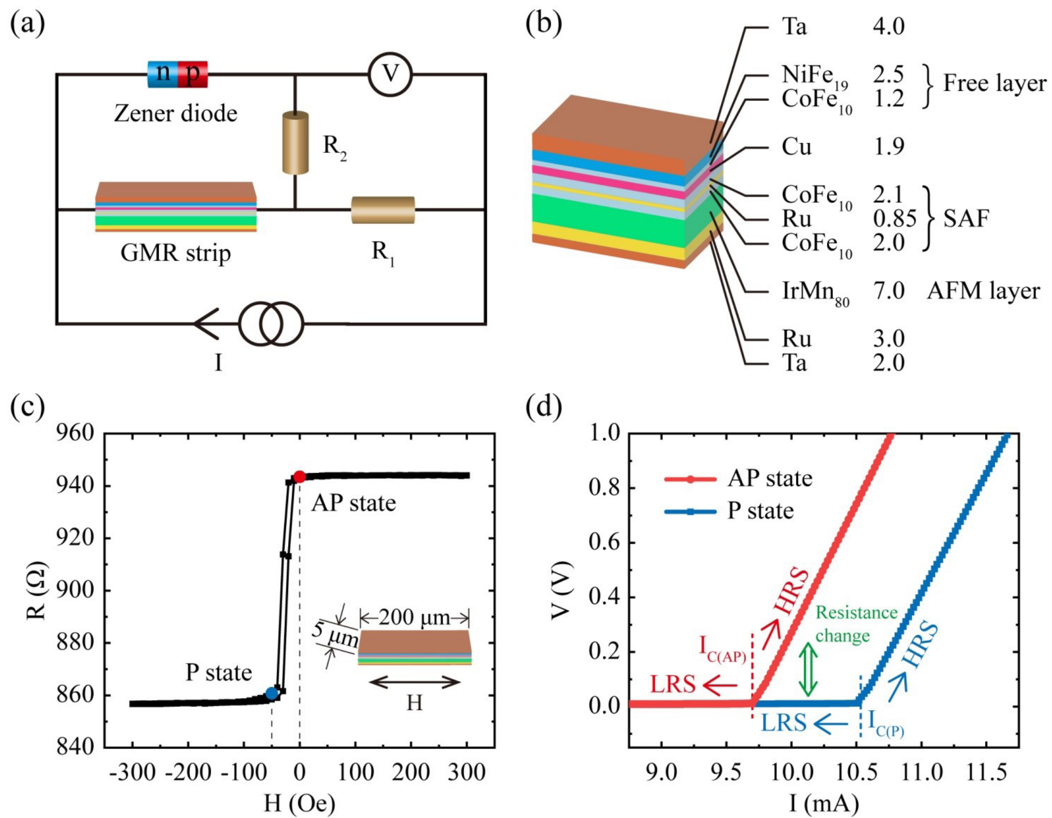

FIGURE 1. **(a) Schematic of the proposed DE-GMR structure to achieve GMR amplification. (b) Schematic of the GMR film stack. (c) R-H loop of the GMR strip. The inset shows the geometry of the GMR strip. (d) V-I curves of the proposed structure.**

the practical implementation. Recently, diode-enhanced MR effect has been reported to optimize both MR ratio and magnetic-field sensitivity [31]–[34]. However, semiconductor materials used for solving the resistor mismatching problem still limit the magnetic-field sensitivity. The complex four-terminal connection method and the use of stray field degrade the downscaling potential of the concept.

In this paper, we propose a diode-enhanced scheme of GMR amplification with high magnetic-field sensitivity, as shown in Fig. 1(a). MR ratio up to 6947% can be reached under a tiny magnetic field (e.g. 50 Oe) in a specially designed diode-enhanced GMR (DE-GMR) structure. A theoretical model describing the amplification behavior is also established, which can be the guidance to extend this scheme to other two-terminal MR devices. The influence of each element integrating in the scheme is experimentally investigated. Based on this scheme, reconfigurable logic functions with high reliability are implemented by amplifying the total resistance change of two GMR strips in different magnetic configurations. Two proofs of concept, AND and OR, are experimentally demonstrated by changing the working current. This scheme can be a promising candidate for building future in-memory computation architectures and can greatly reduce the power consumption for data traffic between memory units and processing units in traditional Von Neumann architectures.

II. DEVICE FABRICATION

Fig. 1(a) shows the schematic of the DE-GMR structure, in which a GMR strip is connected to a Zener diode and two resistors R_1 and R_2. The GMR film stack with high magnetic-field sensitivity illustrated in Fig. 1(b) is used [35]. From the substrate side, Ta(2)/Ru(3)/$IrMn_{80}$(7)/$CoFe_{10}$(2)/Ru(0.85)/$CoFe_{10}$(2.1)/Cu(1.9)/$CoFe_{10}$(1.2)/$NiFe_{19}$(2.5)/Ta(4) (numbers are nominal thicknesses in nanometers) is sputter-deposited on SiO_2 substrate with a base pressure less than 10^{-8} Torr. In this magnetic nanofilms, the $CoFe_{10}$/Ru/$CoFe_{10}$ part constitutes a synthetic antiferromagnetic (SAF) structure. The magnetization of the bottom ferromagnetic layer is pinned to the adjacent antiferromagnetic one by exchange coupling. The upper ferromagnetic layer is called the reference layer. The SAF layers and the composite free layer $CoFe_{10}$/$NiFe_{19}$ are separated by the nonmagnetic spacer layer Cu. The sample is annealed in a vacuum at 270 ° under a magnetic field of 1 T for 1 hour and patterned into strips with dimensions of 5 μm × 400 μm by photolithography and ion-beam etching. The longitudinal side of the strip follows the direction of the magnetic field used for annealing. The contact leads and pads are prepared by photolithography and E-beam evaporation with Cr(10 nm)/Au(100 nm). Fig. 1(c) shows the resistance versus external magnetic field (R-H) loop of the GMR strip. The magnetizations of the free layer and reference layer are antiferromagnetically coupled,

the GMR strip is thus in antiparallel (AP) magnetic configuration when no magnetic field is applied. A negative magnet field with a magnitude of 50 Oe is used to switch the magnetization direction of the free layer, thereby setting the GMR strip into parallel (P) magnetic configuration. The GMR ratio r is defined as

$$r = \frac{R_{AP} - R_P}{R_P} \times 100\% \tag{1}$$

where R_{AP} (R_P) is the resistance of the GMR strip when the strip is in AP (P) state. The GMR ratio of the strip is 9.62% within a tiny magnetic field change of 50 Oe.

III. RESULTS AND DISCUSSION

A. REALIZATION OF LARGE MR RATIO

Fig. 1(d) illustrates the voltage versus current (V-I) curves of the DE-GMR structure where V is the voltage measured by the voltmeter and I is the current supplied by the current source. R_1, R_2 and the critical voltage U_C of the diode are 1 Ω, 820 kΩ and 9.1 V, respectively. These values help to achieve a large MR ratio and will be analyzed in the following. All the transport properties are measured at room temperature with the magnetic field applied parallel to the GMR strip. We define the apparent resistance R as R=V/I. When the GMR strip is in AP state, the apparent resistance R of the structure has two resistance states. When the voltage dropping on the diode is smaller than U_C, the diode is OFF and can be considered as open circuit. The apparent resistance R is equal to R_1. When the voltage dropping on the diode exceeds U_C through increasing applied current, the diode is switched from OFF to ON. Current will flow through the diode and R_2, which leads to a sudden increase in apparent resistance R. These two states can be labelled as low resistance state (LRS) and high resistance state (HRS), respectively, and the critical transition current $I_{C(AP)}$ between LRS and HRS can be calculated by $I_{C(AP)} = U_C/R_{AP}$.

When the GMR strip turns to P state, another critical transition current $I_{C(P)} = U_C/R_P$ occurs due to the resistance change. Hence, when the applied current I is in the range of $I_{C(AP)}$ to $I_{C(P)}$, the intrinsic resistance change of the GMR strip under applied magnetic field induces a transition from LRS to HRS and leads to an enhancement of MR.

Similar to the MR definition of the GMR strip, the MR ratio of DE-GMR structure can be defined as

$$MR = \frac{R\,(H) - R\,(-50\ Oe)}{R\,(-50\ Oe)} \times 100\% \tag{2}$$

where R(H) is the apparent resistance under magnetic field H. Fig. 2(a) demonstrates the MR ratio with different applied currents. Fig. 2(b) summarizes the trend of MR as a function of current. The MR ratio first augments and then decreases rapidly as the applied current increases. The maximum MR occurs at $I_{C(P)}$, i.e. 10.6 mA. Thanks to the property that the magnetization of the GMR strip can be switched by a magnetic field as small as 50 Oe, our structure achieves an extremely large MR ratio (i.e. 6947%) with excellent magnetic-field sensitivity. This sensitivity is much higher than that of existing diode-based structures based on semiconductor materials [34].

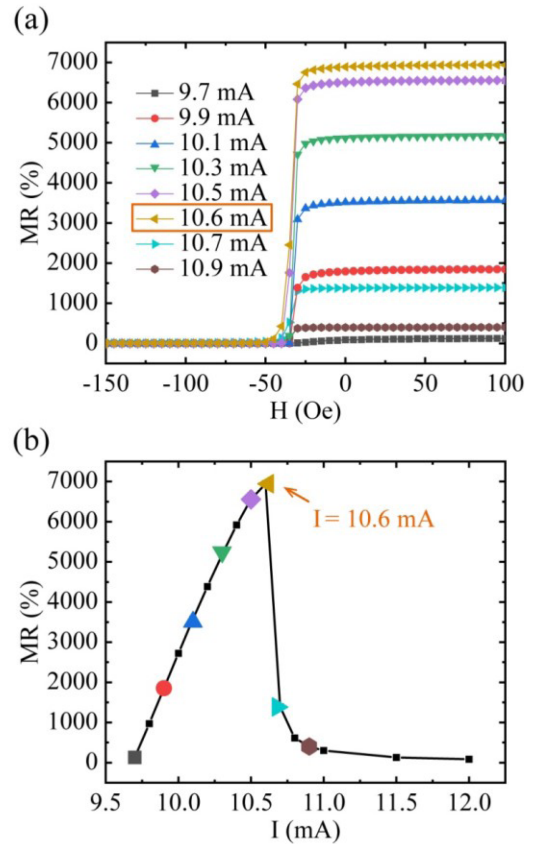

FIGURE 2. (a) MR measurement under different applied currents. Maximum MR occurs at 10.6 mA. (b) MR as the function of applied current. Coloured symbols correspond to the curves listed in (a).

B. ESTABLISHMENT OF THEORETICAL MODEL

The V-I curves and the value of maximum MR are closely related to the nonlinear transport property of the Zener diode, R_1, R_2, and GMR effect of the strip. By analyzing the equivalent resistance circuit, the V-I curves can be described by

$$V = \begin{cases} R_1 \times I\,(0 < I < \frac{U_C}{R_S}) \\ \frac{R_2 \times R_S}{R_2 + R_S} \times \left(I - \frac{U_C}{R_S}\right) + R_1 \times I(I > \frac{U_C}{R_S}) \end{cases} \tag{3}$$

where R_S is the resistance of the GMR strip and U_C is the critical voltage of the diode. The diode is regarded ideal. When R_S takes the value of R_{AP} and R_P respectively, two corresponding V-I curves can be obtained as Fig. 3(a), which are in good agreement with the experimental results illustrated in Fig. 1(d). According to the V-I curves obtained by (3), the dependence of MR on I can be calculated, as shown in Fig. 3(b). These results are consistent with the experimental results shown in Fig. 2(b).

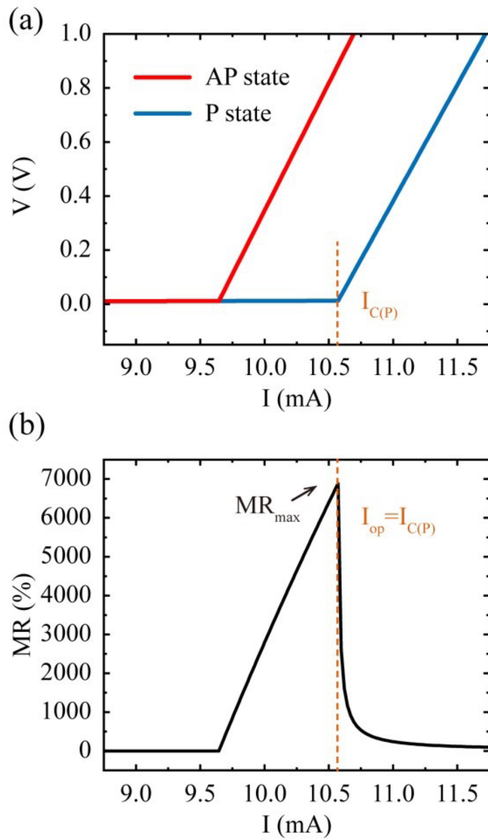

FIGURE 3. (a) Calculated V-I curves of the proposed DE-GMR structure. (b) Calculated relationship between MR and applied current. The optimum current value I_{op} to obtain maximum MR is $I_{C(P)}$.

We can further derive the maximum MR of the DE-GMR structure as follows:

$$MR_{max} = \frac{r}{1+r} \times \frac{R_2 \times R_{AP}}{R_2 + R_{AP}} \times \frac{1}{R_1} \tag{4}$$

where r is the GMR ratio of the strip and R_{AP} is the resistance of the GMR strip when the strip is in AP state. The subscript "max" of MR indicates that the applied current is selected as the optimum value I_{op} to obtain the maximum of MR in each condition. I_{op} equals the critical transition current $I_{C(P)}$ when the GMR strip is in parallel magnetic configuration and can be calculated by

$$I_{op} = I_{C(P)} = \frac{U_C}{R_P} \tag{5}$$

where R_P is the resistance of the GMR strip when the strip is in P state. We find that the MR_{max} increases as the intrinsic GMR of the strip increases. This confirms that the magnetic response of the DE-GMR structure arises from the GMR strip.

We then study the relationship between the MR_{max} and R_1, R_2, R_S, and the Zener diode, respectively. First, we vary R_1 with different resistance values to analyze the dependence of MR_{max} on R_1. Fig. 4(a) demonstrates the results when U_C and R_2 are fixed to 9.1 V and 820 kΩ. Since LRS is determined by the value of R_1, a smaller R_1 increases the contrast between HRS to LRS, resulting in a higher MR ratio. As elucidated from (4), MR_{max} is inversely proportional to R_1, which is in good agreement with the experimental results. It should be noted that MR_{max} is very sensitive to the value of R_1 for R_1 less than 10 Ω. Therefore, the impact of contact resistance should thus be taken into consideration, which can be demonstrated by the error bars of the curve in Fig. 4(a). The contact resistance is estimated to be about 0.4 Ω according to the fitting results.

Fig. 4(b) shows the impact of R_2 on MR_{max} when U_C and R_1 are fixed to 9.1 V and 1 Ω. Contrary to the effect of R_1, R_2 affects the value of HRS. A large R_2 increases the difference between HRS to LRS, thus improving the MR ratio. When $R_2 \gg R_{AP}$, equation (4) can be simplified to $\frac{r}{1+r} \times \frac{R_{AP}}{R_1}$ mathematically, which provides the upper limit of MR_{max} that can be obtained by tuning R_2. This trend can also be confirmed by the experimental results. We find that MR_{max} reaches the upper limit when R_2 is larger than 5 kΩ.

We also fabricate a series of GMR strips with different lengths to study the relationship between MR_{max} and R_S. Here, we choose R_{AP} to represent R_S and R_P is determined by R_{AP} and r. R_1, R_2, and U_C are fixed to 1 Ω, 820 kΩ, and 9.1 V, respectively. The R_S plays the similar role as R_2 to improve the difference between HRS and LRS. Since the selected R_2 is even much larger than the maximum value of this series of R_{AP}, the equation can be simplified as $\frac{r}{(1+r)\times R_1} \times R_{AP}$. This indicates that MR_{max} is proportional to R_{AP}, which conforms to the measured results shown in Fig. 4(c). The variation between the experimental results and perfect linear relationship is due to the fact that the MR ratios in different GMR strips are not exactly identical after the nano-fabrications.

Fig. 4(d) illustrates the MR_{max} with different U_C when R_1 and R_2 remain at 1 Ω and 820 kΩ. The GMR strip applied here is the same with that shown in Fig. 1(c). The MR_{max} increases with the augmentation of U_C. However, according to (4), the MR_{max} should not be directly related to U_C. Here, the critical factor is the sharpness of the resistance transition of the diode, rather than the value of U_C. The inset of Fig. 4(d) provides two cases with different U_C to clarify this point. Compared with the diode with U_C of 4.3 V, the diode with U_C of 9.1 V possesses sharper resistance transition and induces sharper V-I curves of the DE-GMR structure. Much higher MR ratio is then obtained thanks to this sharper transition from LRS to HRS.

IV. IMPLEMENTATION OF RECONFIGURABLE LOGIC OPERATION

In addition to GMR amplification, reconfigurable logic function can also be realized based on our proposed scheme. As demonstrated in Fig. 5(a), two series-connected GMR strips replace the original single strip and work as two inputs in the circuit. R_1, R_2, and U_C are fixed to 1 Ω, 820 kΩ, and 9.1 V, respectively. The AP and P states of the GMR strip are regarded as logic input '1' and '0'. Note that the magnetization directions of the two strips' reference layers are set

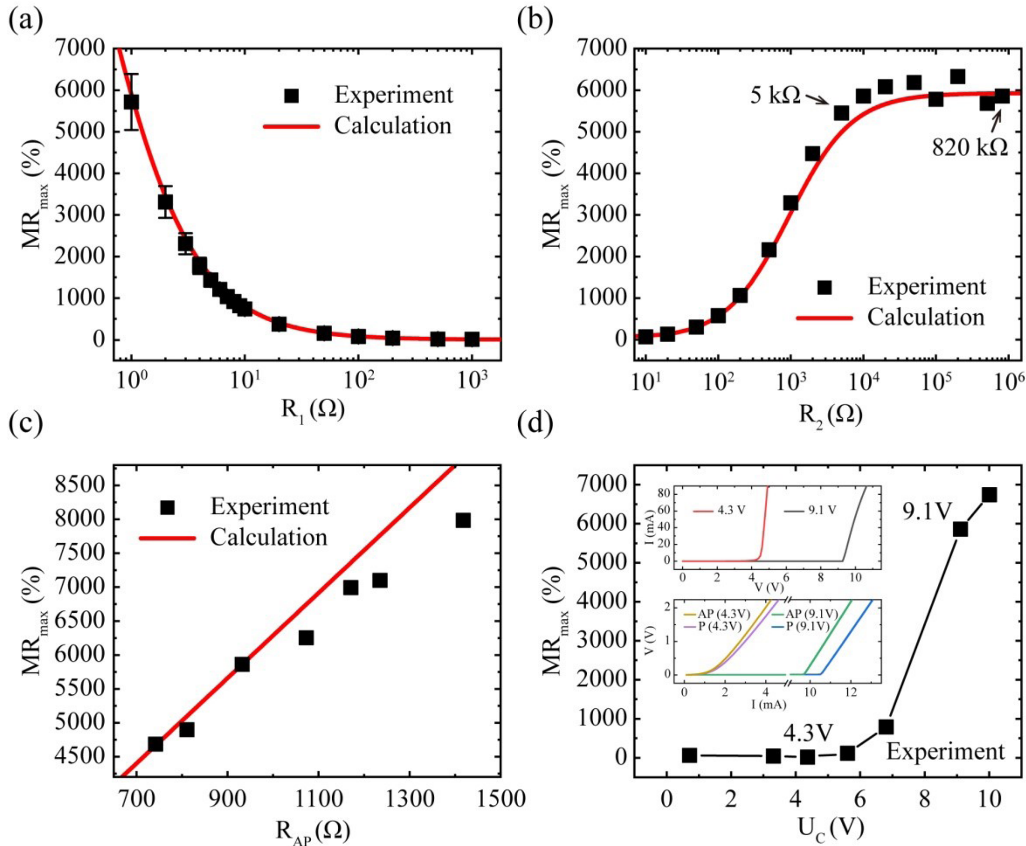

FIGURE 4. (a) Maximum MR as the function of R_1. The error bars reflect changes of contact resistance in different measurements. (b) Maximum MR as a function of R_2. (c) Maximum MR as the function of R_{AP}. (d) Maximum MR as a function of U_C. The above inset shows transport property of the Zener diode with different critical voltages. The below inset shows V-I curves of the structures with different Zener diodes.

to be opposite to each other for experimental demonstration. We anneal two strips in the same magnetic field and rotate one of them by 180°, then the two strips are connected by wire bonding. Fig. 5(b) shows the R-H measurement of the connected two GMR strips. The initial states of the two strips are both set to be AP, which correspond to the input (1,1) with the largest resistance value. When the magnetic field exceeds 50 Oe, the free layer of one of the strips is switched. Two GMR strips are then in P and AP states, corresponding to (1,0). Meanwhile, the input (0,1) is realized under the opposite magnetic field. It is worth noting that a slight difference between the input (1,0) and input (0,1) is owing to the possible distinction of two patterned GMR strips. When the magnetic field is 3000 Oe, the total resistance is smaller than other cases and can be regarded as (0,0). Thus, we set the two logic inputs to (0,1), (1,1), (1,0), and (0,0) by applying different magnetic fields.

Fig. 5(c) shows the V-I curves of the proposed circuit with these four sets of logic inputs. The critical voltage separating logic output '0' and '1' is 130 mV. Different logic function can be implemented by simply changing the working current. For example, setting the working current to 6.1 mA can achieve logic function AND. For the case of logic input

TABLE 1. Truth table for different logic functions.

Logic Input		Logic Output (mV)	
i	j	AND I=6.1 mA	OR I=6.4 mA
0	0	0 (V=7.040)	0 (V=8.375)
0	1	0 (V=7.371)	1 (V=277.236)
1	0	0 (V=7.528)	1 (V=333.808)
1	1	1 (V=252.299)	1 (V=711.175)

(1,1), the output voltage is 252.299 mV > 130 mV and the logic output is '1'. For the other cases, the output voltage is about 7 mV and the logic output is '0'. Similarly, a working current of 6.4 mA can put the output voltage of (0,1), (1,0), (1,1) in the same logic level and achieve the logic function OR. The detailed configurations are summarized in Table 1. The logic output can be amplified by complementary metal oxide semiconductor (CMOS) and be written into the target memory unit by fast and energy efficient magnetic writing process, such as spin transfer torque (STT) [36], [37] or spin orbit torque (SOT) [38]–[40]. In these mechanisms, the change of current direction can work as logic function NOT. Logic function NAND and NOR can thus be implemented.

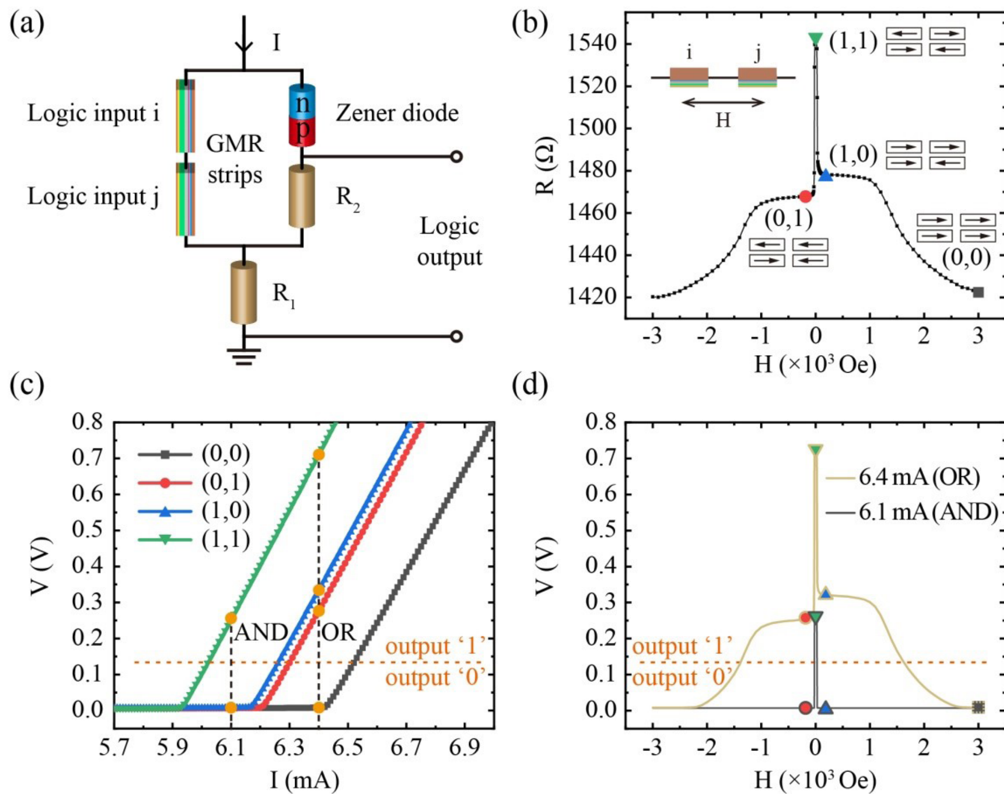

FIGURE 5. (a) Circuit schematic for realizing reconfigurable logic functions. (b) R-H measurement of two connected GMR strips. (c) V-I curves of the proposed circuit with four sets of logic inputs. Two vertical dashed lines indicate the working currents for logic function AND and OR. The horizontal dashed line indicates the critical voltage separating logic output '0' and '1'. (d) Output voltage measurements under different working currents. Coloured symbols correspond to the four logic input states shown in (b).

V. DISCUSSION

The proposed scheme has the following advantages for practical applications. From the point of view of integration density, our proposal applies the two-terminal connection method instead of the four-terminal connection method that is normally used in the existing diode-based structures [32], [34]. The two-terminal connection method is more suitable for integrating a large number of units into an array. In addition, as our logic implementation does not rely on the fringe field of nanomagnets, the scaling of the array will not be limited by the magnetic perturbation between two neighbouring logic units. More importantly, since most of the mainstream MR devices are two-terminal structures, our proposal can be easily extended to other MR devices. Nanoscale MR devices can be used to improve the integration density, and the proposal can also benefit from the further improvement of the magnetic-field sensitivity of the MR devices. From the point of view of reliability, a high contrast between different logic outputs can be achieved thanks to the GMR amplification, as shown in Fig. 5(d), and a tiny fluctuation in working current will not change the results of logic functions, as shown in Fig. 5(c). The logic reliability can thus be greatly improved compared to prior work [32], [34] and other spin-based logic devices [41]. Moreover, since the working currents are not larger than the critical transaction current when the two strips are both in parallel magnetic configuration, as shown in Fig. 5(c), using MR devices with high resistivity and diodes with low U_C can help to reduce the working current as well as the required supply voltage, thereby reducing the energy consumption.

Finally, our scheme can be further optimized. According to (3), R_1 can be removed for simplicity and the functions of our scheme will not change. The reason we take R_1 into consideration is to avoid the dramatic change of the MR ratio induced by the tiny variation of the contact resistance in different measurements, which can lead to the disturbance to our analysis. Equation (3) also reminds us that R_2 does not need to be much larger than R_{AP} if R_{AP} is large enough, allowing us to extend this scheme to a MR device with several thousand ohms. For example, if a magnetic tunnel junction (MTJ) of 7 kΩ [42]–[45] is used, R_2 can be further reduced to about 1 kΩ and a MR ratio with the same order of magnitude as this DE-GMR scheme can be achieved.

VI. CONCLUSIONS

In summary, by combining the GMR effect with the nonlinear transport property of diode, both large MR ratio (e.g. 6947%) and high magnetic-field sensitivity (e.g. 50 Oe) are achieved

in the proposed scheme. The amplification behaviour and the dependences of MR ratio on various integrated elements have been experimentally investigated, which can also be well described by a theoretical model. We then validate the functionality of reconfigurable logic based on the proposed scheme. Performance advantages and further optimizations have been discussed as well. This work can help to build future high-performance computing systems.

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(Jiang Nan and Kun Zhang contributed equally to this work.)

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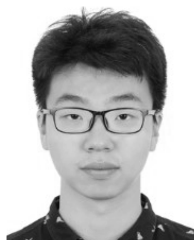

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