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A Study of Transient Voltage Peaking in Diode-Based ESD Protection Structures in 28nm CMOS

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ABSTRACT Transient voltage peaking under very fast electrostatic discharge (ESD), like charged device model (CDM) pulse, is a serious problem to integrated circuits (ICs). A combined TCAD simulation and very fast transmission line pulse (VFTLP) testing method is proposed to thoroughly investigate the transient voltage peaking phenomena of diode-based ESD protection structures under CDM stressing. The study of a set of diode, diode-string and diode-triggered silicon-controlled rectifier (DTSCR) ESD protection structures, fabricated in a 28nm CMOS process, reveals that the inductive impedance along the ESD discharging path may be the root cause of voltage peaking under CDM stressing. The observation provides the design insights overcoming the voltage peaking problem in ESD protection designs before complicate CDM package level testing.

INDEX TERMS Charged device model (CDM), ESD protection, TCAD, very fast transmission line pulse (VFTLP), voltage peaking.

I. INTRODUCTION

Continuous and aggressive scaling in CMOS technologies makes ICs at advanced nodes extremely sensitive to ESD failures [1]–[7]. At sub-28nm nodes, the very high integration level, narrow metal interconnects and extremely thin gate oxide, as well as the fins in FinFET are all very vulnerable to ESD surges [3]. Particularly, the ultra-thin gates can be easily damaged by the super-fast CDM transient spikes, which is an emerging challenge in ESD protection designs for advanced ICs and becomes a sizzling research topic in the field [3]–[12]. For IC designers, simplicity is always the golden rule in circuit designs. Accordingly, diodes have been widely used for on-chip ESD protection in practical designs due to the simple device structure, triggering mechanism and I-V characteristics, and relatively small size and low parasitic capacitance. Therefore, diodes and diode-based ESD protection structures, including diode string, diode-triggered SCR and other diode derivatives, are popular for IC products. A commonly used full-chip ESD protection scheme has double diodes at I/O with a power clamp, which works well for most HBM and CDM ESD protection needs. In advanced CMOS technologies, commonly available diode structures are P+/N-well (PPNW) and N+/P-well (NPPW) diodes with shallow trench isolation (STI) or gate isolation (gated diode), each has its own pros and cons [3]. Typically, a diode string or a DTSCR ESD protection structure utilizes either STI-diode or gated-diode to control ESD triggering. However, it is reported that, under CDM ESD stressing that features extremely fast pulse rise time (t_r∼200ps) and very short pulse duration (t_{d1}∼1ns for the first peak) [13], transient voltage peaking right before the ESD triggering may occur that causes early ESD failures due to the delay in ESD triggering and rupture in the thin gate oxide [8]–[12]. Transient voltage peaking becomes a major CDM ESD protection design problem for ICs at sub-28nm nodes, which must be thoroughly understood. This paper presents a comprehensive study of transient voltage peaking of different diode-based ESD protection structures in 28nm CMOS under very fast ESD stressing, which was investigated using a new combined TCAD simulation and VFTLP testing method. The paper is organized as following: After the Introduction,

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Section II analyzes the voltage peaking in stand-alone STI diodes and gated diodes by TCAD simulation and VFTLP measurement. Section III discusses the voltage peaking behaviors in diode-based ESD protection structures, such as diode string and DTSCR, followed by the Conclusion.

II. VOLTAGE PEAKING IN DIODE ESD STRUCTURES

At high frequency, a PN junction diode may exhibit inductive characteristics possibly due to conductivity modulation [14]–[16]. In addition, the N/P-well pick-up regions will also have inductive effects under fast ESD stressing. These inductive effects in the ESD discharging paths, which delays the turn-on process of PN junction of ESD devices, may result in voltage peaking behaviors, particularly under ultra-fast CDM ESD stressing, leading to on-chip ESD failures not predicted by VFTLP testing for a standalone ESD protection structure. This CDM ESD failure problem, possibly associated with the voltage peaking caused by delay in the turn-on process of ESD devices, is an emerging challenge in CDM ESD protection designs. Commercial TLP and VFTLP testers for HBM and CDM ESD measurements, while intended for transient ESD characterization, actually rely on a quasi-static testing mechanism, i.e., the measured transient voltage under TLP or VFTLP pulsing is extracted by averaging the waveform across the 20% to 80%, typically, period in the time domain. While this 20%-80% averaging method may be reasonable for a relatively slower and longer ESD pulse, e.g., HBM, it may not be adequate for a much faster and shorter ESD pulse, e.g., CDM. It is highly possible that the above inductive characteristics in an ESD discharging path under ultra-fast ESD stressing may substantially delay the full ESD discharging turn-on and conduction [17], resulting in possible significant voltage peaking within the first 20% time period of an ESD waveform. As such, this CDM voltage peaking effect may not be captured by VFTLP testing. To understand this mysterious CDM voltage peaking behavior, a set of diodes ESD protection devices, including N+/P-well (NPPW) and P+/N-well (PPNW) with both STI and gated isolation, were designed and fabricated in a foundry 28nm CMOS technology for an investigation in this study. The 28nm CMOS technology features V_{DD} of 0.85V and BV_G of 2.9V, which sets the ESD Design Window. Table 1 summarizes the diode design split parameters in this work. We found that, often, the CDM voltage peaking cannot be captured correctly by the existing commercial VFTLP tester due to the specification incompliance with the industrial CDM ESD testing standards [4]. Meanwhile, TCAD simulation may not be accurate without thoroughly calibration by VFTLP measurement. Therefore, we propose a new combined TCAD simulation and VFTLP testing method to better understand the CDM voltage peaking phenomena in CDM ESD protection circuit designs, which proves to be efficient and accurate enough for this study. In this work, Synopsys 2D TCAD tool was used to for process, device building and transient ESD simulation, and a VFTLP tester (Barth 4012 VFTLP+ Very Fast High-Speed Pulse Curve Tracer) was used to characterize very fast ESD stressing behaviors of ESD structures at die level using a GS probe. CDM ESD stressing with 125V voltage level was selected for the study.

TABLE 1. Design splits for the diode ESD protection structures.

Types	Finger Length (μm)	Finger Width (μm)	STI/Gate Length (μm)	Finger Number	Total Perimeter (μm)
NPPW	0.5	20	0.15	3	120
PPNW	0.5	20	0.15	3	120

A. CDM SIMULATION BY TCAD

Fig. 1 depicts the common CDM testing setup and the classic CDM pulse waveform used in this work, which is based on the ESDA/JEDEC CDM test standard [13]. In the standard, with a small verification module, the peak current for a 125V test condition is 1.0-1.6A and the pulse rise time is less than 350ps. For TCAD simulation purpose, the important portion (the first peak) of the CDM pulse waveform (t_r~200ps, t_{d1}~1ns and peak current of 1.4A) was used as the injected current pulse directly into the Si anode of the diode ESD protection structures including the STI and gated PPNW and NPPW diodes. No local metal interconnects were used in simulation in order to eliminate any possible metal-induced inductive effect. Fig. 2 shows the simulated cross-sectional

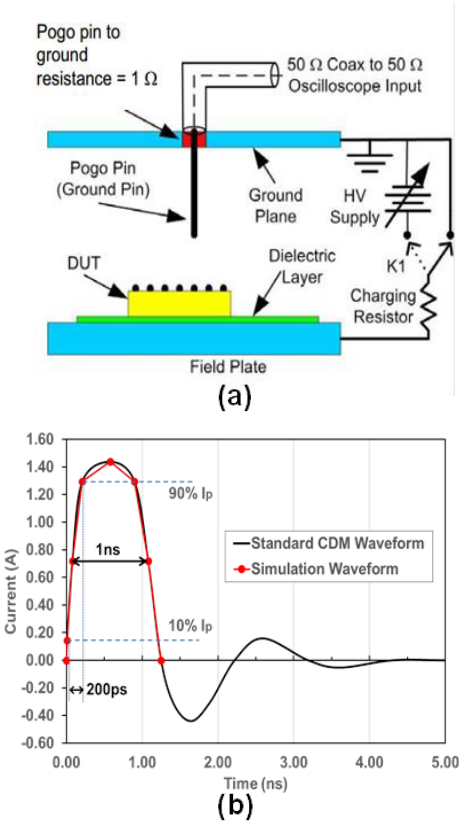

FIGURE 1. A common CDM ESD test setup (a) and a typical CDM ESD waveform per JEDEC CDM standard used in this work.

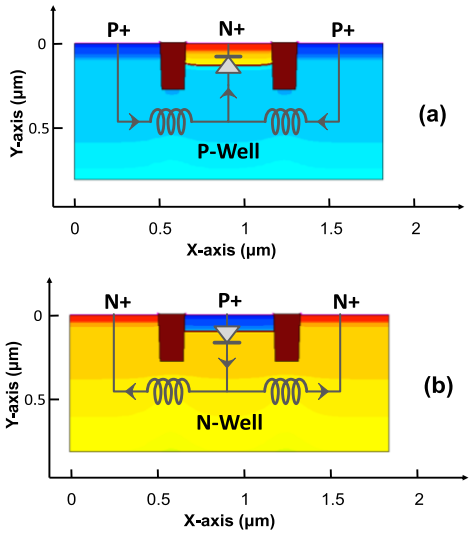

FIGURE 2. Cross-sections for a NPPW ESD diode (a) and a PPNW ESD diode (b) with doping concentration by TCAD simulation. The parasitic inductance effect is modeled by an equivalent circuit.

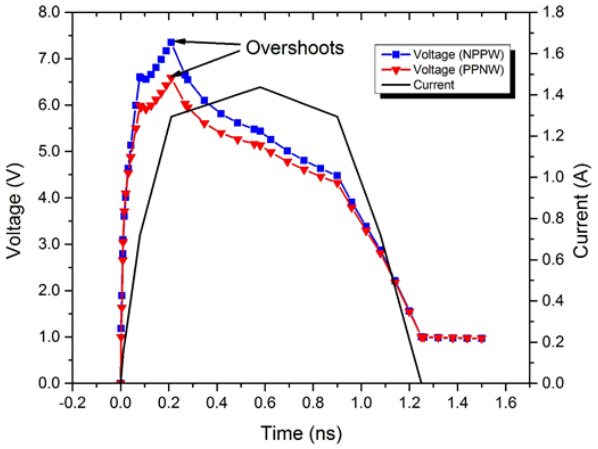

FIGURE 3. The transient voltage waveforms by TCAD simulation for sample STI diodes shows voltage peaking under 125V CDM ESD stressing.

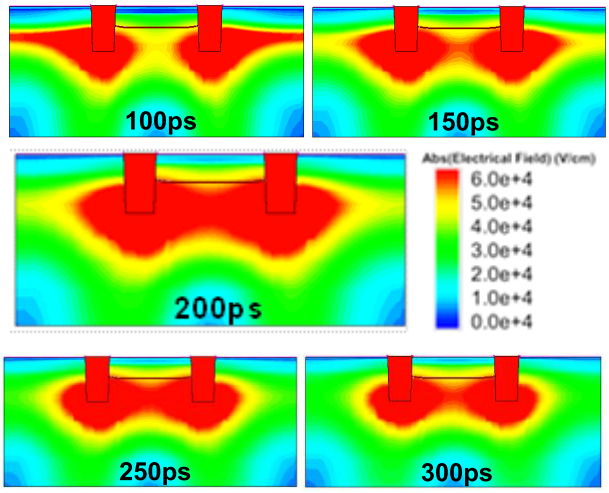

FIGURE 4. Simulated transient electrical field distribution for sample STI NPPW diode reveals the ESD triggering procedures in the time domain.

structures for the STI NPPW and PPNW ESD diodes. The embedded electrical features including junctions, inductance and capacitance are considered in device physics based TCAD simulation. It is believed that the intrinsic capacitance (∼50fF) of the junction and parasitic inductance (∼5pH) of the doped long path may cause significant delay of ESD turn-on process. The simplified equivalent RLC circuit model before diode turn-on features a ∼300GHz underdamped transient resonance, which is much faster than the ESD triggering process, leading to the observed voltage peaking before the ESD triggering. The CDM ESD discharging behavior was first simulated for the diode ESD protection devices, i.e., the devices under test (DUT), by TCAD ESD simulation, which is presented in Fig. 3 for the sample STI NPPW and PPNW diodes. From the time-domain CDM simulation results, it is readily observed that voltage peaking of up to 7V for both ESD diodes occurred well before the peak of the source CDM current pulse that is at about 200ps. Clearly, it takes some time to fully trigger the ESD diodes under the CDM stressing, which is attributed to the inductive effects that lead to the voltage peaking. The variation in voltage peaking for the two different ESD diodes may be attributed to the varying parasitic inductive effect, likely associated with different carrier mobilities in the PW and NW diffusion regions. Since the transient voltage peaking occurs well before the ESD protection structure is turned on, the large voltage spike may cause a dielectric damage to the CMOS gate, a typical CDM ESD failure signature in CMOS.

To understand the voltage peaking mechanism, we explored the transient electrical behaviors by TCAD simulation, which can identify the inductive effect that causes discharging delay. Fig. 4 depicts the simulated transient electrical field density inside a sample NPPW diode with STI isolation at different times before and after the voltage peaking at around 200ps. Dynamic observation reveals that the high electrical field density cloud inside the diode gradually moves towards the intrinsic PN junction boundary as time goes and reaches it at 200ps when the voltage peaks. This is attributed to the parasitic inductive effect within the ESD diode where the ultra-fast CDM transient is postponed in reaching to the intrinsic PN junction of the NPPW ESD diode structure. Since only the Si structures were simulated, the inductive effect must come from the diffusion regions of the STI diode ESD structures, not any local metal interconnects. This translates into a delay in triggering the ESD diode under CDM stressing and driving it into full ESD discharging conduction. After the ESD diode is turned on, it creates a low-impedance conduction channel to discharge the CDM pulse quickly, hence, the electrical field density inside the diode will drop accordingly as shown in Fig. 4. From this model, apparently, the delay in ESD triggering, i.e., the level of the voltage peaking, will be directly affected by the length of the ESD discharging path, i.e., the distance from the pad to the intrinsic PN junction of the diode ESD protection structure. To validate this new model, TCAD simulation

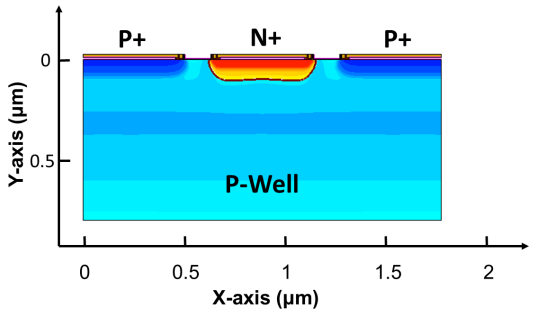

FIGURE 5. Simulated cross-section for a sample NPPW gated ESD diode.

using the same ESD stimuli was conducted for gated NPPW and PPNW diode ESD protection structures. For meaningful comparison, the lateral spacing of gated diodes is set the same as the STI diodes. Fig. 5 shows the simulated cross-section for a sample gated NPPW diode. Fig. 6 depicts the simulated CDM discharging behaviors for both gated NPPW and PPNW diodes under the same 125V CDM stress, which shows that the observed voltage peaking is about 2.6V, much weaker than 7V for the STI diodes. This can be explained that the actual internal conduction path for a STI diode is much longer than that in a gated diode due to the trench depth, as shown in Fig. 2 and Fig. 5. Therefore, the possible internal inductive effect is much stronger for the STI diodes than that for the gated diodes. This can be confirmed by the simulated electrical field density depicted in Fig. 7 where the heavy electrical field density could reach the intrinsic PN junction at around 100ps, much earlier than 200ps observed in its STI diode counterpart. Therefore, due to the significantly shorter conduction path, the parasitic inductive effect is much weaker in a gated diode, resulting in a faster turn-on of the gated diode compared with the STI diode. For the same reason, the difference in the mobility-induced internal inductance in the two different gated diodes with very short discharging paths is not significant, hence, no noticeable difference in the voltage peaking as shown in Fig. 6. This study suggests that, due to possible inductive effect, the inner diode structure may play a key role in preventing the troublesome voltage peaking problem in CDM ESD protection designs. Since only the Si structures of the ESD didoes were simulated without any local metals, it eliminates the possible metal-induced inductive effect that may cause the voltage peaking as reported [18], [19].

B. VFTLP MEASUREMENTS

CDM ESD zapping is commonly modelled by VFTLP testing before final CDM testing for a packaged IC product. A Barth 4012 VFTLP tester was used in this work. A VFTLP tester should comply with the CDM ESD test standard. Unfortunately, due to the extremely fast pulse nature, commercial VFTLP testers do not completely satisfy with the industrial CDM testing standards. In this work, we carefully set the pulsing conditions of the VFTLP tester to be the same as

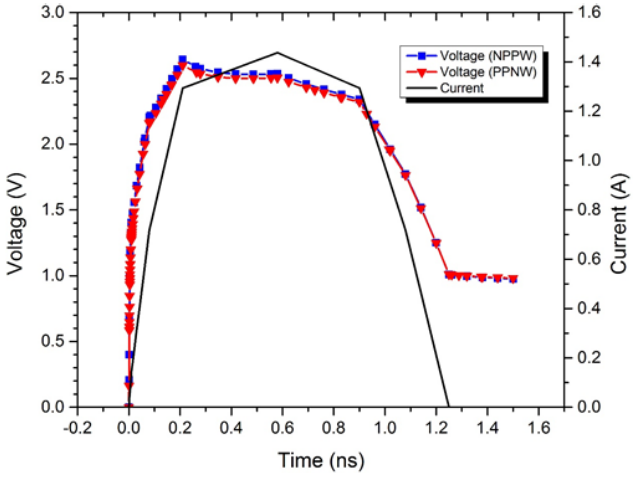

FIGURE 6. Simulated voltage waveform for sample gated ESD diodes under 125V CDM stressing.

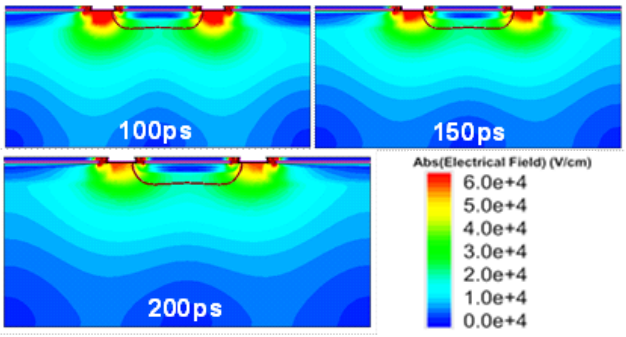

FIGURE 7. Simulated transient electrical field distribution for a sample NPPW gated ESD diode reveals the ESD triggering procedures.

the CDM test standard, i.e., a pulse duration of t_d~1ns and a rise time of t_r~200ps. However, the actual pulse waveform obtained from the VFTLP tester can be quite different from its ideal specs. For example, as shown in Fig. 8, for the selected 125V CDM ESD zapping target with a peak current

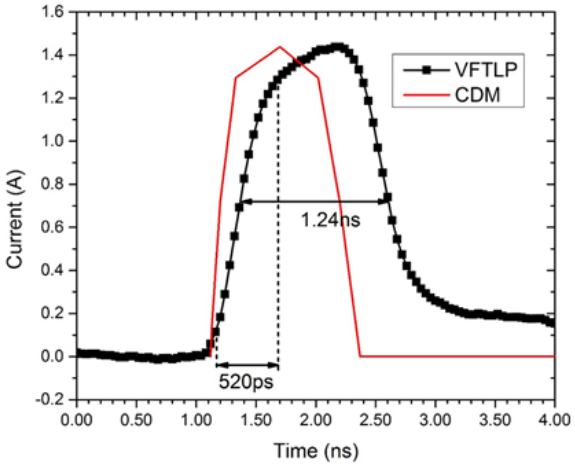

FIGURE 8. The CDM ESD discharging waveforms show substantial difference between an industrial CDM testing standard and a commercial VFTLP tester.

of about 1.4A, the actual pulse for the VFTLP tester are t_d~1.24ns and t_r~520ps, respectively, quite a bit off the CDM test standard. Especially, t_r~520ps is much longer than the t_r = 350ps limit set by the CDM test standard. This may be caused by the pad (100μmX100μm with all stacked metal layers) capacitance and the unpredictable DUT impedance in real tests. The setup parameters for a VFTLP tester are defined for the ideal condition, but in real world, the testing pulse produced may be varying. We expect that the significant timing difference between the CDM standard and a real-world VFTLP tester will cause substantial time domain errors in VFTLP measurements, which was confirmed in our VFTLP testing. Fig. 9 presents the VFTLP-measured transient voltage and current waveforms for sample PPNW and NPPW ESD diodes using both STI and gate isolation methods. Though the local metal interconnects for testing purpose may introduce more inductance and result more significant voltage peaking, there is still no transient peaking was observed, which were predicted by the TCAD simulation for the Si-only devices. In the experiment, the local metal interconnects for all ESD structures studied in this work were minimized and kept to be the same in layout, as much as possible, so that any metal-induced inductance, if any, can be de-embedded in VFTLP testing comparison. We believe that this was due to the fact that the actual rise time of the pulses generated by the VFTLP tester was too slow compared to the CDM testing standard. As such, the averaging method used by the VFTLP tester failed to catch the possible transient peaking in measurements, causing a serious transient ESD measurement error. On the other hand, across the macro scale of the pulse duration, the measured waveforms by VFTLP can still show that the overall voltage level for the STI diodes are higher than that for the gated diodes, due to the shorter path of gated isolation. This observation confirms that ESD testing conditions are critical to analyzing ultra-fast CDM ESD zapping phenomena. However, when using existing VFTLP testers, one must be very cautious in interpreting the complex and super-fast timing details in practical CDM ESD protection designs, and this is where TCAD simulation will help.

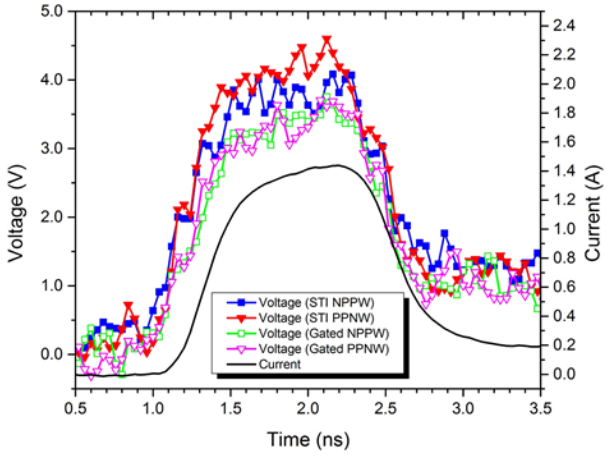

FIGURE 9. VFTLP-measured transient voltage and current waveforms for sample STI and gated ESD diodes fabricated in a 28nm CMOS.

III. DIODE-BASED ESD PROTECTION STRUCTURES

To further understand the transient voltage peaking mechanism related to the parasitic inductive effects, we further investigated a few diode derivatives, i.e., diode string and DTSCR ESD protection structures where the embedded diodes determine the ESD triggering. We expected that the parasitic inductance along the internal ESD discharging path from the pad to the intrinsic PN junction of a diode string and a DTSCR structure will affect the transient voltage peaking phenomena. The same combined TCAD simulation and VFTLP testing method was applied to the diode string and DTSCR ESD protection structures fabricated in the 28nm CMOS technology. The same CDM ESD target of 125V was used.

A. DIODE STRING ESD PROTECTION STRUCTURES

A diode-string ESD protection structure is used to boost the ESD triggering voltage (V_{t1}) to accommodate the core circuits. While a diode-string is advantageous in terms of simplicity and lower parasitic capacitance, it increases the total series resistance that worsens the overheating effect during ESD stresses. Importantly, it is expected that the parasitic built-in inductance in a diode-string ESD protection structure will be worse due to a longer conduction path. In this work, various diode-string ESD protection structures with 2, 3 and 4 diodes were designed and fabricated for a comparison study. Table 2 summarizes the design split parameters for the diode-string ESD protection structures characterized. Fig. 10 depicts simulated cross-section for a sample diode-string ESD protection structure consisting of three NPPW STI diodes. Fig. 11 shows the TCAD-simulated transient voltage responses for the 2/3/4-diode diode-string ESD protection structures under 125V CDM stressing. The zoom-in figure within up to the initial 300ps allows observing the transient voltage details during the ESD triggering phase. It is observed that the level of transient voltage peaking varies according to the number of diodes in a diode string and can reach to 40V for a 4-diode diode string per TCAD simulation. The diode-string ESD structures designed all failed 125V CDM ESD stressing due to much higher total series discharging resistance that led to overheating, so only the first 300ps waveform are shown here. The voltage peaking seems

TABLE 2. Design splits for STI diode string ESD protection structures.

Type	Finger Length (μm)	STI/Gate Length (μm)	Perimeter (um)	Diode Number
NPPW Diode String	0.5	0.15	20	2
	0.5	0.15	20	3
	0.5	0.15	20	4

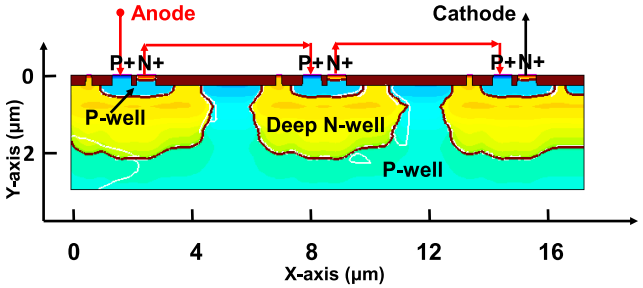

FIGURE 10. Cross-section of a sample 3-diode (3D) diode-string ESD protection structure simulated.

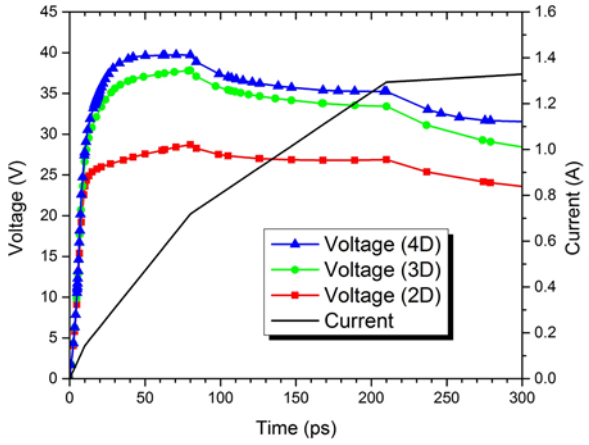

FIGURE 11. TCAD-simulated voltage waveforms for sample diode-string ESD protection structures show voltage peaking.

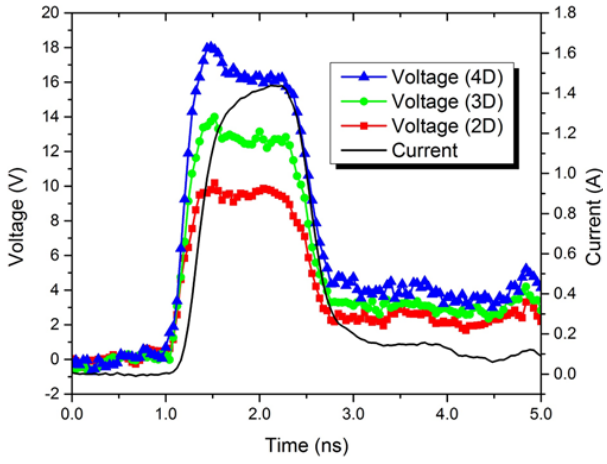

FIGURE 12. VFTLP-measured voltage waveforms for sample diode-string ESD protection structures show voltage peaking.

saturated when the diode number reaches four, which may be because the parasitic capacitance from complex connection above and P/N-well structures below results in better conductivity under fast pulse. Fig. 12 presents the measured transient voltage waveforms for these diode-string ESD structures from VFTLP testing. Clear voltage peaking was observed for these diode-string ESD protection structures, e.g., ∼18V for a 4-diode diode string, which is though lower than that from TCAD simulation. The discrepancy between simulation and testing is largely attributed to the difference of stress pulse speed. In general, both simulation and VFTLP testing clearly indicate that the transient voltage peaking is directly related to the number of diodes in a diode-string ESD structure, which is due to the varying parasitic inductance effect along the varying-length internal ESD discharging paths.

B. DTSCR ESD PROTECTION STRUCTURES

An SCR ESD structure is efficient in ESD discharging due to its unique snapback ESD discharging I-V behavior and very low discharging resistance. However, an intrinsic SCR structure typically has fairly high V_{t1}, making SCR ESD protection structure not suitable for low-voltage ICs. A DTSCR utilizes embedded diode(s) to reduce the ESD triggering voltage, hence, becomes interesting to advanced IC designs. The embedded diodes may be of various fashions in a SCR ESD protection structure to meet the design requirements. Apparently, the internal parasitic inductance associated the embedded diode(s) may cause delay in ESD triggering and, hence, transient voltage peaking in a SCR structure. In this work, we designed and fabricated a set of DTSCR ESD protection structures in 28nm CMOS for a comparison study. Table 3 summarizes the design split parameters for the DTSCR structures, containing 1, 2 and 3 embedded diodes of NPPW and PPNW types with STI and gated isolation, (i.e., 1DTSCR, 2DTSCR and 3DTSCR) respectively. These DTSCR structures were studied by TCAD simulation and VFTLP testing for 125V CDM ESD stressing. Fig. 13 illustrates the cross-section and external connections for a sample DTSCR using two PPNW diodes (2DTSCR) of STI and gated isolation, respectively. During ESD zapping, the embedded diodes will be triggered first, which leads to turn-on of the 2DTSCR eventually. As such, the internal parasitic inductance along the triggering-diode, varying according to the numbers and structural details of the diodes, may cause transient voltage peaking in a DTSCR, which is investigated using the combined TCAD simulation and VFTLP testing method. Fig. 14 shows the TCAD-simulated transient voltage

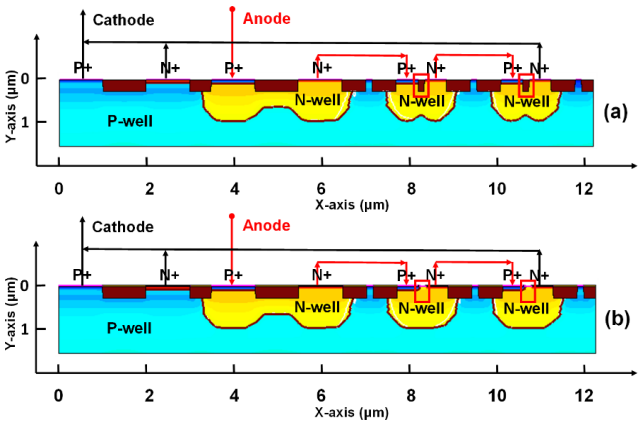

FIGURE 13. TCAD-simulated cross-sections for sample 2-diode STI DTSCR (a) and 2-diode gated-diode DTSCR (b) ESD protection structures.

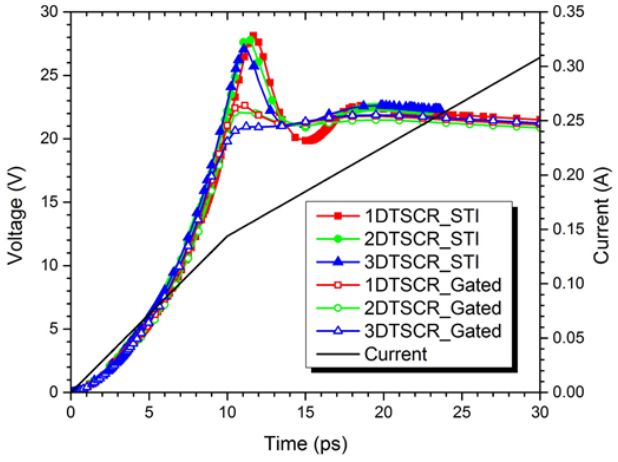

FIGURE 14. TCAD-simulated voltage waveforms for sample DTSCR ESD protection structures under 125V CDM ESD stressing show voltage peaking.

waveforms under 125V CDM ESD zapping, zoomed-in for the initial triggering phase of up to 30ps for clarity, where the voltage peaking is readily observed, reaching to 28V for the STI-type DTSCR structures. Further, it is clear that the transient voltage peaking for the STI-diode-triggered DTSCR structures is much higher than that for the gated-diode-triggered DTSCR structures, mainly due to the much longer and curved conduction path with sharp angles in the STI-type DTSCR structures compared to the very short and straight discharging path in the gated-type DTSCR structures, leading to much stronger internal inductive effect in the STI-type DTSCR structures. Fig. 15 presents the VFTLP-measured transient voltage waveforms for the same DTSCR ESD protection structures. Unlike in the diode-string ESD protection structures, the DTSCR structures show clear transient voltage peaking in VFTLP measurement. The duration of voltage peaking in measurements is larger than that in TCAD simulation, which is due to the slower VFTLP pulse rise time, but the

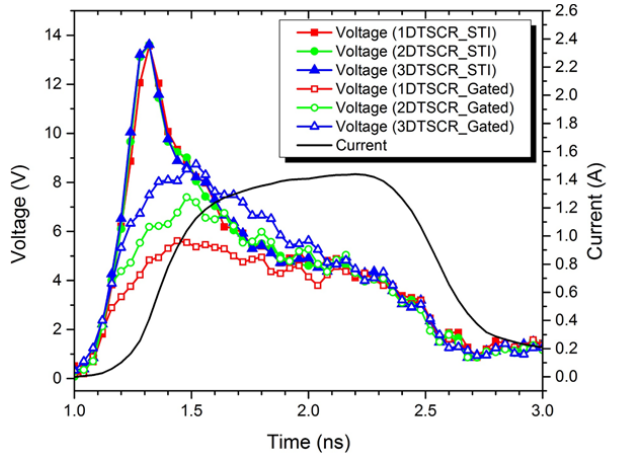

FIGURE 15. VFTLP-measured voltage waveforms for sample DTSCR ESD protection structures show voltage peaking.

TABLE 3. Design splits for STI/Gated Dtscr ESD protection structures.

Type	Diode L (μm)	Diode STI/Gate (μm)	SCR L (μm)	SCR STI (μm)	Total Width (μm)
PPNW DTSCR	0.5	0.15	1	1/0.5/1	50

peak voltage is smaller. This may be because the combination of SCR and diodes in the DTSCR structures slows down the ESD triggering procedure to the point that the VFTLP tester can effectively catch this voltage peaking in measurements. On the other hand, the substantial difference in the voltage peaking observed for the STI-type DTSCR structures and the gated-type DTSCR structures further supports the belief that the internal parasitic inductance plays a key role in delaying the ESD triggering procedure that, in turn, causes transient voltage peaking in CDM ESD zapping. The discrepancy between simulation and measurement may be attributed to two factors: the incapability of an actual VFTLP tester in catching the ultra-fast CDM pulse details and the insufficient TCAD calibration. It is worth noting that, since all the ESD structures designed in this work have the same local metal interconnects in layout, the variation in voltage peaking observed must come from the internal inductive effect inside the Si ESD structures, which is confirmed in Fig. 9, Fig. 14 and Fig. 15 where the comparable ESD structures using STI and gated didoes clearly show significant changes in the observed voltage peaking.

IV. CONCLUSION

This paper presents a comprehensive study of the transient voltage peaking effect observed in diode-based ESD protection structures under CDM ESD stressing. It is found that the VFTLP testers cannot accurately emulate the actual CDM ESD discharging waveform details in the time domain due to its ultra-fast nature. A new combined TCAD simulation and VFTLP testing method is proposed to thoroughly investigate the transient voltage peaking phenomena of various diode-based ESD protection structures. A set of them, including diodes, diode strings and DTSCR structures, were designed and fabricated in a foundry 28nm CMOS and thoroughly studied in this work. With the help of combined TCAD-VFTLP method, it is found that transient voltage peaking may be originated from the internal parasitic inductance along the ESD discharging path, from terminal to terminal through the inner intrinsic PN junction, of a diode-based ESD protection structure. The conduction-modulation-based forward recovery model, originally proposed to model the voltage overshoot effect in power electronics [15], has been applied to model the CDM voltage overshoot phenomena [16], which may not be adequate since many important factors cannot be accounted for, such as the metal interconnects induced inductance that inevitably affects the transient voltage overshoots. This work suggests that the voltage peaking effect may be directly affected by the diode structures

through the internal inductive effect associated with the whole ESD discharging path within a CDM ESD protection structure, including both the bulk semiconductor diffusion regions and the metal interconnects. This analysis offers insights for early-stage ESD design optimization to avoid the troublesome CDM ESD failures due to transient voltage peaking during CDM ESD zapping in practical IC designs at sub-28nm nodes before package level CDM testing.

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