IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 19, 2020, accepted April 27, 2020, date of publication May 6, 2020, date of current version May 18, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2991868

A 320 GHz Octagonal Shorted Annular Ring On-Chip Antenna Array

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This work was supported in part by the Equipment Development Department of the Central Military Commission of China through Pre-Research Project under Grant 6140518040116DZ02001, in part by the State Key Laboratory of Millimeter Waves, Southeast University, under Grant K202010, in part by the Central University Fundamental Research Fund, and in part by the GLOBALFOUNDRIES.

ABSTRACT In this paper, an octagonal shorted annular ring (OSAR) antenna array is presented based on 130-nm SiGe BiCMOS technology without any post-processes. The OSAR antenna consists of annular ring patch, an array of shorted pins and ground which is formed a cavity to enhance the gain and reduce surface waves. The 1×2 OSAR antenna array is designed and fabricated with the die area of $550\times\ 1100\mu m^2$. The measured -10-dB impedance bandwidth is more than 17 GHz (303-320 GHz). The proposed on-chip antenna array is achieved a measurement perk gain of 4.1 dBi at 320 GHz and the simulated radiation efficiency of 38 %.

INDEX TERMS An octagonal shorted annular ring, on-chip antenna array, terahertz (THz), 130-nm SiGe BiCMOS technology.

I. INTRODUCTION

Terahertz (THz) frequency has appealed in various applications ranging from high data rate shorting-rang communication, security imaging, etc. [1]–[4]. Recently, Silicon Germanium (SiGe) technology has been reported to achieve the operating frequency over 300 GHz [5]. The good performance of on-chip antenna is one of the fundamental components, including high gain and wide bandwidth. However, the silicon substrate has a relatively high dielectric constant and large thickness, which causes most of the energy to be trapped in the Si substrate. As a result, the on-chip antennas suffer from higher losses, higher backside power radiation and higher order surface waves. The gain and radiation efficiency of on-chip antenna are normally limited to 0 dBi and 10 %, respectively [6].

Based on the above inherent flaws, several on-chip antennas including cavity antenna with low dielectric constant [7], slot antenna used substrate integrated waveguide (SIW) technology [8], [9], antenna loaded artificial magnetic conductor (AMC) structure [10] and dielectric resonator antennas (DRAs) [6], [12]–[15] have been reported to overcome losses of surface waves and increase the gain. In [7], the Si-cavity is design to remove the semiconductor underneath of antenna by micro-machined process, which achieves the low effective dielectric constant. However, the secondary fabrication process and additional support substrate is required. The designed on-chip Yagi antenna shows a peak gain of 4.7 dBi and radiation efficiency of 82 %. In [8], a circular polarized SIW slot antenna is designed with a gain of -0.5 dBi and a radiation efficiency of 48 % at 410 GHz. The AMC structure can replace perfect electric conductor (PEC) plane for low-profile and high gain antenna. In [10], the double layer dipole on-chip antenna loading AMC is designed for wide bandwidth and low backward radiation. However, gain of the antenna is up to 0 dBi at 235 GHz. In [14], DRAs with a high-order mode can enhance the gain and the radiation efficiency to 7.9 dBi and 48% at 340 GHz. However, these works either show limited gain improvement, complex fabrication process and a large volume.

The shorted annular ring (SAR) antenna can significantly reduce the excitation of surface waves [16], [17], resulting in

The associate editor coordinating the review of this manuscript and approving it for publication was Mohammad Zia Ur Rahman.

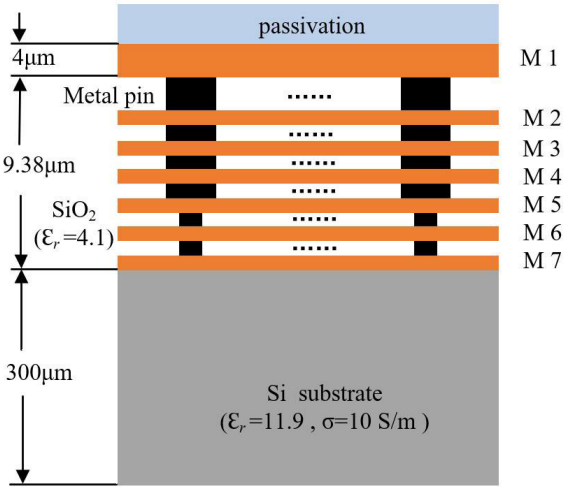

FIGURE 1. Cross-sectional view of the 130-nm SiGe CMOS technology.

less back radiation and high gain. These characteristics make the SAR antenna ideal for applications where the supporting substrate or ground plane of the antenna is small, in which case diffraction of surface and lateral waves from the edges of the structure may be quite significant for conventional microstrip antennas. In [17], the SAR on-chip antenna is designed to achieve much lower levels of radiation along the horizon and toward the backside.

In this paper, a 1 × 2 OSAR on-chip antenna array is presented. The demonstrated antenna is fabricated using 130-nm SiGe BiCMOS process without any post-processes. An octagonal shorted annular ring structure is introduced to reduce surface waves and increase the gain. The die area of the proposed on-chip antenna array is $550 \times 1100\mu m^2$. The −10-dB impedance bandwidth of more than 17 GHz (303-320 GHz) and maximum gain of 4.1 dBi at 320 GHz is observed through on-chip measurement. Good agreements between the simulated and measured results are obtained.

II. OSAR ANTENNA ELEMENT DESIGN

A. ANTENNA CONFIGURATION

In this design, a standard 130-nm SiGe BiCMOS process with 7 metal layers placed in SiO_2 substrate ($\varepsilon_r = 4.19$ and $tan\delta = 0.01$) is shown in Fig. 1. The thickness of top metal (M1) is $4\mu m$ and others (M2-M7) are $1.45\mu m$, $0.55\mu m$, $0.32\mu m$, $0.32\mu m$, $0.32\mu m$, and $0.29\mu m$, respectively. The silicon substrate has the thickness of $300\mu m$ with the dielectric constant of 11.9. The widths of the shorting pins from M1 to M5 and M5 to M7 are $1.24\mu m$ and $0.4\mu m$, respectively.

Since the 130-nm SiGe BiCMOS process cannot process the arc, the geometry of octagonal annular ring (OAR) patch is designed on M1, which is approximate to the circular annular ring (CAR) patch. The configuration of the octagonal microstrip antenna and the OSAR antenna based on the same process is shown in Fig. 2. The OSAR antenna consists of octagonal patch, feeding probe, an array of rectangle metal

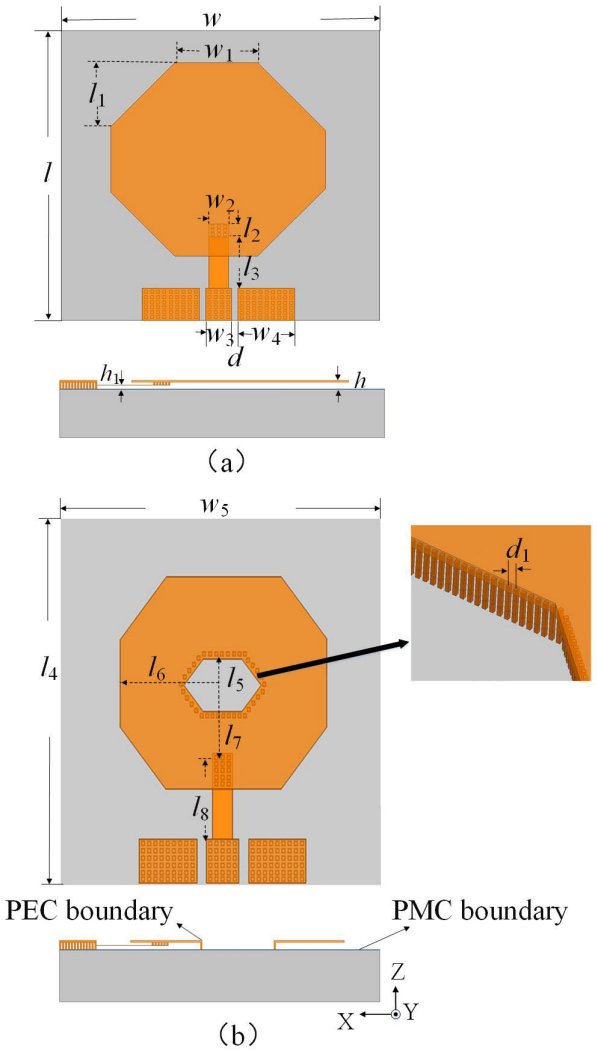

FIGURE 2. The configuration of design antenna (a) Octagonal microstrip antenna (b) OSAR antenna.

pins and ground. An array of rectangle metal pins connects between the octagonal patch (M1) and the ground plane (M8), which form the short-circuited boundary. The short-circuited boundary is established at an inner radius. The inner and outer radius (l_5 and l_6) are chosen to adjust the designed OSAR antenna resonant frequency.

According to the cavity model, a octagonal microstrip antenna can be modeled as a ring of magnetic current. A TM_0 surface wave field is given by [18]:

$$\Psi = -2\pi aB\,(z)\,H_1^{(2)}\left(k_{TM_0}r\right)cos\phi J_1{}'\left(k_{TM_0}a\right) \qquad (1)$$

k_{TM_0} is the propagation wavenumber for the TM_0 surface wave. B(z) is the amplitude factor depends on the source and J_1' is the first kind Bessel functions their derivatives.

Equation (1) is a fundamental design equation, which states that a ring of magnetic current will not excite the TM_0 surface

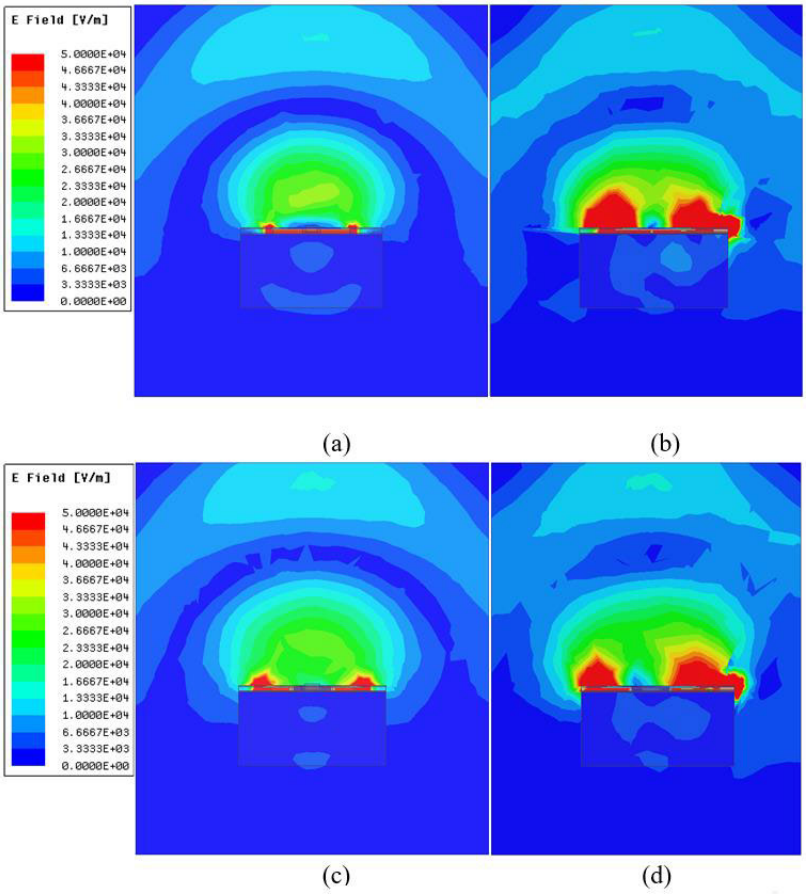

FIGURE 3. Electric field distribution at 320 GHz (a) Octagonal microstrip antenna in x-z plane (b)Octagonal microstrip antenna in y-z plane (c) OSAR antenna in x-z plane (d) OSAR antenna in y-z plane.

wave. The outer radius ($r = l_6$) is chosen to satisfy

$$l_6 = \frac{x'_{11}}{k_{TM_0}} = \frac{1.8412}{k_0} = \frac{1.8412}{2\pi f_0 \sqrt{\varepsilon_0 \varepsilon_r \mu_0}} \tag{2}$$

If $\varepsilon_r = 1$, $k_0 = k_{TM_0}$ is obtained.

The shorting pin is equivalent to inductance, which offset capacitor of dielectric substrate. The inductance of shorting pin can be calculated as [19]

$$L = (\mu_0/\pi)\, cosh^{-1}\,(2d_1/a) \tag{3}$$

Since at the operating frequency of the patch, $C = 1/\omega_0^2 L$, the dielectric permittivity ε_r can be derived as follows:

$$\varepsilon_r = \frac{Ch}{\varepsilon_0 S} = \frac{Ch}{\varepsilon_0 d_1^2} = 2.19 \tag{4}$$

For formula (2) and (4), $l_6 = 186\mu m$.

The inner radius ($r = l_5$) for TM_0 mode resonance satisfies the transcendental equation

$$\frac{J_1\left(k_{TM_0} l_5\right)}{Y_1\left(k_{TM_0} l_5\right)} = \frac{J_1'\left(\frac{k_1 x'_{11}}{k_{TM_0}}\right)}{Y_1'\left(\frac{k_1 x'_{11}}{k_{TM_0}}\right)} \tag{5}$$

J_1 and Y_1 are Bessel functions of the first and second kinds, k_1 the substrate wave number. Y_1' is the second kind Bessel functions derivatives.

TABLE 1. The Optimal dimensions of two on-chip antenna (Unit: μm).

	Parameters	Values	Parameters	Values
Octagonal microstrip antenna	l	550	w	500
	l_1	80	w_1	110
	l_2	20	w_2	20
	l_3	90	w_3	50
	d	15	w_4	100
OSAR antenna	l_4	550	w_5	500
	l_5	45	l_7	104
	l_6	156	l_8	121
	h	12.83	h_1	5.07

After optimization in HFSS, $l_5 = 45\mu m$ and $l_6 = 156\mu m$ are achieved. Table 1 presents the geometrical parameters of the antenna after all optimized design.

Fig. 3 presents the electric field distributions of octagonal microstrip antenna and OSAR antenna at 320 GHz. Results also show that the fields decay much faster along the substrate, due to the absence of the surface wave field. The electric field energy strength of OSAR antenna on the substrate (Si) is lower than that of microstrip antenna. The introduction of octagonal shorted annular ring can obviously suppress surface wave propagation and enhance gain.

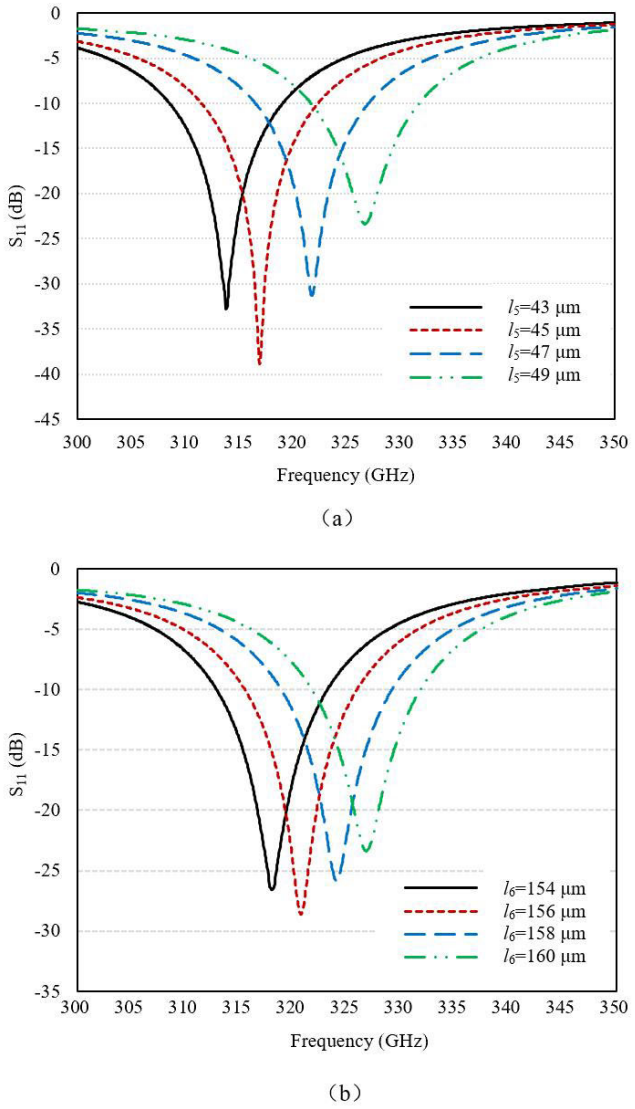

FIGURE 4. Reflection coefficients variation with different l_5 and l_6 (a) l_5 (b) l_6.

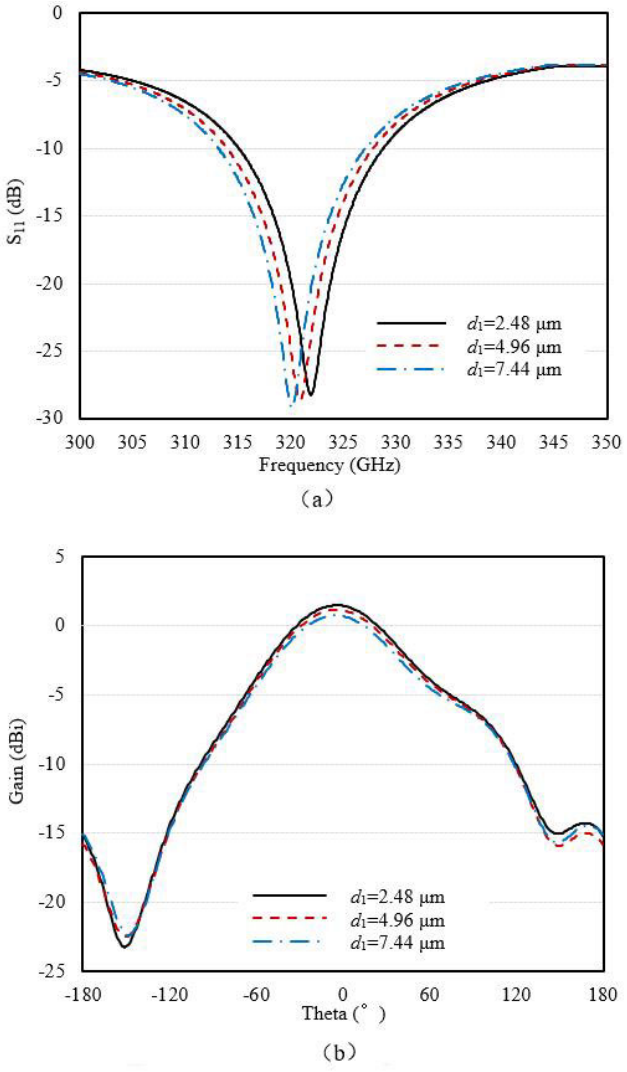

FIGURE 5. Reflection coefficients and gain variation with different d_1 (a) S_{11} (b) Gain.

B. PARAMETER STUDY

The various parameters of OSAR antenna are studied by HFSS. The inner radius (l_5) and outer radius (l_6) are key parameters in controlling the resonant frequency and impedance match. Fig. 4(a) illustrates that when l_5 increases from $43\mu m$ to $49\mu m$, the resonant frequency increases from 314 GHz to 327 GHz. Figs. 4(b) show that when l_6 increases from $154\mu m$ to $160\mu m$, the resonant frequency increases from 318 GHz to 327 GHz. Adjusting l_5 and l_6 is considered to be a good method of achieving the desired impedance bandwidth.

The distance between shorting pins (d_1) is a key parameter in controlling the inductance loaded on the dielectric substrate. Fig. 5 shows the effect of the resonance and gain with different d_1. It is can be seen that when d_1 changes from $2.48\mu m$, $4.96\mu m$, and $7.44\mu m$, the resonant frequency increases from 320 GHz to 322 GHz, while the gain decreases from 1.4 dBi to 0.7 dBi.

The simulated results of microstrip antenna and OSAR antenna are compared in Fig. 6. The simulated −10dB impedance bandwidth of microstrip antenna, OSAR antenna are 10 GHz (318-328 GHz) and 13 GHz (317-330 GHz), respectively. The simulated gain are 0.7 dBi, 1.4 dBi and efficiency is 35.4 %, 41 % at 320 GHz, respectively. The OSAR antenna element achieves 0.8 dB higher gain at 320 GHz, which are much higher than the traditional on-chip patch antenna.

III. A 320 GHz 1 × 2 OSAR ON-CHIP ANTENNA ARRAY DESIGN

Since the high gain performance is required to ensure long distance communication, 1 × 2 OSAR on-chip antenna array is designed to improve the gain, as shown in Fig.7. The 1 × 2 OSAR antenna array consists of two OSAR antenna

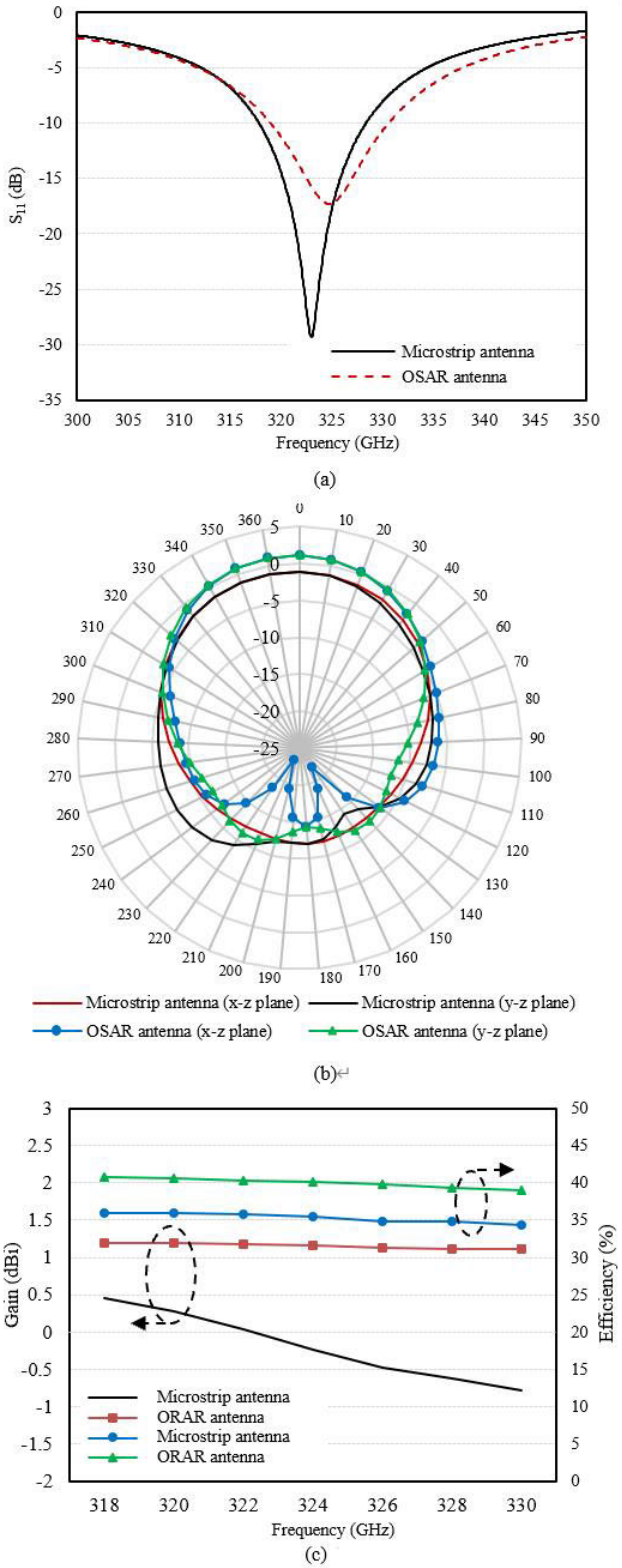

FIGURE 6. Performance comparison of microstrip antenna and ORAR antenna (a) S_{11} versus frequency (b) Gain at 320 GHz (c) Gain and efficiency versus frequency.

elements, ground, power divider, Ground-Signal-Ground (G-S-G) pad. The two OSAR antenna elements are separated with the distance of 0.5 mm ($0.53\lambda_0$). The input impedance

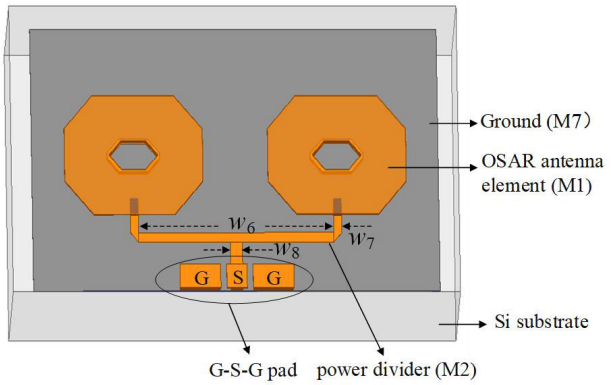

FIGURE 7. Layout of the designed 320 GHz 1 × 2 OSAR on-chip antenna array.

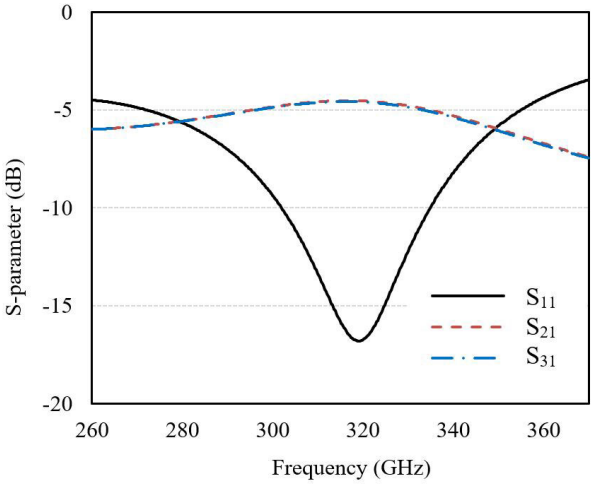

FIGURE 8. Simulated S-parameter results of the power divider.

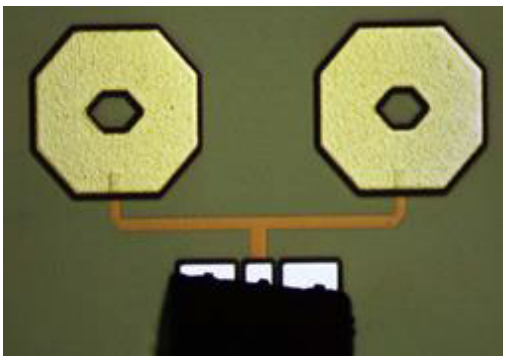

FIGURE 9. Fabricated prototype.

of OSAR antenna element is 100 Ω to design without $1/4\lambda_g$ impedance transformer. The feeding network is placed on the M2 layer, which connect by the feeding probe from M1 layer to M2. The G-S-G pad is design to 50 Ω for measurement.

The length (w_6) and the width (w_7, w_8) of the power divider are 480 μm, 20 μm and 30 μm, respectively. The simulated results are shown in Fig. 8. From the 302-330 GHz, the S_{11} is below −10 dB. The output ratio matches the request of 1:1 and insertion loss of the power divider is less than 1.7 dB.

TABLE 2. Comparison between proposed and reported on-chip antenna.

Ref.	Type	Process	Postprocess	Areas(μm^2)	BW (GHz)	Gain (dBi)	Efficiency (%)
[3]	Patch antenna	40-nm CMOS	No	194×23.15 (patch area)	340*	−5.5*	6.5*
[8]	circular-polarized SIW antenna	65-nm CMOS	No	990×990	32 (251-283)*	−0.5*	21.41*
[9]	SIW slot antenna	130-nm SiGe BiCMOS	No	200×200	2% 410*	−0.5*	49.8*
[12]	Dipole loaded AMC	130-nm SiGe BiCMOS	No	250×410	81 (200-281)	0*	63*
[14]	DRA	SiGe	Dielectric resonator	700×700×730	12% 340*	10	80
This Work	**OSAR antenna**	**130-nm SiGe BiCMOS**	**No**	**500×500**	**13 (317-330)**	**1.4***	**41***
		Antenna array					
[5]	2×2 Slot antenna array	130-nm SiGe	No	860×860	320*	7.9	-
[6]	2×2 cavity-Backed rectangular slot loop antenna array	130-nm SiGe BiCMOS	No	1100×1100	5%	7.7	39%
[15]	2×2 DRA array	180-nm CMOS	Dielectric resonator	1100×1500×1269	16 (334-350) *	8.65*	54*
This Work	**1×2 antenna**	**130-nm SiGe BiCMOS**	**No**	**500×1000**	**More than 17 (303-320)**	**4.1**	**38***

* simulated results

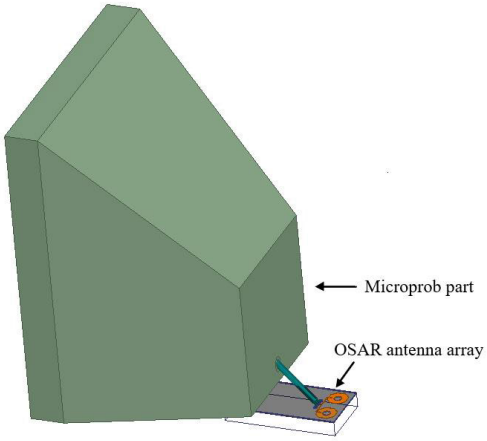

FIGURE 10. 3-D schematic of the chip and probe model.

A 320 GHz 1 × 2 OSAR on-chip antenna array is fabricated with the die area of 550 × 1100μm^2, as shown in Fig. 9. The designed on-chip antenna array is measured by Keysight PNA-X with the VDI extender from 220-320 GHz. A G-S-G probe with a pitch of 100μm is touched on the GCPW (grounded coplanar waveguide) line of the proposed antenna for measurement. The simulation −10dB impedance bandwidth is 12 GHz (311-323 GHz). The measurement −10-dB impedance bandwidth is more than 17 GHz (303-320 GHz), as shown in Fig. 11. The measurement resonant frequency is 1 GHz lower than the simulation results. Discrepancies between measurement and simulation of the proposed antenna could be arose from the probe.

IV. RESULTS AND DISCUSSION

The three-dimensional (3-D) schematic of the probe feeding the designed on-chip antenna is analyzed using the HFSS and shown in Fig. 10. The measured loss of waveguide-to-GSG probe is 4.87 dB from 220-320 GHz, which is fed the RF signal to the antenna under test (AUT). The gain of standard horn antenna is 12.1-16 dBi from 220 to 320 GHz. Since the rotation in the x-z plane is blocked by the scope lifting bar on the probe station, the measured x-z plane patterns are limited to $180° < \theta < 50°$. The measured peak gain is calculated based on [20]:

$$G_{AUT} = P_{AUT} - P_{horn} + G_{horn} + Loss_p + L_{cable} \quad (6)$$

where P_{AUT} and P_{horn} are the power at the spectrum analysis and the standard horn, G_{horn} is the gain of the standard horn antenna, $Loss_p$ and L_{cable} are the insertion losses of the G-S-G probe and coaxial cable.

Simulated and measured gain of the proposed on-chip antenna array are presented in Fig. 11(a)-(d). The simulation results after adding the probe is consistent with the measurement results. When the probe is added, the resonant frequency decreased 1 GHz and the bandwidth increased 4 GHz due to the coupled field generated by the probe. The simulated and measured peak gains are 5.4 dBi and 4.1 dBi at 320 GHz, respectively. However, the measured main beam direction is −5°. The radiation pattern has a lot of burrs. Seem form the Fig.12, the main beam offset, gain reduction and burrs are due to the electromagnetic wave reflection generated by the probe and coaxial cable. The simulated results with probe and measured results agree well.

Compared with previously, reported on-chip antennas based on CMOS process as shown in Table 2, the proposed antenna has a broader bandwidth of about 17GHz and a higher efficiency above 38%. Unlike the traditional slot antenna [3], [5], [8], [9], which has high loss and low gain, the gain of OSAR antenna array improved gain. Moreover, in comparison with the DRA [14] and array [15], the proposed antenna achieved similar efficiency without loading Dielectric resonator.

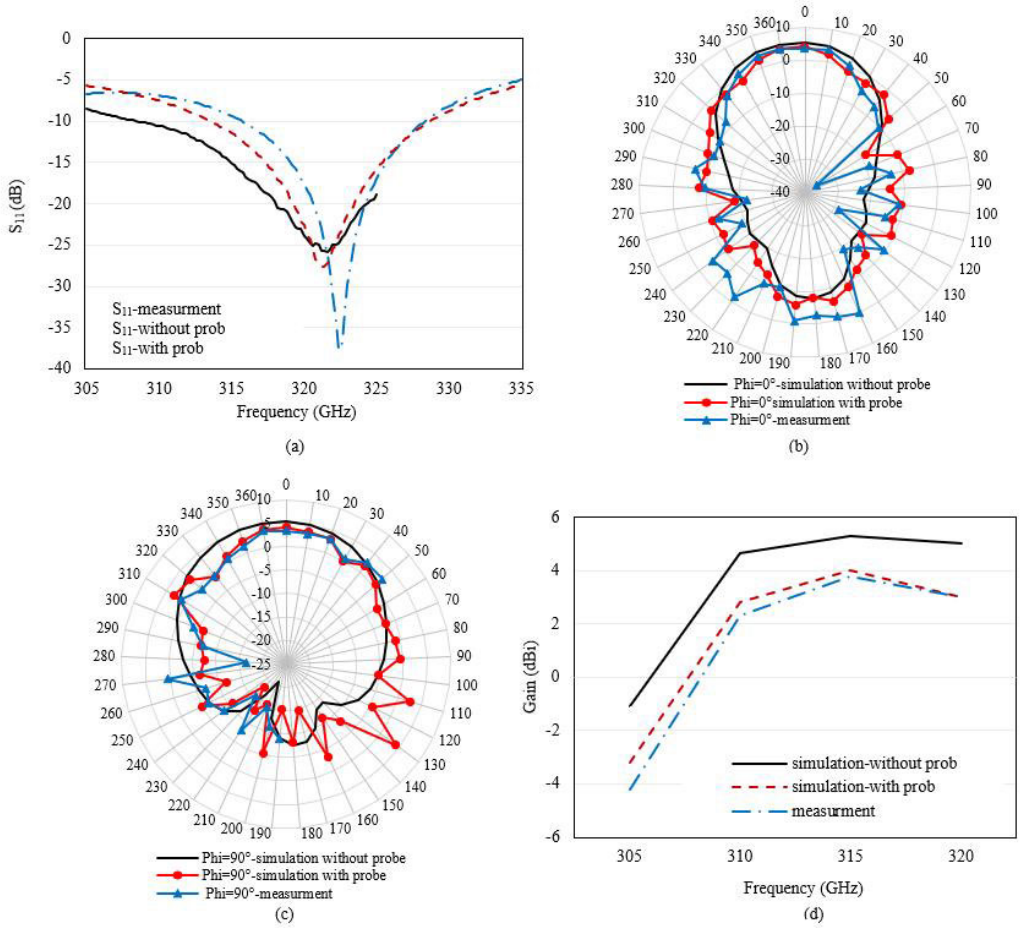

FIGURE 11. Impact of probe on S_{11} and gain of proposed antenna array (a) S_{11} and gain versus frequency (b) Gain at X-Z plane (c) Gain at Y-Z plane (d) Gain versus frequency.

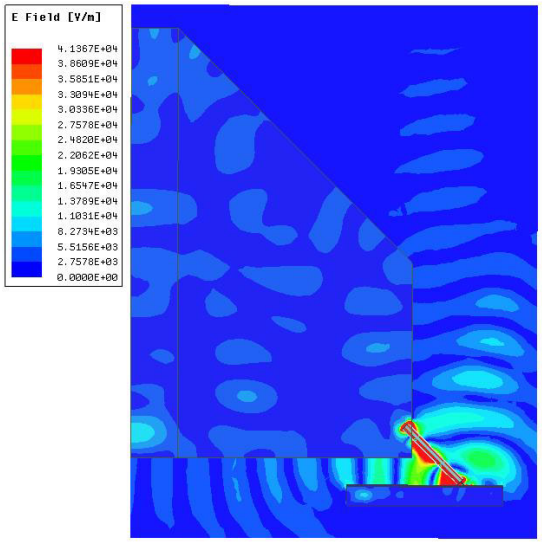

FIGURE 12. Electric field distribution of the on-chip antenna with and with probe.

V. CONCLUSION

A wideband and high efficiency 1×2 OSAR on-chip antenna array has been presented and investigated at 320 GHz. The octagonal shorted annular ring has mainly contributed to improve gain and reduced surface wave based on 130-nm SiGe BiCMOS. The proposed antenna has a die area of $550 \times 1100 \mu m^2$. The measurement -10-dB impedance bandwidth is more than 17 GHz (303-320 GHz). The antenna reaches 4.1 dBi measured gain at 320 GHz. The impact of probe in bandwidth and gain was analysed and both the simulated and measured results agree well. It is demonstrated that the proposed antenna array can be a promising candidate for THz communication systems.

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