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168-195 GHz Power Amplifier With Output Power Larger Than 18 dBm in BiCMOS Technology

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ABSTRACT This paper presents a 4-way combined G-band power amplifier (PA) fabricated with a 130-nm SiGe BiCMOS process. First, a single-ended PA based on the cascode topology (CT) is designed at 185 GHz, which consists of three stages to get an overall gain and an output power higher than 27 dB and 13 dBm, respectively. Then, a 4-way combiner/splitter was designed using low-loss transmission lines at 130-210 GHz. Finally, the combiner was loaded with four single-ended PAs to complete the design of a 4-way combined PA. The chip of the fabricated PA occupies an area of 1.35 mm^2. The realized PA shows a saturated output power of 18.1 dBm with a peak gain of 25.9 dB and power-added efficiency (PAE) of 3.5 % at 185 GHz. A maximum output power of 18.7 dBm with PAE of 4.4 % is achieved at 170 GHz. The 3-dB and 6-dB bandwidth of the PA are 27 and 42 GHz, respectively. In addition, the PA delivers a saturated output power higher than 18 dBm in the frequency range 140-186 GHz. To the best of our knowledge, the power reported in this paper is the highest for G-band SiGe BiCMOS PAs.

INDEX TERMS Cascode, 4-way combiner, G-band PA, power amplifier, SiGe BiCMOS.

I. INTRODUCTION

With the recent progress in the speed of solid-state devices, millimeter-waves and terahertz technologies are continuously improving in terms of cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). This includes transistors based on III-V (InP, GaAs) and Si (SiGe BiCMOS, CMOS) technologies [1]–[6]. Generally, III-V (InP) transistors demonstrate higher f_T/f_{max}, and breakdown voltages (BV_{CEO} and BV_{CBO}) compared to Si devices. Nevertheless, Si devices are preferred over III-V devices due to their advantage in large-scale and high-level integration. Besides, advanced SiGe BiCMOS technologies exhibit f_{max} up to 500 GHz, which have allowed the development of solid-state systems above 100 GHz for different applications including high-speed short-range wireless communication, high-resolution imaging, sensing, phased arrays, and radar systems [7]–[15].

One of the key issues in the realization of high-frequency systems is the limited output power-level attainable with SiGe HBTs (heterojunction bipolar transistors). The low breakdown voltage and scaling down of the transistor periphery to increase the f_T and f_{max} leads to the limitation of obtaining high-output power. Additionally, dominant high-frequency effects in terms of high conductor/substrate losses and increased parasitic elements of the transistor reduce its output power. These challenges make it difficult to design efficient and high power solid-state circuits such as voltage controlled oscillators (VCOs) [16], frequency multipliers [17], [18], and power amplifiers (PAs) [19], [20].

To increase the output power (P_{out}) and power added efficiency (PAE), various high-frequency PAs based on SiGe BiCMOS technology have been reported in [19]–[25]. They can be categorized into single-ended, N-way power

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combined, and balanced (differential) PAs. These PAs are designed using cascode topology (CT), common emitter (CE) and stacked configurations. Single-ended PAs are usually compact and can be utilized in power combiner circuits to obtain large output power. Examples of single-ended PAs are reported in [19], [20] at various frequencies in the range of 110-140 GHz, which are based on CE and CT. Among them, a maximum output power of 13.8 dBm with PAE of 11.6 % is achieved at 116 GHz.

The second most popular category to generate high output power are N-way power combined PAs, which can be further classified by the nature of combining networks into reactive, sub-quarter-wavelength balun, transformers, Wilkinson, and antenna-based free-space combiners [20]–[32]. For instance, the authors of [20], report an 8-way reactive power combined PA using CE configuration at 116 GHz. This PA despite consuming a large amount of chip area delivers a maximum output power of 20.8 dBm with peak PAE and gain of 7.5 %, and 15 dB, respectively. A PA solution with reduced area consumption based on sub-quarter-wavelength baluns and stacked configuration in [21] delivers a peak output power of 22 dBm with PAE of 3.6 % at 120 GHz. However, the peak power gain of this PA is limited to 7.7 dB. Contrarily, solutions based on transformers, Wilkinson combiners, and free-space antenna combining networks [22]–[25], become unpractical for the design of high-frequency PAs. In fact, the Wilkinson and transformer combiners introduce higher losses when the number of combining networks increases, while the free space losses and poor radiation efficiency of the high-frequency antennas limit the effective attainable output power.

The third category of high-frequency PAs is based on differential configurations, which benefits from the availability of virtual ground and presents high common-mode rejection ratio (*CMRR*) for common-mode noise cancellation. Baluns are required for differential to single-ended transformation, which eases the characterization of the differential PAs. Examples of differential PAs without utilizing power combining networks are reported in [26]–[29], where a maximum output power of 14 dBm with a peak gain of 27 dB is demonstrated at 160 GHz. The designs of 4-way combined differential PAs at 170 and 240 GHz using T-junctions are discussed in [30], [31]. A maximum output power of 18 dBm is achieved at 170 GHz by de-embedding the loss of RF pads and baluns. However, this PA is partially characterized, while a full characterization to see the large-signal performance across all frequency bands should be shown. There are very few examples of the high-frequency PAs around 160 GHz in SiGe BiCMOS technology and most of the reported designs demonstrate high-output power in the lower D-band. G-band PAs above 160 GHz with large output power are crucial to drive frequency multipliers for the generation of high-power sub-THz signals.

In this paper, we report a G-band (168-195 GHz) 4-way combined solid-state PA based on 130-nm SiGe BiCMOS technology [32]. The complete G-band PA includes an input splitter, four single-ended PAs, and an output combiner. For the first time, a G-band silicon PA exceeding an output power of 18 dBm with a PAE larger than 3 % has been demonstrated. This performance has been made possible by exploiting the unique features of the 130-nm SiGe technology from IHP with f_T/f_{max} of 300/450 GHz and back-end-of-the-line (BEOL) process suited for millimeter wave applications. The circuit can be used in frequency multiplier chains, radar sensors, and high-speed wireless communication transceivers operating in the 140-200 GHz band. The paper is organized as follows : In section II, the features of 130-nm SiGe BiCMOS technology are discussed. Section III presents the architecture of the 4-way combined PA. Then, section IV presents the detailed design procedure for the single-ended PA, 4-way combiner, and their integration for the realization of the overall PA. The experimental results and comparisons with state-of-the-art works are presented in section V. Finally, the conclusion and summary are reported in section VI.

II. 130-nm SiGe BiCMOS TECHNOLOGY

The 4-way combined PA proposed in this paper was designed and fabricated with commercial IHP's 130-nm SiGe BiCMOS process known as SG13G2. The process offers high performance heterojunction bipolar transistors (HBTs) with $f_T/(f_{max})$ of 300/450 GHz and breakdown voltages of BV_{CEO} = 1.7 V, and BV_{CBO} = 4.8 V, respectively [1]. The HBTs are highly suitable for the design of various mm-wave and sub-THz circuits, which is further supported by the back-end-of-the-line (BEOL) process as shown in Fig. 1. The BEOL provides seven metal layers based on aluminum(Al), which include two thick low-loss metals (TM_2 3 μm thick and TM_1 2 μm thick) and five thin metal layers (M_5-M_1 each 0.49 μm thick). The top thick metals allow higher current densities and present lower sheet resistance, while the lower thin metals help to form various metal contact patterns for different Si-devices. The metal layers together with their heights and thickness enable the customized realization of high-quality inductors, metal-oxide-metal (MOM) capacitors, and transmission lines such as microstrip and coplanar lines. The lower metal layers permit the design of ground plane and dense metal interconnections. In addition, the process offers

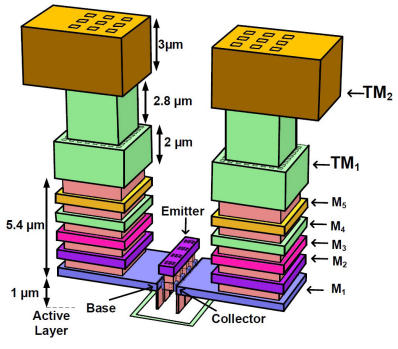


FIGURE 1. BEOL Cross-section of 130-nm SiGe BiCMOS technology [33].

polysilicon resistors and high quality-factor metal-insulator-metal (MIM) capacitors.

III. ARCHITECTURE OF THE 4-WAY COMBINED PA

Fig. 2 shows the block diagram of the G-band 4-way combined PA. It consists of an input splitter, four-unit cells of single-ended PAs, and an output combiner. The proposed structure was aimed to provide a peak output power of more than 18 dBm with a power gain larger than 27 dB at 185 GHz. Assuming ideal lossless components in the design, a unit cell PA (single-ended PA) is able to provide an output power more than 12 dBm with a power gain of 27 dB, which leads to an output power of 18 dBm in a 4-way combination. However, in the actual case with lossy components, the unit cell should provide an output power well above 12 dBm to compensate the loss of power combiner.

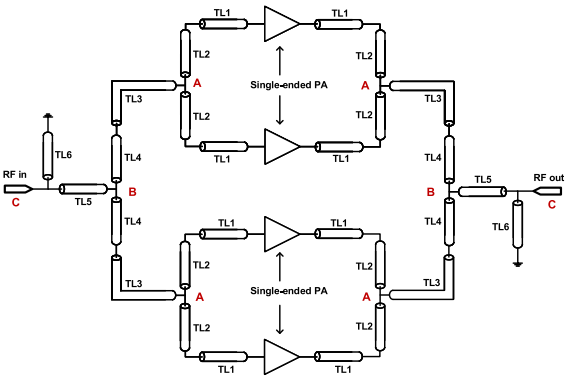


FIGURE 2. Block diagram of the G-band 4-way combined PA.

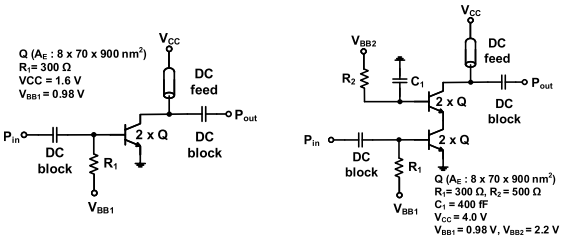
Assuming the input and output of a unit cell is matched to 50 Ω, the splitting/combining networks must be designed to ensure conjugate matching of the input and output of the 4-way combined PA and external 50 Ω standard terminations. Such transformation is ensured with the following steps: the transmission lines $TL_{1,2}$ were used to properly compensate the overall parasitic effects while roughly maintaining 50 Ω on the up and down side of section A (i.e., at A the impedance seen is roughly 25 Ω) then, through the transmission lines $TL_{3,4}$ the impedance is transformed to 50 Ω. This will again make the impedance seen at the junction of node B 25 Ω, which is finally transformed to 50 Ω at node C using $TL_{5,6}$ and parasitic capacitance of the RF pad.

IV. CIRCUIT DESIGN CONSIDERATIONS

A. PA TOPOLOGY

The design of the high-frequency PA requires the investigation of various topologies in terms of gain, output power, and power added efficiency (PAE). CE and CT are the two most adopted solutions for the design of high-frequency PAs. The schematics of a CE and a CT are shown in Fig. 3(a) and 3(b), respectively.

To compare the two topologies, the transistors shown in Fig. 3 are biased at a collector current density



(a) Common Emitter (CE) (b) Cascode Topology (CT)

FIGURE 3. Schematic of CE (a) and CT (b).

of 2.0 mA/μm. Biasing resistors R_{1-2} with values in the range 300-500 Ω were added at the bases of each transistor for optimal gain and output power, which allows the effective collector-emitter breakdown voltage to increase well above BV_{CEO} by presenting an external low impedance to the bases of the transistors [20], [34]. Fig. 4 shows the maximum available gain (MAG) and stability factor (μ_1) for the CE and CT without including the physical metal interconnections. It is noted that the CT shows higher gain and stability compared to the CE. Specifically, at 185 GHz, the CT and CE show a MAG of 12.3 dB and 6.3 dB, respectively. Moreover, better isolation between the input and output of the CT ensures higher stability with respect to the CE.

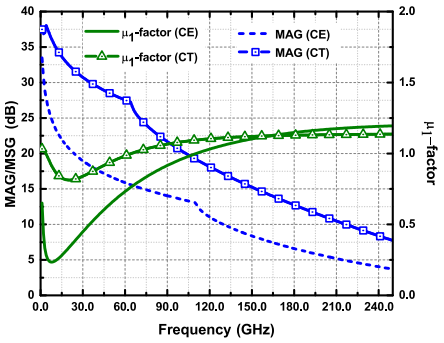


FIGURE 4. Simulated MAG and μ_1-factor of the CE and CT.

For the design of high-frequency power amplifiers, it is certainly more interesting to compare the large-signal performance of the two topologies. Load-pull simulations were performed to find the optimum load impedances resulting in maximum output power and PAE at 185 GHz, while the input was terminated on the conjugate matching condition. Table 1 shows the relevant parameters (input and load impedances,

TABLE 1. Performance parameters of CE and CT at 185 GHz.

Parameter	Common emitter (CE)	Cascode Topology (CT)
Z_{in} (Ω)	3.6-j2	3.9-j3
Z_{load} (Ω)	22.42+j22.2	87+j25.31
Peak Gain (dB)	6.3	12.3
P_{1dB} (dBm)	11.75	13.4
P_{sat} (dBm)	13.5	15.8
Peak PAE (%)	20	19.6

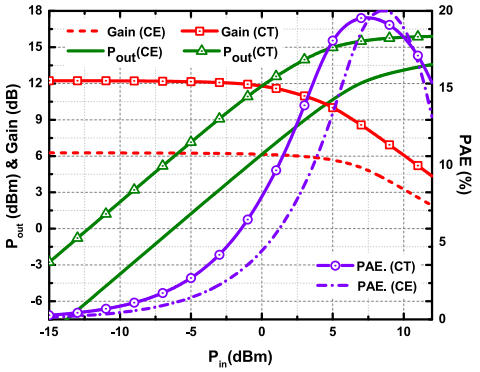


FIGURE 5. Simulated gain, output power, and PAE of CE and CT at 185 GHz.

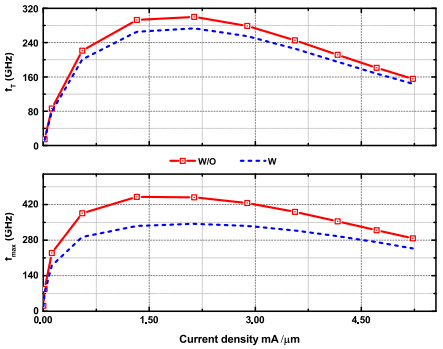


FIGURE 6. f_T and f_{max} of the transistor versus collector current density without (W/O) and with (W) parasitic extracted.

TABLE 2. Performance parameters of CT without (W/O) and with (W) interconnects at 185 GHz.

Parameters	W/O interconnects	W interconnects
Z_{in} (Ω)	3.9-j3	4.5-j0.4
Z_{load} (Ω)	87+j25.31	17.85+j13.35
Peak Gain (dB)	12.3	10.6
P_{1dB} (dBm)	13.4	13.3
P_{sat} (dBm)	15.8	14.7
Peak PAE (%)	19.6	14.6

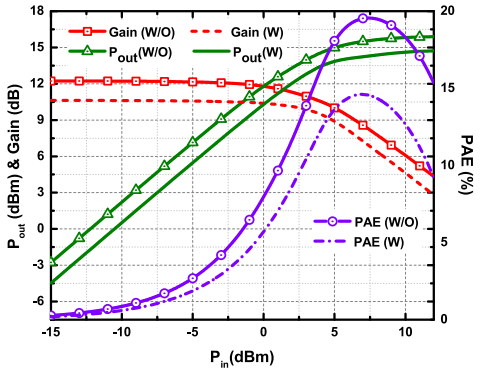


FIGURE 7. Simulated gain, output power, and PAE of the CT power-stage without (W/O) and with (W) interconnections at 185 GHz.

peak gain, output power at 1 dB compression and at saturation, and peak PAE) of CE and CT, while Fig. 5 illustrates the power sweep curves resulting from nonlinear harmonic balance simulations under optimum load/source terminations at 185 GHz. It is noted that the two topologies show almost similar input impedance. The CT shows larger optimum load resistance ($R_{Lopt,CT} = 87\,\Omega$) with respect to CE ($R_{Lopt,CE} = 22.42\,\Omega$). In terms of output power and gain, the CT shows higher values than CE. Both CE and CT show almost similar PAE of about 20 %. However, when the inherent losses introduced by the interconnections and matching networks are taken into account at 185 GHz, it will result in a severe reduction of the attainable gain, output power and PAE. The lower gain resulting from the CE makes such solution less attractive in comparison to the CT, which was adopted for the design of the single-ended PA at 185 GHz.

B. UNIT CELL: SINGLE-ENDED PA

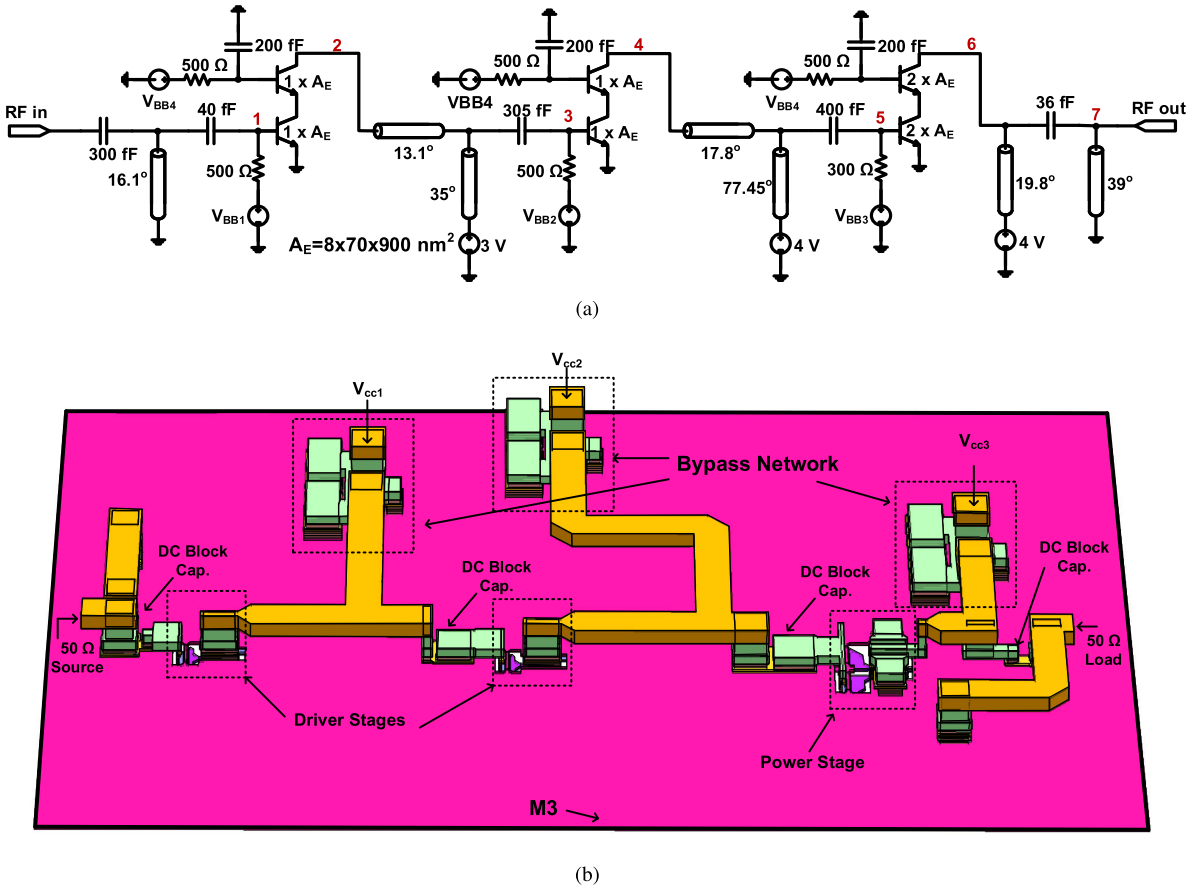
The high-frequency PA typically consists of a power stage and finite driver stages. The former provides the required output power, whereas the latter allows to satisfy the gain specification. To design a power stage with output power higher than 13 dBm at 185 GHz, the active area of each transistor in CT was picked as an aggregation of two parallel 8-finger HBTs (see Fig.3(b)). This provides a saturated output power of 15.8 dBm without including metallic interconnections. Suitable metal interconnections were designed for the power stage to satisfy metal current density and electromigration rules. The interconnections were EM-simulated in ADS-Momentum from Keysight to see their effect on f_T/f_{max}, output power, gain and PAE. Fig. 6 shows the f_T/f_{max} of the transistor with parasitics extracted (with interconnects). The f_T/f_{max} drops from 300/450 GHz to 270/350 GHz, which is still better than CMOS [35]. This degradation in f_T/f_{max} reduces the output power, gain and PAE of the PA.

Load-pull simulations were repeated to optimize output power, and PAE at 185 GHz. The resulting parameters of the power stage without (lossless, i.e., ideal) and with interconnections are summarized in Table 2, while Fig. 7 shows the output power, gain and PAE curves at 185 GHz.

It is noted that the interconnections introduce a loss of 1.6 dB, which reduces the peak gain from 12.2 to 10.6 dB. The output power, PAE, and optimum input/load impedances are also affected by the interconnections. The maximum power and PAE are dropped to 14.7 dBm, and 14.6 %, respectively, due to the loss introduced by the interconnections.

To drive the power stage and attain an overall gain larger than 27 dB, two identical driver stages were adopted. The transistor's size in the driver stages is half with respect to power stage. Table 3 provides summary of the different parameters of the two driver stages biased with voltage supplies of 3 V and 4 V for the 1^{st} and 2^{nd} stage, respectively. 4 V supply could be selected for the 1^{st} driver stage instead of 3 V to increase the overall gain. However, 3 V supply was opted to reduce the total DC power consumption of the PA.

The optimum impedances required by each stage were properly synthesized through the design of the input, interstages, and output matching networks to complete the



(a)

(b)

FIGURE 8. Schematic of the: a) single-ended PA and its b) 3D layout view.

TABLE 3. Performance parameters of driver stages with interconnects at 185 GHz.

Parameter	Stage I (3 V supply)	Stage II (4 V supply)
Z_{in} (Ω)	9-j3.5	9-j3.5
Z_{load} (Ω)	51+j27	94.3+j27.7
Peak Gain (dB)	10.7	11.45
P_{1dB} (dBm)	7.6	9.9
P_{sat} (dBm)	9.6	11.43

design of the single-ended PA. The matching networks were designed using MIM capacitors, and 50 Ω transmission lines with different electrical lengths. The DC-block capacitors were optimized as part of the matching networks. Unlike high impedance lines, 50 Ω transmission lines have been utilized for sustaining higher current densities, which improves the reliability of the PA. The three stages of the single-ended PA were AC coupled by using bypass capacitors. The matching networks, including bypass capacitors were EM-simulated in ADS momentum. Fig. 8(a) shows the final schematic of the single-ended PA, while the corresponding 3D-layout is shown in Fig. 8(b).

Fig. 9 shows the simulated S-parameters of the single-ended PA. A good matching is achieved at the input ($|S_{11}| < -10$ dB) and output ($|S_{22}| < -10$ dB) with a gain of 28.2 dB at 185 GHz, which is inherently smaller than the

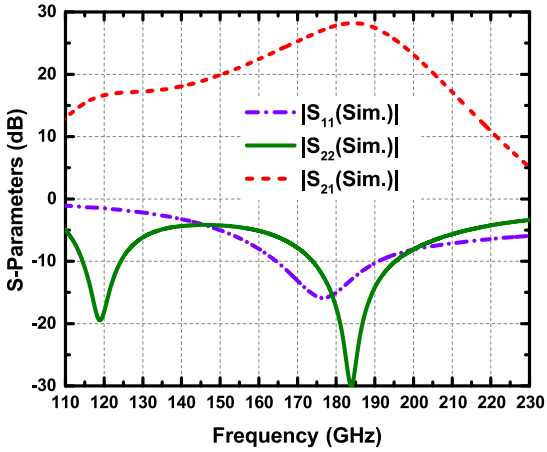


FIGURE 9. Simulated S-parameters of the single-ended PA.

summation of the gains of each stage due to the loss of matching networks. Fig. 10 shows the gain, output power, and PAE of the single-ended PA at 185 GHz. A peak output power of 13.1 dBm with a PAE of 7.7 % is obtained. To quantify the losses associated with the matching networks, Fig. 11 was generated where the output power is reported at various nodes (see Fig. 8(a)). For the ease of readability, the powers are also specified for a fixed input power of −18 dBm in the

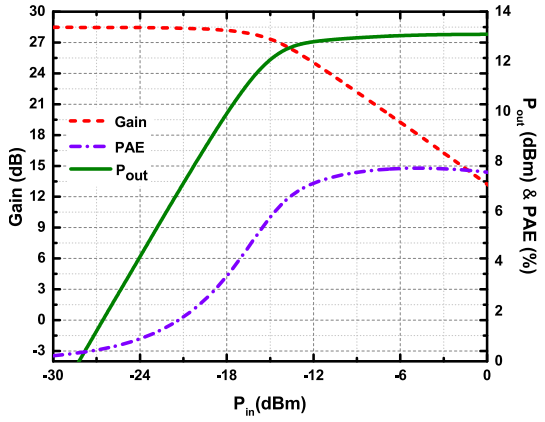


FIGURE 10. Simulated gain, output power, and PAE of the single-ended PA at 185 GHz.

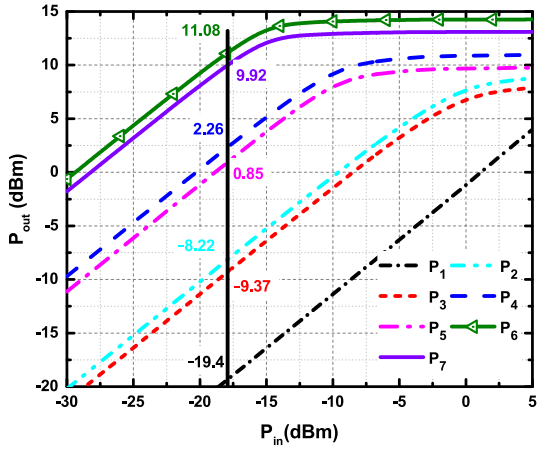


FIGURE 11. Simulated output power at various nodes of the single-ended PA at 185 GHz.

same figure. The input, first interstage, second interstage, and output matching networks introduced loss of 1.4, 1.15, 1.41, and 1.16 dB, respectively. The overall loss of the passive networks is 5.12 dB.

C. 4-WAY SPLITTER/COMBINER

To combine the four-unit cells of single-ended PAs, a low-loss 4-way splitter/combiner earlier discussed in section III was designed. Fig. 12 shows the final layout of the 4-way combiner/splitter illustrating various transmission lines with different characteristic impedances and electrical lengths. The combiner was optimized in ADS-momentum, while ensuring good matching at each nodes (see points A, B, and C in Fig. 2).

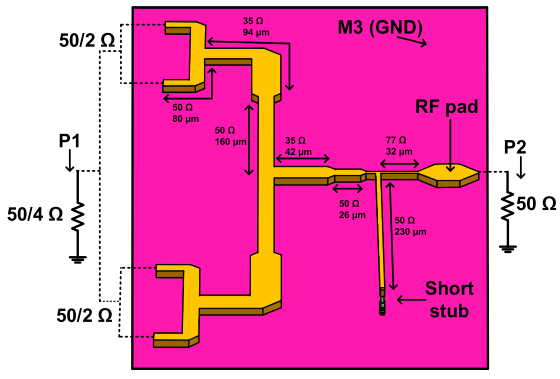


FIGURE 12. Layout of the 4-way combiner/splitter.

Fig. 13 shows the simulated S-parameters of the 4-way combiner. A good matching is achieved in wide bandwidth with both $|S_{11}|$ and $|S_{22}|$ better than -10 dB at 130-270 GHz. The combiner presents an insertion loss less than 1 dB at 140-205 GHz.

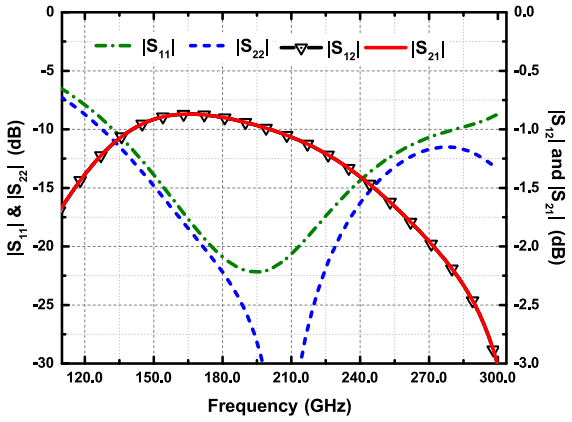


FIGURE 13. Simulated S-parameters of the 4-way combiner/splitter.

D. 4-WAY COMBINED PA IMPLEMENTATION

The transmission lines used in the matching networks and power combiner were realized using top thick metal (TM_2) for the RF lines with bottom thin metal M_3 acting as the ground plane (See Fig. 1). The lower metals M_1 and M_2 were used for various interconnections to route DC lines. Separate collector and base supplies were used to bias the transistor. Besides, collector supplies of each stage are separated to improve stability. Additionally, Large bypass capacitors with a series resistor of 10 Ω are included in the supply lines.

The full layout of the 4-way combined PA consists of integrated input splitter, four-unit cells of single-ended PAs, output combiner and bonding pads. The final PA was fabricated with the standard 130-nm SiGe BiCMOS process and its micro-photograph is shown in Fig. 14. It occupies a very small area of $0.97 \times 1.4\,\text{mm}^2$, including RF and DC pads. It is noted that the chip contains dummy metal layers, which were included to satisfy the metal density rules of the 130-nm BEOL process. Such dummy metal layers were placed at least 30-50 μm away from the RF lines to avoid any coupling with the main circuitry, which was further verified by including them in EM-simulation during the design of the matching networks.

V. EXPERIMENTAL RESULTS

The realized power amplifier was characterized on wafer under small and large signal conditions. During the characterization, the supply voltages were set as $V_{CC1} = 3$ V, $V_{CC2} = 4.0$ V, and $V_{CC3} = 4.0$ V.

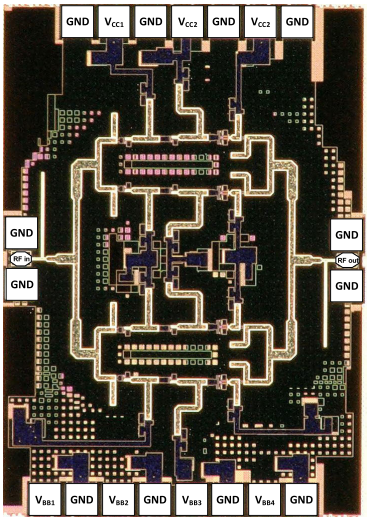


FIGURE 14. Chip micro-photograph of the 4-way combined PA (0.97 × 1.4 mm^2 including pads).

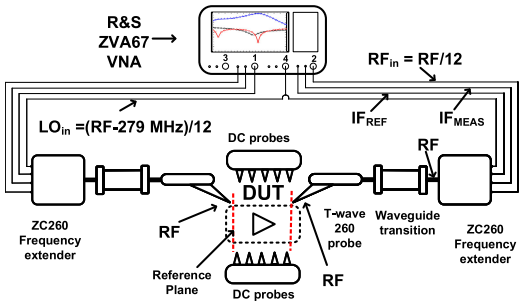


FIGURE 15. S-parameters measurement setup showing different blocks in WR-4.0 band.

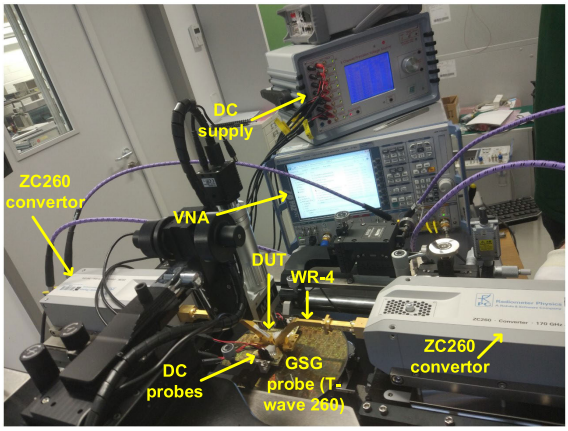
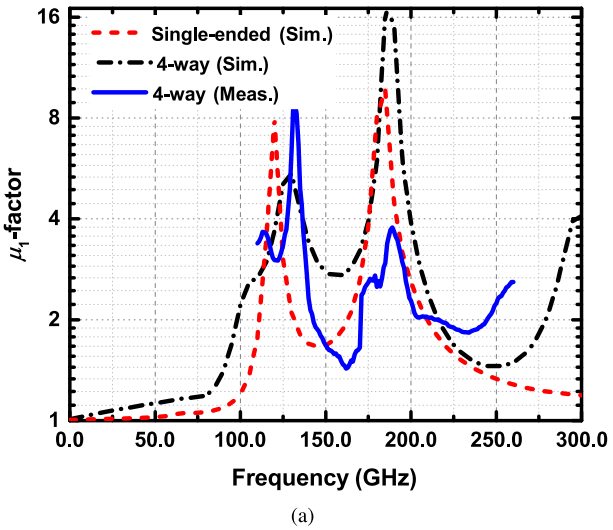
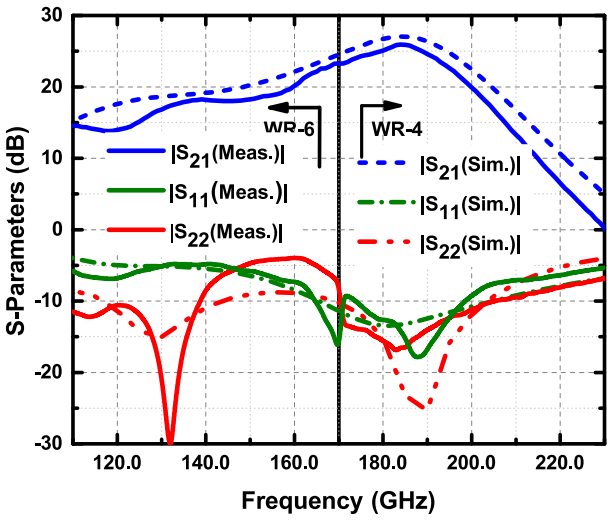


FIGURE 16. In-house measurement setup at IHP for the characterization of S-parameters of the 4-way combined PA in G-band.



(a)



(b)

FIGURE 17. (a) Stability factor (μ_1) and (b) S-parameters of the 4-way combined PA. The stability factor is compared to the single-ended PA.

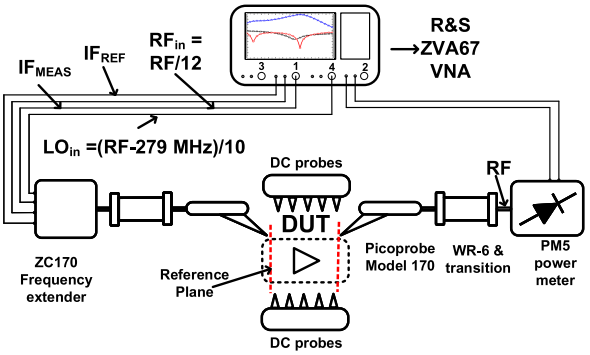


FIGURE 18. Output power measurement setup in D-band using ZC170 frequency extender.

A. SMALL-SIGNAL

The small-signal (S-parameters) characterization was carried out using the setup shown in Fig. 15. The Rohde & Schwarz ZVA67 VNA (Vector Network Analyzer) and ZC260 frequency extender were used to perform measurements in G-band. The input RF (RF_{in}) and LO (LO_{in}) signals of the frequency extender are generated by the VNA and locked with the frequency of measurement, i.e., $RF_{in} = RF/12$

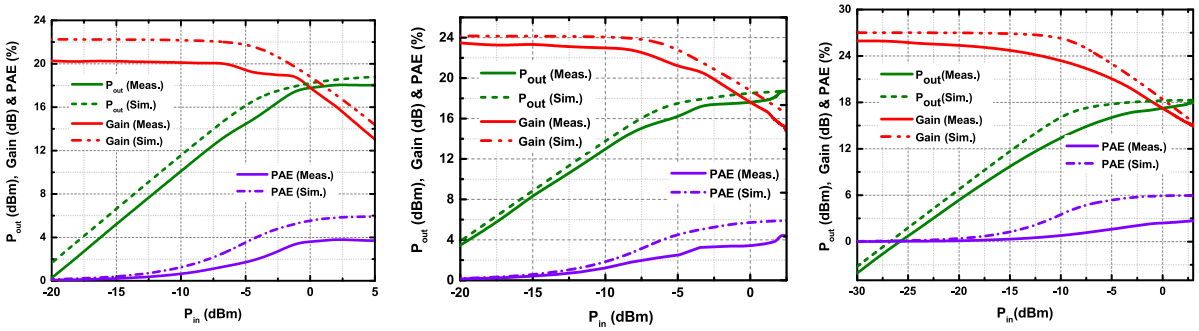


FIGURE 19. Experimental output power, gain, and PAE of the 4-way combined PA: (a) at 160 GHz, (b) at 170 GHz, and (c) at 185 GHz.

and $LO_{in} = (RF - 279MHz)/12$. The LO_{in} signal is further divided into two using a power divider. These RF_{in} and LO_{in} signals then feed the two ZC260 frequency extenders, which generates the required RF_{out} signals needed to feed the two terminal device under test (DUT i.e., PA in this case). The DUT contains an identical set of DC and RF probes, and waveguide fixtures at each side. The reflected and measured intermediate frequency (IF) signals (279 MHz) are later captured by the VNA. The multiplication factors for the ZVA260 frequency extenders are 12. In addition, the attenuator of the frequency extender can be used to adjust the incident power of the RF signal feeding the DUT.

Similar setup with the replacement of RF probe and frequency extender (ZC170) was used to measure the S-parameters of the PA in D-band (110-170 GHz). A photo of the measurement setup available at IHP laboratory is shown in Fig. 16.

Fig 17(a) and Fig 17(b) show the stability-factor (μ_1) and S-parameters of the 4-way combined PA, respectively. In general a good co-relation is found between the simulation and measurement. The PA is stable as the μ_1-factor is above 1. The measured stability is only shown at 110-260 GHz due to non-availability of RF probes and sources to cover a large frequency range from DC to f_{max}. Nevertheless, the simulated stability of the PA was assessed under even and odd-mode excitation and it was found unconditionally stable. Also, the single-ended and 4-way combined PAs are unconditionally stable. The PA shows a maximum small-signal gain of 25.9 dB with $|S_{11}|$ and $|S_{22}|$ better than -10 dB at 185 GHz. The measured gain at 185 GHz is slightly (1.3 dB) lower than the simulated one (27.2 dB). The discontinuity at 170 GHz is clearly related to the change of measurement set-up (D- or G-band). The 3 dB and 6 dB bandwidth of the PA are 27 GHz and 42 GHz, respectively.

B. LARGE-SIGNAL

The large-signal characterization of the PA was performed using a setup similar to the small-signal test bench with the difference in the use of a power meter at the output of the DUT. Fig. 18 shows the D-band output power

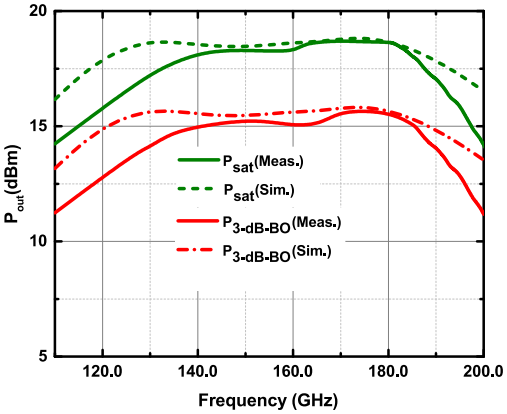


FIGURE 20. Measured and simulated output power of the 4-way combined PA at 3-dB back-off and saturation.

measurement setup. The input signal feeds the DUT, which is generated using similar method discussed in section V-A. The amplified signal at the output of DUT is detected by the VDI Erickson PM5 power meter. For the characterization in G-band, the frequency extender ZC170 was replaced with ZC260, while WR 4.0 probes were adopted. The loss of RF-probes found from the data-sheet was de-embedded in the power measurement.

Fig. 19 shows the measured large-signal parameters of the 4-way combined PA compared with the simulation. These parameters include output power, gain, and PAE at various frequencies in G-band. The PA shows almost similar performance in terms of maximum output power with the difference in gain. For instance, at 185 GHz, the PA achieves 18.1 dBm of saturated output power with 25.9 dB of peak gain and 3.5 % of PAE. Similarly, a maximum output power of 18.7 dBm with a PAE of 4.4 % is demonstrated at 170 GHz. The degradation in measured PAE is due to the output power and gain, which are lower than the simulation. Nevertheless, a good correlation is found between them. The PA consumed maximum overall dc current of 431 mA, which is the sum of currents from each supply ($V_{CC1} = 3$ V, $I_{CC1} = 85.4$ mA, $V_{CC2} = 4$ V,

TABLE 4. State of the Art PAs comparison. Parameters of the PAs are shown at the frequency, which resulted in maximum output power.

3-dB Freq. (GHz)	Process	Topology	Max. Gain (dB)	3-dB Bandwidth (GHz)	P_{sat} (dBm)	PAE (Max. %)	Area (mm^2)	Ref
126-143	40-nm CMOS	3-stage Bal.CT	20.3	17	14.8	8.9	0.34	[2]
130-160	50-nm GaAs mHEMT	3-stage 4-way Comb.CS	15	30	13.1	4	3.1	[3]
191-225*	35-nm GaAs mHEMT	3-stage Bal. CT	12.5	34	10	1.5	0.75	[4]
112.2-147.8	250-nm InP HBT	5-stage 4-way Comb. CE	27.8	35.6	24.0	7.0	1.9	[5]
120.7-188.2	250-nm InP HBT	5-stage Bal. CE	25.3	66.5	20.6	8.0	1.2	[6]
108-123	90-nm SiGe	4-stage CE 8-way Comb.	15	15	20.8	7.6	4.95	[20]
110-122	90-nm SiGe	4-stage Single Ended CE	20	12	13.8	11.6	0.78	[20]
107-142	90-nm SiGe	2-stage Stacked 8-way Comb.	7.7	35	22	3.6	0.62	[21]
109-137	130-nm SiGe	3-stage Diff. CT	26.5	28	16.5	12.8	0.74	[27]
135-170	130-nm SiGe	3-stage Diff. CT	17	35	8	1.6	0.57	[28]
153-159	130-nm SiGe	3-stage Diff. CT	35.4	6*	14	4.8	N.A	[26]
131-180	130-nm SiGe	5-stage Diff. CT	27	49	14	5.7	0.48	[29]
155-180	130-nm SiGe	4-stage Diff. CT 4-way Comb.	30.2	25	18**	4.0	0.85	[30]
200-255	130-nm SiGe	3-stage Diff. CT 4-way Comb.	12.5	55	12*	N.A	0.83	[31]
168-195	**130-nm SiGe**	**3-stage CT 4-way Comb.**	**23.6**	**27**	**18.7**	**4.4**	**1.35**	**This Work**

∗ Data estimated from the graph. NA: Not Available
∗∗ Loss of RF pad and balun de-embedded.

I_{CC2} = 102.7 mA, V_{CC2} = 4 V, I_{CC2} = 242.9 mA). The resulting overall dc power consumption is about 1.6 W.

Fig. 20 shows the simulated and measured output power at 3-dB back-off and at saturation. In the simulation, the saturated output power is found for a fixed input of 5 dBm. The PA provides a 3-dB back-off output power larger than 15 dBm and a P_{sat} larger than 18 dBm at frequencies ≈140-186 GHz. Such performances make the PA highly desirable for various broadband applications.

Table 4 shows summary of the various parameters of state-of-the-art PAs based on both Si (SiGe BiCMOS, CMOS) and III-V (InP, GaAs) technologies at various frequencies in D and G-bands. Advanced InP process achieves high output power and PAE than GaAs and Si based technologies. However, SiGe BiCMOS is still getting close to InP with highest power demonstrated in the lower D-band around 115 GHz. Few works have shown high output power in the upper D-band, which are still not fully characterized. The PA presented in this work delivers high output power in the G-band at $f \geq 170$ GHz. Also, it achieved saturated output power ≥ 18 dBm over a wide range of frequencies at 140-186 GHz, which is state-of-the-art for SiGe BiCMOS technology.

VI. CONCLUSION

A fully integrated G-band PA based on the 130-nm SiGe BiCMOS technology with an output power larger than 18 dBm is presented. The large-signal performance of the PA relies on the low-loss wide-band on-chip power combiner and single-ended PAs. Besides, detail procedure about the design of 4-way combined PA is presented, which includes selection of the topology, effect of the interconnections, schematic and complete layout of the single-ended PA, and four-way combiner.

The future work can focus on improving the small-signal bandwidth, reducing the DC power and chip area consumption of the PA without significantly degrading the large-signal performance. The procedure adopted in this paper can be applied at higher frequencies above 200 GHz to design high power PA. Also, the PA can be utilized in the design of different solid-state systems for various future applications.

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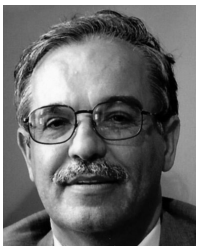

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