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An Efficient Reconfigurable RF-DC Converter With Wide Input Power Range for RF Energy Harvesting

DANIAL KHAN[1], (Student Member, IEEE), SEONG JIN OH[1], (Student Member, IEEE), KHURAM SHEHZAD[1], (Student Member, IEEE), MUHAMMAD BASIM[1], (Student Member, IEEE), DEEKSHA VERMA[1], (Student Member, IEEE), YOUNG GUN PU[1], (Member, IEEE), MINJAE LEE[2], (Senior Member, IEEE), KEUM CHEOL HWANG[1], (Senior Member, IEEE), YOUNGOO YANG[1], (Senior Member, IEEE), AND KANG-YOON LEE[1], (Senior Member, IEEE)

[1]Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea
[2]School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology, Gwangju 61005, South Korea

Corresponding author: Kang-Yoon Lee (klee@skku.edu)

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ABSTRACT This paper presents a reconfigurable radio frequency to direct current (RF-DC) converter operating at 902 MHz frequency designed to efficiently harvest RF signals and convert into useable DC voltages for RF energy harvesting applications. The proposed scheme employs a dual-path, a series (low-power) path and a parallel (high-power) path, to maintain high power conversion efficiency (PCE) over wide input power range. The dual-path is composed of two identical rectifier blocks utilizing internal threshold voltage cancellation (IVC) technique to efficiently compensate the threshold voltage of the transistors used as rectifying devices. An adaptive control circuit (ACC) consisting of a comparator, an inverter and three switches is used in the proposed scheme. The ACC activates the series path or the parallel path to maximize the harvested power based on the input power range. The proposed scheme is designed and fabricated in a 180 nm complementary metal-oxide semiconductor (CMOS) technology. The measurement results show that PCE of the proposed circuit is above 20% from −18 dBm to −5 dBm, maintaining 13-dB input power range with peak PCE of 33% at −8 dBm for 200 kΩ load resistance. The proposed circuit demonstrates −20.2 dBm sensitivity across 1 MΩ load resistance while producing 1 V output DC voltage.

INDEX TERMS CMOS technology, dual path, power conversion efficiency, reconfigurable, RF-DC power converter, RF energy harvesting.

I. INTRODUCTION

In recent years, radio frequency (RF) energy harvesting has become an intensive area of research for remote power supply of wireless sensors/devices in the Internet of Things (IoT), radio frequency identification (RFID) systems and biomedical implanted devices by eliminating the need for battery and its limited lifetime [1]–[4]. Depending upon batteries as reliable energy source for wireless sensors/devices impose several constraints including regular charging and maintenance of the batteries due to their limited lifetime and their replacement in harsh environments. An RF-DC converter in an RF energy harvesting system scavenges the electromagnetic energy from ambient sources and converts into DC voltage for power supply of wireless sensor/devices [5].

Fig. 1 shows a block diagram of an entire far-field wireless power transfer (WPT) system which consists of a RF power source connected to a transmitting antenna, a radio channel, and a receiving antenna connected to an RF energy harvester [6]–[9]. The receiving antenna receives the incoming RF energy and forwards it to an impedance matching circuit which ensures the maximum power transfer from the receiving antenna to an RF-DC power converter. The RF-DC converter rectifies the incoming RF energy and converts into

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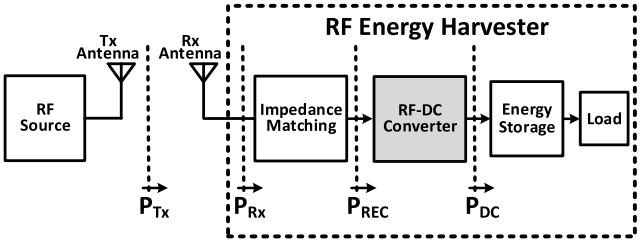


FIGURE 1. Block diagram of a far-field wireless power transfer system.

the output DC power. Finally, an energy storage component (capacitor or battery) is used to store the output DC voltage. The performance of the RF-DC converter, being the main component in RF energy harvesting system, can be evaluated by its power conversion efficiency (PCE) and sensitivity. The PCE is the ratio of power, harvested by the RF-DC converter, delivered to the load to the RF input power while sensitivity is the minimum input power required to generate DC voltage at the output. The PCE of the RF-DC converter can be expressed as [20]:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{OUT}^2}{R_L \cdot P_{in}} \times 100\% \quad (1)$$

where P_{in} is the input power applied to the RF-DC converter, V_{OUT} is the output DC voltage across the resistive load R_L.

In a far-field WPT system, the performance of an RF energy harvester is strongly affected by several factors. For example, limited signal strength received at the input of the RF energy harvester due to path loss, the unpredictable attenuations in the signal strength over distance from the power source [10], presence of hurdles/obstacles between the RF energy harvester and the power source, antenna orientation, and transmission medium in which the RF energy harvester is utilized. As a result, the overdrive voltages generated by the RF voltage levels are not large enough for the rectifying devices to have low conduction losses even after boosted by the impedance matching circuit. Consequently, the RF energy harvester fails to harvest the maximum possible energy and its performance degrades. Therefore, designing a high performance RF energy harvester over a wide input power range is a major challenge, especially at low input power levels.

A number of threshold voltage compensation techniques for the rectifying devices have been proposed in order to increase the efficiency of the RF energy harvesters. Technology-based techniques use Schotty diodes [11] or HSMS diodes [12] to implement the rectifier circuit. The drawbacks of these techniques are high production cost that is caused by the additional fabrication steps and integration with the standard CMOS integrated circuits. Circuit-based techniques including active/passive circuits are alternatively used for threshold voltage (V_{th}) compensation of transistors used as rectifying devices [13]–[27]. The active circuit reported in [13] requires external battery that results in increased cost and maintenance. On contrary, passive techniques generally do compensation of threshold voltage of the rectifying devices by using additional circuitry. An adaptive threshold voltage compensated scheme proposed in [14] uses auxiliary transistors to control gate-source voltage of the rectifying devices. A differential dual-path CMOS rectifier described in [15] employs an adaptive control circuit to control both high-power path and low-power path over extending input power range. However, high-power is always connected to antenna which increases the parasitic capacitances once the low-power path is activated to harvest the RF energy. Authors in [16], [17] implement maximum power point tracking (MPPT) technique selecting optimum number of rectifier stages to maintain high PCE over wide input power range. A differential CMOS rectifier used in [18] implements a reconfigurable circuit that reconfigure the stages from parallel to series and vice versa based on the RF power level. A hybrid threshold voltage compensated scheme used in [19] employs PMOS transistors as rectifying devices in all rectifier's stages except in first stage in order to eliminate the need of NMOS triple-well transistors. Author in [20] reports a dual-band rectifier implementing an internal threshold voltage compensation technique. A differential cross-coupled rectifier reported in [21] compensates the threshold voltage of the rectifying devices and minimizes their leakage current. A self-compensation scheme used in [22] consists of triple-will NMOS transistors in order to provide individual body biasing. A self-biasing circuit described in [23] provides DC biasing voltage by using off-chip impedance resistive network. Author in [24] presents a threshold voltage compensation circuit where passively generated compensated voltage stored on the capacitor is applied to gate-source terminal of the rectifying devices. A differential cross-coupled rectifier reported in [25] reduces the reverse-leakage current problem occurred in the conventional cross-coupled rectifier. However, differential circuits require a PCB balun for conversion of single-ended to differential or differential antenna which result in additional cost and large area on the PCB board. Authors in [26], [27] report a cascaded rectifier using dynamic threshold voltage cancellation (DVC) technique in combination with the internal threshold voltage cancellation (IVC) technique to efficiently compensate threshold voltages of the rectifying devices.

Most of the circuit solutions proposed in the literature have been designed to produce maximum PCE at a specific input power level and failed to harvest RF energy at wide low input power range. This paper presents a reconfigurable RF-DC converter that harvests the maximum possible RF energy and maintains high PCE over wide low input power range. The proposed circuit demonstrates superior performance to the published state-of-the-art work.

This paper is organized as follows. Section II describes the working principle of the proposed reconfigurable RF-DC converter. Section III explains the circuit description of the sub-blocks of the proposed architecture. Sections IV depicts the measurement results. Section V finally concludes the paper.

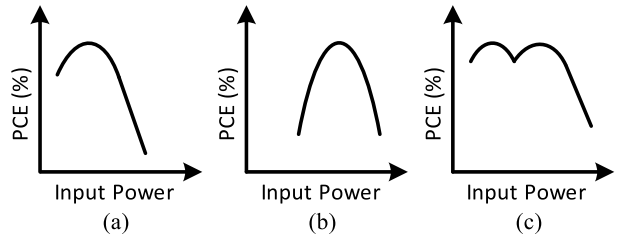


FIGURE 2. Conventional rectifier's performance (a) at low power, (b) at high power, and (c) reconfigurable rectifier's performance.

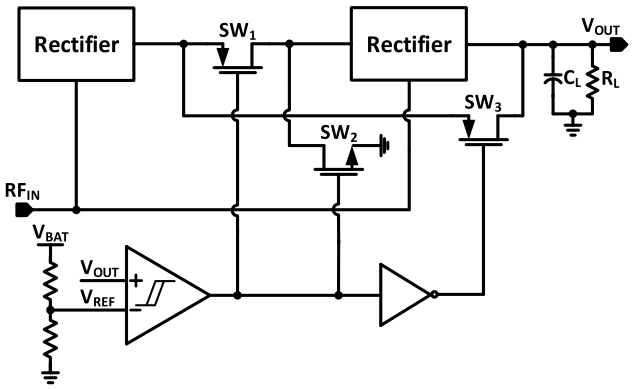


FIGURE 3. Block diagram of the proposed reconfigurable RF-DC power converter.

II. PROPOSED RECONFIGURABLE RF-DC CONVERTER

Fig. 2 presents the conceptual idea applied in the proposed reconfigurable circuit. Fig. 2(a) and (b) display the PCE of a conventional single-path power converter that is optimized to operate efficiently at low input power and high input power, respectively. It is clear that the high-PCE can only be achieved over a narrow input power range for the single-path rectifier. On the contrary, Fig. 2(c) depicts a high PCE graph of the reconfigurable circuit. This high PCE, over wide input power range, is achieved by combining both graphs of Fig. 2(a) and (b).

Fig. 3 shows block diagram of the proposed reconfigurable RF-DC converter. The proposed scheme is composed of two identical rectifier blocks, three MOSFET switches (SW_1, SW_2 and SW_3), a comparator, and an inverter. The switches are used to reconfigure the proposed circuit and are controlled by the output of the comparator and the inverter. The transistors used in the proposed architecture are low threshold voltage (LVT) of general purpose (GP). Fig. 4 presents the working principle of the proposed circuit. Fig. 4(a) shows the series-path operation of the proposed circuit for low input power range. The comparator compares output voltage (V_{OUT}) of the proposed circuit to a reference voltage (V_{REF}). As long as the V_{OUT} is lower than the V_{REF}, the comparator gives low-voltage "VCMP = L" and the inverter gives high-output "H". This mechanism turns-on the switch SW_1 and turns-off the switches SW_2 and SW_3 to allow the two identical rectifier blocks to operate in series with each other. This increases the harvested power at the output and eventually increases the PCE of the proposed scheme at the low input power range. Fig. 4(b) represents parallel-path operation of the proposed circuit for high input power range. When V_{OUT} becomes higher than the V_{REF}, the comparator produces high-voltage "VCMP = H" and inverter produces low voltage "L". This process turns-off the switch SW_1 and turns-on the switches SW_2 and SW_3 to allow the two identical rectifier blocks to operate in parallel with each other. This increases the PCE of the proposed scheme at high input power level. Consequently, the overall PCE of the proposed reconfigurable circuit is extended and improved over extended input power range.

III. CIRCUIT DESCRIPTION

A. RF-DC CONVERTER DESIGN

Fig. 5 presents circuit description of one of the rectifier blocks used in the proposed reconfigurable power converter scheme. The rectifier circuit used in the proposed scheme is similar to the rectifier proposed in [20]. The rectifier circuit employs internal threshold voltage cancellation (IVC) technique for threshold voltage (V_{th}) compensation of the transistors used as rectifying devices. The main rectification body is composed of one NMOS transistor (M_n) and two PMOS transistors (M_{p1} and M_{p2}). An auxiliary block is made-up of two PMOS transistors, namely M_a and M_b, which are referred as back-compensated transistor and forward-compensated transistor, respectively. The width of M_n is chosen 7 μm while widths of M_{p1} and M_{p2} are set to be 14 μm each. The widths of M_a and M_b are selected to be 1 μm each, and channel lengths of all the transistors are set to be minimum. The value of both coupling capacitor (C_{in}) and auxiliary capacitor (C_{aux}) are chosen 2 pF. The transistors M_a and M_b reduce V_{th} of forward-biased transistors and minimize the reverse leakage current of the reverse-biased transistors in the main rectification chain, respectively. During positive phase of input power, as shown in Fig. 5(a), the back-compensated transistor M_a reduces V_{th} of the forward-biased transistors (M_{p1} and M_{p2}), and increases harvested power in the main rectification chain. The forward-compensated transistor M_b remains turned-off as its source-gate voltage (V_{sg}) lies below V_{th}. During negative phase of input power, as shown in Fig. 5(b), the rectifying devices M_{p1} and M_{p2} are reversed-biased, and V_{sg} of M_b is larger than its V_{th} to turn it on. This reduces source-gate voltages (V_{sg1} and V_{sg2}) of transistors (M_{p1} and M_{p2}) to zero, respectively, and consequently minimizes the leakage current in the rectification chain. The auxiliary capacitor, C_{aux}, stores some charge which is lost during reversed-biased condition. Indeed, the voltage drop (V_{aux}) across capacitor C_{aux} is obtained from both forward and reverse conduction and can be written as:

$$V_{aux} = C_{aux} \times (Q_{fwd} + Q_{rev}) \tag{2}$$

By applying the Kirchhoff Voltage Law (KVL) in Fig. 5.

$$V_{in} = V_{sg1} + V_{aux} \tag{3}$$

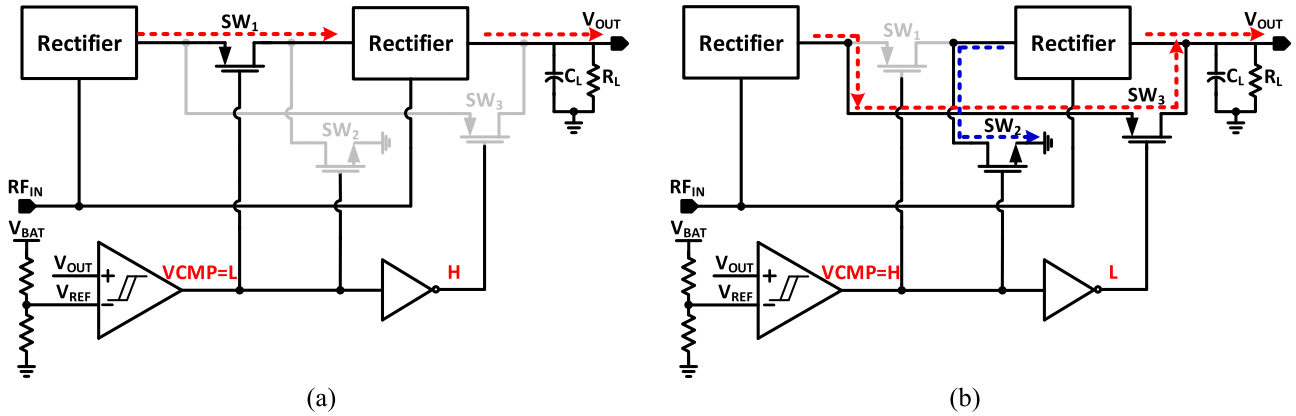


FIGURE 4. Proposed reconfigurable RF-DC converter with (a) series path operation, and (b) parallel path operation.

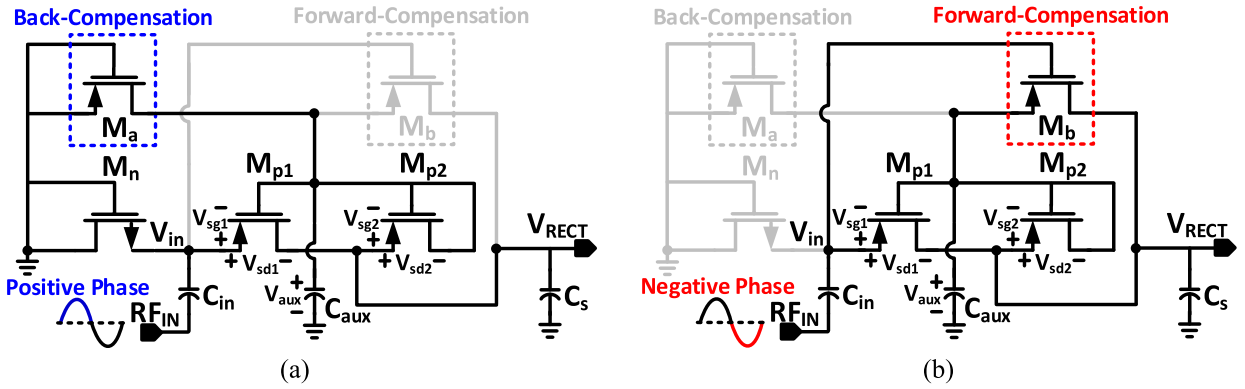


FIGURE 5. Rectifier circuit with (a) positive phase operation, and (b) negative phase operation.

where V_{in} is the peak RF input amplitude. The output DC voltage (V_{RECT}) of the rectifier can be written as:

$$V_{RECT} = V_{in} - V_{sd1} \tag{4}$$

where V_{sd1} is the source-drain voltage of the M_{p1}. By replacing V_{in} of Eq. (3) in Eq. (4), V_{RECT} can be written as:

$$V_{RECT} = -V_{sd1} + V_{sg1} + V_{aux} \tag{5}$$

Similarly,

$$V_{RECT} = V_{sg2} + V_{aux} \tag{6}$$

By subtracting (6) from (5), it can be written as:

$$V_{sd1} = V_{sg1} - V_{sg2} \tag{7}$$

The V_{sg2} of the M_{p2} increases as long as the output voltage (V_{RECT}) of the rectifier increases. When the V_{sg2} is equal to the threshold voltage of the M_{p2}, the M_{p1} enters the saturation region. As a result, the proposed circuit compensates the effect of threshold voltage and improves the PCE and output DC voltage V_{RECT}.

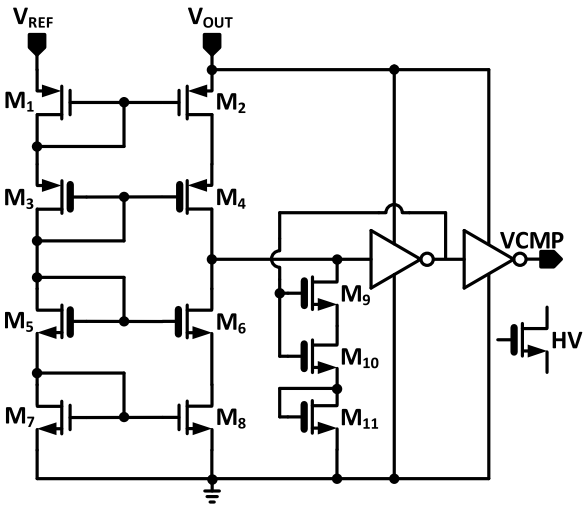
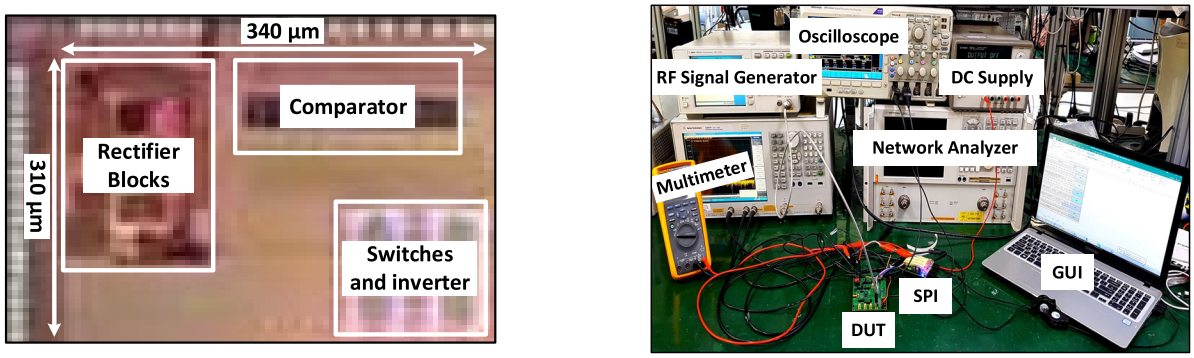


FIGURE 6. Circuit diagram of the common-gate input comparator.

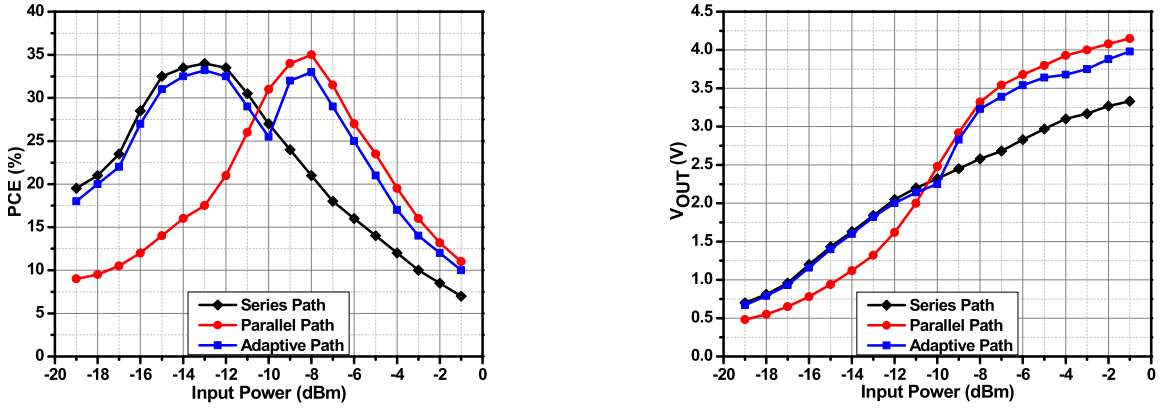
B. ADAPTIVE CONTROL CIRCUIT DESIGN

Due to limited harvested power from ambient environment, power consumption must be taken into account when design low-power adaptive control circuit (ACC). The ACC consists of a common-gate input comparator, an inverter and three switches (SW_1, SW_2 and SW_3). The common-gate input



(a) (b)

FIGURE 7. (a) Microphotograph of the fabricated chip, and (b) Measurement setup to test the proposed circuit's chip.



(a) (b)

FIGURE 8. Measurement results of the proposed circuit versus input power for 200 kΩ load. (a) PCE, and (b) output DC voltage.

comparator is the key circuit of the ACC. Fig. 6 displays the circuit diagram of the common-gate input comparator having same structure as described in [15]. The comparator compares the output voltage (V_{OUT}) of the proposed circuit to the reference voltage (V_{REF}) and controls the switches (SW_1, SW_2 and SW_3) in order to reconfigure the proposed circuit depending upon the input power level. At low input power conditions, the current consumption of the comparator is exponential and is negligible. Moreover, high voltage devices with low-current conduction are used in the comparator to avoid extra current consumption at high input power conditions.

IV. MEASUREMENT RESULTS

A. CHIP MICROPHOTOGRAPH AND MEASUREMENT SETUP

The proposed reconfigurable RF-DC converter is fabricated in a standard 180 nm CMOS technology. Fig. 7(a) presents the chip microphotograph of the proposed circuit having an active die area of 340 μm $\times$ 310 μm, excluding the pads. Fig. 7(b) depicts the measurement setup to check the performance of the proposed circuit. The fabricated chip is wire-bonded on a PCE board. A single-tone sinusoidal signal operating at 902 MHz is generated by Agilent E4438C signal generator to test the chip. An Oscilloscope, Tektronix TDS 2024B, and a digital voltmeter are used to record the output DC voltage. An off-chip pi-matching circuit is implemented onto the PCB board to match the input impedance of the proposed circuit to 50 Ω and reflection co-efficient $|\boldsymbol{S_{11}}|$ is calculated. The net input power that is given to the chip is calculated after excluding the transmission losses and the reflection losses.

B. PERFORMANCE MEASUREMENT

The performance of the proposed circuit is determined by the PCE and the output DC voltage versus input RF power. The measured reflection co-efficient $|S_{11}|$ at 902 MHz of the proposed circuit is −27.5 dB. To check the performance of the series path and parallel path separately, two off-chip control pins can be used to enable/disable the series and the parallel path. When both pins are connected to a high voltage, the proposed circuit operates in the adaptive selection mode.

Fig. 8(a) shows measured PCE of the proposed circuit versus input power range for an optimum load resistance of 200 kΩ. Measurement results show that more than 20% PCE is achieved from −18 dBm to −8 dBm for series (low-power) path with peak PCE of 34% at −13 dBm. Similarly, PCE is above 20% from −12 dBm to −5 dBm for parallel (high-power) path with peak PCE of 35% at −8 dBm. When the adaptive control circuit automatically selects the

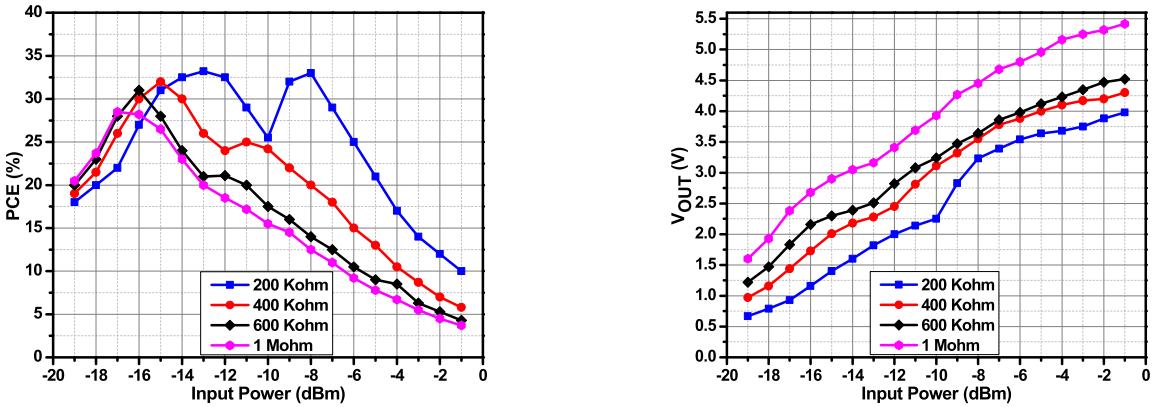


FIGURE 9. Measurement results of the proposed circuit versus input power for different loads. (a) PCE, and (b) output DC voltage.

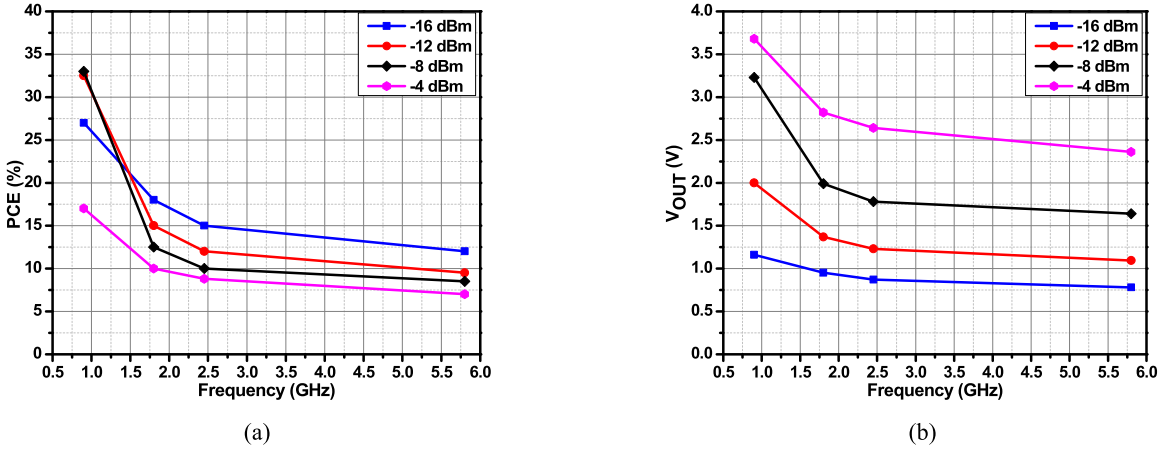


FIGURE 10. Measurement results of the proposed circuit versus frequency for 200 kΩ load. (a) PCE, and (b) output DC voltage.

dual-path depending upon the value of V_{OUT} and V_{REF}, the PCE of the proposed circuit is above 20% from −18 dBm to −5 dBm with peak PCE of 33% at −8 dBm and maintains 13-dB input power range. Even though the switches used to reconfigure the proposed circuit are not ideal switches due to process variations, the PCE of the proposed scheme with adaptive path control circuit is still improved.

Fig. 8(b) depicts the measured output DC voltage versus input power range for load resistance of 200 kΩ. The output DC voltage of the series (low-power) path is higher than the parallel (high-power) path from −19 dBm to −11 dBm. From −10 dBm to onward, output DC voltage of the parallel path is higher than the series path. Fig. 9(a) shows the measured PCE of the proposed circuit for different loads. The peak efficiencies of the proposed circuit are 33%, 32%, 31%, and 28.5% at input power levels of −8 dBm, −15 dBm, −16, and −17 dBm for load resistances of 200 kΩ, 400 kΩ, 600 kΩ, and 1 MΩ, respectively. Fig. 9(b) displays the measured output DC voltages of the proposed circuit for different loads. It can be seen that the output DC voltage increases with the increase in load resistances. Fig. 10(a) and (b) depict measured PCE and output DC voltage of the proposed circuit versus frequency at different input power levels for 200 kΩ load, respectively. Since the proposed circuit is optimized and designed for 902 MHz, it gives superior performance at 902 MHz to the other frequencies. The proposed circuit achieves a sensitivity of −20.2 dBm while producing 1 V output DC voltage for 1 MΩ resistive load.

C. COMPARISON WITH PUBLISHDED WORKS

Table 1 summarizes the measurement results of the proposed circuit and its performance is compared with the published state-of-the-art works. The proposed circuit provides a reconfigurable structure to achieve high PCE over extended input power range. Despite being single-ended structure, the proposed circuit shows better performance than most of the reported works. The PCE is above 20% from −18 dBm to −5 dBm over 13-dB input power range. The peak PCE of 33% is achieved at −8 dBm with an output DC voltage of 3.23 V across 200 kΩ load resistance. The proposed circuit achieves wider input power range than the circuits reported in [14], [15], and [21] while demonstrates better sensitivity than the circuits reported in [15], [16], [22], and [25].

TABLE 1. Performance summary.

	This Work	[14]	[15]	[16]	[21]	[22]	[25]
Technology	180 nm	130 nm	65 nm	180 nm	90 nm	90 nm	180 nm
Frequency	902 MHz	915 MHz	900 MHz	900 MHz	868 MHz	915 MHz	1 GHz
Reconfigurable	Yes	-	Yes	Yes	-	-	-
Additional requirements	-	-	Differential antenna	Maximum Power Point Tracking	Differential antenna	Triple-well	Differential antenna
Peak PCE and at different input power levels	Peak: 33.0% @ -8 dBm 20% @ -18 dBm 21% @ -5 dBm	Peak: 32.0% @ -15 dBm 18% @ -19 dBm 18% @ -10 dBm	Peak: 36.5% @ -10 dBm 20% @ -16 dBm 20% @ -5 dBm	Peak: 48.2% @ 0 dBm 31.8% @ -20 dBm 41.1% @ 20 dBm	Peak: 24.0% @ -21 dBm 18% @ -15 dBm 10% @ -11 dBm	Peak: 11.0% @ -18.8 dBm 9% @ -15 dBm 3.5% @ -10 dBm	Peak: 65.0% @ -18 dBm 30% @ -25 dBm* 30% @ -10 dBm*
Output DC Voltage	3.23 V @ -8 dBm	3.2 V @ -15 dBm	2.3 V @ -10 dBm	3.32 V @ 0 dBm	1.4 V @ -21 dBm	1.2 V @ -18.8 dBm	1 V @ -18 dBm
Load	R_L = 200 kΩ	R_L = 1 MΩ	R_L = 147 kΩ	R_L = 23 kΩ	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 100 kΩ
Effective area	0.105 mm^2	0.25 mm^2	0.048 mm^2	0.32 mm^2	0.029 mm^2	0.19 mm^2	0.00845 mm^2
Input power range for PCE > 20%	13 dB	7.5 dB	11 dB	40 dB	8 dB	N.A.	17 dB*
Voltage Sensitivity: 1 V for R_L	-20.2 dBm for R_L = 1MΩ	-20.5 dBm	-16 dBm	-20 dBm for R_L = 1MΩ	-23 dBm	-17.5 dBm	-18 dBm

* Estimated from the figure.

V. CONCLUSION

In this paper, a reconfigurable RF-DC converter operating at 902 MHZ frequency to efficiently harvest radio frequency energy is presented. The proposed architecture uses a dual-path, a series (low-power) path and a parallel (high-power) path, to maintain high PCE over extended input power range. The adaptive control circuit activates the series path or the parallel path based on the input power level to maximize the harvested power at the output. Despite of process variations of the switches, the proposed circuit still achieves better PCE over extended input power range. The proposed scheme has been designed and fabricated in 180 nm CMOS technology. The measurement results show that the PCE of the proposed scheme is above 20% from −18 dBm to −5 dBm with peak measured PCE of 33% at −8 dBm. The proposed circuit obtains −20.2 dBm sensitivity for 1 MΩ load while producing 1 V output DC voltage.

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DANIAL KHAN (Student Member, IEEE) received the B.S. degree in electrical and electronic engineering from the University of Engineering and Technology, Peshawar, Pakistan, in 2011. He is currently pursuing the combined M.S. and Ph.D. degree with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. His research interests include RF energy harvesting systems, wireless power transfer (WPT) systems, and power management ICs designs.

SEONG JIN OH (Student Member, IEEE) received the B.S. degree from Sungkyunkwan University, Suwon, South Korea, in 2014. He is currently pursuing the combined M.S. and Ph.D. degree with the School of Information and Communication Engineering, Sungkyunkwan University. His research interests include CMOS RF transceivers, all digital phase locked loops, wireless power transfer receivers, and rectifiers.

KHURAM SHEHZAD (Student Member, IEEE) received the B.S. degree in electrical engineering with specialization in telecommunication from Government College University, Faisalabad, Pakistan. He is currently pursuing the combined M.S. and Ph.D. degree in electrical and computer engineering from the College of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea. His research interests include design of high performance data converters including SAR and SD ADC, and CMOS RF Transceiver.

MUHAMMAD BASIM (Student Member, IEEE) received the B.S. degree in electrical (telecommunication) engineering from the University of Science and Technology, Bannu, Pakistan, in 2015. He is currently pursuing the M.S. degree with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. His research interests include RF energy harvesting systems and power management ICs designs.

DEEKSHA VERMA (Student Member, IEEE) received the B.S. degree from CSJM University, Kanpur, India, and the M.S. degree in information and communication engineering from Gautam Buddha Technical University, Lucknow, India. She is currently pursuing the Ph.D. degree with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. Her research interests include design of high-performance data converters including SAR, Power IC, including DC–DC converters.

YOUNG GUN PU (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the Department of Electronic Engineering, Konkuk University, Seoul, South Korea, in 2006, 2008, and 2012, respectively. His research interests include CMOS fully integrated frequency synthesizers and oscillators and on transceivers for low-power mobile communication.

MINJAE LEE (Senior Member, IEEE) received the B.Sc. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 2008. In 2000, he was a consultant with GCT semiconductor, Inc., and Silicon Image Inc., designing analog circuits for wireless communication and digital signal processing blocks for Gigabit Ethernet. He joined Silicon Image Inc., Sunnyvale, CA, in 2001, developing Serial ATA products. In August 2008, he joined Agilent Technologies in Santa Clara, CA, where he was involved with the development of next generation high-speed ADCs and DACs. Since 2012, he has been with the School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju, Korea, where he is currently an Assistant Professor. He was a recipient of the 2007 Best Student Paper Award at the VLSI Circuits Symposium, Kyoto, Japan, and the GIST Distinguished Lecturer Award, in 2015.

KEUM CHEOL HWANG (Senior Member, IEEE) received the B.S. degree in electronics engineering from Pusan National University, Busan, South Korea, in 2001, and the M.S. and Ph.D. degrees in electrical and electronic engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2003 and 2006, respectively. From 2006 to 2008, he was a Senior Research Engineer with the Samsung Thales, Yongin, South Korea, where he was involved with the development of various antennas including multiband fractal antennas for communication systems and Cass-grain reflector antenna and slotted waveguide arrays for tracking radars. He was an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, South Korea, from 2008 to 2014. In 2015, he joined the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include advanced electromagnetic scattering and radiation theory and applications, design of multiband/broadband antennas and radar antennas, and optimization algorithms for electro-magnetic applications. He is a Life-Member of KIEES and a member of IEICE.

YOUNGOO YANG (Senior Member, IEEE) was born in Hamyang, South Korea, in 1969. He received the Ph.D. degree in electrical and electronic engineering from the Pohang University of Science and Technology (Postech), Pohang, South Korea, in 2002. From 2002 to 2005, he was with Skyworks Solutions Inc., Newbury Park, CA, where he designed power amplifiers for various cellular handsets. Since March 2005, he has been with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea, where he is currently an Associate Professor. His research interests include power amplifier design, RF transmitters, RFIC design, integrated circuit design for RFID/USN systems, and modeling of high-power amplifiers or devices.

KANG-YOON LEE (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Seoul National University, Seoul, South Korea, in 1996, 1998, and 2003, respectively. From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, USA, where he was the Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University, as an Associate Professor. Since 2012, he has been with College of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently a Professor. His research interests include implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.