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Temperature-Dependent Logic Behavior of Logic Transistors Based on WS_2

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ABSTRACT With the advantages of two-dimensional (2D) materials, the small footprint logic transistor architecture can realize the primary logic function (OR and AND) in a single cell. Compared with silicon transistors, the logic transistor is expected to be a competitive candidate for next-generation electronic technology with distinct functions and high area-efficiency. We report on the fabrication of logic transistors based on WS_2 using the new architecture and the investigation of the temperature-dependent logic behavior. Notably, the device shows general trends of logic function on different operating voltages and switches AND logic to OR logic from low temperatures to high temperatures. We also measured the transport properties of the WS_2 logic transistors at different temperatures to demonstrate our theoretical analysis. The threshold voltage, saturation current, and field-effect mobility are extracted from transport characteristics, which is in line with our mechanism explanation. This work reveals that temperature is of much significance to the logic function of logic transistors.

INDEX TERMS Logic transistor, temperature-dependent, WS_2.

I. INTRODUCTION

The development of modern electronic devices has been spurred by continuous downscaling of silicon-based architectures, which includes scaling down the active area such as the channel length and the gate dielectric thickness. However, Moore's Law is facing great challenges for traditional CMOS (Complementary Metal Oxide Semiconductor) technology based on silicon is approaching its physical limitation. Liu *et al.* proposed a brand new MoS_2 logic transistor architecture for logic application to realize high area efficiency compared with conventional silicon transistors to meet the demand of rapidly developing electronics [1]. By taking advantage of the unique characteristics of 2D materials, such as atomic-level thickness and diverse electrical properties [2]–[4], a single transistor can achieve the basic logic function (OR and AND). But at least two silicon transistors are required to build a logic gate. Remarkably, with variable intriguing properties of channel materials, the new transistor architecture provides an alternate computing technology, which paves the way towards the development of tailor-made 2D circuits in the future.

The measurement environment like light illumination can switch the logic function [1] for the light can excite carriers in the 2D material channel. Temperatures can also influence the carrier concentration due to energy band changing [5]–[7] and scattering [8]. Therefore, the logic transistor is expected to show different logic functions in variable temperatures. For practical application, it is critical to investigate the thermal properties of logic transistors. However, one of the limitations of the potential application for MoS_2 is the relatively low phono-limited mobility at room temperature [9], [10]. We choose WS_2 as the new channel material to fabricate the logic transistor and investigate its temperature-dependent logic behavior. WS_2, another representative member of transition metal dichalcogenides (TMDs) family, has a similar crystal structure of MoS_2 but is less explored. WS_2 is an n-type semiconductor and goes through a transition from a direct bandgap of 2.1 eV in monolayer [11] to an indirect bandgap of 1.4 eV in bulk [12], which behaves

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like most of TMDs. Owing to its small effective electron mass, WS_2 is supposed to possess the highest mobility over 1000 $cm^2V^{-1}s^{-1}$ among TMDs members. There have been some previous studies about temperature-dependent electrical transport behavior of WS_2 FETs [13], [14], however, the temperature-dependent logic behavior of WS_2 logic transistor has never been reported.

In this work, we have studied the temperature-dependent logic behavior of logic transistors based on WS_2. The transistor shows the general trend of logic function from AND logic at low temperatures to OR logic at high temperatures. We investigated the electronic properties of WS_2 transistors in the temperature range from 10 K to 320 K and analyzed the physical mechanism by extracting key parameters such as threshold voltage and field-effect mobility. The experimental results are consistent with our mechanism explanation for temperature-dependent logic behavior.

II. CHARACTERIZATION

Here, we fabricate a logic transistor based on WS_2. FIG. 1(a) shows a schematic diagram of the logic transistor measured in the temperature range from 10 K to 320 K. WS_2 serves as the channel material and we choose hBN as the top and back dielectric layers. WS_2 and hBN thin films are obtained from bulk materials by the mechanical exfoliation method. The detailed fabrication processes are described in Appendix section 1. In the structure, the back gate and top gate are considered as input 1 (IN1) and input 2 (IN2), respectively. FIG. 1(b) demonstrates the false-color scanning electron microscopy (SEM) of the transistor. We use atomic force microscopy (AFM) to determine the thickness of the channel WS_2, the top and the bottom hBN, which are 7, 18, 17 nm, respectively. The detailed AFM information is shown in Appendix section 2. In the device fabrication process, we try to choose hBN with the same thickness for the symmetrical dielectric layer, which ensures the logic function of the device and avoids the extra voltage sacrifice to make up for asymmetric gate control ability. We identified the channel material using photoluminescence. The photoluminescence (PL) spectra of WS_2 measured with a solid-state laser (532 nm wavelength) is presented in FIG. 1(c). The wide emission peak around 1.9 eV, which corresponds to the valence band in spin-orbit coupling [15]. There is another small peak around 1.5 eV, which indicates the channel material WS_2 in the device is the multi-layer film. Furthermore, we confirm the channel material WS_2 by Raman force microscopy in FIG. 1(d). WS_2 possesses two distinct peaks around 350 and 420 cm^{-1}, corresponding to the redshift and broadening of the A_{1g} mode and blueshift of 2LA mode. The in-plane mode E1 2g is merged into the 2LA mode peak.

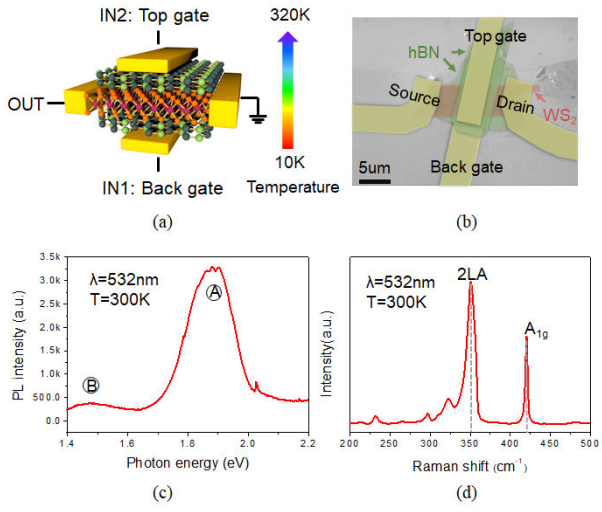

FIGURE 1. Schematic and morphological characterization of the WS_2 logic transistor. (a) Schematic diagram of the WS_2 transistor. (b) False-colored SEM images of the transistor structure. (c) PL spectra for the channel WS_2 using a solid-state laser with 532 nm wavelength. The two peaks are labeled, indicating the channel is the multi-layer WS_2 film. (d) Raman spectra for the channel WS_2 obtained by a laser with a 532 nm wavelength.

III. LOGIC FUNCTION SWITCHING

To describe the logic function using electrical parameters, we have some definitions. We observe the logic behavior of the WS_2 transistor by the synchronous I/V measurement process. A positive or negative gate voltage denotes an input signal with a value of 1 or 0, respectively. And the amplitudes of the positive and negative should be kept the same. The output signal depends on the channel output current, which indicates that OUT-1 and OUT-0 are represented by high and low output current.

To demonstrate the logic behavior of the transistor directly, we use four colored squares to denote the logic function from the original data (see insets in FIG. 2). The detailed data extraction method is introduced in Appendix section 3. Blue/red square represents low/high channel output current and we can easily identify the logic behavior of the WS_2 transistor. If a complete and cascadable voltage-in

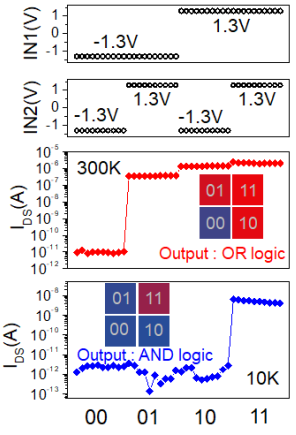

FIGURE 2. The logic function of the WS_2 transistor at a high temperature of 300 K and a low temperature of 10K. Demonstration of the OR logic gate at 300 K and the AND logic gate at 10K with the drain-source voltage at 1.3 V. Top two panels, input signals; Bottom two panels, output signals. The insets present the colored squares of the output currents.

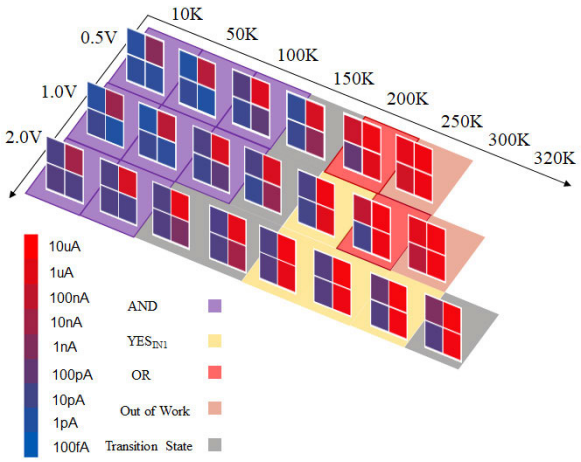

FIGURE 3. Demonstration for the temperature-dependent logic behavior of the device in different operating voltages. The amplitude of operating voltages is 0.5V, 1V, and 2.0V, respectively. The colorful map shows the trend of logic function switching from AND at low temperatures to OR at high temperatures.

voltage-out logic gate is needed in a circuit, a load resistor can be introduced to transfer the current signal to the voltage signal. The detailed measurement configuration and results are demonstrated in Appendix section 4. Because the electronic properties of WS_2 are easily influenced by the adsorbates such as H_2O and O_2 from the atmosphere, the performance in ambient conditions is much worse than in the case of MoS_2. All electrical measurements of WS_2 transistors are performed under vacuum to eliminate the influence.

To ensure the device performance, we first observed logic OR when applied a series of input voltage signals of amplitude 1.3V (IN-00, IN-01, IN-10, IN-11) at room temperature (300K) in the dark. However, when the measured temperature drops to 10K, the situation is quite different, as FIG. 3(b) shows. Only when both gates apply positive voltages, the transistor outputs the high current and shows logic AND. The performance of the logic transistors is stable during 100 periods logic function test (Appendix section 5). Therefore, the device can switch the logic function between OR and AND with temperature changing, which is an interesting phenomenon. To figure out why the logic function is dependent on temperatures, we carried out further experiments to investigate the logic behavior at more different temperatures.

IV. TEMPERATURE-DEPENDENT LOGIC BEHAVIOR

A. TEMPERATURE-DEPENDENT LOGIC BEHAVIOR

We carry out a series of binary inputs to investigate its logic function response in the temperature range from 10 K to 320 K. The colorful map (see FIG. 3) shows detailed temperature-dependent logic behavior of the WS_2 transistor on the different operating voltages in the dark. On the operating voltage of 1.0 V, the device demonstrates a complete temperature-dependent logic changing behavior. Below 100 K, the device exhibits the stable AND logic, which means that only the top and the back gate simultaneously apply positive voltages, can the channel be turned on. As temperature rises, the control of the back gate is getting stronger than that of the top gate. Then the device will experience a transition state that the output current is in the medium state with the input signal of IN-10. Subsequently, we observe the special logic YES_{IN1} that output current is determined by the input signals applied by the back gate. At high temperatures, the control of the back gate and the top gate is strong. The electric field applied by any gate will excite carriers in the corresponding surface channel and the transistor will output high current. Thus, the device shows the OR logic function.

Above 300 K, the voltage of -1.0 V can not turn the channel off, which indicates the device is out of work in this condition. This is because the threshold voltage has an impact on the operating voltage for logic function. As temperature increases, the threshold voltage shifts from positive values to negative values, which leads to that device will be out of work earlier at lower operating voltage. And it also explains that the device will experience different logic behavior in the different operating voltages. The device possesses a lower operating voltage with the threshold voltage value approaching 0 V [1]. In low temperatures, the device can work at lower operating voltages for the threshold voltage is close to 0 V. However, the threshold voltage at high temperatures deviates from 0 V too much, to achieve AND logic needs higher temperatures on the operating voltage of 2 V. Compared with illumination condition, the logic behaviors of the WS_2 transistor show mirror differences in the same temperature range, which implies that temperature is the major factor of influencing the logic function of the device.

Due to temperature-dependent logic behavior, the logic transistor has great potential for applications of reconfigurable circuits. A designer can construct reconfigurable circuits to exactly fit the needs of different functions. It means that one circuit can achieve more than one function in different configurations. The temperature-dependent behavior will be helpful in tailor-made reconfigurable circuits based on 2D materials in the future. The reconfigurable circuit can be designed according to our colorful logic map. For example, at high temperatures, logic transistors behave logic OR and the circuit can achieve the corresponding function; while at low temperatures, the circuit can switch to another function without extra addition elements because logic transistors behave logic AND. Therefore, the reconfigurable circuits based on the logic transistors can meet the need of evolvable applications with high area-efficiency.

B. MECHANISM EXPLANATION

Compared with conventional silicon transistor architecture, the primary logic function can be achieved in a single transistor by taking advantage of 2D materials according to our previous work [1]. Based on that, we can use the bandgap and scattering theory to explain why temperature can influence the logic function of the WS_2 transistor. The output current of the WS_2 transistor is determined by the number of carriers. The bandgap width of WS_2 will get narrow when temperature

increases [5]. The temperature-dependent bandgap is widely studied in the field of 2D materials [6], [7].

At low temperatures, only when both gates apply positive voltage can the channel be turned on. Because large bandgap requires higher activation energy. Low temperatures can not provide enough thermal energy. The conduction band is relatively far to the Fermi level and one positive voltage can not excite enough carriers. Additionally, charge-impurities scattering hinders the motion of the carriers [8]. Therefore, the transistor outputs the high current only with an input signal of IN-11 and shows logic AND. With the temperature increasing, the bandgap width is getting narrow and the conduction band is close to the Fermi level. The activation energy for electrons is reduced and higher temperatures can also provide extra energy. The changes of these two parameters both lead to the increase of the electron density. Thus, the lower voltage can excite plenty of carriers at high temperatures. Moreover, the impact of charge-impurities scattering gets weaker for carriers and directional motion of carriers is easily achieved. Therefore, either the top gate or the back gate can control the corresponding channel. Unfortunately, because of slightly different thicknesses of the dielectric layers and defects caused by the fabrication process, the control of the back gate is stronger than that of the top gate. It resulted in the transition state and special logic YES_{IN1}. When the temperature is high enough, one positive voltage can switch the transistor to on state, which is the observation of logic OR. Thus, we can explain the interesting phenomenon using band theory that the increase of temperature causes the reduction of the bandgap and scattering effect.

V. ELECTRICAL TRANSPORT PROPERTIES

To verify our mechanism explanation, we also performed electrical measurements from 10 K to 320 K at every 50 K step in Lakeshore cryogenic probe station under $<10^{-4}$ mbar. In the process of increasing measurement temperature, we observed some interesting changes in the electrical properties of the device, which is in agreement with our mechanism explanation.

A. TRANSFER CHARACTERISTIC

FIG. 4(a) and (b) show the characteristic curves of the top and back gate with fixing V_{ds} at 500 mV at different temperatures, respectively. As a whole, transfer curves belonging to the top and back gate are reflecting the same trend from the low temperature at 10K to above room temperature. There exist some subtle differences between the two groups of transfer curves, which mainly results from different thicknesses and defects of the top and bottom dielectric layer. The on/off ratio of the device at 320 K is above 10^5, and even apparent at lower temperatures, which means good control of two gates.

B. OUTPUT CHARACTERISTIC

FIG. 4(a) shows the output characteristics of the WS_2 logic transistor with gate voltage fixed at 0V from 10K to 320K. I_{ds} varies nearly linearly with V_{ds}, which indicates good

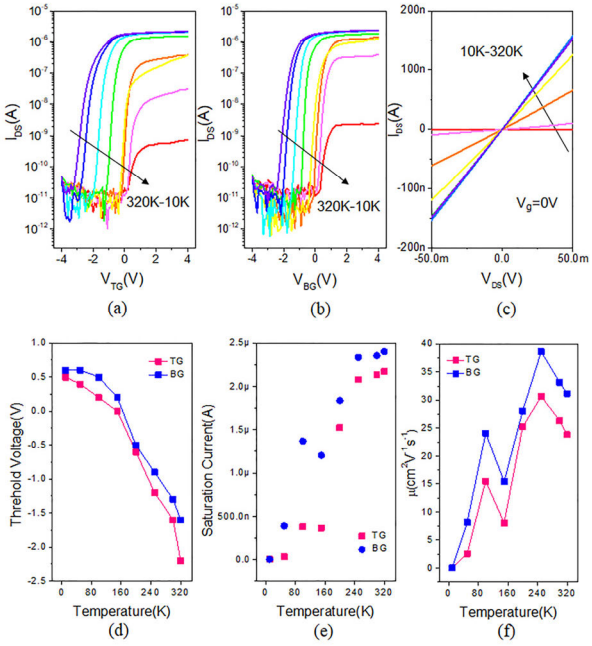

FIGURE 4. Electrical properties of the device at different temperatures. Transfer characteristics ($I_{ds} - V_g$) of the WS_2 transistor from (a) top-gate (b) back-gate controls with V_{ds} fixing at 500 mV in the temperature range from 10 K to 320 K. (c) Output characteristics ($I_{ds} - V_{ds}$) of the WS_2 transistor with gate voltage fixed at 0V from 10K to 320K in linear coordinate. (d) Threshold voltage V_{th} as a function of temperature. (e) Drain-source saturation current as a function of temperature. (f) Field-effect mobility as a function of temperature.

ohmic contact between the electrodes and the channel WS_2. It can be also seen from the symmetrical curves in the logarithmic coordinate system (see Appendix section 6). Moreover, the source-drain current increases as the temperature increases, which is consistent with the transfer characteristics.

C. PARAMETERS EXTRACTION AND ANALYSIS

We can extract some parameters such as threshold voltage, saturation current, field-effect mobility, subthreshold slope, transconductance from characteristic curves. By analyzing the temperature-dependent transport properties of the WS_2 transistor, we can verify our mechanism explanation.

The subthreshold slope of the WS_2 transistor generally increases with temperature, which is consistent with the conventional semiconductor theory (see Appendix section 6). FIG. 4(d) shows the dependence of threshold voltage on temperatures. Lower temperatures lead to a shift of the threshold voltage towards positive values because the density of conducting electrons is related to temperature owing to thermally excited carriers to extended states [14]. It indicates that the activation energy for electrons reduces with increasing temperatures, which is in agreement with bandgap narrowing theory. In general, the source-drain off-state current is stable at the magnitude of pA. However, the source-drain saturation current increases as a function of temperature (see FIG. 4(e)). Because higher temperatures provide extra energy

and bandgap gets narrow as temperature increases. It leads to an increase of carriers in the channel. Notably, the decline of the saturation corresponds to the field-effect mobility in the temperature range between 100 K and 150 K.

The field-effect mobility can be extracted by the expression

$$\mu = [dI_{ds}/dV_g] \times [L/(WC_iV_{ds})] \quad (1)$$

where L=10 um is the channel length, W=5 um is the channel width and C_i is the capacitance between the channel and the gate per unit area. FIG. 4(f) shows the field-effect mobility as a function of temperature. The temperature-dependent mobility is ascribed to a complex interaction between Coulomb scattering, homopolar phono mode quenching, and temperature-dependent screening. At low temperatures, the localized trap states in the bandgap mainly result in low field-effect mobility which monotonically increases below 100 K. In this regime, the charge transport is dominated by Mott variable-range hopping and most electrons are within the trap states [8]. The electron-phonon scattering dominates at high temperatures, which leads to a drop of mobility above 100K. However, charge carriers tend to find percolation pathways when they confront structural defects in the channel [16]. The pathways are available with temperature increasing from 150K to 250K for the charge carrier transport. Additionally, because carriers move faster with temperature increasing, they are less susceptible to impurity-charge scattering, which is in agreement with mechanism explanation. The field-effect mobility reaches a climax of 38 $cm^2V^{-1}s^{-1}$ (31 $cm^2V^{-1}s^{-1}$) for the back gate (the top gate) at 250 K. At higher temperatures, the field-effect mobility is affected by external scattering which results from Coulomb impurities near the WS_2/hBN interface and thermal motion. The screening effect resulting from the polarized charge around Coulomb impurities is weakened, which leads to higher electrical resistance [8]. These reasons lead to a slight drop in the field-effect mobility above 250K. On a whole, the experimental values are much lower than theoretical phonon-limited mobility, which is attributed to charged impurities, charge traps, defects derived from device fabrication. The field-effect mobility could be improved by using a high-K dielectric like HfO_2 to suppress Coulomb scattering owing to dielectric effects [17], [18]. Moreover, *in situ* annealing can improve the contact resistance to enhance mobility [13].

VI. CONCLUSION

In conclusion, our experimental results reveal that the logic WS_2 transistor shows interesting temperature-dependent behavior including electrical properties and logic performance from 10K to 320K. In general, the transistor will experience AND logic, transition state, OR logic as temperature changes from low to high. This work reveals that temperature is a main factor for the logic function. And the logic transistor has great potential for applications of tailor-made reconfigurable 2D circuits in the future.

APPENDIX

1) PREPARATION METHOD

Firstly, the back gate on the 30 nm HfO_2, heavily p-doped Si substrate is prepared by electron beam lithography and sequential electron beam evaporation of 5 nm Cr / 15 nm Au. Then we obtain thin films of WS_2 and hBN from bulk materials onto the 30 nm Al_2O_3, heavily p-doped Si substrate with the method of mechanical exfoliation. Using a wet transfer method, the bottom dielectric layer hBN, the channel WS_2, and the top dielectric layer hBN are transfer onto the substrate with the back gate, respectively. At last, grow the top gate and source/drain electrodes by electron beam lithography and sequential electron beam evaporation of 5 nm Cr / 30 nm Au.

2) AFM CHARACTERIZATION OF THE DEVICE

Figure 5 shows the optical image and the AFM images of different parts of the WS_2 transistor. The thickness of the bottom hBN, channel WS_2, and top hBN is 17nm, 7nm, and 18nm, respectively.

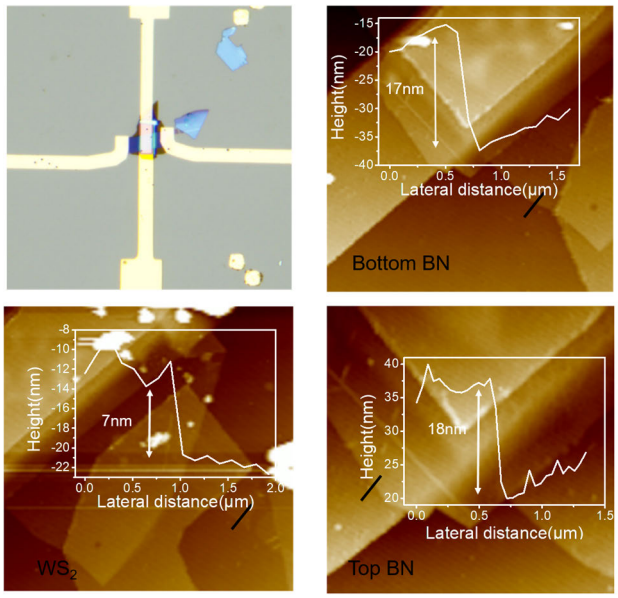

FIGURE 5. AFM images of the device.

3) EXTRACTION METHODS OF LOGIC DATA

In this section, we demonstrate the methods of how to transform the electrical performance to the color pattern. The basic color squares are blue (R=0, G=90, B=180) and red (R=255, G=0, B=0), representing the current values of 100fA and 10μA, respectively. The color squares of the output currents are obtained by computing the RGB with the calculation formula in Figure 6.

4) VOLTAGE-IN VOLTAGE-OUT LOGIC GATE

If a complete and cascadable voltage-in voltage-out logic gate is needed in circuits, a load resistor (22MΩ) can be introduced to transfer the current signal to the voltage signal. Figure 7 shows the measurement configuration and the logic function

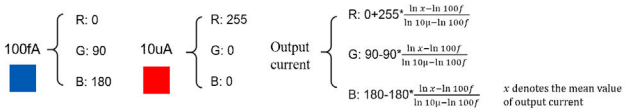

FIGURE 6. **Data process methods.**

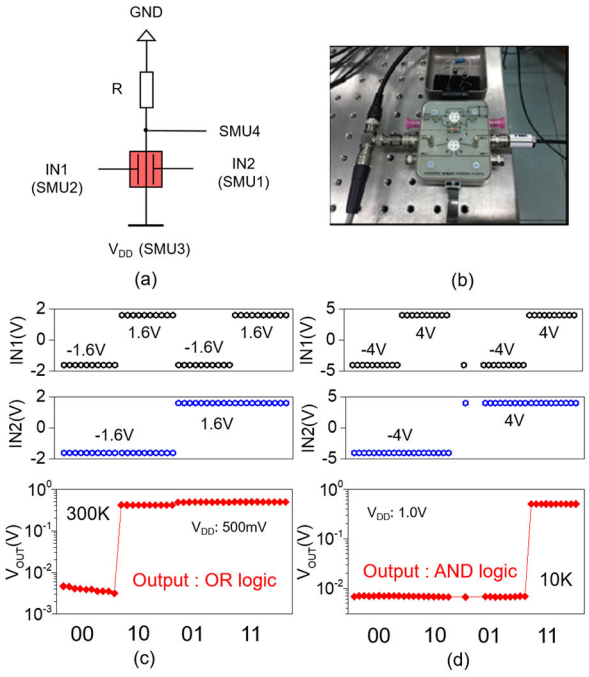

FIGURE 7. **Voltage-in voltage-out logic gate measurement configuration and results. (a) The schematic of measurement configuration. (b) The photography of the load resistor. Demonstration of the OR logic gate at 300 K (c) and the AND logic gate at 10K (d).**

of the WS_2 transistor at 300K and 10K. The logic function can be achieved properly at 300K (OR logic) and 10K (AND logic), respectively. We can use the output voltage swing to measure the ability of the logic level restoration. At 300 K, the output voltage swing is 489 mV with V_{DD} at 500 mV. It indicates the logic transistor has a good ability to drive the next stage logic gate at room temperature. Because of the low output current of the device at 10K, we apply the input voltage and drain-source voltage with a higher amplitude to obtain better results. The results show that a complete and cascadable voltage-in voltage-out logic gate can be achieved by our logic transistor and a load resistor. Because of the relatively high resistance of the WS_2 transistor and wiring loss, the output voltage has some loss.

5) RELIABILITY OF LOGIC TRANSISTORS

To evaluate the reproducibility and reliability of WS2 logic transistors, we have fabricated several batches of devices. Nearly all devices show the general trend from AND logic at low temperatures to OR logic at high temperatures. Figure 8 shows the reliability of the logic behavior (both AND logic at 10 K and OR logic at 300 K). The devices show stable logic behavior during the 100 periods logic function test.

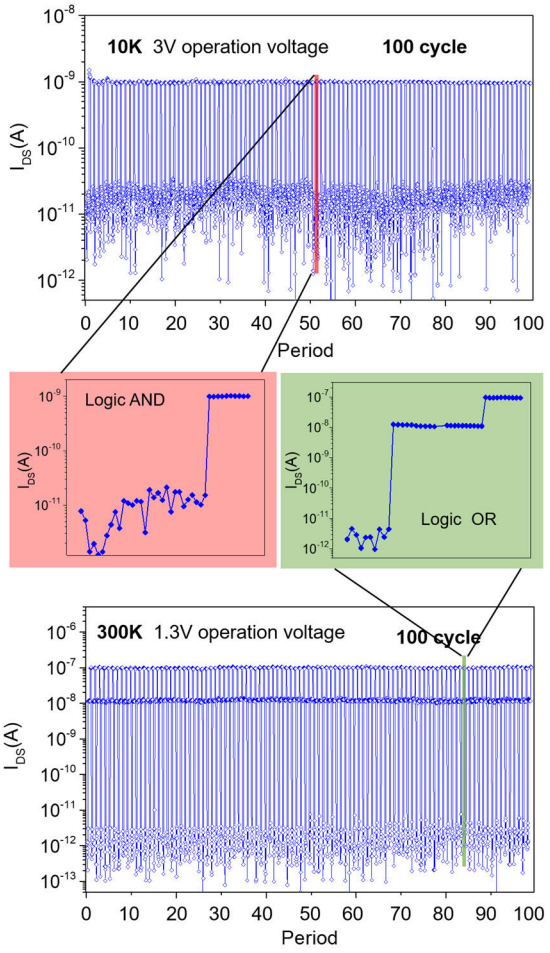

FIGURE 8. **Voltage-in voltage-out logic gate measurement configuration and results.**

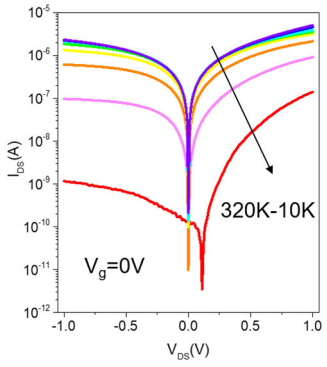

FIGURE 9. **Output characteristics of the WS_2 transistor with gate voltage fixed at 0V from 10K to 320K in logarithmic coordinate.**

6) ELECTRICAL PERFORMANCE OF LOGIC TRANSISTORS

Figure 9 shows the symmetrical output curves in the logarithmic coordinate, which indicates good ohmic contact between electrodes and the channel.

We extracted the subthreshold slope of WS_2 transistors from the transfer characteristics. Figure 10 shows the dependence of the subthreshold slope on temperature. At 10 K, the subthreshold slope is relatively large (220 mV/decade

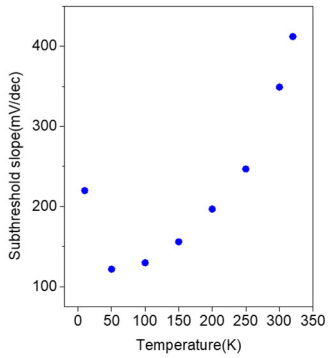

FIGURE 10. Dependence of subthreshold slope on temperature.

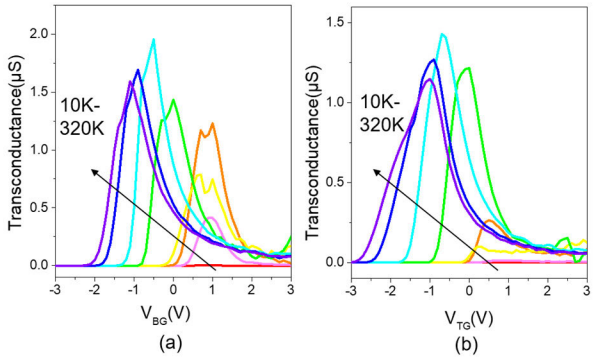

FIGURE 11. Dependence of transconductance of the WS_2 transistor on the gate voltage applied by the back gate (c) and the top gate (d) from 10K to 320K.

due to strong scattering. As temperature rises, the subthreshold slope monotonically increases with temperature, which is consistent with the conventional semiconductor theory. The subthreshold slope reaches the minimum value of 122 mV/decade at 50K.

Figure 11 (a) and (b) show the dependence of transconductance of the WS_2 transistor on the gate voltage applied by the back gate and the top gate, respectively. The transconductance reaches the maximum value of 1.96 μS (the back gate) and 1.43 μS (the top gate) at 250 K.

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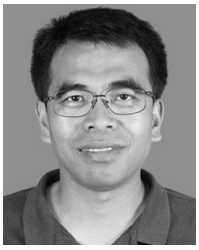

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