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Proposal of Global Strain Clocking Scheme for Majority Logic Gate

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ABSTRACT A stairs-type global strain clocking mechanism for nanomagnetic majority logic gate based on shape engineering of nanomagnets was designed in this paper. Reasonable size nanomagnets and proper strain clocking scheme ensure the computing architecture pipelined at room temperature. The optimal global strain clocking scheme was obtained by investigating the impact of magnetic layer thickness and width on clocking period and strain magnitude. Encouragingly, for the global strain clocking, information transmission speed of majority logic gate is increased 1-2 times as against the local strain clocking scheme due to decreasing the number of start-ups during information transmission. While the energy dissipated per clock cycle of the global strain clocking scheme consumes 3-4 times less energy than that of local strain clocking scheme. Moreover, global clocking is used to control a nanomagnetic logic device(NMLD), in which case single device consisted of many nanomagnets can be treated as single nanomagnet. However, magnetization switching is error-prone in the presence of thermal noise at room temperature. Therefore, the proper structure parameters of the device are obtained at room temperature, in which case the error probability of the majority logic gate is 0.5% in theoretical simulation. These results provide essential guidance for the design of energy-efficient multiferroic nanomagnetic logic devices.

INDEX TERMS Energy-efficient, global strain clocking, nanomagnetic logic device (NMLD), shape engineering, spintronics.

I. INTRODUCTION

With the dimensions of CMOS devices further scaling, the problems of quantum tunneling effect and power consumption have become stumbling block to improving integration [1]. Nanomagnetic logic device (NMLD) has become a applicable candidates to replace the traditional CMOS technology due to its nonvolatile storage, high density integration and ultra-low power dissipation [2], [3]. NMLD is composed of the elongated nanomagnets with uniaxial shape anisotropy, e.g. rectangle and ellipse nanomagnets [4], [5]. The binary information "0" (magnetization pointing down) and "1" (magnetization pointing up) are encoded in bistable magnetization state. Magnetization will be unstable (high energy state) while the magnetization along the short axis, which is defined as "NULL" [6], [7]. Therefore, Boolean logic can be performed by bistable elongated nanomagnets. In NMLD, unidirectional propagation of the data depends on dipole coupling effect between nanomagnets [8]. However, the dipole coupling effect is not enough to switch the magnetization of neighbouring nanomagnet due to the dipole–dipole interaction less than the shape anisotropy of the nanomagnet [9], [10]. In order to overcome the energy barrier between two steady magnetization states, we need an external energy apart from dipole-dipole interaction energy to hold the magnetization along short axis and drive the data transmission, which is termed as clocking [11]. In other words, the clocking is the heart in the design of NMLD.

The basic circuit of CMOS technology is phase inverter, while the basic circuit of NNLD technology is majority logic gate [12]–[15]. How to achieve high-speed lower energy consumption clocking scheme of majority logic gate are problems to be solved urgently now. Traditional clocking schemes of majority logic gate include current-induced magnetic field generated [16], spin-transfer torque [17] and spin orbit torque [18], [19]. Imre *et al*. successfully driven

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three-input majority logic gate in the experiment by using an external magnetic field clocking [20]. Crocker *et al*. constructed majority logic gates by using external driven nanomagnets and magnetic field clocking [21]. However, this method increases the layout area as well as the gate delay, and reduces the working frequency. Zhang *et al*. designed the majority logic gates that was composed of three trapezoid nanomagnets with different aspect ratios and two rectangular nanomagnets, which adopted bidirectional magnetic fields as clocking scheme [22], [23]. Although this method reduces the layout area and gate delay, the trapezoid nanomagnets is prone to form vortex state. Its output signal only depends on the direction of the magnetic field, which prevents signal transmission from input to output. Moreover, magnetic field clocking schemes have a problem not to be neglected, which is high energy dissipation. Cui *et al*. proposed an ultra-low-energy strain clocking schemes by generating a strain in a piezoelectric layer to accomplish electric field control magnetic anisotropy of magnetostrictive layer [24]. This method is based on the converse piezoelectric effect of piezoelectric materials and the inverse magnetostrictive effect of magnetostrictive materials. Wei *et al*. studied the local strain clocking scheme of majority logic gate, which realized pipelined logic operation [25]. Although the local strain clocking can greatly reduce the energy dissipation, it has lower operating frequency. In addition, the thermal fluctuation at the room temperature is prone to cause magnetization switching errors [26]. To overcome the thermal fluctuation, ramp local strain clocking scheme was applied in majority logic gate. This method achieves adiabatic magnetization switching, but linear ramping change of strain in the piezoelectric layer is so difficulty. Yilmaz *et al*. designed the strain clocking of majority logic gate that can realize effective nanopipelining, but the local strain clocking period is not less than 9 ns [27]. The global magnetic field clocking scheme proposed in [28] can improve the information transmission speed, but it has the disadvantage that propagating the logic bit is non-pipelined as well as error-prone.

In this paper, we designed a majority logic gate as well as a global strain clocking scheme based on the shape engineering of single domain ellipse nanomagnet, as shown in Fig.1. Firstly, to prove that it can perform logic computing correctly, the majority logic gate was simulated by using the object-oriented micro-magnetic framework (OOMMF). Secondly, the dynamic magnetization mathematical model of this majority logic gate at the room temperature was established. The optimal global strain clocking scheme was obtained by studying information propagation of this majority logic gate at the room temperature. Compared with the traditional clocking scheme, the global strain clocking consumes less energy to perform majority computing and significantly improves the operation frequency of the majority logic gate. These results have important guiding significance to the development of nanomagnetic logic circuits based on shape engineering.

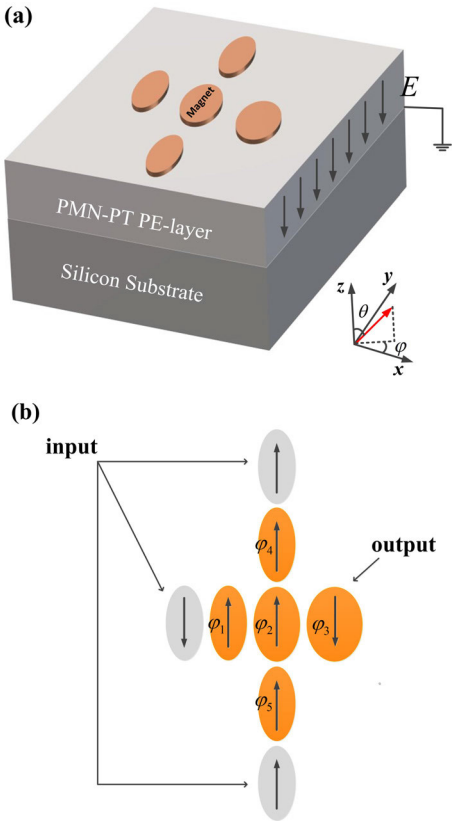

FIGURE 1. **(a) Schematic of strain-driven majority logic gate device. *E* is electric field. The red arrow display the direction of magnetization, θ is the polar angle (out-of-plane) and φ is the azimuth angle (in-plane). (b) The top view of majority logic gate, and the nanomagnets were numbered.**

II. MODELING OF MAJORITY LOGIC GATE IN THE PRESENCE OF THERMAL NOISE

Fig. 1(a) presents a potential implementation of majority logic gate controlled by global strain clocking. Three-layer structure is based on the strain clocking structure proposed by D'Souza *et al* [29]. A spatial coordinate system was established, where the x-axis parallel to the short axis of the nanomagnet and the y-axis parallel to the long axis of the nanomagnet. We select Terfenol-D as the magnetic layer (thickness *th*), whose damping coefficient α is set as 0.1 [5]. The magnetic material has a saturation magnetization Ms of 8×10^5 A/m [30]. we select PMN-PT (Pb(Mg1/3Nb2/3)O3-PbTiO3) as the piezoelectric layer material (thickness $t_{\mathrm{p}} = 450$ nm), because it has the higher piezoelectric coefficient. The piezoelectric layer can be construct on silicon-substrate. The Fig.1(b) shows the top view of majority logic gates comprised three type A nanomagnets(120nm×60nm× *th*), one type B nanomagnet(120nm×75nm× *th*), and one type C nanomagnet (120nm×90nm×*th*). The distance between two adjacent centre of nanomagnets is $d = 290$nm. The evolution of the magnetic moment vector $\boldsymbol{M}$ of single nanomagnet can be described by the Landau-Lifshitz-Gilbert equation [31].

$$\frac{\mathrm{d}\vec{M}}{\mathrm{d}t} = -\gamma\vec{M} \times \vec{H}_{\mathrm{eff}} - \frac{\alpha\gamma}{M_S}[\vec{M} \times \left(\vec{M} \times \vec{H}_{\mathrm{eff}}\right)] \qquad (1)$$

where α is the damping coefficient, M_s is the saturation magnetization, γ is the gyromagnetic ratio, and $\boldsymbol{H}_{\mathbf{eff}}$ is the effective field [32]:

$$\vec{H}_{\text{eff}} = -\frac{1}{\mu_0 V}\frac{\mathrm{d}E_{\text{total}}}{\mathrm{d}\vec{M}} \tag{2}$$

where $\mu_0 = 4\pi \times 10^{-7}$ is the vacuum permeability and V is the volume of single nanomagnet. The total energy E_{total} includes dipole coupling energy, shape anisotropy energy, stress anisotropy energy and thermal fluctuations [33]:

$$\begin{aligned} E_{\text{total}} = {} & E_{\text{dipole-total}} + E_{\text{shape-anisotropy}} \\ & + E_{\text{stress-anisotropy}} + E_{\text{thermal fluctuations}} \end{aligned} \tag{3}$$

Two adjacent nanomagnet in this device (the ith and jth nanomagnet), whose magnetizations have polar and azimuthal angles of θ_{i}, φ_{i} and θ_{j}, φ_{j}. The dipole–dipole interaction energy $E_{\text{dipole-total}}$ include horizontal coupling [34] and vertical coupling [35]:

$$E_{\text{dipole-total}} = E_{\text{dipole-horizontal}} + E_{\text{dipole-vertical}} \tag{4}$$

$$\begin{aligned} E_{\text{dipole-horizontal}} = {} & \frac{\mu_0 M_S^2 V^2}{4\pi R^3}\sum_{j-1}^{j+1}[-2\sin\theta_{\text{i,j}}\cos\varphi_{\text{i,j}}\sin\theta_{\text{i,k}}\cos\varphi_{\text{i,k}} \\ & + \sin\theta_{\text{i,j}}\sin\varphi_{\text{i,j}}\sin\theta_{\text{i,k}}\sin\varphi_{\text{i,k}} \\ & + \cos\theta_{\text{i,j}}\cos\theta_{\text{i,k}}] \quad (\text{k} \neq \text{j}) \end{aligned} \tag{5}$$

$$\begin{aligned} E_{\text{dipole-verticall}} = {} & \frac{\mu_0 M_S^2 V^2}{4\pi R^3}\sum_{i-1}^{i+1}[\sin\theta_{\text{i,j}}\cos\varphi_{\text{i,j}}\sin\theta_{\text{k,j}}\cos\varphi_{\text{k,j}} \\ & - 2\sin\theta_{\text{i,j}}\sin\varphi_{\text{i,j}}\sin\theta_{\text{k,j}}\sin\varphi_{\text{k,j}} \\ & + \cos\theta_{\text{i,j}}\cos\theta_{\text{k,j}}] \quad (\text{k} \neq \text{i}) \end{aligned} \tag{6}$$

The shape anisotropic energy of a nanomagnet is [36]:

$$\begin{aligned} E_{\text{shape-anisotropy}} = {} & \frac{\mu_0 M_S^2 V}{2}[N_{\text{dx}}(\cos\theta\sin\varphi)^2 \\ & + N_{\text{dy}}(\sin\theta\sin\varphi)^2 + N_{\text{dz}}(\cos\varphi)^2] \end{aligned} \tag{7}$$

where N_{dx}, N_{dy}, and N_{dz} are the demagnetization factors of elliptical nanomagnets, they can be calculated through [37]:

$$N_{\text{dx}} = \frac{\pi}{4}(\frac{th}{a})[1 + \frac{5}{4}(\frac{a-b}{a}) + \frac{21}{16}(\frac{a-b}{a})^2] \tag{8}$$

$$N_{\text{dy}} = \frac{\pi}{4}(\frac{th}{a})[1 - \frac{1}{4}(\frac{a-b}{a}) - \frac{3}{16}(\frac{a-b}{a})^2] \tag{9}$$

$$N_{\text{dy}} = 1\text{-}\frac{\pi}{4}(\frac{th}{a})[2 + (\frac{a-b}{a}) + \frac{18}{16}(\frac{a-b}{a})^2] \tag{10}$$

where a is the length of the long axis(length of nanomagnet), b is the length of the short axis(width of nanomagnet), and th is the thickness of the nanomagnet.

The stress anisotropy energy is given by [34]:

$$E_{\text{stress-anisotropy}} = -\frac{3}{2}\lambda_{\text{s}}\sigma V \sin^2\theta \sin^2\varphi \tag{11}$$

where (3/2) λ_s is the saturation magnetostriction and σ is the stress applied in magnetic layer. The relationship between applied voltage U and the stress σ is [30]

$$\sigma = \frac{Y(d_{31} - d_{32})U}{t_{\text{p}}(1+\nu)} \tag{12}$$

where $Y = 200$GPa is the Young's modulus and $\nu = 0.3$ is the Poisson's ratio. The dielectric constant of PMN-PT layer is 1000, $d_{31} = -3000$ pm/V and $d_{32} = 1000$ pm/V [38].

The field h(t) is related to thermal fluctuation energy $E_{\text{thermal-fluctuations}}$, which can be described by a Langevin random field [39]:

$$h(t) = \sqrt{\frac{2\alpha kTf}{\gamma\mu_0 M_S V}}G_{(0,1)}(t) \tag{13}$$

where $k = 1.38\times10^{-23}$ J/K is the Boltzmann constant, $T = 300$ K is the room temperature, $f = 1$ THz is the frequency of thermal noise oscillations, and $G_{(0,1)}(t)$ is the standard Gaussian distribution random vector. By plugging (3)–(10) in (2), the components of the effective field at room temperature can be obtained:

$$\begin{aligned} h_{\text{x}} = {} & -\frac{1}{\mu_0 M_S V}\frac{\partial E_{\text{dipole-total}}}{\partial\sin\varphi\cos\theta} - M_S N_{\text{dx}}\cos\theta\sin\varphi \\ & + \sqrt{\frac{2\alpha kTf}{\gamma\mu_0 M_S V}}G_{(0,1)}(t) \end{aligned} \tag{14}$$

$$\begin{aligned} h_{\text{y}} = {} & -\frac{1}{\mu_0 M_S V}\frac{\partial E_{\text{dipole-total}}}{\partial\sin\varphi\sin\theta} - M_S N_{\text{dy}}\sin\theta\sin\varphi \\ & + \frac{3\lambda_{\text{s}}\sigma}{\mu_0 M_S}\sin\theta\sin\varphi + \sqrt{\frac{2\alpha kTf}{\gamma\mu_0 M_S V}}G_{(0,1)}(t) \end{aligned} \tag{15}$$

$$\begin{aligned} h_{\text{z}} = {} & -\frac{1}{\mu_0 M_S V}\frac{\partial E_{\text{dipole-total}}}{\partial\cos\theta} - M_S N_{\text{dz}}\cos\theta \\ & + \sqrt{\frac{2\alpha kTf}{\gamma\mu_0 M_S V}}G_{(0,1)}(t). \end{aligned} \tag{16}$$

III. RESULTS AND DISCUSSIONS

A. STRAIN-INDUCED MAGNETIZATION SWITCHING:SIZE-DEPENDENT

The strain-mediated magnetization switching dissipates less energy, but the incoherent switching of strain-mediated nanomagnets results in information errors. The nanomagnet that has reached a vortex state will remain in this state even after the strain is removed. The incoherent switching is depending on the size of nanomagnet. Therefore, selecting reasonable size nanomagnets is necessary for us to design the strain-mediated NMLD. To obtain the appropriate size range, extensive three-dimensional micromagnetic simulations were performed by using OOMMF with the following parameters: exchange constant A=9pJ/m.

Simulation results indicated that both the thickness and the width of nanomagnet have a significant impact on the incoherent switching, as displayed in Fig. 2. For the nanomagnet with the 60-90 nm width, the incoherent magnetization switching occurs when the thickness is 21 nm or more, and voltage-driven 90° magnetization switching is achieved when the thickness is 9 −15 nm. At the same aspect ratio, the larger the thickness of nanomagnet, magnetization is the more prone to occur incoherent switching [40]. Therefore, we should choose the nanomagnet as thin as possible.

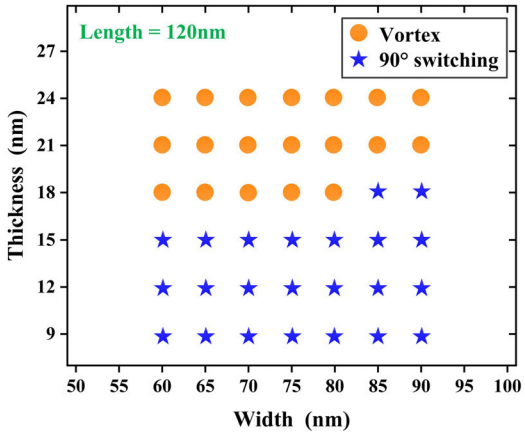

FIGURE 2. Nanomagnets thickness-width phase diagram showing the range of successful strain-mediated 90°magnetization switching.

However, the magnetization is prone to deviate from the in-plane due to the perpendicular magnetic anisotropy when the thickness is too small [41]. Therefore, the authors selected the nanomagnet is 120nm length, 9-15nm thickness, and 60-90nm width.

These results can be used to help us choice appropriate size nanomagnets in the design of NMDL. According to the reasonable size given in Fig. 3, we select type-A nanomagnet (120nm×60nm×*th*), type-B nanomagnet (120nm×75nm×*th*) and type-C nanomagnet (120nm×90nm×*th*) as the basic cells of a device. In order to acquire the critical stress value needed for achieving 90° magnetization switching (namely the coercive field), the normalized hysteresis loops of three kind of nanomagnets are obtained by micromagnetic simulation, as shown in Fig. 3.

It can be observed from Fig.3 that the larger aspect ratio (length/width) leads to the larger coercive field at the same thickness. On the other hand, the larger the coercive field, the larger the stresses required for implementing 90° magnetization switching. While the coercive field also increase with the thickness at the same aspect ratio. Based on the results obtained above, we designed a stairs-type global strain clocking scheme of majority logic gate, as shown in Fig. 4. *Stress A, Stress B*, and *Stress C* are the stress value needed for achieving 90° magnetization switching of type-A, type-B, and type-C nanomagnets, respectively. The global clocking method not only makes the computing architecture pipelined but also has a higher operating frequency and less energy dissipation than traditional local strain clocking. Additionally, compared with the global clock, the disadvantage of the local clock is that it requires individual access to each nanomagnet.

B. OOMMF SIMULATION RESULTS

The authors use OOMMF software to study the information propagation in majority logic gates. The specific parameters of the majority logic gate have been given in the previous sections. The OOMMF software cannot directly set terms for

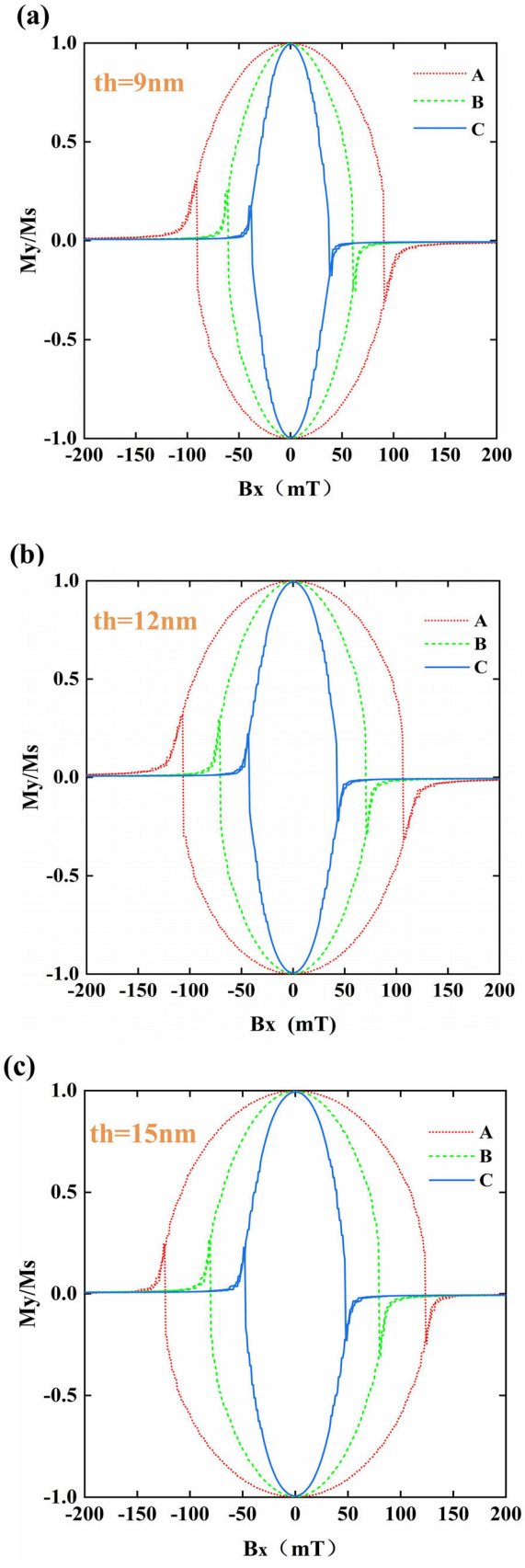

FIGURE 3. Hysteresis loops of type-A, type-B, and type-C nanomagnets with different thickness (a) 9 nm, (b) 12 nm, (c) 15 nm, respectively.

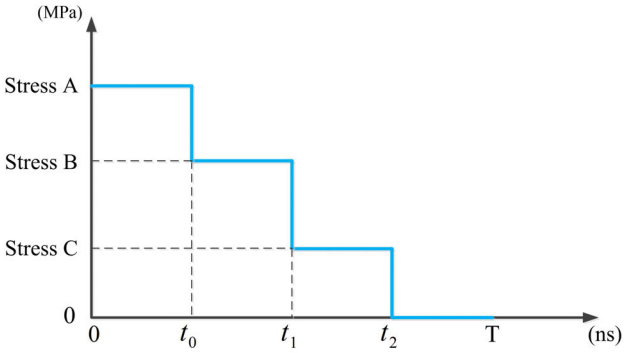

FIGURE 4. The stairs-type global strain clocking scheme of majority logic gate. *Stress A*, *Stress B* and *Stress C* are the stress value needed for achieving 90° magnetization switching of type-A, type-B and type-C nanomagnets, respectively. T is the clocking period.

stress anisotropy field, we use a uniaxial magnetocrystalline anisotropy field to replace it due to the magnetocrystalline anisotropy of the polycrystalline magnetostrictive material can be ignored [42]. Results show that the majority logic gates with different thickness (*th*=9nm, 12nm, 15nm) all can successfully realize the majority calculation. Take the 12nm thick majority logic gate as an example: the input of the majority logic gate is "111". The stresses of the global strain clocking used in the simulation are *Stress A* = 55MPa, *Stress B* = 32MPa and *Stress C* = 22MPa. The majority logic gates is given an initial steady-state of "11011". Fig.5.(b) shows the magnetization process of majority logic gate, which has four stages. The first stage (t < 0.4ns), *Stress A* is applied to all nanomagnets. The total nanomagnets will be in "Null" state at the same time, and waiting for further operation. This is because the stress anisotropy energy can overcome the dipole–dipole interaction energy and shape anisotropy energy at this time. The second stage (0.4ns< t <0.8ns), *Stress B* is applied to all nanomagnets. At this time, the dipole–dipole interaction energy from the input nanomagnets makes the magnetizations of no.1, no.4 and no.5 nanomagnets rotate to long axis. The *Stress B* can't prevent the magnetization switching of the no.1, no.4 and no.5 nanomagnets (type-A), because the summation of shape anisotropy energy and dipole–dipole interaction energy is so high that stress anisotropy energy cannot counteract it. Meanwhile, no.2 nanomagnet and output nanomagnet (no.3) remain "Null" state. The third stage (0.8ns< t <1.2ns), the *Stress C* is applied to all nanomagnets. At this time, the no.2 nanomagnet performs majority operation, the dipole–dipole interaction energy nudges the magnetization to the final steady state successfully. Output nanomagnet is "Null" state. The fourth stage, the stress reduction to zero. The magnetization of output nanomagnet is downward, which represents a logic "0". The time that the majority logic gate realizes one-time computing is equal to the clocking period.

The energy curves of the majority logic gate also prove the correctness of the magnetization process mentioned above,

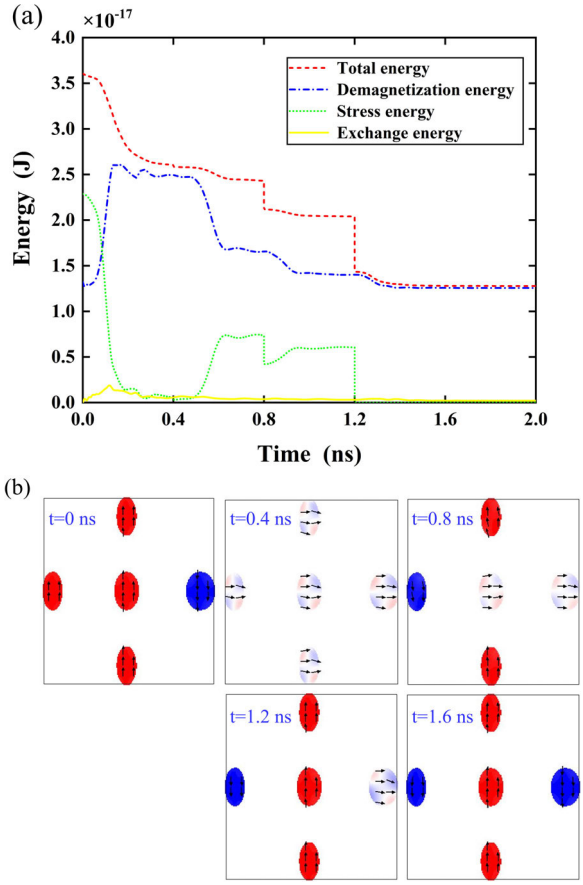

FIGURE 5. Micromagnetic simulation results of majority logic gate. (a) Various energies curves with time.(b) Magnetization processes image of the majority logic gate when input "111".

as shown in Fig.5(a). The first stage, the demagnetization energy increases to maximum and stress anisotropy energy gradually decreases to 0, which validate magnetization along the short axis. This process can be named the start-up process of the nanomagnet. The stress anisotropy energy increases and the demagnetization energy decreases in the second stage, which is consistent with the variation trend of energy when the in-plane magnetization switches from short axis to long axis. The stress anisotropy energy gradually increases when the magnetization of the no. 2 nanomagnet from the short axis rotate to the long axis (0.8ns < t < 1.2ns). The fourth stage, the total energy of the majority logic gate reaches the minimum, and majority calculation is completed.

We need to obtain a reasonable stairs-type global strain clocking, which can correctly drive majority logic gate. Therefore, we study the interconnection lines by using this global strain clocking before designing a majority logic gate. The incorrect signal transmission while investigating the stair-type strain clocking scheme attracted the author's attention. This shows that the size difference between two adjacent nanomagnets (actually the stress difference required between two adjacent nanomagnets) has an important influence on the design of majority logic gates. We replaced

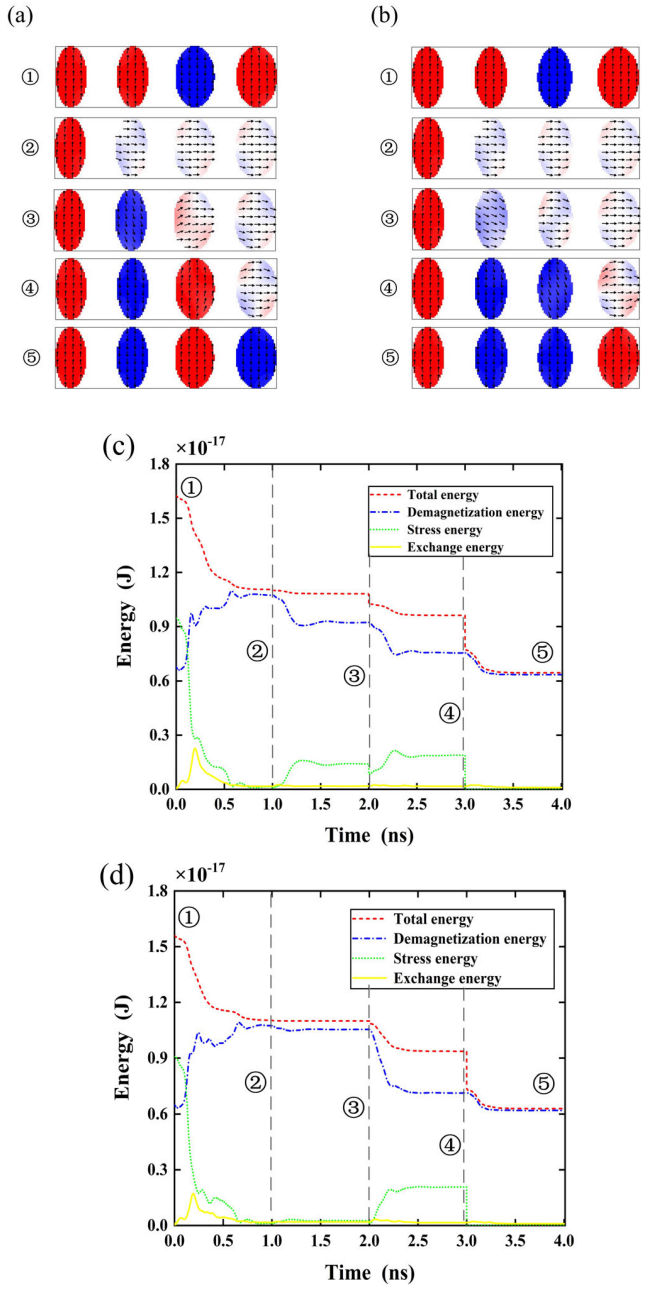

FIGURE 6. (a) The magnetization process and (c) energy curve of nanomagnets chain when signal is transmitted correctly. (b) The magnetization process and (d) energy curve of nanomagnets chain when signal is transmitted incorrectly.

the 120nm×75nm×12nm nanomagnet in Fig.6 (a) with a 120nm×65nm×12nm nanomagnet, as shown in Fig.6 (b). At this time, *Stress B* = 50MPa makes magnetization of the third nanomagnet in Fig.6 (b) rotate 90°. We found that the second nanomagnet did not successfully rotate to downward (logic "0"), as shown in Fig.6(b) ③, which led to the wrong signal transmission in Fig.6(b) ④. In order to show the physical essence clearly, we study the interactions between the stress anisotropy energy and demagnetization energy, as shown in Fig.6 (c) and Fig.6 (d). When the signal propagates correctly in nanomagnet array, the energy curves as shown in Fig.6(c).

When the signal propagates incorrectly in nanomagnet array, the energy curves as shown in Fig.6(d). Comparing the ③ in Fig.6 (c) and ③ in Fig.6 (d), it can be found that the stress anisotropy energy of the ③ in Fig.6 (c) is significantly increased and the demagnetization energy is significantly reduced when achieving the 90° magnetization switching. However, there was no significant change in stress anisotropy energy and demagnetization energy in ③ of Fig.6 (d). The dipole–dipole interaction cannot overcome the stress anisotropy at this time, which leads to the slight magnetization switching. Therefore, there is a critical width difference of two adjacent nanomagnets, as shown in Fig.7. Only the widths difference is higher than the critical value, and the signal can be transmitted correctly. The calculation results of the mathematical model at the room temperature is shown by a blue line, and the green line shows the simulation results of OOMMF software. The stairs-type global strain clocking scheme was verified by these micromagnetic simulations in this section. However, NMLD is extremely error-prone in the presence of thermal noise, so it is necessary to discuss the computing operating of majority logic gate at room temperature.

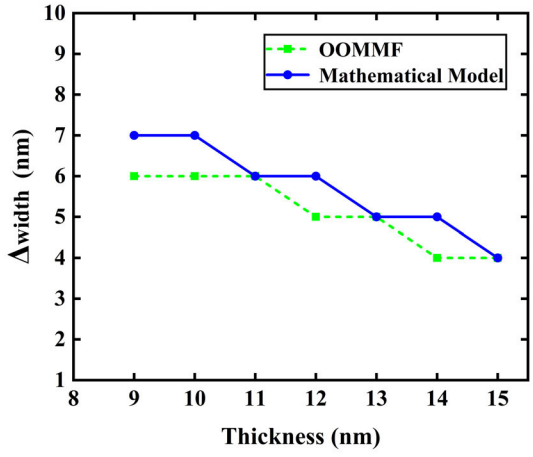

FIGURE 7. The critical width difference of two adjacent nanomagnets. The width difference of two adjacent nanomagnets greater than critical value, in which case the signal can be correctly transmitted.

C. SIMULATION RESULTS AT THE ROOM TEMPERATURE

In this section, we used the mathematical model in chapter 2 to investigated magnetization process of the majority logic gate at room temperature. Table.1 shows the Stress magnitude and minimum clocking periods of global clocking scheme for simulation at a different thickness. To dissipate lower energy, the stresses used in the simulation is the critical stress of type-A, type-B, and type-C nanomagnets, respectively. Results present that the minimum clock period T=1.9ns when the thickness is 12 nm at the same conditions. The in-plane magnetizations dynamic of majority logic gate (*th*=12nm)

TABLE 1. Stress magnitude and clocking period at the room temperature.

Thickness (nm)	Stress (MPa)			Time (ns)			
	A	B	C	t_0	t_1	t_2	T
9	48	25	18	0.8	1.3	1.8	2.2
12	55	32	22	0.7	1.1	1.5	1.9
15	60	38	28	0.9	1.4	1.9	2.4

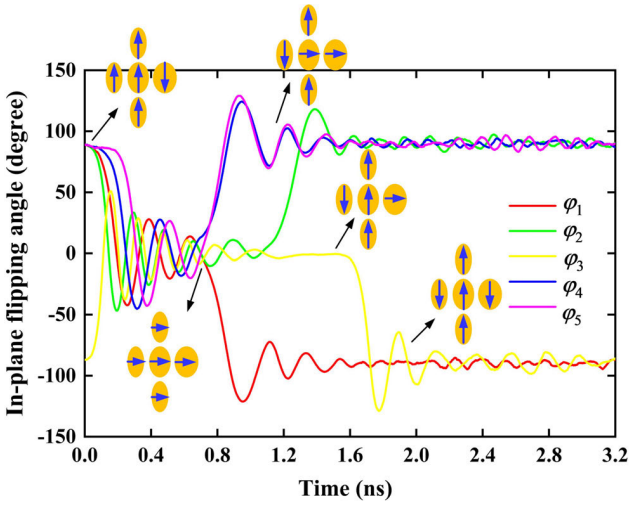

FIGURE 8. Magnetization azimuth angle φ versus time plotted for the five nanomagnets in the majority logic gate of Fig.1 at room temperature. *Stress A*, *Stress B* and *Stress C* are applied abruptly on the five nanomagnets at $t = 0.7$ns, $t = 1.1$ns and $t = 1.5$ ns, respectively.

are calculated by MATLAB software, as shown in Fig.8. The initial state of majority logic gate is "11011," and the input is "111". The majority logic gate has a final steady-state with logic "01011" after the global strain clocking is applied, which successfully performs the majority calculation at room temperature. The other seven inputs were also simulated, and correct outputs corresponding to these inputs were successfully obtained.

The operation cycle of this majority logic gate is 1.9 ns, which is nearly 1-2 times faster than the local strain clocking scheme of majority logic gate due to the local strain clocking only operated single nanomagnet each time. This is because the stairs-type global strain clocking scheme dramatically reduces the start-up time. Nanomagnets need start-up time to kick the magnetization out of the stagnation state before it can be switched. This start-up time significantly reduces the operating frequency of the NMLD. Start-up time (the first stage) is about 1-2 times higher than the magnetization switching time (other stages), as can be seen from Fig. 5 (a) and Fig.8. After the *Stress A* is applied, the start-up time required to rotated magnetization from long axis to short axis is 0.7ns. However, the time required for the magnetization switching from the short axis to the long axis is 0.3-0.4ns after the stress is removed. The stairs-type global strain clocking scheme only needs one-time start-up instead of multiple times. Nanomagnets no longer needs to be restarted during information transmission and only requiring magnetization switching time to complete the information pipelining transmission. To obtain the error probability in the presence of thermal noise, we performed 1000 simulations (macro-spin model) with fixed input and counted the number of correct output. Results show that the error probability of the majority logic gate is 0.5%, which is approximately consistent with what predecessors did [43], [44]. For a single majority logic gate, reliable computation is possible only if the error probability is less than 0.0073 [45]. Therefore, a reliable calculation of the majority logic gate we designed is possible in theory.

The energy dissipation of single nanomagnet in turn-on phase of the clocking is $(1/2)CU^2$, where C is the capacitance of the PMN-PT PE-layer and $U = E \cdot t_p$ is the voltage applied in the PMN-PT PE-layer [46]. The total energy dissipation of single nanomagnet is CU^2 in a clock period due to each clock period includes turn-on phase and turn-off phase. Therefore, the energy dissipation per clocking period $E_{\text{local-dissipation}}$ when applying a local strain clocking to a majority logic gate is $3CU_A^2 + CU_B^2 + CU_C^2$. However, the energy dissipation of the global strain clocking is $E_{\text{global-dissipation}} = CU_A^2$ due to the global strain clocking only includes one-time turn-on phase and turn-off phase. The U_A, U_B and U_C are the voltages applied to generate the *Stress A*, *Stress B* and *Stress C*, respectively. So this stair-type global strain clocking needs less energy dissipation than local strain clocking to perform majority calculation.

IV. CONCLUSION

In summary, we proposed an ultra-low-energy global strain clocking scheme and a high operation frequency majority logic gate based on shape engineering of nanomagnets. To demonstrate this computing architecture, OOMMF software is applied to simulate. Micromagnetic simulation results show that this device and clocking scheme are achievable when nanomagnets have reasonable sized (length is120nm, width is 60-90nm, thickness is 9-15nm). However, the error switching will appear in signal transmission if the width difference between two adjacent nanomagnets is too small. We obtained the critical width difference (at least Δ width>4nm), the signal can be propagated correctly from input to output when the width difference is larger than critical value. An optimal global strain clocking scheme was obtained by formulating and solving the appropriate Landau-Lifshitz-Gilbert equations in the presence of thermal fluctuations. For the stairs-type global strain clocking scheme, the energy dissipated per clock cycle is one-third of that of the local strain clocking scheme, while the computing efficiency is 1-2 times higher than that of the local strain clocking scheme due to reducing the start-up time during information transmission. The error probability of the majority logic gate is 0.5% in theoretical simulation. Additionally, the stairs-type global strain clocking is a consecutive voltage pulse,

which is more feasible than the ramping voltage of the local strain clocking in fabrication. These results provide essential design guidelines for spintronic devices.

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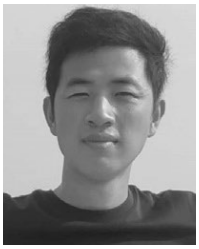

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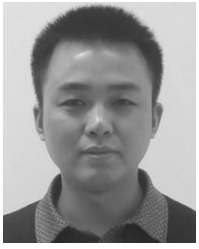

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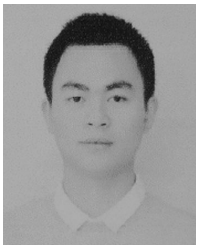

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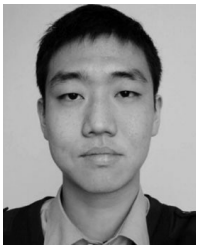

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