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A Full X-Band Phased-Array Transmit/Receive Module Chip in 65-nm CMOS Technology

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ABSTRACT In this paper, we present a phased-array transceiver chip operating in full X-band (8-12 GHz) in 65-nm CMOS technology. The presented transceiver for the transmit/receive module (TRM) consists of a 6-bit passive phase shifter, a 6-bit attenuator, a bi-directional gain amplifier (BDGA), and a single pole double throw (SPDT) switch connected to the internal power amplifier (PA) and the low-noise amplifier (LNA) to serve as a duplexer. A 64-bit SPI scan-chain is integrated for digital TRM control. The transmitter achieves greater than 15 dB of power gain with 11.84 dBm at the output 1-dB compression point (OP1dB). To achieve a wideband operation of the passive phase shifter, we assigned two different resonant frequencies for the phase leading and lagging networks and aligned the slopes of their phase responses to have the desired phase shifts at the center frequency. The RMS phase error is less than 5°, and the RMS amplitude error is less than 0.45 dB for all phase and attenuation states within 8-12 GHz while dissipating 216 mW dc power from a 1 V power supply. The receiver shows greater than 15 dB of power gain and has a noise figure (NF) of less than 8.4 dB for the entire X-band. The RMS phase error and the RMS amplitude error are less than 5° and 0.45 dB, respectively, for all control states within 8-12 GHz. The receiver consumes 110 mW with a 1 V power supply. The transceiver chip occupies an area of 4×1.88 mm^2.

INDEX TERMS CMOS, phased arrays, phase shifter, transceivers, wideband.

I. INTRODUCTION

Active phased-array antenna (APAA) systems have been extensively spotlighted in areas such as satellite communications, wireless communications, and radar applications owing to their increased channel capacity, reduced transmit power requirement, improved signal-to-noise ratio, and immunity to strong interference.

Until recently, phased array systems have been used primarily in defense and space applications since an electrically scanned APAA can support much faster beam scanning in a more compact volume than a mechanically scanned antenna. The traditional phased-array antenna system in defense and space applications has employed an expensive transmit/receive module (TRM) assembled with high-cost and bulky III-V MMICs [1], [2] combined with a silicon-based baseband and digital control chip to achieve high performance.

Since hundreds or even thousands of TRMs can be incorporated in a phased array antenna system, depending on the application, it is essential that the TRM be compact, be low-cost, and have a low-power design without compromising its performance. Therefore, enormous amounts of research have been directed at silicon-based (SiGe BiCMOS or CMOS) fully integrated transceiver for the TRM in X-band APAA systems to resolve this challenging issue [3]–[16]. A successful design solution in conventional digital CMOS technology must address power consumption and production cost.

An all-RF phase shifting architecture (phase-shifting performed at RF frequencies) is usually used to construct typical APAA systems. Compared to an architecture that uses local oscillator (LO) or IF phase-shifting methods, an

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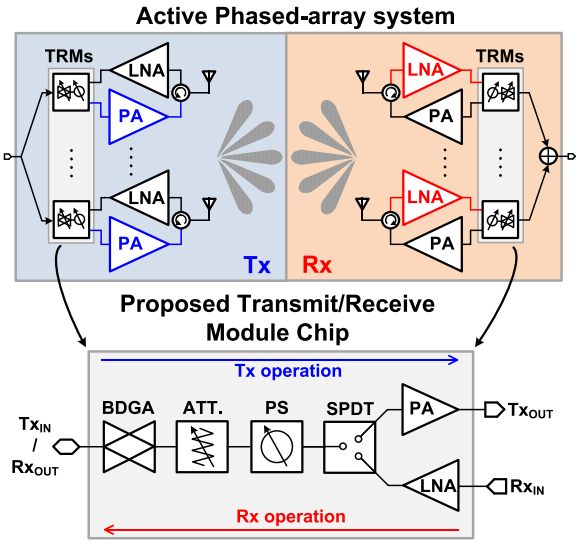


FIGURE 1. Block diagrams of the active phase-array system and proposed transceiver configuration.

all-RF phased array architecture has excellent suppression of interference [5] with better linearity at the system level. It is a simple system with relatively low power consumption as it requires only a single high-performance receiver in the sum port, as illustrated in Fig. 1.

The RF phase shifter is a crucial element in phase array systems [17]. Therefore, in designing a TRM, its phase-shifting capability should be agile enough to steer the main lobe of the array antenna precisely, and its bandwidth should be wide enough to support various applications. In the design of wide-band phase shifters with high linearity and low power consumption in CMOS, the use of phase shifter topology configured with a high-pass (HP) / low-pass (LP) passive network has been widespread because it has negligible power dissipation, a simple control mechanism, and less reliance on the RF performance of the active device [18], [19]. However, the HP/LP phase shifter only satisfies the desired phase shift with an acceptable port impedance match over a narrow frequency range. Thus, the inherent broadband characteristics of this type of phase shifter have not been efficiently deployed. Also, the conventional iterative design approach takes more time to achieve the required bandwidth and phase error.

In this paper, we present a fully integrated TRM chip operating in full X-band (8 – 12 GHz) in 65-nm CMOS technology. Compared with the previous work [15], the proposed TRM chip is designed to cover the full X-band by designing a broadband phase shifter, and a high-performance power amplifier is designed in the Tx path to achieve output power higher than 11 dBm. The implemented transceiver achieves an RMS phase error of less than 5°, and an RMS attenuation error of less than 0.45 dB with linearity and noise performance comparable to the recently reported SiGe transceiver [3]–[10] and III-V TRM MMICs [1], [2], and with much lower power consumption.

In order to improve the operating frequency range of the passive phase shifter, we misaligned the resonant frequency of the HP/LP network from the center frequency using derived formulae. With this approach, more than 50 % of the operating range under 5° of RMS phase error was enhanced. A detailed analysis with derived design equations is presented in Section II.

A block diagram of the proposed X-band TRM chip is illustrated in Fig. 1. In comparison with [7], [8], the proposed TRM chip utilizes not only a single SPDT (three SPDT switches in [7]), but also shared phase shifter and attenuator (separate phase shifters and attenuators for Tx and Rx path [8]) by employing a bi-directional gain amplifier (BDGA) in Tx and Rx operations. Therefore, the proposed architecture has the advantage of reducing path loss and chip occupancy. Moreover, a wideband operation of the passive phase shifter could be achieved by assigning two separate resonant frequencies for the leading/lagging networks for the phase-shifting units where we controlled the slopes of their phase responses to meet the desired phase shifts at the center frequency.

Since the output power and the noise figure of the bi-directional transceiver with two-ports [13], [15] was limited by the performance of the BDGA, we implement a TRM chip with an SPDT switch to add PA and LNA separately. Also, the SPDT switch was used as a duplexer to select the Rx/Tx signal for bi-directional operation. The Rx path of the SPDT switch is connected to the output of the LNA from the Rx input, while the Tx path is connected to the PA for improved Tx output power. The TRM chip was fabricated in 65-nm CMOS technology with eight copper metal layers and one aluminum metal layer, and the top layer (3 μm) was used for passive component design.

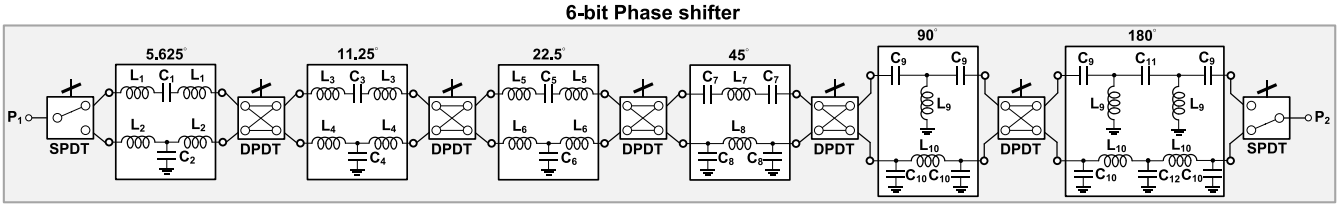
This paper is structured as follows: Section II describes the detailed designs for the core blocks including the phase shifter, attenuator, switches, and amplifiers for wideband operation. The measurements of the chip are presented in Section III, followed by the conclusion in Section IV.

II. X-BAND TRANSCEIVER DESIGN

A. 6-BIT BROADBAND PASSIVE PHASE SHIFTER

The typical structure of an HP/band-pass(BP)/LP phase-shifting cell includes third-order T-type HP filters, L-C-L BP filters, C-L-C BP filters and π-type LP filters as shown in Fig. 2 to minimize the number of inductors required. In comparison with [13], [15], we designed a 5.625° phase shift cell with BP and LP networks instead of switch to significantly enhance the operating frequency range. Inductors usually consume most of the chip area. The element values of each HP and LP network can be determined from its resonant frequency and the insertion phase at a given frequency by assuming that the network is well matched at its input and output ports (i.e., $|\angle S_{21}| = \phi$ and $S_{11} = S_{22} = 0$). The element values of the networks can be calculated as follows [20]:

$$L_1 = \frac{Z_0}{2\pi f_1 \sin(\phi_1)}; \tag{1}$$



Device parameters

L_1	L_2	C_1	C_2	L_3	L_4	C_3	C_4	L_5	L_6	C_5	C_6	L_7	L_8	C_7	C_8	L_9	L_{10}	C_9	C_{10}	C_{11}	C_{12}
170 pH	100 pH	3 pF	80 fF	160 pH	120 pH	1.6 pF	95 fF	210 pH	180 pH	750 fF	135 fF	650 pH	515 pH	800 fF	145 fF	1.25 nH	510 pH	700 fF	145 fF	350 fF	290 fF

FIGURE 2. Schematic and all device parameters of the proposed X-band 6-bit passive phase shifter using HP/BP/LP networks.

$$C_1 = \frac{1}{2\pi f_1 Z_0 \tan(\phi_1/2)} \tag{2}$$

$$L_2 = -\frac{Z_0 \sin(\phi_2/2)}{2\pi f_2}; \tag{3}$$

$$C_2 = -\frac{\tan(\phi_2/2)}{2\pi f_2 Z_0}, \tag{4}$$

where ϕ_1 and ϕ_2 are insertion phases of HP and LP networks at their resonant frequencies f_1 and f_2, respectively. In conventional design methodology, HP and LP networks are considered to resonate at the same frequency, that is, the center frequency of operation f_0. It is also assumed that each network has half of the expected insertion phase shift but with opposite signs at f_0. Each circuit element is calculated from (1) – (4) by setting $f_1 = f_2 = f_0$ and $\phi_1 = -\phi_2 = \Delta\phi_0/2$.

However, this simplification undesirably limits the design space, which prohibits the network from operating at wideband. Thus, we eliminate this simplification in our work to significantly improve the phase error performance over the frequency band of interest. The phase responses of HP and LP networks, ϕ_{HPN} and ϕ_{LPN}, as a function of frequency f are presented in (5) and (6), respectively.

$$\phi_{HPN}(f) = \tan^{-1}\left[\frac{f_1}{f}\tan\left(\frac{\phi_1}{2}\right)\frac{1+\cos^2(\phi_1/2)-(f_1/f)^2\sin^2(\phi_1/2)}{1-2(f_1/f)^2\sin^2(\phi_1/2)}\right], \tag{5}$$

$$\phi_{LPN}(f) = \tan^{-1}\left[\frac{f}{f_2}\tan\left(\frac{\phi_2}{2}\right)\frac{1+\cos^2(\phi_2/2)-(f/f_2)^2\sin^2(\phi_2/2)}{1-2(f/f_2)^2\sin^2(\phi_2/2)}\right]. \tag{6}$$

A derivative of (5) and (6) with respect to f represents the slope of the insertion phases of two networks, as expressed in (7) and (8):

$$\frac{d}{df}\phi_{HPN}(f) = -\frac{f_1}{f^2}\frac{a_1\left[2c_1^2(f_1/f)^4+c_1(2b_1-3)(f_1/f)^2+b_1\right]}{\left[1-2c_1(f_1/f)^2\right]^2+a_1^2(f_1/f)^2\left[b_1-c_1(f_1/f)^2\right]^2}, \tag{7}$$

$$\frac{d}{df}\phi_{LPN}(f) = \frac{1}{f_2}\frac{a_2\left[2c_2^2(f/f_2)^4+c_2(2b_2-3)(f/f_2)^2+b_2\right]}{\left[1-2c_2(f/f_2)^2\right]^2+a_2^2(f/f_2)^2\left[b_2-c_2(f/f_2)^2\right]^2}, \tag{8}$$

where a_1, b_1, c_1, and a_2, b_2, c_2 are simplified as in

$$a_1 = \tan(\phi_1/2); \quad b_1 = 1+\cos^2(\phi_1/2); \quad c_1 = \sin^2(\phi_1/2)$$

$$a_2 = \tan(\phi_2/2); \quad b_2 = 1+\cos^2(\phi_2/2); \quad c_2 = \sin^2(\phi_2/2)$$

To achieve wideband operation of the phase shifter with HP/LP networks, the slope of the phase response of each filter network should be equal and kept constant over the target frequency band. Figure 3 shows the phase responses of the HP and LP filter network for a 90° phase shift and their corresponding slopes. It can be observed that the slope of the phase response of the HP network is steadier in the high-frequency region about its resonant frequency f_1 whereas that of the LP network is more stable in lower frequency region about its resonant frequency f_2. Thus, to have the minimum phase error over the target frequency band, it is necessary to shift the resonant frequency of the HP network f_1 lower than the center frequency and that of the LP network f_2 higher than f_0. By setting the phase responses of each HP and LP network in opposite directions, we can achieve a flatter phase response slope in the band of interest. With this approach, the phase error is significantly improved within the band. The phase shift of a specific cell is the difference between the two transmission phases as expressed in (9). The phase slopes of the two networks at the center frequency f_0 should be aligned to achieve a constant phase shift over a specific frequency range. In other words, the optimized phase error happens when (10) and (11) are satisfied.

$$\Delta\phi(f) = \phi_{HPN}(f) - \phi_{LPN}(f) \tag{9}$$

$$\Delta\phi(f_0) = \Delta\phi_0 \tag{10}$$

$$\frac{d}{df}\phi_{HPN}(f_0) = \frac{d}{df}\phi_{LPN}(f_0) \tag{11}$$

As can be observed from (7) and (8), (11) naturally happens when setting these constraints: $f_1 f_2 = f_0^2$ and $\phi_1 = -\phi_2$.

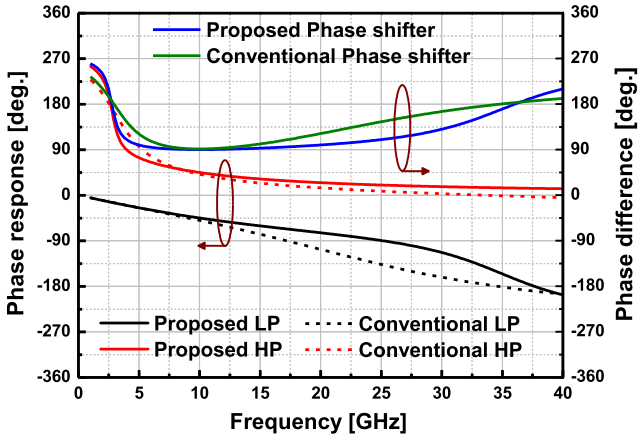


FIGURE 3. The demonstration of bandwidth improvement of the proposed method.

Applying the above constraints, (9) becomes

$$\Delta\phi_0 = \tan^{-1}\left[\frac{f_1}{f_0}\tan\left(\frac{\phi_1}{2}\right)\frac{1+\cos^2(\phi_1/2)-(f_1/f_0)^2\sin^2(\phi_1/2)}{1-2(f_1/f_0)^2\sin^2(\phi_1/2)}\right]-\tan^{-1}\left[\frac{f_0}{f_2}\tan\left(-\phi_1/2\right)\frac{1+\cos^2(-\phi_1/2)-(f_0/f_2)^2\sin^2(-\phi_1/2)}{1-2(f_0/f_2)^2\sin^2(-\phi_1/2)}\right] \quad (12)$$

The values of ϕ_1 can be obtained by solving the above equation with f_1 and f_2 corresponding to the frequency band of interest. The value of each element in the HP and LP networks can be calculated from (1)-(4).

The circuit size of HP/LP phase shifters depends on their operating frequency range. For some frequency bands, the above topology and analysis generate impractical inductance and capacitance values. Therefore, it is necessary to employ a different configuration as a realizable solution. One of the candidates uses the BP configuration shown in Fig. 2 as the leading phase network, while the lagging phase network is realized with a third-order LP filter. The transmission phase of the BP network as a function of frequency is expressed in (13).

$$\phi_{BPN}(f) = \tan^{-1}\left(\frac{1-af^2}{bf}\right), \quad (13)$$

where $a = 8\pi^2 L_1 C_1 = 1/f_1^2$, $b = 4\pi Z_0 C_1$, and f_1 is the resonant frequency. The derivative of (13) concerning the frequency f is the slope of the transmission phase of the BP network as shown in (14) where ϕ_{B0} is the transmission phase at f_0.

$$\frac{d}{df}\phi_{BPN}(f) = \frac{\left[(f_0/f_1)^2-1\right]\left[(f/f_1)^2+1\right]f_0\tan\phi_{B0}}{\left[1-(f_0/f_1)^2\right]^2 f^2+\left[1-(f/f_1)^2\right]^2(f_0\tan\phi_{B0})^2} \quad (14)$$

From the condition $\Delta\phi_0 = \phi_{BPN}(f_0)$ - $\phi_{LPN}(f_0)$, we have (15):

$$\phi_{B0} = \tan^{-1}\left[\frac{f_0}{f_2}\tan\left(\frac{\phi_2}{2}\right)\frac{1+\cos^2(\frac{\phi_2}{2})-\frac{f_0^2}{f_2^2}\sin^2(\frac{\phi_2}{2})}{1-2\frac{f_0^2}{f_2^2}\sin^2(\frac{\phi_2}{2})}\right]+\Delta\phi_0 \quad (15)$$

From the condition $d/df\ [\phi_{BPN}(f_0)] = d/df\ [\phi_{LPN}(f_0)]$, we have (16):

$$\frac{\left[(f_0/f_1)^2-1\right]\left[(f_0/f_1)^2+1\right]f_0\tan\phi_{B0}}{\left[1-(f_0/f_1)^2\right]^2 f_0^2+\left[1-(f_0/f_1)^2\right]^2(f_0\tan\phi_{B0})^2} = \left(\frac{1}{f_2}\right)\times\frac{2a_2c_2^2(f_0/f_2)^4+a_2c_2(2b_2-3)(f_0/f_2)^2+a_2b_2}{\left[1-2c_2(f_0/f_2)^2\right]^2+a_2^2(f_0/f_2)^2\left[b_2-c_2(f_0/f_2)^2\right]^2}, \quad (16)$$

where $a_2 = \tan(\phi_2/2)$, $b_2 = 1 + \cos^2(\phi_2/2)$, and $c_2 = \sin^2(\phi_2/2)$.

The value of ϕ_2 can be obtained from (15) and (16) with f_1 and f_2 as the frequency band of interest. The value of L and C for each network can then be easily calculated. Because the analysis does not take parasitic elements into account for simplicity, there are errors in the relative phase shift between the calculation and the simulation results.

The basic structures utilized in the proposed wideband phase shifter are third-order HP and LP filters. The phase response of each network is determined by the location of its poles and zeros. Thus, the shape of the phase response of the networks can be manipulated to increase phase error bandwidth by appropriately adjusting the relative location of the poles and zeros. For a qualitative examination, the transfer function of the HP network is expressed in (17):

$$S_{21} = \frac{s^3}{\left(s+\frac{1}{Z_0C}\right)\left(s^2+\frac{Z_0}{2L}s+\frac{1}{2LC}\right)} \quad (17)$$

The network has a simple pole and a pair of complex poles as follows:

$$p_1 = \frac{1}{Z_0C}; \quad (18.a)$$

$$p_{2,3} = -\frac{Z_0}{4L}\pm\frac{1}{2}\sqrt{\frac{Z_0^2}{4L^2}-\frac{2}{LC}} \quad (18.b)$$

Capacitance and inductance values can be calculated at the resonant frequency f_1 given by

$$L_1 = Z_0/[\omega_1\sin(\phi_1)] \quad (19)$$

$$C_1 = [Z_0\omega_1\tan(\phi_1/2)]^{-1} \quad (20)$$

Substituting (19) and (20) into (18.a) and (18.b) leads to

$$p_1 = \omega_1\tan(\phi_1/2) \quad (21.a)$$

$$|p_{2,3}| = \omega_1\sin(\phi_1/2) \quad (21.b)$$

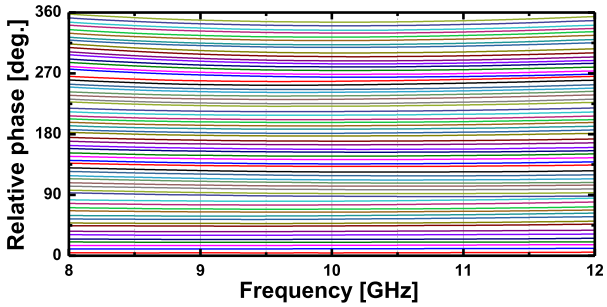


FIGURE 4. The simulated relative phase shift levels in all phase states.

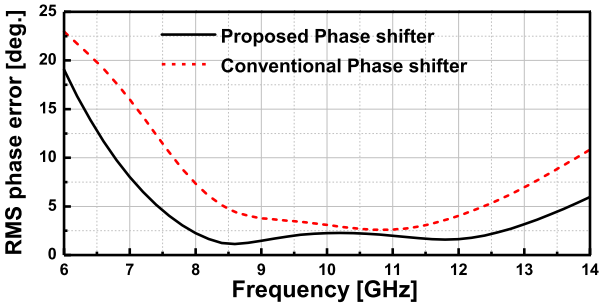


FIGURE 5. The simulated RMS phase error of the proposed method and the conventional method.

Similar results for the LP network can also be obtained as in (22). Substituting (19) and (20) into (18.a) and (18.b) leads to

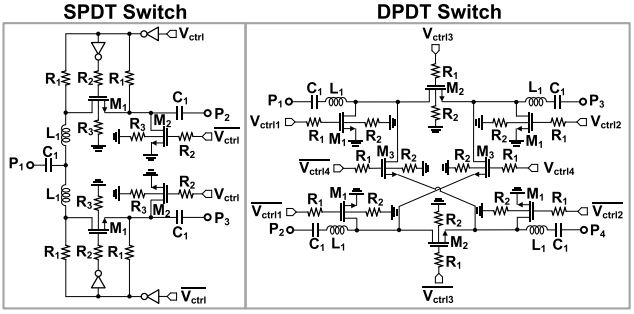
$$p_1 = \omega_2 / \tan(\phi_2/2)\,; \tag{22.a}$$

$$|p_{2,3}| = \omega_2 / \sin(\phi_2/2) \tag{22.b}$$

As can be seen from (21) – (22), the pole locations are directly proportional to the resonance frequencies of the networks. Thus, when a resonant frequency is shifted, its pole locations move accordingly. If the resonant frequency of the LP network is increased and that of the HP network is decreased, the poles of the LP network will be pushed further apart, and the poles of the HP network will be pulled nearer together on the frequency axis. By doing that, the transition area of the phase responses of the two networks is expanded, resulting in a constant relative phase shift over a broader range of frequency. A phase-shifter with the proposed method is compared with a conventional one, which illustrates a definite bandwidth improvement as shown in Fig. 3.

The phase-shifting cells for 5.625°, 11.25°, and 22.5° are constructed with a combination of *L*-*C*-*L* BP and T-type LP networks designed with the available sizes of inductances and capacitances. The phase-shifting cell of 45° is constructed with a *C*-*L*-*C* BP and a π-type LP network to minimize its area consumption compared with a T-type network configuration. The phase-shifting cell for 90° comprises a T-type HP filter and a π-type LP filter with third-order filter networks, while 180° phase shifting is formed with two 90° cells in series. Figure 4 shows the relative phase shift levels which are very flat over the entire X-band. The RMS phase error is less than 2.3° in 8-12 GHz which is much smaller than that of the conventional design as presented in Fig. 5.

A low loss switching mechanism is required to perform the phase-shifting function with coverage of 360° in steps of 5.625°. The SPDT and DPDT switches configure the path through the phase-shifting elements to produce the desired insertion phase shift. The phase shifter employs two SPDT (single pole double throw) switches and four DPDT (double pole double throw) switches as shown in Fig. 6 [15]. For the SPDT switch, the series transistor (M_1) performs the primary switching function. Shunt transistors (M_2) are added to improve the isolation between different paths. In the design of the SPDT and DPDT switches, the gate terminals are biased through a large resistor R_G to reduce fluctuations of V_{GS}, and V_{GD} due to voltage swings at drain and source. This R_G will keep the on-resistance of the transistors unchanged and avoid excessive voltage across the gate dielectric which causes breakdown issues. The SPDT switch is also used as a duplexer in the proposed transceiver.



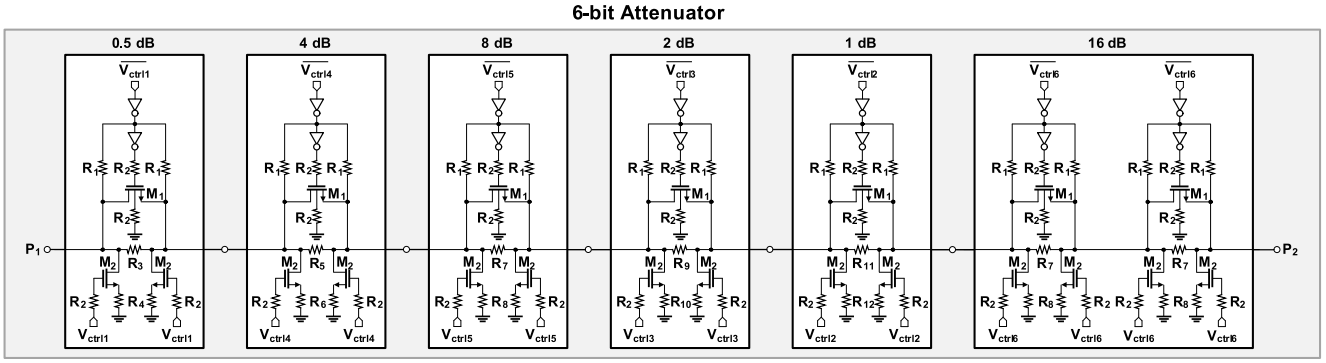
Device parameters				Device parameters			
M_1	M_2	L_1		M_1	M_2	M_3	
130 µm(W) / 60 nm(L)	20 µm(W) / 60 nm(L)	610 pH		20 µm(W) / 60 nm(L)	130 µm(W) / 60 nm(L)	156 µm(W) / 60 nm(L)	
C_1	R_1	R_2	R_3	L_1	C_1	R_1	R_2
3.2 pF	20 kΩ	14 kΩ	11 kΩ	510 pH	3.2 pF	14 kΩ	11 kΩ

FIGURE 6. Schematic [15] and all device parameters of the SPDT (left) and DPDT (right) switches.

B. 6-BIT STEP ATTENUATOR

There are two basic topologies commonly employed in the digital attenuator designs: resistive π-type attenuators, and resistive T-type attenuators. These conventional structures consist of series/shunt switches and resistors. The switches are usually realized as a single NMOS transistor, so NMOS transistors are crucial elements in determining the performance of a digital step attenuator. Explicitly, NMOS switches can be approximately modeled by the resistor R_{ON} in the ON state and the capacitor C_{OFF} in the OFF state.

In this design, a 6-bit CMOS digital attenuator is designed with a resistive π-type structure as depicted in Fig. 7. The attenuator covers the range of 0 to 31.5 dB with steps of 0.5 dB. The relative attenuation level is obtained by taking the



Device parameters

M_1	M_2	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}
130 µm(W) / 60 nm(L)	130 µm(W) / 60 nm(L)	20.2 kΩ	13.8 kΩ	6.7 Ω	9.1 kΩ	31 Ω	82.5 Ω	78.5 Ω	33.5 Ω	21.7 Ω	372.4 Ω	15.2 Ω	3 kΩ

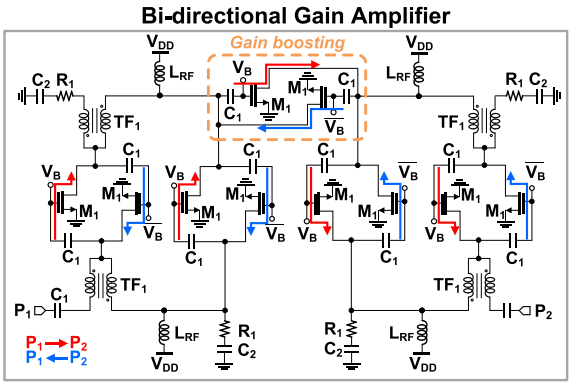
FIGURE 7. Schematic and all device parameters of the designed X-band 6-bit step attenuator.

difference between the attenuation state and the thru state as controlled by single NMOS switches. One of the challenges in designing an attenuator is to sustain reasonable impedance matching for both of its states. The large resistor R_2 at the gate keeps V_{GS} and V_{GD} almost the same during its operation, which relieves the impedance changes that depend on the switch states. By using two inverters with large resistors to bias source and drain terminals of the series switch, the contrast of the channel resistance of the series switch (M_1) for ON/OFF states can be improved to provide less insertion loss of the attenuator at the thru state than that of the attenuators in [13], [15].

C. CASCADED DISTRIBUTED AMPLIFIERS

Distributed gain amplifiers (DGA) have been widely used in wideband applications in the microwave regime due to their excellent input and output matching characteristics as well as their wideband frequency response [21], [22]. However, the summing nature of the distributed amplifier cells results in a power gain limitation, which is typically less than 10 dB. A wideband low-noise amplifier (LNA) and bi-directional gain amplifiers (BDGAs) composed of cascading distributed amplifiers with a common source (CS) stage in the middle were used to provide higher power gain as illustrated in Figs. 8 and 9. Furthermore, a transformer was used to reduce area occupancy, minimizing the number of inductors used for the artificial transmission line by combining the parasitic capacitance of the DGA transistors.

The schematic diagram for the BDGA is presented in Fig. 8. The circuit is composed of four-stage bi-directional distributed gain amplifiers (BDGAs) and a cascading connection stage for gain-boosting at the middle. Like the conventional BDGA, on-chip transformers and the parasitic capacitance of transistors form artificial transmission lines at the input and output, enabling the amplifier's broadband operation. Because of the cascading connection between



Device parameters

M_1	TF_1	L_{RF}	C_1	C_2	R_1
60 µm(W) / 60 nm(L)	720 pH	800 pH	815 fF	3.2 pF	50 Ω

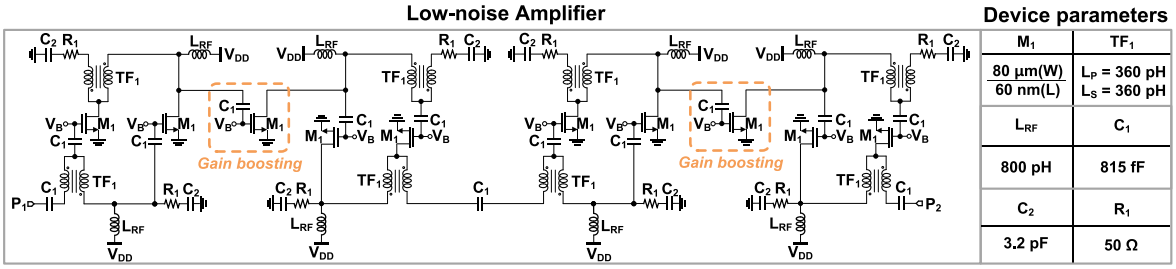
FIGURE 8. Schematic and all device parameters of the transformerbased BDGA.

the BGA stages, the cascaded BDGA takes advantage of multiplicative gains.

The schematic and the device parameters for the LNA are presented in Fig. 9. The LNA consists of gain amplifiers (GAs) and the cascading connection stage for gain-boosting in the middle. It is noteworthy that the center frequency of the LNA is around 12 GHz since the phase shifter has quite a large amount of insertion loss at this frequency. In other words, the LNA is designed to compensate for the loss in the whole transceiver at that frequency.

D. WIDEBAND POWER AMPLIFIER

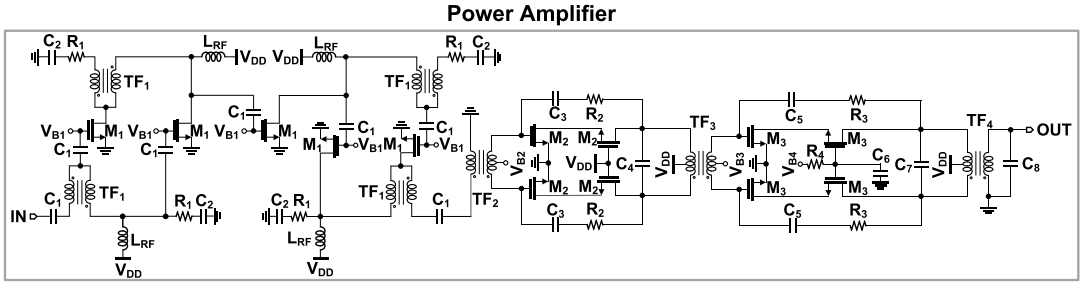
The wideband PA was employed after the SPDT duplexer for Tx operation to enhance the output power and provide a proper power gain of the transmitter as shown in Fig. 10. The PA is constructed from two stages of push-pull amplifiers using a cascode configuration combined with two stages of a transformer-based distributed amplifier. The push-pull



Device parameters

M_1	TF_1
80 µm(W) / 60 nm(L)	L_P = 360 pH L_S = 360 pH
L_{RF}	C_1
800 pH	815 fF
C_2	R_1
3.2 pF	50 Ω

FIGURE 9. Schematic and all device parameters of the transformer-based LNA.



Device parameters

M_1	M_2	M_3	L_{RF}	TF_1	TF_2	TF_3	TF_4
80 µm(W) / 60 nm(L)	250 µm(W) / 60 nm(L)	1200 µm(W) / 60 nm(L)	800 pH	L_P = 360 pH L_S = 360 pH k = 0.63	L_P = 390 pH L_S = 1.19 nH k = 0.68	L_P = 370 pH L_S = 300 pH k = 0.67	L_P = 130 pH L_S = 450 pH k = 0.65

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
50 Ω	300 Ω	300 Ω	600 Ω	815 fF	3.2 pF	500 fF	530 fF	500 fF	530 fF	530 fF	282 fF

FIGURE 10. Schematic and all device parameter of the full X-band PA.

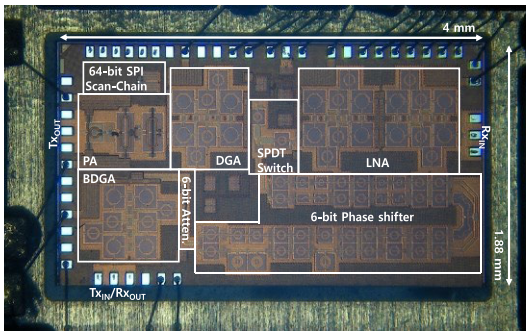


FIGURE 11. Chip-photograph of the fabricated X-band phased-array transceiver in 65-nm CMOS technology.

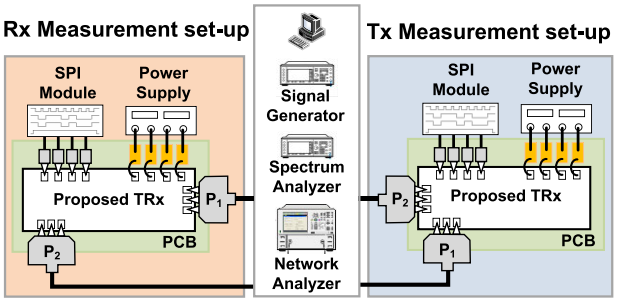


FIGURE 12. The measurement setup for the S-parameters, phase shift, attenuation, and output power of the chip in Rx/Tx operation.

structure naturally delivers the combined power of two independent transistors to the load. Moreover, by using a 1:2 transformer at the output, the load impedance seen by the transistors could be effectively reduced [23]. Therefore, more current can be drawn by the transistor, which results in higher output power delivered to the load. In this design, an RC bias circuit which is similar to the bias configuration used for a stacked transistor in SOI-CMOS technology [24], [25] is employed to bias the gate of the cascode transistor M_3 to achieve equally distributed voltage over the two stacked NMOSs in the cascade configuration. An RC feedback network is also used to make the PA stable with its improved bandwidth [26].

III. MEASUREMENT RESULTS

The X-band phased-array TRM chip was fabricated in 65- nm CMOS technology. Figure 11 shows the chip-photograph of the implemented transceiver, which occupies 4 mm × 1.88 mm, including all the pads. As shown in Fig. 12, the TRM chip was measured with on-chip probing. A 64-bit serial-peripheral-interface (SPI) scan-chain was integrated for digital control of each block. The equipment used for measurement was as follows: Agilent E4407B spectrum analyzer, Keysight DSO-X 6002A digital oscilloscope, Agilent 83623B signal generator, and Keysight N5224A network analyzer.

TABLE 1. Comparison with previously reported state-of-the-art X-Band Phased-Array Transceivers.

Ref.	This work	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]
Tech.	*65nm CMOS*	*0.2μm pHEMT*	*0.25μm pHEMT*	*0.25μm SiGe*	*0.25μm SiGe*	*0.18μm SiGe*	*0.13μm SiGe*	*0.13μm SiGe*	*0.25μm SiGe*	*0.18μm SiGe*	*0.13μm SiGe*	*0.13μm CMOS*	*0.18μm CMOS*	*0.13μm CMOS*	*0.13μm CMOS*	*65nm CMOS*	*0.13μm CMOS*
f_{RF} [GHz]	*8-12*	*9-12*	*8.5-11.5*	*8-11*	*8-11*	*6-18*	*8-10.7*	*9-11*	*8-12*	*8-16*	*8-12*	*8.5-10.5*	*8.5-10*	*8.5-10.5*	*7.9-9.6*	*8-10.5*	*9-10*
Phase-shifter /Attenuator # of bits	*6/6*	*7/7*	*6/5*	*5/5*	*5/5*	*4/NA*	*5/NA*	*5/NA*	*6/6*	*7/7*	*6/6*	*5/NA*	*6/6*	*6/5*	*4/3*	*6/6*	*6/5*
Function	*Rx/Tx*	*Rx/Tx*	*Rx/Tx*	*Rx/Tx*	*Rx/Tx*	*Rx*	*Rx*	*Rx/Tx*	*Rx/Tx*	*Rx/Tx*	*Tx/Rx*	*Rx*	*Rx/Tx*	*Rx/Tx*	*Tx*	*Rx/Tx*	*Rx/Tx*
# of channel	*1*	*1*	*1*	*1*	*1*	*8*	*1*	*1*	*1*	*4*	*4*	*4*	*1*	*1*	*4*	*1*	*4*
Rx/Tx Gain [dB]	*15 /15*	*5 /5*	*27 /NA*	*20 /30*	*17 /17*	*24.5 /NA*	*11 /NA*	*25 /22*	*17.8 /17.7*	*16/21*	*13/NA*	*12.2 /NA*	*12 /11*	*3.5 /3.5*	*NA /11.5*	*3.7 /3.7*	*9 /12*
Rx/Tx OP_{1dB} [dBm]	*NA /11.84*	*NA /14*	*13 /19*	*NA /18*	*NA /12*	*NA /NA*	*12.5 /NA*	*6 /28*	*NA /17*	*NA/8.5*	*NA/12*	*-7.5 /NA*	*11 /11.5*	*6.5 /6.5*	*NA /8.8*	*NA /5.1*	*NA /11*
Rx NF [dB]	*8.4*	*8*	*2.3*	*9*	*10*	*4.2*	*4.1*	*3*	*9.8*	*10*	*11.5*	*3.4*	*8.5*	*7.5*	*NA*	*10*	*NA*
RMS phase error [deg.]	*5*	*1.5*	*NA*	*6*	*6*	*5.7*	*9*	*3.8*	*2*	*2.8*	*3*	*12*	*2*	*4.3*	*5*	*4*	*2.3*
RMS amplitude error [dB]	*0.45*	*0.08*	*5.5*	*1.5*	*2*	*0.9*	*0.6*	*1.2*	*0.25*	*0.3*	*0.5*	*0.4*	*0.25*	*0.8*	*0.5*	*0.5*	*0.4*
Chip area [mm^2]	*7.52*	*18.48*	*20*	*8.4*	*16*	*5.39*	*13.3*	*15.6*	*9*	*16*	*54*	*7.25*	*12.8*	*1.2*	*8.7*	*9.56*	*2.8*
Rx/Tx DC power [mW]	*110 /216*	*600 /600*	*1200 /1200*	*1500 /1500*	*800 /800*	*561 /NA*	*33 /NA*	*352 /4128*	*330 /792*	*215 /280*	*NA*	*144 /NA*	*670 /640*	*154 /154*	*870 /870*	*170 /170*	*500 /800*

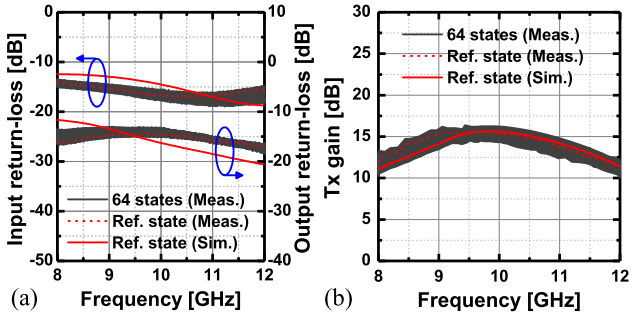


FIGURE 13. Simulated and measured results for (a) the S_{11}, S_{22}, and (b) Tx gain of the transceiver in Tx operation depending on 64 different phase-shift states.

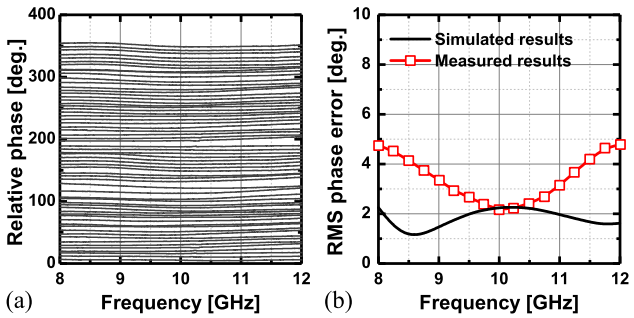


FIGURE 14. (a) Measured relative phase shift of the transceiver in Tx operation. (b) Simulated and measured results for the RMS phase error of the transceiver in Tx operation.

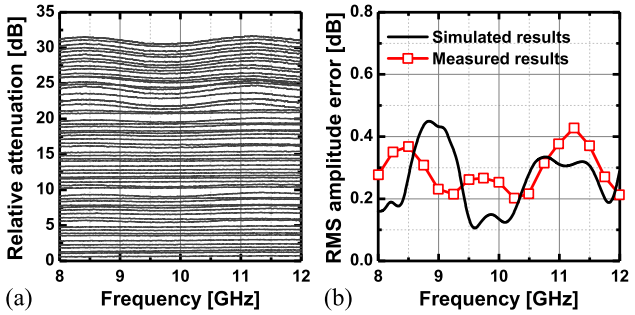


FIGURE 15. (a) Measured relative attenuation level of the transceiver in Tx operation. (b) Simulated and measured results for the RMS amplitude error of the transceiver in Tx operation.

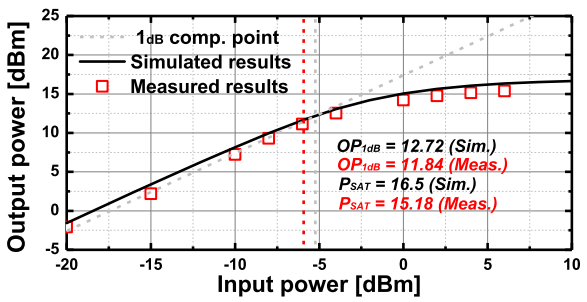


FIGURE 16. Simulated and measured results for the output power of the transceiver in Tx operation at 10 GHz.

In Tx mode, the simulated and measured S_{11} and S_{22} for 64 different phase states are presented in Fig. 13(a). Between 8 and 12 GHz, the input and output return losses are better than 10 dB. Figure 13(b) shows the simulated and measured gain of the Tx for 64 different phase states. The gain flatness is about $\pm$ 2 dB. As shown in Fig. 14(a), the measured relative phase-shift in the X-band has a resolution of 5.625° and

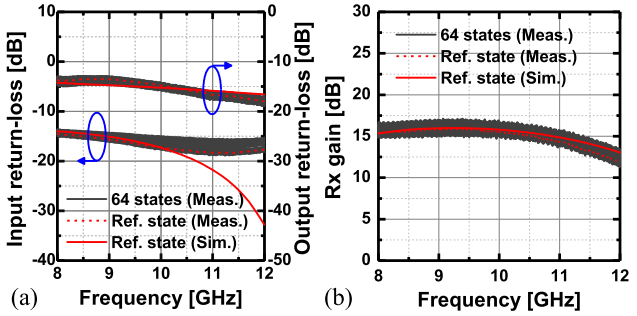


FIGURE 17. (a) Measured relative attenuation level of the transceiver in Tx operation. (b) Simulated and measured results for the RMS amplitude error of the transceiver in Tx operation.

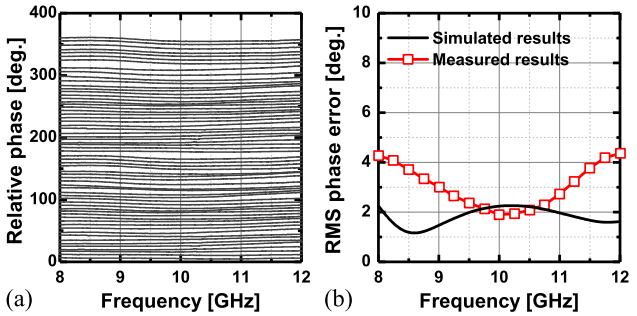


FIGURE 18. (a) Measured relative phase shift of the transceiver in Rx operation. (b) Simulated and measured results for the RMS phase error of the transceiver in Rx operation.

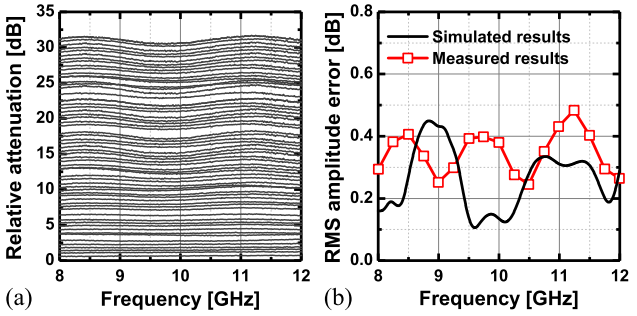


FIGURE 19. (a) Measured relative attenuation level of the transceiver in Rx operation. (b) Simulated and measured results for the RMS amplitude error of the transceiver in Rx operation.

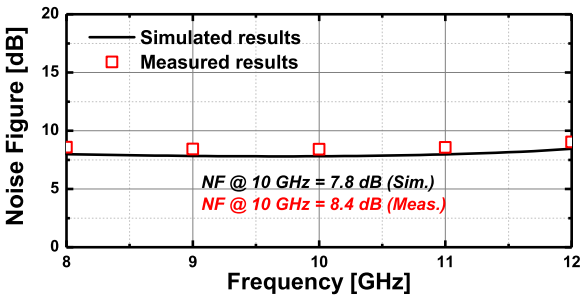


FIGURE 20. Simulated and measured NF of the transceiver in Rx operation.

covers 0° to 360°. The simulated and measured results for the RMS phase error in the X-band are depicted in Fig. 14(b). The measured RMS phase error is less than 5°, which is smaller than the resolution. The measured relative attenuation level of the transceiver in the Tx operation is shown in Fig. 15(a). It shows a resolution of 0.5 dB in the whole X-band. The simulated and measured results for the RMS amplitude error of the transceiver in the Tx operation are illustrated in Fig. 15(b). In full X-band, the measured RMS amplitude error is less than 0.45 dB, which is smaller than the amplitude resolution. Figure 16 shows the output power response of the transceiver in Tx operation measured with a 10-GHz input signal at the reference state of the phase shifter (i.e., all zero-bit state). The saturated output power (P_{SAT}) of 15.18 dBm and output 1-dB compression point (OP_{1dB}) of 11.84 dBm can be observed. The total power consumption of the transceiver with 1 V supply is 216 mW at the OP_{1dB} output point.

In Rx mode, the simulated and measured S_{11} and S_{22} for 64 different phase states are shown in Fig. 17(a). The input and output return losses are better than 10 dB. Figure 17(b) illustrates the simulated and measured gain of the Rx depending on 64 different phase states. The gain flatness is about ± 2 dB, and the 3-dB bandwidth is wider than 5.2 GHz (7 to 12.2 GHz). As shown in Fig. 18(a), the measured relative phase-shift in the X-band has a resolution of 5.625° and covers 0° to 360°. The simulated and measured results for the RMS phase error in the X-band are depicted in Fig. 18(b). The simulated and measured RMS phase error is less than 5°, which is smaller than the resolution. The measured relative attenuation level of the transceiver in the Rx operation is shown in Fig. 19(a). It shows a resolution of 0.5 dB in the X-band. The simulated and measured RMS amplitude error of the transceiver in the Rx operation is illustrated in Fig. 19(b). In full X-band, the measured RMS amplitude error is less than 0.45 dB which is smaller than the resolution. The simulated and measured noise figure (NF) of the transceiver in the Rx operation is presented in Fig. 20. The NF measurement was carried out from the Y-factor method, showing a minimum NF of 8.4 dB in the whole X-band.

Table 1 compares the implemented transceiver with previously published III-V chipsets and SiGe based transceivers for X-band phased-array systems. It shows that the implemented TRM chip shows the highest OP_{1dB}, gain, and widest opera ting frequency range among the CMOS based phased-array chips and has RF performance comparable with SiGe transceivers and III-V chipsets with much lower power consumption.

IV. CONCLUSION

We demonstrated a full X-band transmit/receive module (TRM) chip for phased-array antenna systems in 65-nm CMOS technology. The implemented TRM chip integrates a BDGA, a 6-bit attenuator, a 6-bit passive phase shifter with a resonant frequency misalignment technique to expand the operating frequency range. A wideband PA and LNA were also integrated with an SPDT switch as a duplexer for bi-directional operation of the half-duplex transceiver. The measurement results demonstrated that the performance of the implemented TRM chip achieved the highest OP_{1dB},

gain and widest operating frequency range among recently reported CMOS based phased-array chips. The TRM has RF performance comparable withseveral recently reported SiGe transceivers and III-V TRM chipsets with a distinct advantage of low-power dissipation.

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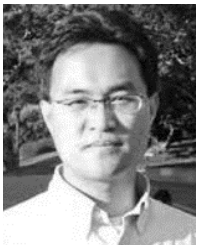

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