IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 11, 2020, accepted April 4, 2020, date of publication April 9, 2020, date of current version April 28, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2986949

Fully Synthesizable Low-Area Analogue-to-Digital Converters With Minimal Design Effort Based on the Dyadic Digital Pulse Modulation

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This work was supported from Mediatek Singapore (chip fabrication) and the NRF-CRP20-2017-0003 CogniVision grant from the Singapore National Research Foundation. Also, this project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 703988.

ABSTRACT In this paper, fully-synthesizable Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) suitable for low-cost integrated systems are proposed both for voltage and current input. The proposed ADCs are digital in nature and are based on the Dyadic Digital Pulse Modulation (DDPM) Digital-to-Analog (DAC), instead of a traditional capacitive DAC. The proposed fully-digital ADC architectures enable low-effort design, silicon area reduction, and voltage scaling down to the near-threshold region. Compared to traditional analog-intensive designs, their digital nature allows easy technology and design porting, digital-like area shrinking across CMOS technology generations, and also drastically reduced system integration effort through immersed-in-logic ADC design. The voltage-input ADC architecture is demonstrated with a 40-nm testchip showing 3,000-μm^2 area, 6.4-bit ENOB, 2.8kS/s sampling rate, 40.4dB SNDR, 49.7dB SFDR, and 3.1μW power at 1V. A current-input ADC is also demonstrated for direct current readout without requiring a trans-resistance stage. 40-nm testchip measurements show a 5-nA to 1-μA input range, 4,970μm^2 area, 6.7-bit ENOB and 2.2-kS/s sample rate, at 0.94-μW power. Compared to the state of the art, the proposed ADC architecture exhibits the highest level of design automation (standard cell), lowest area, and the unique ability to cover direct acquisition of both voltage and current inputs, suppressing the need for transresistance amplifier in current readout.

INDEX TERMS Analog-to-digital converter (ADC), fully-digital, fully-synthesizable, standard cell design, low design effort, low area, analog sensing Analog-to-digital converter (ADC), current sensing.

I. INTRODUCTION

Analog-to-digital converters are essential building blocks in systems-on-chip embedding sensing capabilities. As exemplified by Internet of Things applications, the widespread adoption of distributed sensing imposes a very tight cost target, leading to the demand for very low-cost, low-design effort (both at the block and the system integration level), low-area, design-portable, and technology scaling-friendly components [1]–[3]. ADCs and other blocks in sensor interfaces are particularly critical on such respects, as they tend to be analog design-intensive, and hence porting to new technologies requires fundamental redesign, while bringing very limited area down-scaling compared to digital. The resulting design effort, area and cost issues have motivated significant research effort on digital-intensive data converters over the last years [4]–[18]. In the related state of the art, various ADC architectures that can be partially or fully synthesized with standard cells (and hence fully-automated design flows) have been explored for applications allowing relaxed specifications (e.g., resolution in the 6-9 bit range) [9]–[18]. As side benefit, fully-synthesizable ADCs are inherently amenable for low-voltage operation, simplifying system integration with the digital sub-system, and the on-chip power delivery.

Prior art in mostly-digital data converters is restricted to voltage-input ADCs and has explored various principles.

The associate editor coordinating the review of this manuscript and approving it for publication was Stavros Souravlas.

Probabilistic process variations in comparators in stochastic Flash ADCs has been exploited, targeting relatively high sampling frequencies in the order of a hundred MS/s, although at an input dynamic range limited to very few hundreds of mVs [9]–[11]. Mostly-digital ADCs based on voltage controlled oscillators (VCO) were proposed for sampling rates of hundreds of MS/s with limited resolution, and an energy efficiency that significantly degrades at lower sample rates [12]. Sigma-Delta ($\Sigma\Delta$) MASH ADCs (e.g., [13]) achieve the highest resolution at relatively low sample rates, but require significant analog design in addition to their digital components. Mostly-digital successive approximation register (SAR) ADCs have also been demonstrated for low-area and low-resolution targets, while achieving rail-to-rail input range [15], [16].

In this paper, a Nyquist-rate fully-synthesizable SAR voltage-input ADC based on the Dyadic Digital Pulse Modulation (DDPM) is proposed. Its voltage-input implementation is demonstrated through a 40-nm testchip, showing 6.4-bit resolution in dynamic conditions (7 bits in static conditions). Measurements demonstrate operation at 2.8 kS/s with a power consumption down to 3.1 μW under voltage scaling, as enabled by its standard cell design approach. Based on the same general principle, a current-input ADC architecture is also introduced. To the best of the authors' knowledge, this is the first fully-synthesizable current-input ADC for direct acquisition of current signals, with no need for a transresistance amplifier stage. Its implementation in 40 nm exhibits a 5nA-1μA input range, 7-bit static resolution, 2.2-kHz sample rate, 0.94-μW power, and the very compact area of 4,970μm^2 (in addition to the area savings due to the suppression of the transresistance stage).

Operation of the proposed ADCs in the kS/s range makes them suitable for a wide range of applications where physical signals with kHz-range bandwidth need to be sensed, at the relatively low resolutions allowed by digital ADC architectures [9]–[15]. Compared to prior art, the proposed ADCs exhibit the lowest area and the highest resolution among mostly- and fully-digital ADCs to date, while being designed with fully-automated digital design flows. This allows the highest level of design automation and integration with digital logic, substantially reducing design and system integration effort via immersed-in-logic implementation, compared to traditional analog architectures.

The paper is structured as follows. Section II introduces the proposed DDPM-based voltage-input ADC (named as ADC-V in the following). ADC-V measurement results are reported in Section III. Section IV and V respectively present the current-input ADC (ADC-I) architecture and measurement results. Conclusions are drawn in Section VI, along with remarks on future work.

II. FULLY-SYNTHESIZABLE VOLTAGE-INPUT ADC ARCHITECTURE

The proposed voltage-input DDPM ADC is based on the architecture in Fig. 1. This comprises only logic gates and two passive components, which can all be instantiated, placed and routed automatically (i.e., through scripting, without requiring any analog design). The analog multiplexer (AMUX) is implemented by CMOS transmission gates. Although such components are often used as switches in digital designs, they might not be available in commercial standard cell library. In this case, such circuits can be straightforwardly integrated with an existing library by

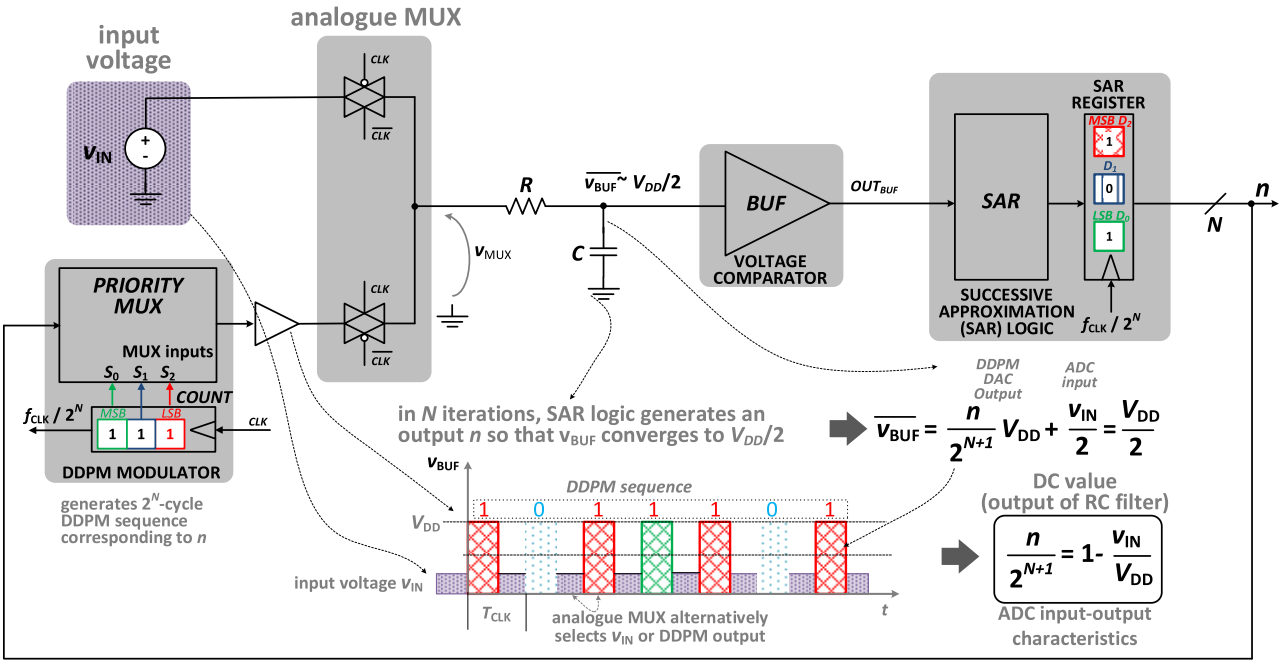

FIGURE 1. Architecture of the proposed standard cell-based voltage-input Analog-to-Digital Converter (ADC-V).

creating[1] the corresponding cell views, for automated place&route.

The input voltage $v_{\rm IN}$ is applied to one of the two inputs of the AMUX. The other input is connected to the output of a Dyadic Digital Pulse Modulator (DDPM) [7], [8], [19], which provides a digital stream with a pulse density $n/2^N$ over a 2^N clock cycles as illustrated in Fig. 2, being $n = \sum_{i=0}^{N-1} D_{in,i}2^i$ ($D_{in,i}$ are the bit values of its input digital word). The DDPM modulator effectively generates a feedback analog voltage, performing the DAC conversion of its digital input. In particular, it converts the input n to a voltage $\frac{n}{2^N}V_{DD}$ that is clearly proportional to the pulse density and the supply voltage V_{DD}. In turn, the DAC input word is provided by the successive approximation register (SAR) logic to progressively approach the input voltage $v_{\rm IN}$, as detailed in the following.

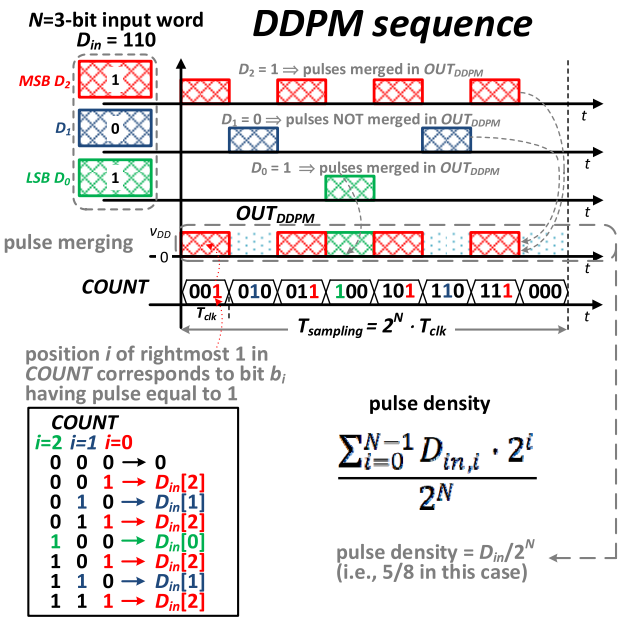

FIGURE 2. Detailed structure of the output sequences generated by a DDPM modulator [7], [8], [19] (example with $N = 3$ bit).

During the conversion, the AMUX selection signal is generated by a clock signal with 50% duty cycle, hence its output $v_{\rm MUX}$ is forced to the DDPM output voltage during the first half of each clock cycle, whereas it is set to the input voltage $v_{\rm IN}$ in the second half of the clock cycle (see the inset of Fig. 1). It follows that the time average of $v_{\rm BUF}$ over a whole DDPM period that is extracted by the RC low pass filter in Fig. 1 (see filter at the AMUX output) can be expressed as

$$\bar{v}_{\rm BUF} = \frac{\frac{n}{2^N}V_{DD} + v_{IN}}{2} = \frac{n}{2^{N+1}}V_{DD} + \frac{1}{2}v_{IN}. \qquad (1)$$

From Fig. 1, the RC-filtered voltage is then applied to the input of a CMOS inverter, which is employed as a single-ended voltage comparator with logic threshold set at $V_{DD}/2$ (as achieved through common transistor sizing).

Based on the comparator output, the SAR register is updated every SAR cycle consisting of 2^N DDPM clock periods, i.e. the number of DDPM clock cycles required to complete the DAC conversion from n to the $v_{\rm MUX}$ voltage. During the i-th SAR cycle, the first term of (1) is increased by $2^{-i-1}V_{DD}$ if $\bar{v}_{\rm BUF} < V_{DD}/2$, whereas it is decreased by $2^{-i-1}V_{DD}$ if $\bar{v}_{\rm BUF} > V_{DD}/2$, thus progressively approaching $V_{DD}/2$ over the successive SAR conversion cycles. Accordingly, at the end of the N SAR cycles, the time-averaged voltage $\bar{v}_{\rm BUF}$ in Fig. 1 (i.e., at the output of the RC filter) converges to the threshold of the comparator $V_{DD}/2$ within one LSB of the DDPM modulator. As a consequence, from (1) the final voltage $v_{\rm MUX}$ at the end of the N SAR conversion cycles is

$$v_{\rm MUX,final} = \frac{n}{2^{N+1}}V_{DD} + \frac{1}{2}v_{IN} = \frac{V_{DD}}{2} \qquad (2)$$

where the above residual sub-LSB quantization error was ignored, as intrinsic error in any ADC architecture.

From (2), the digital code n stored in the SAR register at the end of the conversion can be expressed as

$$n = 2^N\left(1 - \frac{v_{IN}}{V_{DD}}\right) \qquad (3)$$

which is proportional to the analog input v_{IN}/V_{DD} normalized to the dynamic range, as expected from an ADC.

III. FULLY-SYNTHESIZABLE VOLTAGE-INPUT ADC: EXPERIMENTAL RESULTS

The proposed ADC-V was implemented in the 40nm CMOS testchip shown in Fig. 3, and occupies a silicon area of $3{,}000\mu\text{m}^2$. To fairly evaluate it in a technology-independent manner, this area corresponds to $1.87 \cdot 10^6$ F^2, where F is the minimum feature size allowed by the process (i.e., 40 nm in this case). The design was carried out with a conventional fully-automated standard cell design flow to place and route the architecture in Fig. 1. The filter capacitor C and the resistor R were implemented by automatically instantiating them as widely available parametric cells, and then placing and routing automatically. In particular, Metal-Oxide-Metal (MOM) capacitor and a high-resistivity poly resistor p-cells

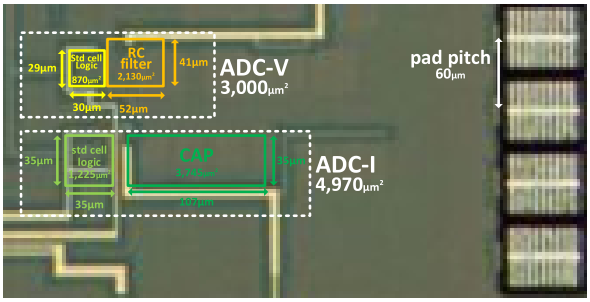

FIGURE 3. Micrograph of the two ADCs in the 40nm testchip.

[1]This can be done very easily by reusing the widely available transmission gate-based MUX standard cell [15], and eliminating its output driver.

were used, as available in the adopted design kit. The overall 20-pF capacitance and 500-kΩ resistance enable operation at clock frequency of at least 160MHz.

The testchip was characterized at 25°C temperature, whereas the supply was varied from 0.7 to 1 V, at 2.8-kHz sample rate. The power consumption measured at the two supply voltages is respectively 3.1 μW and 7.3 μW. From the static characterization of the ADC in Fig. 4, the maximum (RMS) integral nonlinearity INL is 2.2 (0.9) LSB at 8-bit nominal resolution, whereas the maximum (RMS) differential nonlinearity DNL is 2.3 (0.9) LSB. The results were confirmed to be consistent across 6 dice, whose maximum INL (DNL) were measured to be in the 1.8-2.2 LSB (2.0-2.3 LSB) range.

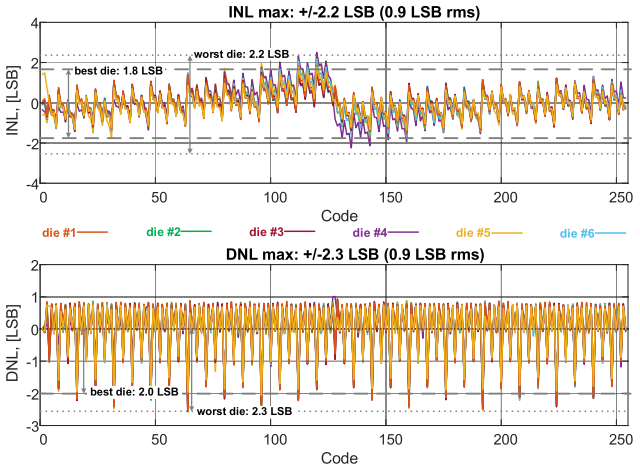

FIGURE 4. Measured INL and DNL of the proposed ADC-V (6 dice).

The results of the dynamic characterization of the ADC are reported in Fig. 5, as performed under a 30-Hz sine wave input with full-swing amplitude. Results in Fig. 6 show a THD of 47.8dB, a SFDR of 49.7dB and an SNDR of 40.4dB, which translate into 6.4 effective bits of resolution (ENOB). The results of the amplitude and frequency characterization in Fig. 5 confirm consistent performance across frequencies, and highlight that the effective resolution is significantly affected by the harmonic distortion, as observed by low frequency SNDR and THD differing by less than 6dB. From Fig. 1, this is likely due to the linearity degradation of CMOS transmission gates below 0.8 V supply voltages due to their supply-dependent on resistance., Although being the main resolution bottleneck in the presented design, such distortion is not a fundamental limitation since it can be improved by simply improving the linearity of the transmission gate resistance (e.g., gate voltage boosting). In other words, the proposed ADC architecture is potentially able to achieve higher resolutions, at the cost of the adoption of multiple voltages or the creation of additional standard cells. The effect of voltage down-scaling on the measured SNDR and THD is shown in Fig. 6, which reveals a relatively minor 2-dB SNDR degradation at 0.8-V supply. A 6.3-dB SNDR degradation is also observed at low frequency.

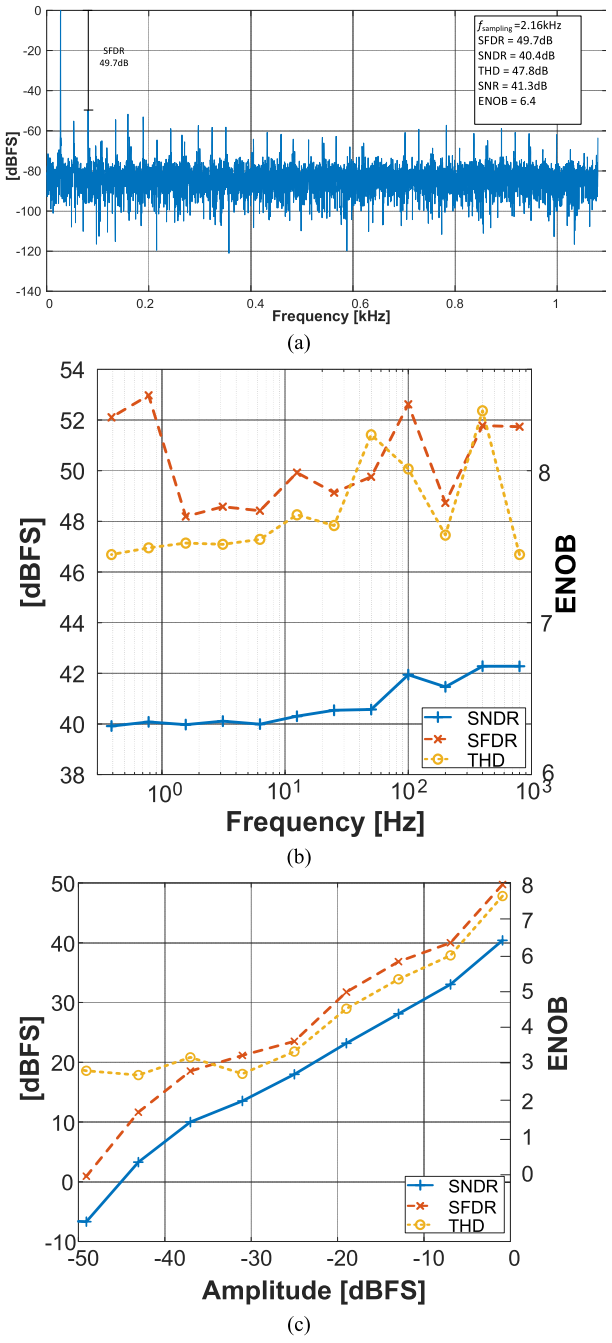

FIGURE 5. ADC dynamic characterization measurements at nominal supply voltage (1 V): (a) output spectrum for full-swing 30Hz sinewave input, (b) dynamic performance parameters versus input frequency at full-swing sine wave amplitude, and (c) sine wave amplitude at 30-Hz input frequency.

The measured ADC performance is compared to state-of-the-art fully-synthesizable ADCs in Table 1. The table shows that the proposed ADC architecture exhibits the smallest area normalized to F^2, as needed to fairly compare to other demonstrations regardless of the adopted technology. In particular, the proposed ADC architecture occupies 12–95x less area than Flash ADCs [6]–[8], and 1.4x less normalized area than the very compact SAR architecture in [9]. The proposed

TABLE 1. Comparison with state-of-the-art fully- or partially-synthesizable ADCs. Best performance in bold.

	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]	This work	
type of input	voltage	voltage	voltage	voltage	voltage	voltage	voltage	voltage	voltage	current
architecture	Flash	Flash	Flash	VCO-based	MASH ΔΣ	Flash	SAR	SAR	SAR	SAR
technology [nm]	180	90	130	65	65	65	28	40	40	40
area [μm^2]	94,000	180,000	510,000	26,000	14,000	756,000	2,000	11,300	3,000	4,970
normalized area [$10^6 F^2$]	2.90	22.2	30.2	6.15	3.31	179	2.55	7.06	**1.87**	3.11
sampling rate F_S [S/s]	50M	21M	140M	**205M**	150M	100M	500k	32M	2.8k	2.2k
SNDR [dB]	35.6	34.61	28.5	50.3	**56.3**	39	34.2	47.4	40.4	42.1
SFDR [dB]	44	41.46	37	**55.3**	N/A	N/A	N/A	57.8	49.7	51
ENOB [bit]	5.62	5.45	4.5	8.1	**9.06**	6.2	5.4	7.6	6.4	6.7
supply voltage	1.3V	0.7V	0.7V	0.6V	1V	0.9	0.5V	1.2V	1 (0.7)	0.6V
input range	±280mV	±140mV	±400mV	full scale	full scale	±220mV	full scale	full scale	full scale	1μA
power [μW]	312	1,110	2,300	3,300	872	33,000	92	187	**7.3 (3.1)**	**0.94**
FoM [fJ/convstep]	127	1,200	**726**	940	348.6	4,530	4,390	30.7	30,900	4,110
synthesizable*	partially	fully	fully	partially	partially	partially	fully	no	partially	fully
degree of design automation	digital w/ custom circuits	standard cell design flow	standard cell design flow	digital w/ custom circuits	digital + added standard cells	digital + added standard cells	standard cell design flow	partial design automation	digital + added standard cells	standard cell design flow

*Partially synthesizable = mixture of standard cells and custom design, fully synthesizable = standard cells only, designed with automated digital design flow
F = minimum feature size of the process

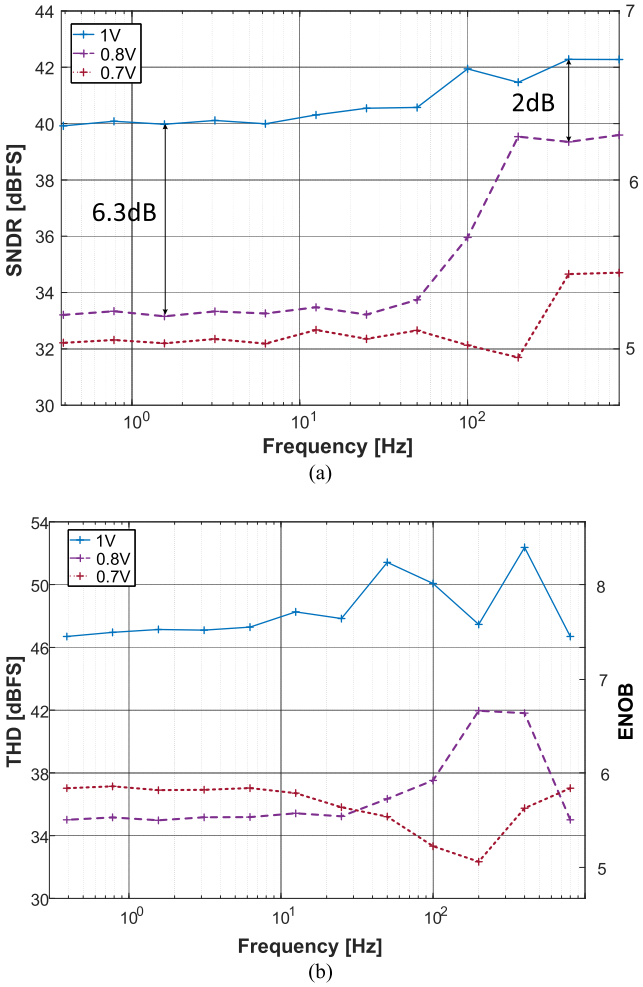

FIGURE 6. Effect of voltage scaling on the degradation in the measured (a) SNDR and (b) THD versus sine wave input frequency.

ADC architecture also achieves the highest effective resolution of 6.4 bits across fully-synthesized ADCs reported to date, as well as the best performance in term of SNDR and SFDR (i.e., resolution). As drawback, the proposed ADC has 7-42x worse Walden energy efficiency figure of merit (FoM, defined as the energy per conversion per step, as relevant to ADCs operating at moderate to relatively high sample rate targets). However, the proposed ADC is still reasonably efficient in applications targeting kS/s-range sample rates. Indeed, the proposed ADC operates at the lowest reported power of 7.3 μW at nominal voltage (and down to 3.1 μW at 0.7-V supply), which is lower than other fully-synthesized ADCs [6]–[9] by 12–4,520x.

IV. FULLY-SYNTHESIZABLE CURRENT-INPUT ADC

A. GENERAL ARCHITECTURE OF ADC-I

Current sensing and conversion are generally required to read out sensors having a current-domain output, or high output impedance [1]. This is the case for several sensors and applications, such as electrochemical biosensors [2], temperature sensing [21] (e.g., thermistor-based), environmental monitoring [22] (e.g., gas sensing), biomedical signal acquisition [23] (e.g., potentiostat-based), light sensing [24] (e.g., photodiodes and photoconductors), imaging [25], and on-chip leakage/variation monitoring [26], which require relatively coarse conversion in the μA and kHz range or below.

Traditionally, current sensing is performed by combining a voltage-input ADCs with an analog-intensive transresistance amplifier to first convert the input current into a voltage, negating the benefits of a synthesizable design approach. For this reason, a novel current-input ADC architecture is proposed and represented in Fig. 7, which directly converts the input current without a transresistance amplifying stage. In this figure, the negative feedback loop makes the feedback current magnitude $I_{feedback}$ equal to the input current I_{in} (and opposite direction) by the end of each conversion, as a result of a successive approximation current search.

As first component encountered in the forward path in Fig. 7, the digital buffer *BUF* effectively implements a

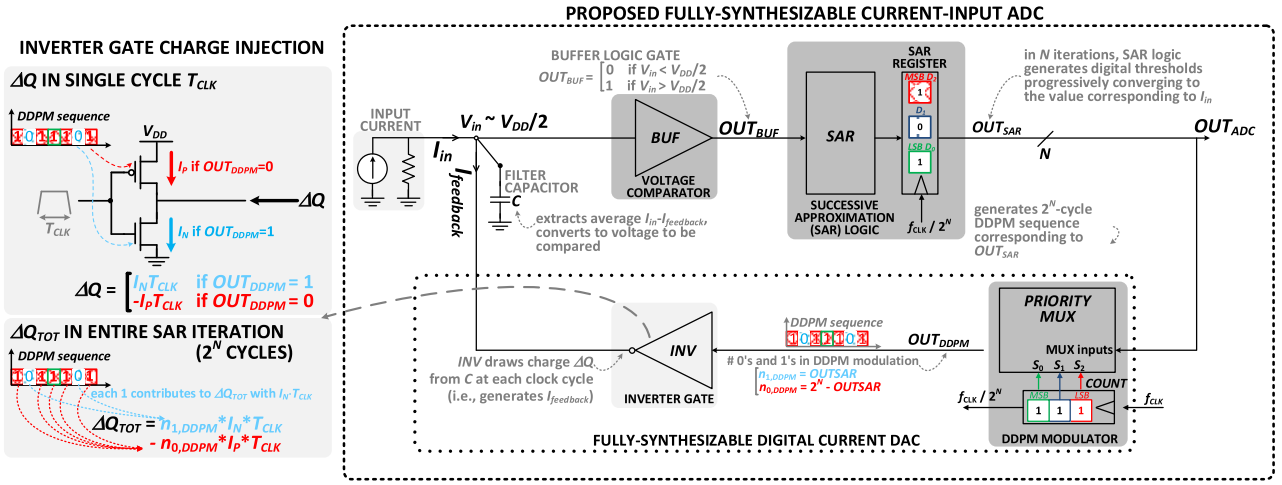

FIGURE 7. Architecture of the proposed fully-synthesizable current-input Analog-to-Digital Converter (ADC-I), as exemplified with $N = 3$ bit.

voltage comparator, with its output OUT_{BUF} being high (low) when its input is above (below) its logic threshold V_{LT}. The *BUF* logic threshold is set to $V_{LT} = V_{DD}/2$ under a supply voltage V_{DD} via symmetric transistor sizing (see considerations on matching in Section IV). In turn, OUT_{BUF} is the input of the successive approximation logic that is commonly encountered in general SAR ADCs [15]. The SAR logic generates a sequence of digital values that progressively converges to the input value in N SAR iterations.

B. DETAILED ADC-I OPERATION AND PROPERTIES

At each step of the SAR conversion, the SAR logic digital output is converted to an analog current by the fully-digital current DAC shown in Fig. 7. The DDPM modulator in this figure converts the SAR logic output OUT_{SAR} into a pulse train output OUT_{DDPM}, whose pulse density $n_{1,DDPM}/2^N$ is set to OUT_{SAR}. Such DDPM pulse density is then converted into the average current $I_{feedback}$ by the subsequent inverter gate *INV* driving the filter capacitor C, thus closing the loop. From a temporal viewpoint, at each clock cycle the inverter gate *INV* draws from the load capacitor C an amount of charge ΔQ equal to

$$\Delta Q = \begin{cases} I_N T_{CLK} & \text{if } OUT_{DDPM} = 1 \\ -I_P T_{CLK} & \text{if } OUT_{DDPM} = 0 \end{cases} \tag{4}$$

being I_N the NMOS on-current as shown in the left inset of Fig. 7. I_N is nominally set to be equal to the PMOS on-current I_P via symmetric transistor sizing. Regarding the capacitor C, its value is set high enough to make the voltage ripple $\Delta Q/C$ at the *BUF* input voltage V_{in} negligible (i.e., a small fraction of an LSB), under a given inverter strength and DDPM modulator clock frequency. Such ripple suppression in turn allows to mitigate drain voltage-induced mismatch in I_N and I_P (e.g., due to the DIBL effect), and the related *INV* offset.

In each 2^N-cycle SAR iteration, the average feedback current $I_{feedback}$ generated by *INV* is equal to the ratio of the overall charge ΔQ_{TOT} injected in C and the overall time period $2^N T_{CLK}$. This yields the following expression

$$\begin{aligned} I_{feedback} &= \frac{\Delta Q_{TOT}}{2^N T_{CLK}} = \frac{n_{1,DDPM} - n_{0,DDPM}}{2^N T_{CLK}} I_N \cdot T_{CLK} \\ &= \frac{OUT_{SAR} - \left(2^N - OUT_{SAR}\right)}{2^N} I_N \\ &= \frac{OUT_{SAR} - 2^{N-1}}{2^{N-1}} I_N . \end{aligned} \tag{5}$$

At the end of each SAR iteration, the voltage across C is set by the overall current $I_{in} - I_{feedback}$ injected in it. From a circuit point of view, for simplicity let us first consider the circuit in Fig. 7 at a zero-current bias point, at which $I_{in} = 0$. At the end of the SAR conversion, *INV* has to provide an average current $I_{feedback} = I_{in} = 0$ (within one LSB, as usual), and hence an amount of charge $\Delta Q = 0$. From (5), this means that the DDPM modulator output has $n_{1,DDPM} = n_{0,DDPM}$, and hence an equal number of 1's and 0's. Accordingly, the DDPM modulator output is simply a square wave having 50% duty cycle, and its input must be constantly equal to 100…0 (i.e., the SAR input is equal to 1 for the first SAR iteration, and 0 for the following N-1 iterations). Such input digital value corresponds to the middle-point value $V_{LT} = V_{DD}/2$ of the dynamic range of V_{in} in Fig. 7, as expected for a current range centered around zero.

Interestingly, the above condition $V_{in} = V_{LT} = V_{DD}/2$ obtained at the end of the conversion under zero-current bias point is actually true at the end of any conversion, under any non-zero input current. This is because $I_{feedback}$ inherently converges to I_{in} at the last SAR iteration, as usual in any SAR conversion. To assure the condition $I_{feedback} = I_{in}$ at the end of any SAR conversion, *INV* invariably needs to inject an extra charge ΔQ to compensate the charge drawn by I_{in} during the $2^N T_{CLK}$ cycles of the last DDPM sequence at the N-th SAR iteration. ΔQ must make the average *INV* current in (5) equal to I_{in}, which immediately yields the following

condition on the ADC output OUT_{ADC}

$$OUT_{ADC} = OUT_{SAR} = 2^{N-1}\frac{I_{in}}{I_N} + 2^{N-1}. \quad (6)$$

through very similar derivations as in (5). From (6), the digital output of the architecture in Fig. 7 is equivalent to the static transfer characteristics of an ADC having a current input centered around $I_{in} = 0$, as its corresponding output is equal the middle point 2^{N-1} (i.e., $OUT_{ADC} = 100\ldots0$ expressed in binary). From (6) the lowest value of the dynamic range is $I_{in} = -I_N$ (corresponding to $OUT_{ADC} = 00\ldots0$), whereas the highest is $I_{in} = I_N$. From (6), the LSB is equal to $I_N/2^{N-1}$. In other words, the static transfer characteristics of the proposed current-input ADC is defined by the on-current I_N in *INV* in Fig. 7, and the bit width N of the SAR and the DDPM logic.

Regarding the effect of circuit non-idealities, the effect of the mismatch between I_P and I_N leads to a digital output different to the middle point $OUT_{ADC} = 100\ldots0$, when the input current is zero. Equivalently, an offset error is introduced since the two currents I_P and I_N do not compensate each other perfectly. In addition, the effective resolution is expectedly lower than the ideal value N, due to input-referred noise of the comparator and nonlinearity. Such effects are discussed in detail in the next section.

V. FULLY-SYNTHESIZABLE CURRENT-INPUT ADC: EXPERIMENTAL RESULTS

The current-input ADC architecture ADC-I described in Section IV was demonstrated with a 40nm CMOS testchip, as shown in Fig. 3. The logic is implemented in the form of standard cell-based buffer, inverter gate, SAR logic and DDPM modulator, as in Fig. 7. Again, these were synthesized, placed and routed automatically, occupying a silicon area of 1,225μm^2, not including the reconstruction filter for fair comparison with prior art. The filter capacitor C was again implemented via place&route scripting as in Section III. Based on ripple considerations as in Section IV, C was set to 10pF to allow operation at a clock frequency down to 27MHz under minimum-strength inverter gate *INV*. Being implemented as metal-oxide-metal capacitor (MOM) using the first four metal layers, the filter capacitor takes up a silicon area of 3,745μm^2. This area can be approximately halved when using the full 10-metal stack. Both the inverter *INV* and the buffer *BUF* standard cells in Fig. 7 are symmetrically sized and have minimum strength. From the comparison with prior art in Table 1, the overall ADC area of 4,970μm^2 is the lowest reported to date. This advantage is expected to be retained at technologies with smaller minimum feature size, considering that standard cells are more technology scaling-friendly than analog components. Similarly, finer technologies enjoy a similar MOM capacitor area reduction, due to the inherent increase in the wire capacitance per unit area. More quantitatively, the area of the proposed ADC-I is 39-111X smaller than other fully-synthesizable voltage-input ADC architectures [10], [11]. In addition, further savings are achieved thanks to the suppression of the area that would traditionally be required by the transresistance amplifier necessary under the adoption of a voltage-input ADC.

The ADC-I testchip was characterized at a temperature of 25°C, a 0.6-V supply, and 2.2-kHz sample rate. The measured power consumption is 0.94μW (10% is due to leakage), and is approximately the same regardless of whether constant or dynamic input waveforms are applied. From the static characterization detailed in Fig. 8, the measured dynamic range is 45.2dB. The maximum integral nonlinearity (INL) is ±1.5LSB at 8-bit nominal resolution, and its RMS value is 0.5 LSB. The maximum and RMS differential nonlinearity (DNL) are respectively ±1.9LSB and 0.3 LSB.

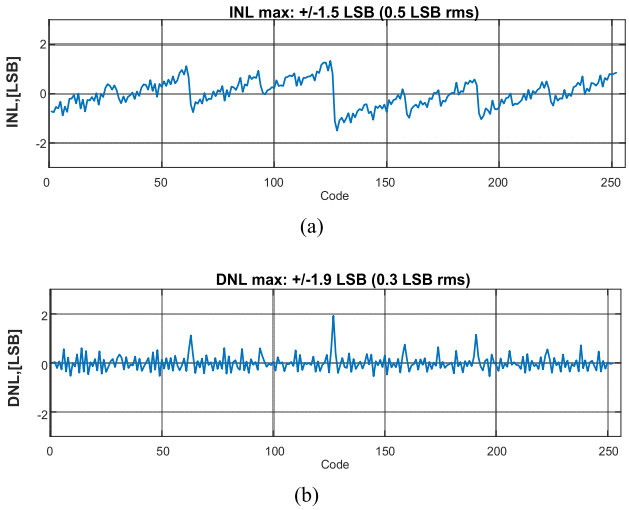

FIGURE 8. ADC static characterization: a) INL and b) DNL vs code.

The dynamic characterization of the ADC is presented in Fig. 9, based on a 30-Hz sine wave input with an amplitude equal to 90% of the ADC full-scale value. From this figure, the measured SNDR is 42.1dB, which is equivalent to 6.7-bit ENOB. As summarized in Table 1, the achieved resolution is better than state-of-the-art digital standard cell-based [10] and digital ADCs requiring customized circuits [4]. On the other hand, the resolution is 1.4-bit worse than the VCO-based ADC in [12], and 0.9-bit worse than the automatically synthesized SAR ADC in [16], which however require partially custom design. As expected, $\Delta\Sigma$ ADCs based on digital custom circuits outperform all other classes, although at the cost of increased design complexity and power. From Fig. 9a, the ADC SFDR (THD) performance is 51dB (54.7dB), which exceeds the SNR performance (42.2dB) and leads to 8 (9) equivalent bits. This suggests that the testchip effective resolution is mainly limited by the input noise, rather than its non-linearity. In turn, the input noise is mainly due to the contribution of the *BUF* voltage comparator in Fig. 7, as expectable from its minimum size.

As shown by Figs. 9b-c, the SNDR, SFDR and THD have consistent performance across input frequencies from DC to the Nyquist frequency. An 1dB/dB roll-off versus the input

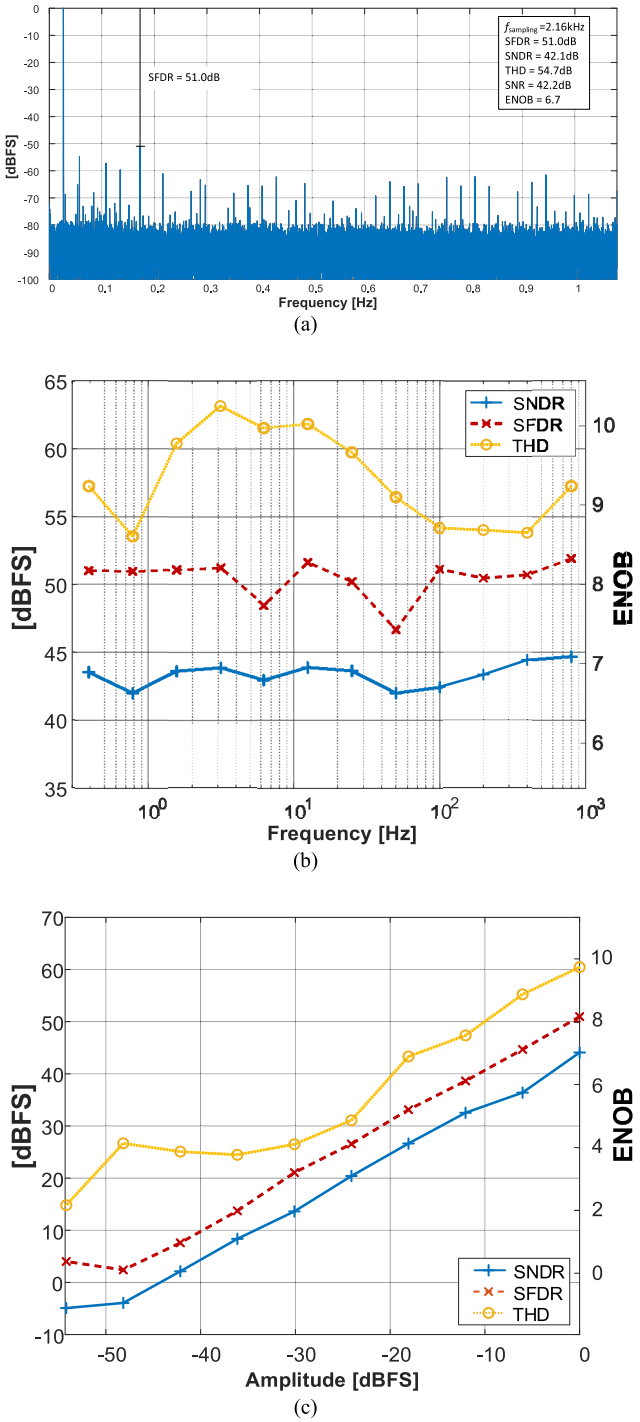

FIGURE 9. ADC dynamic characterization measurements: (a) output spectrum @ 30Hz sine wave input, (b) SNDR, SFDR and THD versus input sine wave input frequency, (c) SNDR, SFDR and THD versus sine wave input amplitude.

signal amplitude is observed from Fig. 9c. Such considerations still hold under the effect of process variations, as shown by their consistency across six measured dice in Fig. 10. Quantitatively, Fig. 10 shows that the maximum SNDR difference across dice is 8dB, leading to 1.3 ENOB change.

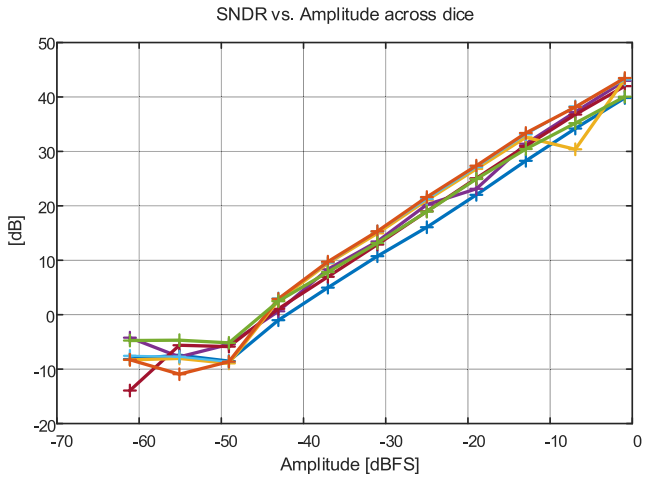

FIGURE 10. ADC dynamic characterization (SNDR) across six dice.

From the above considerations, the resolution of ADC-I can be readily enhanced through the adoption of a *BUF* standard cell having larger strength than minimum, so that its input-referred noise is reduced. This comes at insignificant design effort, and at the cost of slightly larger power consumption due to the increase in both the dynamic and leakage consumption. As further improvement, adopting an *INV* cell with larger size improves the matching of NMOS and PMOS transistors, thus reducing the offset due to the within-die variations as per the Pelgrom's law [1]. Further offset mitigation can be readily achieved through conventional digital PMOS/NMOS strength calibration, which can compensate both die-to-die and within-die variations.

Once larger *BUF* and *INV* strength is used, the ADC-I resolution is ultimately bounded by the limited small-signal voltage gain of the comparator *BUF* in Fig. 7, which limits its ability to discriminate small changes down to the LSB.

VI. CONCLUSION

In this paper, standard cell-based Nyquist-rate DDPM ADCs have been explored in terms of architectures, as well as in terms of their limits and potential for moderate resolutions. The proposed architectures exhibit the lowest area and the highest level of design automation (i.e., fully-automated standard cell design), as crucial in low-cost systems such as sensor nodes.

Based on the same principle leveraging a DDPM DAC, both voltage- and a current-input ADC architectures have been proposed. The ADC-V exhibits the minimum area of $1.87 \cdot 10^6$ F^2 reported to date, corresponding to only 5 kgates (including passives). Testchip measurements on a 40-nm testchip have shown operation at 2.8 kS/s with a power consumption of down to 3.1 μW at 0.6 V. Similarly, the ADC-I occupies a silicon area of only 4,970μm^2, corresponding to 10 kgates. The ADC-I also exhibits the highest resolution compared to prior fully-synthesizable ADCs, i.e. 6.7 bits (8 bits) in dynamic (static) conditions. Its operation at the maximum sample rate of 2.2kS/s leads to a power

consumption of 0.94 μW, which is the lowest reported and 100× less than [15]. The kHz-range sampling frequency of the proposed ADCs is lower than other fully-synthesizable ADCs, and is well suited for a wide range of voltage and current sensing applications (see Section IVA).

To the best of the authors' knowledge, this work reports the first demonstration of a truly fully-synthesizable current-input ADC. This enables direct current readout while suppressing the traditional need for an input transresistance amplifier. The elimination of its analog-intensive design effort and area allows to take full advantage of having a fully-synthesizable ADC, as opposed to sensor interfaces using conventional voltage-input ADCs.

Overall, the proposed class of ADCs is well suited for area- and design cost-sensitive applications, enabling the I [9]–[16] design of compact ADCs with very low area in the order of 10 kgates, and low design turnaround time within hours (including the integration with the digital sub-system). The proposed class of ADCs also exhibits the highest resolution reported to date in mostly- or fully-digital ADC architectures. The above characterization of the limitations of the testchip implementation offers directions to further push the envelope of the resolution of mostly- and fully-digital ADC architectures.

ACKNOWLEDGMENT

The authors would like to thank Gopalakrishnan Ponnusamy and Ayushparth Sharma for testing support.

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