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A Non-Isolated Step-up DC-AC Converter With Reduced Leakage Current for Grid-Connected Photovoltaic Systems

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ABSTRACT In this paper, a non-isolated step-up single-phase dc-ac converter is proposed for distributed low voltage photovoltaic (PV) systems. The proposed converter has a common ground between the dc photovoltaic input and ac output voltage, which can reduce the leakage current to a very low level and thus improve the reliability and power generation efficiency. By analyzing and comparing the two modulation methods, a unified half cycle modulation is selected for the design of the proposed converter, in which only two switches are operated at high frequency in a line cycle. Therefore, the conduction and switching loss can be reduced greatly. In addition, due to the unified half cycle modulation for the active switches of the proposed inverter, the dc-link capacitor does not need to have a decoupling function. The capacitor can then be optimized to a small value for improving the reliability and power density. A theoretical analysis of the proposed converter is described, and an experimental prototype is implemented to verify the performance of the presented converter topology.

INDEX TERMS Step up, dc-ac, common ground, photovoltaic system.

I. INTRODUCTION

Grid-connected dc-ac converters play an increasing important role in distributed photovolatic (PV) generation systems, in which the dc-ac converters are used to feed the PV power into the utility grid. It is important for the PV inverter to have high reliability, high efficiency and a small size. Usually, the topologies of PV inverters can be divided into two categories: namely transformer isolation PV inverters and transformerless PV inverters. From the safety point of view, most of PV inverters employ line frequency transformers or high frequency transformers to guarantee galvanic isolation between the grid and the PV system [1], [2]. However, the existence of line frequency transformer significantly increases the system size and weight. Although the PV inverters with high frequency transformers have the advantages of low cost and small size. However, these types of inverters with high-frequency transformers have several power stages, which increases the complexity of system.

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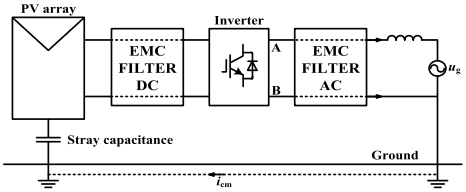

FIGURE 1. The leakage current path for the transformerless PV inverter.

As a result, the PV inverters without transformer are widely used in the low-power distributed PV generation, because of the advantages of simple structure, low cost, and high efficiency. However, when the transformer is omitted, the leakage currents i_{cm} may appear on the parasitic capacitor between the PV panels and the ground, as shown in Fig. 1. The existence of the leakage current may reduce the power conversion efficiency, increase the grid current distortion,

deteriorate the electric magnetic compatibility, and more importantly, give rise to the safety threats [3]–[5].

In order to suppress the leakage current, a lot of topologies have been proposed for transformerless PV inverters such as the H5, H6 inverter, the HERIC inverter, *etc.* [6]–[12]. In the H5 and H6 topologies, extra switches or diodes are embedded in the dc or ac side of the full bridge inverter, which can eliminate the leakage current by separating PV array away from the grid. In the HERIC inverter, a freewheeling branch is added between the bridge arm and the filter inductors for eliminating the leakage current. However, they are buck type inverters and their output peak ac voltage does not exceed the input dc voltage. Therefore, for applications in which the output peak ac voltage needs to be higher than the input dc voltage, an additional boost dc-dc converter is often required at the front end [13]. Single-stage Z-source inverters in [14]–[16] can realize higher ac output voltage than the dc input voltage by using an impedance network, but they cannot solve the problem of leakage current to ground.

In order to overcome the disadvantages of the aforementioned classic circuits, some new common-ground-type step-up PV inverters are proposed in recent literature works [17]–[22]. These topologies eliminate leakage current by connecting the negative terminal of the PV directly to the neutral point of the grid. However, they used more switches, which can result in higher conduction losses and a larger size.

Following this trend, this paper proposes a non-isolated dc-ac step-up converter with reduced leakage current for grid-connected PV systems, as shown in Fig. 2. The proposed converter connects the PV negative terminal to the neutral line of the utility grid directly, effectively suppressing the leakage current. The unipolar sinusoidal pulse width modulation (SPWM) or double frequency SPWM can be adopted to this converter. Moreover, the dc-link capacitor can be designed as small as possible so that thin film capacitor can be used.

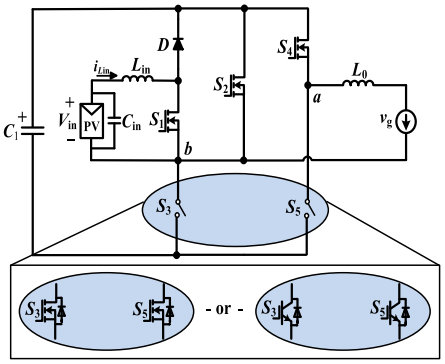

FIGURE 2. Proposed inverter structure.

II. CIRCUIT CONFIGURATION AND ANALYSIS

The proposed converter is mainly composed of five switches (S_1–S_5), a diode D, an energy storage inductor L_{in} at the input, a capacitor C_1, and a filter. Modulation schemes are presented in Section II-*A* and operating modes of the proposed converter, which is modulated with a unipolar SPWM, are described in Section II-*B*. Meanwhile, the voltage gain of the proposed converter and voltage and current stresses of all switches are discussed in Section II-*C* and Section II-*D*, respectively.

A. MODULATION SCHEME OF THE PROPOSED CONVERTER

In view of the characteristics of the proposed step-up dc-ac converter, a unified unipolar SPWM and a double-frequency SPWM methods are adopted to provide the control signals for all the active devices. The detailed analysis is introduced as follows.

1) UNIPOLAR SPWM

The waveform of the unipolar SPWM of the proposed inverter is displayed in Fig. 3. The gate drive signals for the power switches are generated by comparing a reference wave (u_r) of a line frequency to a carrier wave (u_c) at a high frequency.

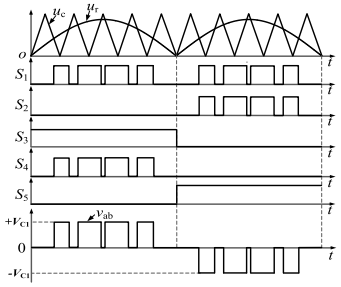

FIGURE 3. Unipolar SPWM for the proposed topology.

We can observe that switch S_1 is always operated at the high frequency. Switches S_2 and S_4 are also operated at the high frequency, but only for a half of the line cycle, respectively. Moreover, at the other half line cycle, switches S_2 and S_4 are turned off accordingly. Switch S_3 is kept on for the positive half line cycle while switch S_5 is on for the negative half line cycle.

As the description in Section II-*B*, the proposed topology has three operating modes in one switching cycle. In the positive half cycle of the line frequency, the converter is operated in modes 1, 2, and 3. In the negative half cycle of the line frequency, the converter is operated in modes 6, 7, and 8 repeatedly. When the switch or the diode is turned on, it is indicated by $S_X = 1$ or $D = 1$. When the switch or the diode is turned off, it is indicated by $S_X = 0$ or $D = 0$ ($x = 1 - 5$). The switching sequence of the unipolar SPWM scheme in one switching cycle is shown in Table 1.

TABLE 1. Switching sequence of unipolar SPWM.

	Operating mode	D	S_1	S_2	S_3	S_4	S_5
Positive half cycle	Mode 1	0	1	0	1	1	0
	Mode 2	1	0	0	1	0	0
	Mode 3	0	0	0	1	0	0
Negative half cycle	Mode 6	0	1	1	0	0	1
	Mode 7	1	0	0	0	0	1
	Mode 8	0	0	0	0	0	1

2) DOUBLE-FREQUENCY SPWM

The proposed topology can also work with double-frequency SPWM to achieve a higher equivalent switching frequency, as shown in Fig. 4. In the double-frequency SPWM, the five power switches are all working at the high switching frequency, and are modulated by two inverse sinusoidal waves, respectively. Switches S_4, S_5 are modulated by the reference wave u_{r1}, while switches S_2 and S_3 are modulated by the reference wave u_{r2}.

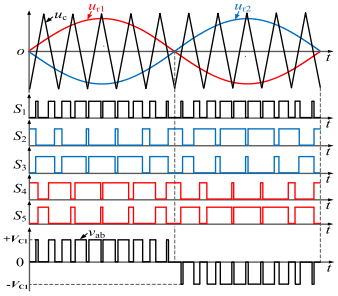

FIGURE 4. Double-frequency SPWM for the proposed topology.

During the positive half grid cycle, the circuit rotates in the sequence of "mode 1-mode 4-mode 1-mode 5" and the output voltage v_{ab} varies between $+V_{C1}$ and 0 with the twice of the carrier frequency. During the negative half grid cycle, the circuit rotates in the sequence of "mode 6-mode 9-mode 6-mode 10" and the output voltage v_{ab} varies between $-V_{C1}$ and 0. Similarly, the switching sequence of double-frequency SPWM scheme in one switching cycle is shown in Table 2.

TABLE 2. Switching sequence of double-frequency SPWM.

Operating mode		D	S_1	S_2	S_3	S_4	S_5
Positive half cycle	Mode 1	0	1	0	1	1	0
	Mode 4	1	0	0	1	0	1
	Mode 1	0	1	0	1	1	0
	Mode 5	1	0	1	0	1	0
Negative half cycle	Mode 6	0	1	1	0	0	1
	Mode 9	1	0	0	1	0	1
	Mode 6	0	1	1	0	0	1
	Mode 10	1	0	1	0	1	0

The aforementioned two modulation strategies both have their own advantages. The double-frequency SPWM can provide a higher equivalent switching frequency so that the size and weight of the filter inductor can be reduced. On the other hand, there are only two switches operated at the high frequency in a line cycle with the unipolar SPWM. Based on this concept, MOSFETs can be chosen for switches S_1, S_2, and S_4, which are working in a high frequency. Whereas, IGBTs can be chosen for switches S_3 and S_5, which are operated at power frequency. Hence, the higher efficiency can be achieved by this mixed switch technology [23]. In this paper, the unipolar SPWM is chosen as an example for the performance evaluation and experimental verification.

B. THE OPERATED MODE ANALYSIS

To simplify the inverter analysis, the assumptions are shown as follows:

(1) All semiconductor power devices are considered ideal.

(2) The capacitor C_1 is large enough to keep its voltage constant during one switching period.

(3) The current of inductor L_{in} is operated in discontinuous conduction mode (DCM).

For the unipolar SPWM method, there are three operating modes during one switching period in a positive or negative half cycle and the key waveforms of the proposed converter in DCM are shown in Fig. 5. The corresponding equivalent circuits are presented in Fig. 6.

In the whole positive half cycle of ac output, the switch S_3 maintains on and switches S_2, S_5 are always off. Switches S_1, S_4 are operated in SPWM. The corresponding operating modes are given as follows:

Mode 1 ($t_0 - t_1$) [Fig. 6.(a)]: Before this mode, the current i_{Lin} has dropped to zero at the input. At time t_0, the switch S_3 is turned on and keep on in the positive half cycle. Switches S_1 and S_4 are turned on, and the diode D are off. The inductor L_{in} is charged by the input voltage V_{in} and its current is linearly increased from zero to its maximum value. Meanwhile, the capacitor C_1 is discharged for the output and the inverter output voltage v_{ab} of inverter is V_{c1}. The current i_{Lin} can be described as:

$$i_{Lin}(t) = \frac{V_{in}}{L_{in}}(t - t_0) \tag{1}$$

Mode 2 ($t_1 - t_2$) [Fig. 6.(b)]: At time t_1, switches S_1 and S_4 are turned off and diode D is turned on. The inductor L_{in} is discharged to the output, and the current i_{Lin} is linearly decreased from the maximum to zero in this mode. At the same time, the anti-paralleled diode of switch S_5 is freewheeling to provide a current flowing path for the output current of inductor L_0. The expression of current i_{Lin} in this mode can be written:

$$i_{Lin}(t) = \frac{V_{in} - V_{C1}}{L_{in}}(t - t_1) + i_{Lin}(t_1) \tag{2}$$

Mode 3 ($t_2 - t_3$) [Fig. 6.(c)]: At time t_2, as the current i_{Lin} reduces to zero, diode D is turned off. The anti-paralleled diode of switch S_5 is still on to provide a current flowing path for output inductor L_0 current. This mode ends at time t_3. Then, modes 1, 2, and 3 occur cyclically until the negative half cycle of ac output.

$$i_{Lin}(t)=0 \tag{3}$$

In the whole negative half cycle of ac output, the switch S_5 maintains on and switches S_3, S_4 are always off. Switches S_1, S_2 are operated in SPWM. The corresponding operating modes are given as follows:

Mode 6 ($t_4 - t_5$) [Fig. 6.(f)]: Before time t_4, switch S_5 is turned on and the current i_{Lin} is zero. At time t_4, switches S_1 and S_2 are turned on, the switch S_5 maintains on. Whereas, switches S_3, S_4, and diode D are turned off. The inductor L_{in} is charged by the input voltage V_{in} and its current is linearly increased from zero to the maximum. Meanwhile, the capacitor C_1 is discharged to the output. In this mode,

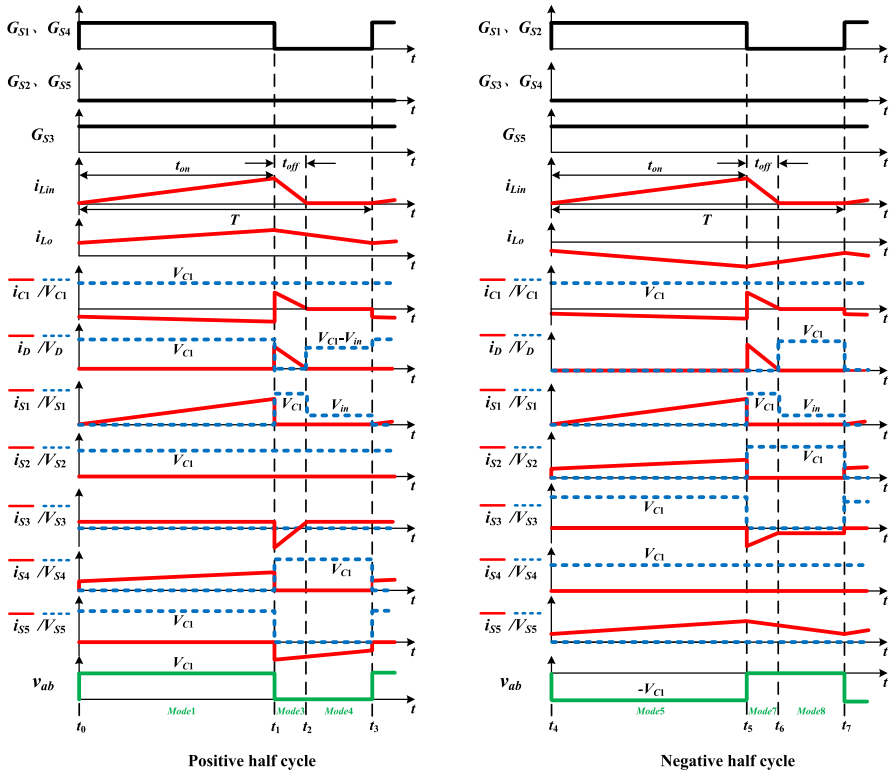

FIGURE 5. The key waveforms of the converter in DCM.

the input current i_{Lin} can be obtained as follows:

$$i_{Lin}(t) = \frac{V_{in}}{L_{in}}(t - t_4) \tag{4}$$

Mode 7 ($t_5 - t_6$) [Fig. 6.(g)]: At time t_5, switches S_1 and S_2 are turned off and diode D is turned on. The inductor L_{in} is discharged and the current i_{Lin} is linearly decreased from the maximum to zero. At the same time, the anti-paralleled diode of switch S_3 is freewheeling to provide a current flowing path for ac output current. In this mode, the equation of current i_{Lin} can be established as follows:

$$i_{Lin}(t) = \frac{V_{in} - V_{C1}}{L_{in}}(t - t_5) + i_{Lin}(t_5) \tag{5}$$

Mode 8($t_6 - t_7$) [Fig. 6.(h)]: At time t_6, the current i_{Lin} decreases to zero, and diode D is turned off. The anti-paralleled diode of switch S_3 is still on to provide a current flowing path for ac output current of the filter inductor L_0. This mode ends at time t_7. Then, modes 6, 7, and 8 are cyclically presented in the negative period of the sinusoidal modulation wave. In this stage, the current i_{Lin} is always zero.

$$i_{Lin}(t)=0 \tag{6}$$

C. VOLTAGE GAIN ANALYSIS

From the previous analysis, we can know that the inductor L_{in} is charged by the input voltage V_{in} and the current i_{Lin} is linearly increased from zero to its maximum. Then, inductor L_{in} is discharged to the output, and the current i_{Lin} is linearly decreased from the maximum to zero. From the flux (volt-second) balance condition on inductor L_{in}, the following relation is obtained:

$$V_{in}t_{on} = (V_{C1} - V_{in})\, t_{off} \Rightarrow t_{off} = \frac{V_{in}t_{on}}{V_{C1} - V_{in}} \tag{7}$$

According to the regular symmetry sampling rule, the conducting time of switch S_1 can be expressed as (8).

$$t_{on} = mT\,|\sin(wt)| \tag{8}$$

The average current i_{Lin} of the inductor in a modulation wave period T is as follows:

$$i_{Lin} = \frac{(t_{on} + t_{off})\,\Delta i}{2T} = \frac{(t_{on} + t_{off})\,\frac{V_{in}}{L_{in}}t_{on}}{2T} \tag{9}$$

To simplify the analysis, all devices losses in the circuit are neglected, so that the input power is equal to the output power P_o. Therefore, when the converter is assumed working in a unity power factor, the input average current I_{in} can be expressed as:

$$I_{in} = \frac{P_o}{V_{in}} = \frac{v_g^2}{V_{in}R} \tag{10}$$

Meanwhile, the output voltage v_g of the inverter can be approximately expressed as:

$$t_{on}V_{C1} = v_g T \Rightarrow v_g = \frac{t_{on}}{T}V_{C1} \tag{11}$$

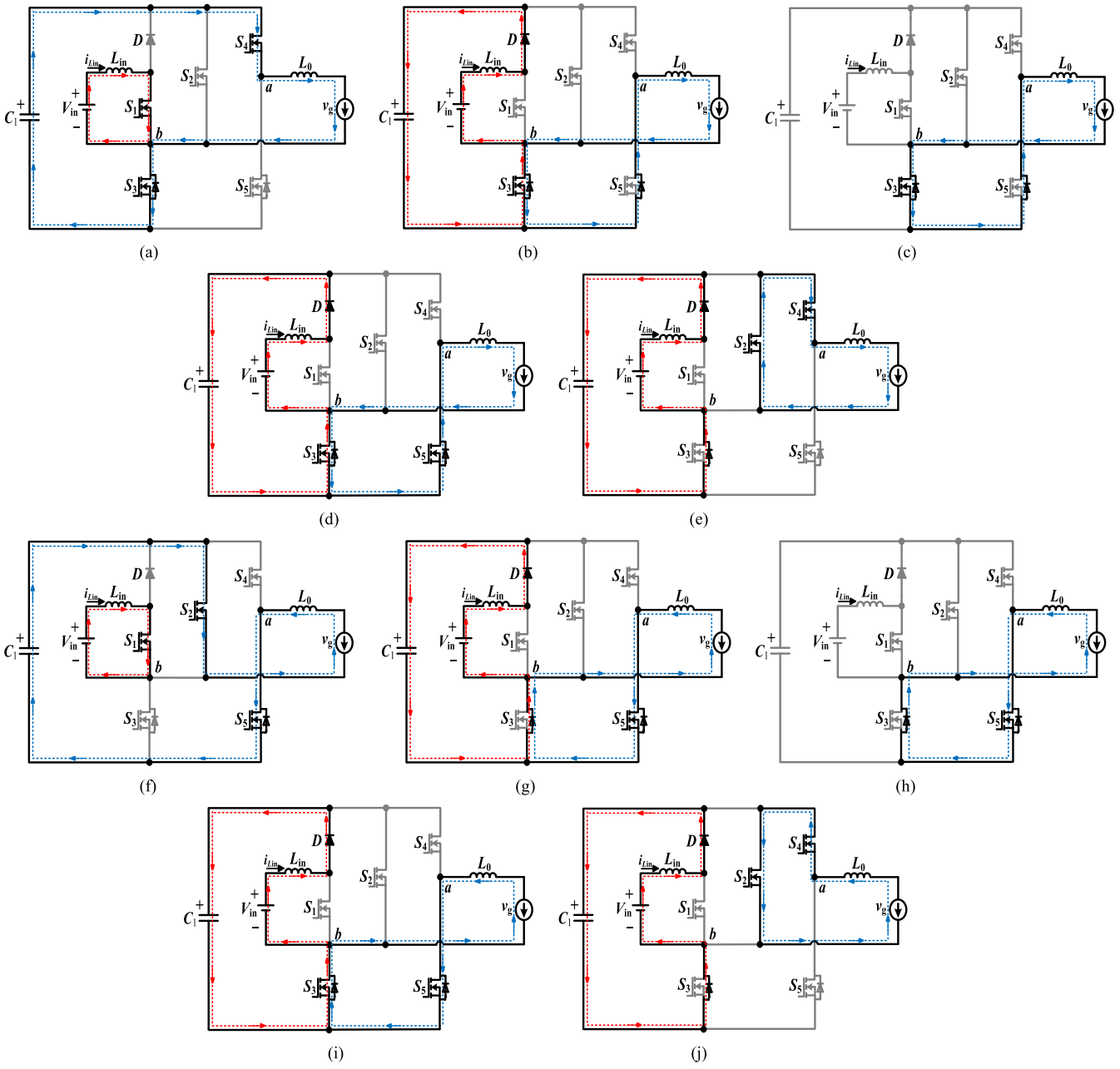

FIGURE 6. Equivalent circuit of each operating mode of the proposed converter: (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.(i) Mode 9. (j) Mode 10.

For this proposed converter, The average current i_{Lin} and the input average current I_{in} are equalized and the value of $sin(wt)$ is converted to effective value $\sqrt{2}/2$ to simplify the analysis, thus the voltage gain G is derived as:

$$G = \frac{v_g}{V_{in}} = \frac{\sqrt{2}m}{4}\left(1 + \sqrt{1 + \frac{2R}{L_{in}f}}\right) \tag{12}$$

Fig. 7 shows the three-dimensional relationships of voltage gain G versus input inductor L_{in} and modulation ratio m when $f = 20\text{kHz}$, $R = 50\Omega$ are given. From Fig. 7, we can see that the voltage gain G increases when the modulation ratio m increases or the value of L_{in} decreases.

D. THE VOLTAGE AND CURRENT STRESS OF SWITCHES

During the DCM operation, the voltage stresses on the switches S_1–S_5 and the diode D are derived as:

$$\begin{aligned} V_{S1\_max} &= V_{S2\_max} = V_{S3\_max} \\ &= V_{S4\_max} = V_{S5\_max} = V_{D\_max} = V_{C1} \end{aligned} \tag{13}$$

The average current i_{C1} is zero in the steady state. Thus, the average current that flows through switches S_2, S_4, and

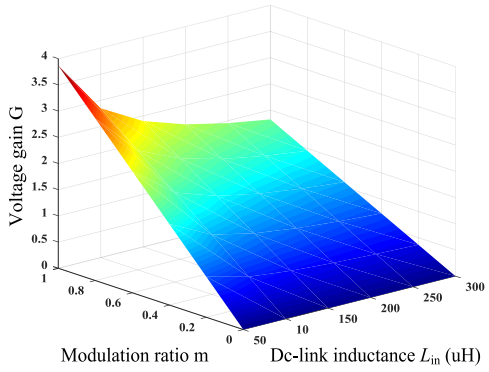

FIGURE 7. Diagram of voltage gain, modulation ratio m and input inductor value L_{in}.

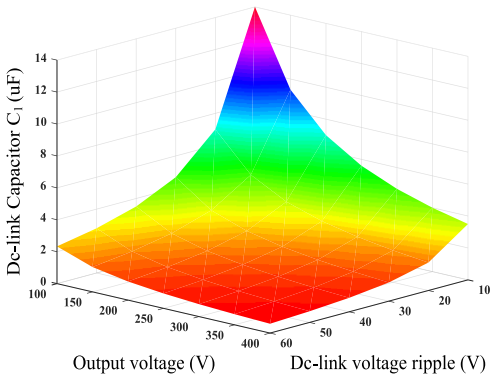

FIGURE 8. The capacitor value C_1 in relationship with voltage ripple ΔV_{C1} and output voltage V_g.

S_5 is nearly equal to the RMS of the current of I_g. The current stresses on switches $S_1 - -S_5$ and the diode D are expressed as follows:

$$i_{S2\_max} = i_{S4\_max} = i_{S5\_max} = i_{g\_max} \tag{14}$$

$$i_{S1\_max} = i_{D\_max} = \Delta i_{Lin\_max} \tag{15}$$

$$i_{S3\_max} = \Delta i_{Lin\_max} - i_{g\_max} \tag{16}$$

III. THE PARAMETER DESIGN OF PASSIVE COMPONENTS

A. THE SELECTION OF DC-LINK CAPACITOR C_1

During the operation of the converter, the capacitor is continuously charged or discharged with a different switching state. The capacitor charge change ΔQ can be written as (17), in which I_{C1} and ΔT represent the average current of the capacitor C_1 and the corresponding charging time or discharging time, respectively.

$$\Delta Q = C_1 \Delta V_{C1} = I_{C_1} \Delta T \tag{17}$$

The design of capacitor C_1 depends mainly on the following factors including the maximum transferring power P_o, the output voltage v_g, the operating frequency f, and the maximum tolerant voltage ripple ΔV_{C1}. In practice, the tradeoff is often considered. The estimated capacitor is obtained as:

$$C_1 \geq \frac{P_o}{v_g \Delta V_{C1} f} \tag{18}$$

When $P_o = 300\text{W}, f = 20\text{kHz}$, the relationship between the dc-link voltage ripple ΔV_{C1}, the grid voltage v_g, and the dc-link capacitor value C_1 is shown in Fig. 8.

In this paper, the RMS of ac output voltage is 110V, the voltage ripple ΔV_{C1} is designed as 40V. As a result, the minimum capacitor value is calculated to be $3.18uF$. In practice, a thin film capacitor with $4.7uF$ can be selected.

B. THE DESIGN OF ENERGY STORAGE NIDUCTOR L_{in}

When the proposed converter is operated under critical mode in steady state, the current i_{Lin} of the input inductor is exactly zero at the beginning or the end of each switching cycle. So, the following equation can be derived as:

$$I_{in} = \frac{1}{2} \Delta i_{Lin} \tag{19}$$

According to the operating principles and the formula (8), the current ripple on the energy storage inductor L_{in} can be derived as:

$$\Delta i_{Lin} = \frac{V_{in} t_{on}}{L_{in}} = \frac{mTV_{in} |sinwt|}{L_{in}} \tag{20}$$

Ignoring all the component losses in the circuit, then the input power is equal to the output power. Thus, there is the following formula:

$$I_{in} = \frac{P_o}{V_{in}} \tag{21}$$

According to formulas (19), (20), and (21) and the critical inductance is assumed to be L_c. Then, the value of critical inductor L_c can be derived as (22).

$$L_c = \frac{mV_{in}^2 |\sin(wt)|}{2P_o f} \tag{22}$$

In practice, the value of $|sin(wt)|$ changes in range of [0,1]. Therefore, if the value of inductor L_{in} is designed less than the value of L_c, the proposed converter will be operated in DCM. Therefore, the value of inductor L_{in} should be designed according to the formula (23).

$$L_{in} \leq L_c = \frac{mV_{in}^2}{2P_o f} \tag{23}$$

As a result, the energy storage inductor selection range based on (23) can be derived as $[0, mV_{in}^2/(2P_o f)]$. Ripple in the inductor current will be high if a small value of L_1 is chosen but transient response will be better. Thus, there is a trade-off in choosing the value of L_1. Based on simulation and experiment studies, the value of L_1 is finalized.

C. DESIGN OF INPUT CAPACITOR C_{in}

The input capacitor C_{in} is designed to minimize the peak to peak input voltage ripple (ΔV_{in}) due to the double frequency

component. For the rated power P and the frequency of output voltage f_s, the value of C_{in} is obtained as:

$$C_{in} = \frac{P_o}{2\pi f_s V_{in} \Delta V_{in}} \tag{24}$$

D. DEVICES LOSS CALCULATION

The losses of semiconductor devices include conduction loss of MOSFETs, loss of diodes, switching loss of MOSFETs.

The voltage drop of MOSFETs can be shown in (25), in which R_{ds} is the resistance of switches $S_1 - S_5$.

$$v_{ds} = i_{ds} \times R_{ds} \tag{25}$$

For a PWM cycle, the conduction time of switch S_1 and the current i_{ds} are given by

$$t_{on} = mT \sin wt \tag{26}$$

$$i_{ds} = I_{ds} \sin wt \tag{27}$$

1) CONDUCTION LOSS OF SWITCHES

For the positive half cycle, the conduction loss on high frequency switches S_1 and S_4, and line frequency switch S_3 are expressed as (28) and (29).

$$\begin{aligned} P_{S1} = P_{S4} &= \frac{1}{\pi T}\int_0^{\pi} i_{ds}(t) v_{ds}(t)\, t_{on} d(wt) \\ &= \frac{1}{\pi}\int_0^{\pi} I_{ds}^2 R_{ds} m \sin^3(wt)\, d(wt) = \frac{4m}{3\pi} I_{ds}^2 R_{ds} \end{aligned} \tag{28}$$

$$\begin{aligned} P_{S3} &= \frac{1}{\pi T}\int_0^{\pi} i_{ds}(t) v_{ds}(t)\, Td(wt) \\ &= \frac{1}{\pi}\int_0^{\pi} I_{ds}^2 R_{ds} \sin^2(wt)\, d(wt) = \frac{1}{2} I_{ds}^2 R_{ds} \end{aligned} \tag{29}$$

Similarly, the conduction loss on high frequency switches S_1 and S_2, and line frequency switch S_5 can be calculated in the negative half cycle as follows.

$$\begin{aligned} P_{S1} = P_{S2} &= \frac{1}{\pi T}\int_0^{\pi} i_{ds}(t) v_{ds}(t)\, t_{on} d(wt) \\ &= \frac{1}{\pi}\int_0^{\pi} I_{ds}^2 R_{ds} m \sin^3(wt)\, d(wt) = \frac{4m}{3\pi} I_{ds}^2 R_{ds} \end{aligned} \tag{30}$$

$$P_{S5} = \frac{1}{\pi}\int_0^{\pi} I_{ds}^2 R_{ds} \sin^2(wt) d(wt) = \frac{1}{2} I_{ds}^2 R_{ds} \tag{31}$$

Therefore, the total conduction loss of allswitches is given in (32).

$$P_{con} = P_{S1} + P_{S2} + P_{S3} + P_{S4} + P_{S5} = \left(1 + \frac{16m}{3\pi}\right) I_{ds}^2 R_{ds} \tag{32}$$

2) CONDUCTION LOSS OF DIODES

The voltage drop of diode D can be simplified as a channel resistor that is shown in (33), in which the current i_d is expressed as (34).

$$v_d = i_d \times R_d \tag{33}$$

$$i_d = I_d \sin wt \tag{34}$$

For a PWM cycle, the conduction loss of diodes P_D is calculated as:

$$\begin{aligned} P_D &= 2 \times \frac{1}{\pi T}\int_0^{\pi} i_d(t) v_d(t) (T - t_{on})\, d(wt) \\ &= \frac{2}{\pi}\int_0^{\pi} i_d(t) v_d(t) [1 - m \sin(wt)]\, d(wt) \\ &= \left(1 - \frac{8m}{3\pi}\right) I_d^2 R_{ds} \end{aligned} \tag{35}$$

3) SWITCHING LOSS OF SWITCHES

The switching losses of high-frequency switches S_1, S_2, S_4 are the voltage and current overlap losses, which can be estimated through the formula(36).

$$\begin{aligned} P_{wS1} &= 2P_{wS2} = 2P_{wS4} \\ &= f_s \int_{t_{on}}^{t_{on}+t_r} v_{ds} i_{ds} dt + f_s \int_{t_{off}}^{t_{off}+t_f} v_{ds} i_{ds} dt = \frac{1}{2} f_s V_{ds} I_{ds} (t_r + t_f) \end{aligned} \tag{36}$$

where f_s is the switching frequency of converter, t_r is the current rise time when the switches is on, and t_f is the current fall time when the switches is off. Therefore, the total switching loss P_{wcon} is shown as:

$$P_{wcon} = P_{wS1} + P_{wS2} + P_{wS4} = f_s V_{ds} I_{ds} (t_r + t_f) \tag{37}$$

The histogram of power losses distribution under different power levels is shown in the Fig. 9.

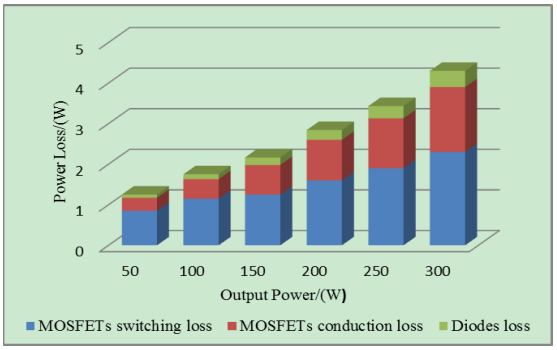

FIGURE 9. The histogram of loss distribution under different power levels.

E. THE PERFORMANCE COMPARISON

The performance comparison between the representative structures and the proposed inverter is shown in Table 3.

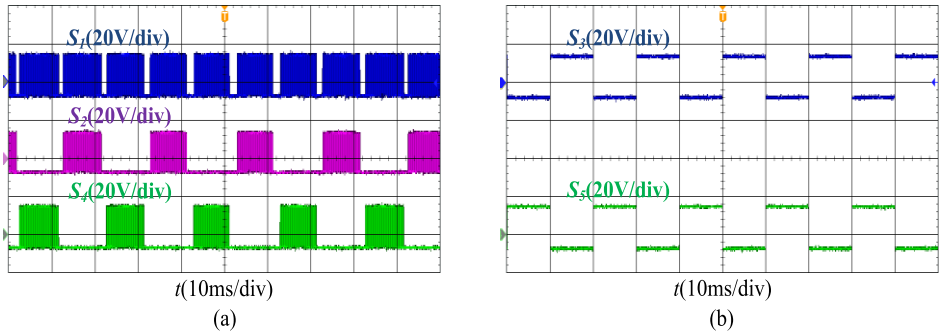

FIGURE 10. Experimental waveforms of the proposed converter (a) Driving waveforms of the switches S_1, S_2, S_4. (b) Driving waveforms of the switches S_3, S_5.

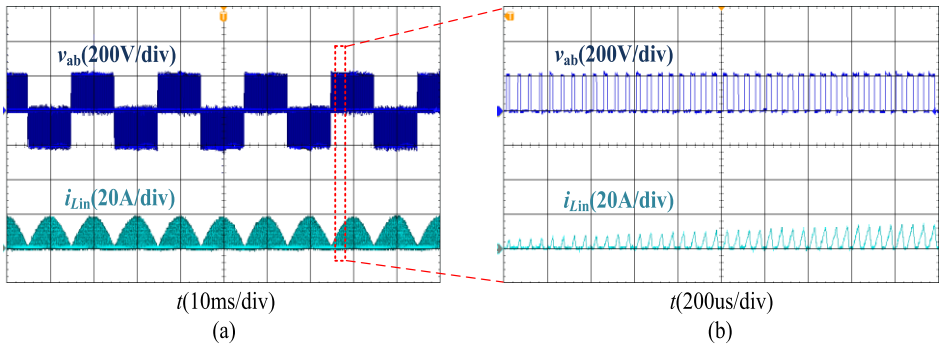

FIGURE 11. Experimental waveforms of the proposed converter (a) The voltage v_{ab} and the currents i_{Lin}. (b) Zoomed-in waveform of (a).

TABLE 3. Comparison of the proposed converter.

converter	Semiconductors		Passive elements		Other characteristics		
	Switches	Diodes	Capacitors	Inductors	Gain	Leakage current	Efficiency
H5 inverter[6]	5	0	1	2	<1	Large	High, 98%
HERIC inverter[7]	6	1	1	2	<1	Large	Good, 97%
H6 inverter with dc bypass[8]	6	0	1	2	<1	Large	Good, 97%
H6 inverter with ac bypass[10]	6	2	1	2	<1	Large	Good, 97%
Two-stage inverter[13]	6	0	1	3	>1	Large	Low, 90%
Literature[17]	9	0	3	1	>1	Low	Good, 96%
Literature[18]	4	1	1	4	>1	Low	Good, 97%
Literature[19]	6	2	2	2	>1	Low	Good, 96%
Proposed	5	1	1	2	>1	Low	Good, 96%

From Table 3, I observe that the HERIC and H6 inverter have more switches than the proposed inverter and do not have the boosting capability. Despite the literature [6] has fewer power devices than the proposal, the extra stage to boost the input voltage also is not considered. If this extra stage is needed, more components will be required.

A two-stage inverter is proposed in [13], in which a boost dc-dc converter is cascaded with a dc-ac inverter. This topology provides the required boosting gain but also offers the large leakage current and low efficiency. The converters reported in [17]–[19] can achieve voltage boosting and reduce the leakage current. However, the number of power devices and passive elements is large, which increases the overall system size and cost.

In conclusion, the proposed topology represents an excellent choice in order to provide the voltage boosting capability, a low leakage current with good efficiency and fewer components.

IV. EXPERIMENTAL RESULTS

A prototype converter is built to verify the effectiveness of the proposed topology. The special parameters are shown in Table 4.

TABLE 4. Electrical specifications of the proposed converter.

Input voltage	50Vdc
Output voltage	110Vrms/50Hz
Output power	300W
Switching frequency	20kHz
MOSFET	IXFK64N50P
Diode(D)	DSE160-06A
Inductance(L)	0.1mH
Inductance(L_0)	3mH
Capacitance(C_1)	4.7μF/250V

Figs 10, 11, and 12 show the experimental results for the proposed topology. Fig. 10 presents the driving waveforms of switches S_1, S_2, S_3, S_4, and S_5. From Fig. 10.(a), one can see that only switch S_1 is always operated at the high frequency.

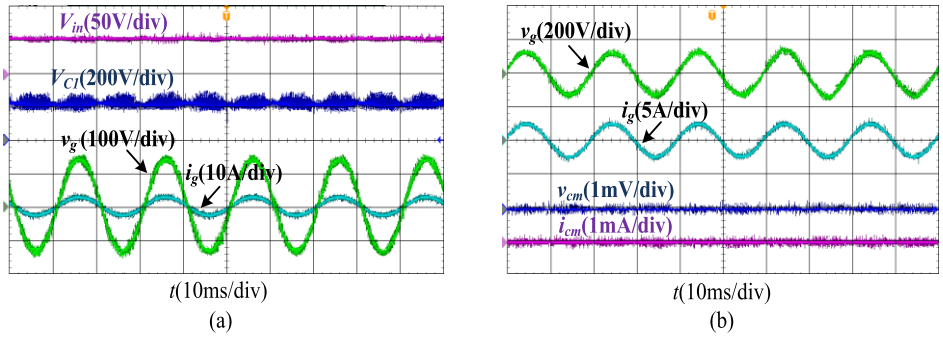

FIGURE 12. Experimental waveforms of the proposed converter (a) The capacitor voltage V_{C1}, the input voltage V_{in} and the output voltage v_g. (b) The output voltage v_g, the current i_g, the common-mode voltage v_{cm} and the common-mode current i_{cm}.

Switch S_2 or S_4 works at the high frequency in half of the ac output. From Fig. 10.(b), the switches S_3 and S_5 are operated with low frequency in half line cycle.

Fig. 11 presents the output voltage v_{ab} of the inverter bridge and the input current i_{Lin}. We can observe that the output voltage v_{ab} has a symmetrical characteristic and the current of L_{in} is also in a symmetrical waveform, which clearly shows the inductor L_{in} works in the DCM from the extended waveforms of Fig. 11.(b). Fig. 12.(a) presents the capacitor voltage V_{C1}, the input voltage V_{in} and the ac voltage v_g after the filter. Assuming the parasitic capacitor is $5nF$, Fig. 12. (b) provides the experimental results including the waveforms of ac voltage v_g, the output current i_g, the common-mode voltage v_{cm}, and the common-mode current i_{cm}. Because of the inherent characteristics of the proposed inverter, the leakage current i_{cm} is nearly zero. These experimental results validate the theoretical analysis of the proposed circuit structure.

In the experiment, the PV arrays simulator power is used to replace the real PV arrays, and the high speed processor TMS320F2812 is used as the core control device. The picture of the experimental setup is shown in Fig.13.

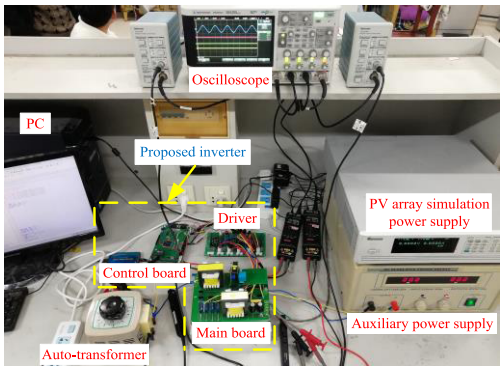

FIGURE 13. Experimental prototype developed for the proposed topology.

In terms of PV generation applications, the output voltage from PV panels often varies greatly due to different environmental conditions. When the input voltage ranges from 50 to 60 V, the measured efficiency curves versus the different output power are shown in Fig. 14. We can observe that the proposed topology can achieve high efficiency in the whole range of PV voltage variation.

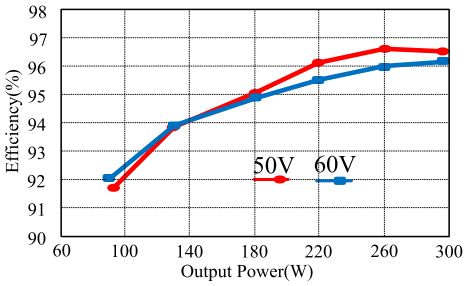

FIGURE 14. Measured efficiency of the proposed topology.

V. CONCLUSION

This paper proposed a single-stage step-up dc/ac converter without transformer and leakage current for distributed PV power generation systems. The proposed inverter is developed from embedding a boost dc-dc unit into a conventional full bridge inverter. A simple unipolar SPWM strategy for the driving signals of all the active switches has been presented and discussed in detail. The greatest advantage of the proposed PV generation system is that the neutral line of the ac output is directly connected to the negative terminal of the input PV array, eliminating the ground leakage current.

In addition, the input inductor current is designed in DCM, which guarantees that the low frequency input current ripples can meet the requirements. The operation principle and steady analysis are introduced in detail and verified by the experiments.

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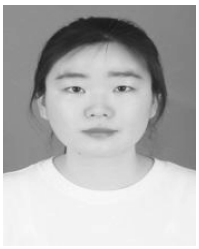

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