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A Blended Improved H5 Topology With ILQG Controller to Augment the Performance of Microgrid System for Grid-Connected Operations

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ABSTRACT The development of the world demands on the progress of electricity operation and quality enhancement. Microgrid (MG) is a solution that manages the additional need of electricity. The MG generates electricity mostly from renewable energy sources, e.g. solar, wind and hydro. Most renewable energy sources require energy storage system as they are highly unpredictable in nature. An inverter is needed to convert that stored DC power to AC. The presence of a capacitor within the grid provides a galvanic connection that varies the common mode (CM) voltage of the inverter. Thus, the leakage current as well as the total harmonic distortion (THD) of the grid voltage and current increases. The increase of the leakage current hampers the safe operation of the MG. Now-a-days transformerless inverter is gaining more attention because of high efficiency, low cost, less weight and the capability of eliminating the high frequency component from the inverter CM voltage. In addition, a controller inclusion with a transformerless inverter can maintain a near-seamless performance. This paper proposes a blended technique of an improved H5 topology with an Integral Linear Quadratic Gaussian (ILQG) controller for grid-connected MG operations, that reduces the inverter leakage current by keeping the CM voltage constant. Thus it has the capability to reduce the THD of voltage and current. A comparative analysis has been carried out between this technique and existing topologies with different modulation techniques that helps to find out the most optimum inverter package to eliminate the leakage current and reduce the THD of grid voltage and grid current to almost zero.

INDEX TERMS Microgrid, transformerless inverter, improved H5 inverter, ILQG controller.

I. INTRODUCTION

The revolution of the modern world is accelerating the uses of the natural assets such as fossil fuels, coil, gas and oil to produce electricity. The large use of these natural assets is responsible for producing greenhouse gas that adversely affects the environment such as global warming [1], [2]. The researchers are motivated to innovate a new approach to overcome these problems and provide a safe and clean process to produce power to fulfill the demand of the world. Microgrid (MG) is one of the most promising solutions that has less adverse affect on the environment due to the use of clean resources to produce electricity [3], [4].

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The need of MG in the present world is increasing day-by-day due to its higher stability, sustainability and reliability. It has the ability to produce electricity from the renewable energy sources with or without the connection of the main grid. The frequency and voltage of the grid connected MG are completely controlled by main grid [5], [6]. The grid connected mode is more reliable and reduce the energy losses.

Distribution generation (DG) unit, voltage source inverter (VSI), filter, storage system, voltage distribution system, point of common coupling (PCC) and loads are the key elements of a MG [7]. Fig. 1 shows a simple MG scheme, which is commonly used in grid connected system. Renewable energy sources such as, wind, solar system, biomass, water, biogas, geothermal etc. are used as DG unit of the MG to produce electricity. These sources are widely

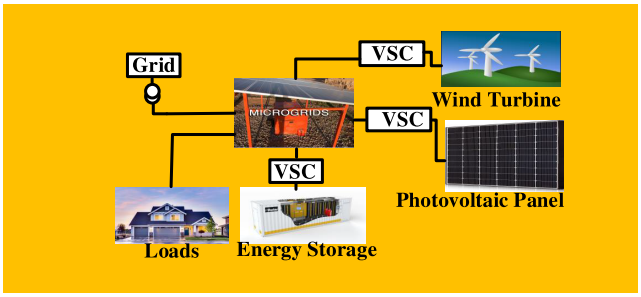


FIGURE 1. Illustration of MG scheme.

used in transportation, power generation and heating. The future world will mostly depend on these sources to fulfill their demand of electricity due to the lack of fossil fuels. At present, it is seen that, people are interested in making their own farms such as, wind farm, solar farm and biomass farm to produce electricity for their own purpose and supply the surplus electricity to the grid [8], [9].

The MG can be connected or disconnected with/from the main grid by switching the PCC. During the large disturbance, the MG is disconnected from the main grid through PCC and allow to operate independently. The VSI is the key element that converts the DC power which is stored in the energy storage system to AC whose operation is quite challenging [10], [11]. These inverters are built with or without transformer. An inverter with transformer consists of galvanic isolation that acts as voltage boosters which provides the galvanic isolation safety during the operation of the MG [12], [13]. Moreover the leakage current is reduced by omitting the continuous current flow between the DG units and the ground. But the line frequency transformers are bulky in size, expensive and costly due to their low frequency nature. On the other side, the high frequency transformer introduces large harmonic and extra losses [14], [15].

Transformerless inverter is a solution to overcome these problems. These inverters are low cost, smaller in size and less weight. But when a galvanic connection between the grid side and DC side is made, a common mode (CM) voltage exists which generates leakage current [16], [17]. This leakage current flows through an unwanted capacitance named parasitic capacitance formed between the DC source and the ground. Additionally, power loss, electromagnetic interference, the THD of the grid voltage and current will be increased. This reduces the stability of the system by making the operation unsafe due to the presence of external disturbances and the leakage current [18], [19].

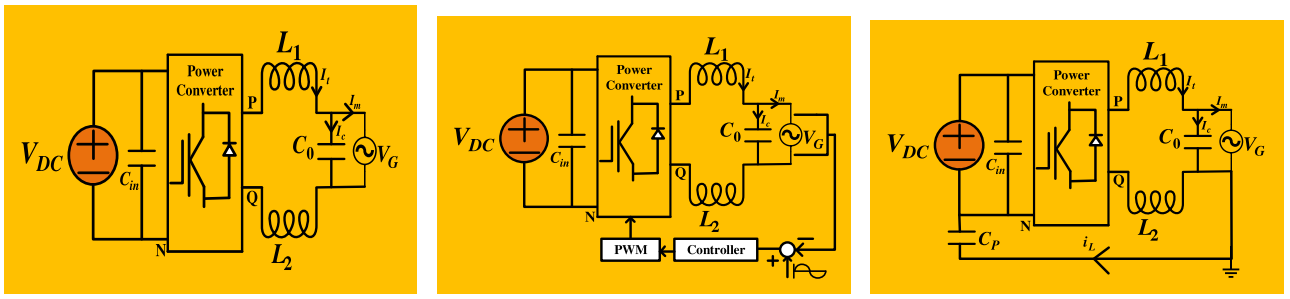
The elimination of the leakage current and the variation of the CM voltage of the inverter are the challenges to the researchers. Conventional full-bridge inverter has been proposed using bipolar modulation technique to eliminate the leakage current [20]. The requirement of two-level bipolar output voltage increases the inductor voltage stress by rising the switching losses, thus the current ripple is increased. However, conversion efficiency is reduced due to the presence of reverse power of these inverters [21], [22]. This problem has been solved by inserting a large filter inductor, but it increases the cost and makes the system bulky. Reference [19] has developed a full-bridge inverter that improves the efficiency of the system but the continuous injection of the leakage current can not be solved.

A lot of galvanic isolation topologies such as H5 [15], H6 family [23], highly efficient and reliable inverter concept (HERIC) family [24] have been presented to reduce the leakage current for transformerless inverter by introducing a clamping circuit within the system or separating the sources from the grid. The modification of the half-bridge with an extra switch is known as H5 topology [25].

The HERIC family is another reliable topology that has been proposed to reduce the leakage current of the inverter with two insulated gate bipolar transistors (IGBTs) as a bypass path in the AC side. It minimizes electromagnetic inference of the system. But the requirement of the additional switches makes the system costly. The HERIC family consists of a class of inverters, such as, HERIC-I [24], HERIC-I-PNPC [16], HERIC-II [26], HERIC-III [27], HERIC-IV [28], HERIC-V [20], HERIC-V-PNPC [29]. These topologies suffer due to higher conduction and switching losses.

The H6 family is another improved inverter group that reduces the fluctuation of CM voltage. This group consists of H6 [30], H6-PNPC [31], H6-ANPC [32] and improved H6 [33]. But the presence of the transistor junction capacitance increases the leakage current of these inverters.

This paper proposes the combined approach of an improved H5 topology [34] with an Integral Linear Quadratic Gaussian (ILQG) controller to reduce the leakage current by making the variation of the CM voltage constant in different modes of operation. This proposed technique is also able to reduce the THD of the grid voltage and current to a negligible number. A clamping circuit with two capacitors, five switches and one clamping diode are added to construct this H5 topology. The performance of the proposed blended technique has been investigated with different modulation techniques such as third harmonic injection PWM (THI PWM), bipolar PWM, unipolar PWM and third harmonic injected equal loading ninety degree clamped PWM (THIELNDC PWM). A detailed analysis of different topologies such as H5, HERIC and H6 family with ILQG controller have been investigated in this paper and their performances are compared with the proposed technique. This comparison ensures the reliability and high performance of the proposed technique against different modulation techniques. Here, an ILQG controller has been designed to control the gate signal of the transformerless inverter to reduce the THD of the grid voltage and current. This control algorithm has been designed based on the Linear Quadratic Gaussian (LQG) controller with integral action that can efficiently track the reference signal to produce the gate signal for the inverters. Performances are carried out in terms of leakage current, the CM voltage and the THD and it is shown that the proposed blended



(a) (b) (c)

FIGURE 2. Circuit diagram of (a) Open-loop, (b) Closed-loop grid connected microgrid and (c) leakage current path.

technique provides excellent performance for transformerless grid-connected MG application.

II. MICROGRID MODELLING

The basic block diagrams of open and closed-loop grid connected MG are presented in Fig. 2(a) and Fig. 2(b) respectively. The function of the LCL filter is to stabilize the grid connected inverter voltage and eliminate the high frequency produced by switching ripple. The voltage across the inductor can be represented as [35], [36],

$$V_t = L_t \frac{dI_t}{dt} \tag{1}$$

where, $L_t = L_1 + L_2$. Then, the derivative of the current through the inductor can be given as,

$$\frac{dI_t}{dt} = \frac{V_t}{L_t} \tag{2}$$

Again, the inductor voltage is the phasor sum of the inverter switching voltage V_s and the grid voltage V_G, i.e. $V_t = V_s - V_G$. It is worth mentioning that, V_s is the product of duty ratio (α) of the VSI and the V_{DC}, i.e. $V_s = \alpha \times V_{DC}$. Then, the laplace transform of "(2)" can be presented as,

$$sI_t(s) = \frac{V_t(s)}{L_t} = \frac{V_s(s) - V_G(s)}{L_t}$$
$$I_t(s) = \frac{V_s(s) - V_G(s)}{sL_t} \tag{3}$$

The current through the capacitor is given by,

$$I_c = C_0 \frac{dV_G}{dt} \tag{4}$$

Then, voltage across the capacitor i.e. grid voltage V_G can be presented as,

$$\frac{dV_G}{dt} = \frac{I_c}{C_0} \tag{5}$$

The capacitor current is the phasor sum of the inductor current I_t and grid current I_m, i.e. $I_c = I_t - I_m$. Then "(5)" can be represented as,

$$\frac{dV_G}{dt} = \frac{[I_t - I_m]}{C_0} \tag{6}$$

TABLE 1. Parameter selection for microgrid with transformerless inverter.

Parameter	Symbol	Value
Source Voltage	V_{dc}	$300V$
Grid Voltage	V_G	$220V$
Input Capacitor	C_{in}	$940\mu F$
Filter Inductor	L_1 and L_2	$0.8mH$
Filter Capacitor	C_0	$0.15\mu F$
Parasitic Capacitor	C_p	$75nF$
Switching Frequency	f_{sw}	$20kHz$

Applying the laplace transform, "(6)" can be written as,

$$sV_G(s) = \frac{[I_t(s) - I_m(s)]}{C_0}$$
$$V_G(s) = \frac{[I_t(s) - I_m(s)]}{sC_0} \tag{7}$$

The representation of any linear system can be done as,

$$\dot{x} = Ax + Bu$$
$$y = Cx + Du \tag{8}$$

where, A, B, C and D are the system, input, output and transition matrices of the plant respectively with state x, input u and output y. Then the state space of grid connected MG from "(2)" and "(6)" can be presented as,

$$\frac{d}{dt}\begin{bmatrix} I_t(s) \\ V_G(s) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_t} \\ \frac{1}{C_0} & 0 \end{bmatrix}\begin{bmatrix} I_t(s) \\ V_G(s) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_t} \\ 0 \end{bmatrix}[V_s(s)] + \begin{bmatrix} 0 \\ -\frac{1}{C_0} \end{bmatrix}[I_m(s)] \tag{9}$$

$$y = [V_G(s)] = [0\ 1]\begin{bmatrix} I_t(s) \\ V_G(s) \end{bmatrix} \tag{10}$$

The parameter values are listed in Table 1.

III. MODULATION TECHNIQUES

A proper modulation technique is required to produce the gate pulse of the inverter to reduce the THD of the system. Different PWM techniques have been proposed to produce the gate pulse of the inverter such, bipolar PWM [37], unipolar PWM [38], third harmonic injection PWM (THI PWM) [39] and third harmonic injected equal loading ninety degree clamped PWM (THIELNDC PWM) [40].

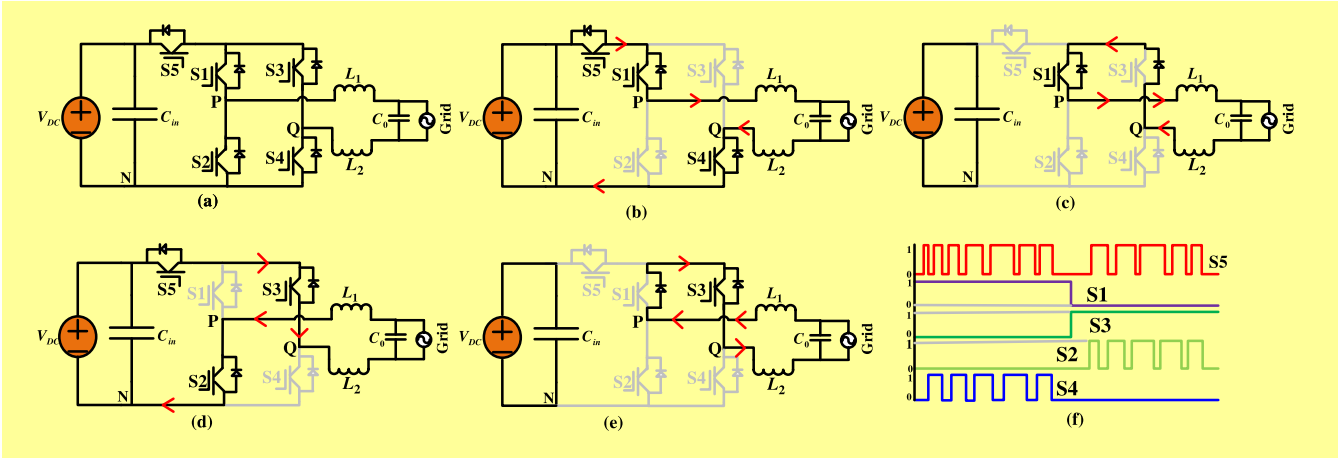


FIGURE 3. Operating modes of H5 topology.

The bipolar PWM technique uses a sinusoidal signal which is compared with the carrier having high frequency to control the on/off states of the inverter. A large amplitude of the reference signal as compared to the carrier turns on the inverter switches and produces gate pulse. The inverter switches are turned off when the reference signal becomes lower than the carrier [38], [41]. On the other hand, unipolar PWM uses two sinusoidal signals whose phase shift is 180°, but the magnitude and the frequency of those sinusoidal signals are kept same [41].

The reference signal is combined with high frequency sinusoidal signal in THI PWM technique. The carrier frequency is used to find the pulse number where the pulse width is calculated by the magnitude of the reference signal. This technique inserts a third harmonic signal to the modulation signal that reduces the THD of the voltage [42]. The THIELNDC PWM is a technique that not only reduces the switching losses and THD but also increases the lifetime of the inverter. The modulation signal is combined with the third harmonic signal having amplitude of 1/6 times larger than the modulation signal which is shifted by 180° [40].

IV. LEAKAGE CURRENT PROBLEM ANALYSIS OF TRANSFORMERLESS INVERTER

A resonant circuit is formed when transformer is removed from the inverter. This resonant circuit is formed with parasitic capacitor (C_P), filter inductors (L_1 and L_2) and output capacitor (C_0) as shown in Fig. 2(c). Here, the inverter is represented by power converter block where terminal P and Q are connected to the grid side through filter inductors. The leakage current is thus the function of grid voltage(V_G), parasitic capacitance (C_P), V_{PN}, V_{QN} and filter inductances and capacitance, where, V_{PN} is the voltage between the points P and N, and V_{QN} is the voltage between the points Q and N. Thus, The differential mode (DM) voltage, V_{PQ} can be represented as [43],

$$V_{PQ} = V_{PN} - V_{QN} \tag{11}$$

and the CM voltage is,

$$V_{CM} = 0.5(V_{PN} + V_{QN}) \tag{12}$$

The leakage current largely affects the V_{PQ} voltage that produces additional CM voltage which is given by [34],

$$V_{CM-PQ} = 0.5(V_{PN} + V_{QN}) \times \frac{L_1 - L_2}{L_1 + L_2} \tag{13}$$

Then the total CM voltage can be represented as,

$$V_{CM-all} = V_{CM} + V_{CM-PQ} = 0.5(V_{PN} + V_{QN}) + 0.5(VPN + VQN) \times \frac{L_1 - L_2}{L_1 + L_2} \tag{14}$$

Now, the representation of the leakage current is,

$$i_L = C_p \frac{dV_{CM-all}}{dt} \tag{15}$$

It is clear from "(15)" the leakage current will be zero for a constant V_{CM-all}. If $L_1 = L_2$, "(13)" gives $V_{CM-PQ} = 0$ and "(14)" indicates $V_{CM-all} = V_{CM}$. Any little fluctuation of this CM voltage may result leakage current.

V. EXISTING TRANSFORMERLESS INVERTER STRUCTURE

The circuit structure of existing topologies such as H5, HERIC family (HERIC-I, HERIC-I-PNPC, HERIC-II, HERIC-III, HERIC-IV, HERIC-V, HERIC-V-PNPC), H6 family (H6, H6-ANPC, H6-PNPC, improved H6) are shown in Figs. 3(a)-14(a) respectively. Figs. 3(f)-14(f) exhibit the waveforms of the gate drive signal for those topologies. There are four operation modes of each topology, which are shown in Figs. 3(b to e)-14 (b to e) respectively. The operations of those topologies have been summarized in Table 2 where AP, FP, AN and FN indicate the active mode for positive half cycle, freewheeling mode for positive half cycle, active mode for negative half cycle and freewheeling mode for negative half cycle respectively.

Table 2 shows that the CM voltage of all existing topologies varies between $\frac{V_{DC}}{2}$ to $\approx \frac{V_{DC}}{2}$ for every active to freewheeling

TABLE 2. Operating modes analysis.

Topology	Mode	Switches On	Inductor Current Path	V_{PN}	V_{QN}	DM Voltage, V_{PQ}	CM Voltage, V_{CM}
H5	AP	S1, S4, S5	S5, S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S1	S1, the antiparallel diode of S3	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S5	S5, S3, S2	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S3	S3, the anti-parallel diode of S1	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
HERIC-I	AP	S1, S4, S5	S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S5	S5, D1	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S6	S2, S3	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S6	S6, D2	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
HERIC-I-PNPC	AP	S1, S4, S5	S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S5	S5, D1	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S6	S2, S3	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S6	S6, D2	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
HERIC-II	AP	S1, S4, S5	S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S5	S5, the anti-parallel diode of S6	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S6	S2, S3	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S6	S6, the anti-parallel diode of S5	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
HERIC-III	AP	S1, S3, S5	S1, S3	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S5	S5, the anti-parallel diode of S6	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S4, S6	S2, S6, S4	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S6	S6, the anti-parallel diode of S5	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
HERIC-IV	AP	S1, S3, S5	S1, S5, S3	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S5	S5, D1	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S4, S6	S2, S6, S4	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S6	S6, D2	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
HERIC-V	AP	S1, S4	S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S5	S5, D3, D4	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3	S2, S3	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S5	S5, D1, D2	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
HERIC-V-PNPC	AP	S1, S4	S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S5	S5, D2, D4	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3	S2, S3	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S5	S5, D1, D3	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
H6	AP	S1, S4, S5	S1, S5, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S1, S5, S6	S1, S5, D1, S6, D2, the anti-parallel diode of S2	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S6	S2, S3, S6	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S6, S2, S5	S6, D2, the anti-parallel diode of S1, S2, S5, D1	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
H6-ANPC	AP	S1, S4, S5	S5, S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S1, S6	S1, the anti-parallel diode of S3	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S5	S2, S3, S5	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S3, S6	S3, the anti-parallel diode of S1	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
H6-PNPC	AP	S1, S4, S5, S6	S5, S1, S4, S6	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S1, S4	S1, S4, D1, D2	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S5, S6	S5, S2, S3, S6	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S2, S3	S2, S3, D1, D2	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
Improved H6	AP	S1, S4, S5	S5, S1, S4	V_{DC}	0	V_{DC}	$0.5V_{DC}$
	FP	S1	S1, the anti-parallel diode of S3	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$
	AN	S2, S3, S6	S6, S2	0	V_{DC}	V_{DC}	$0.5V_{DC}$
	FN	S3	S3, the anti-parallel diode of S1	$\approx 0.5V_{DC}$	$\approx 0.5V_{DC}$	0	$\approx 0.5V_{DC}$

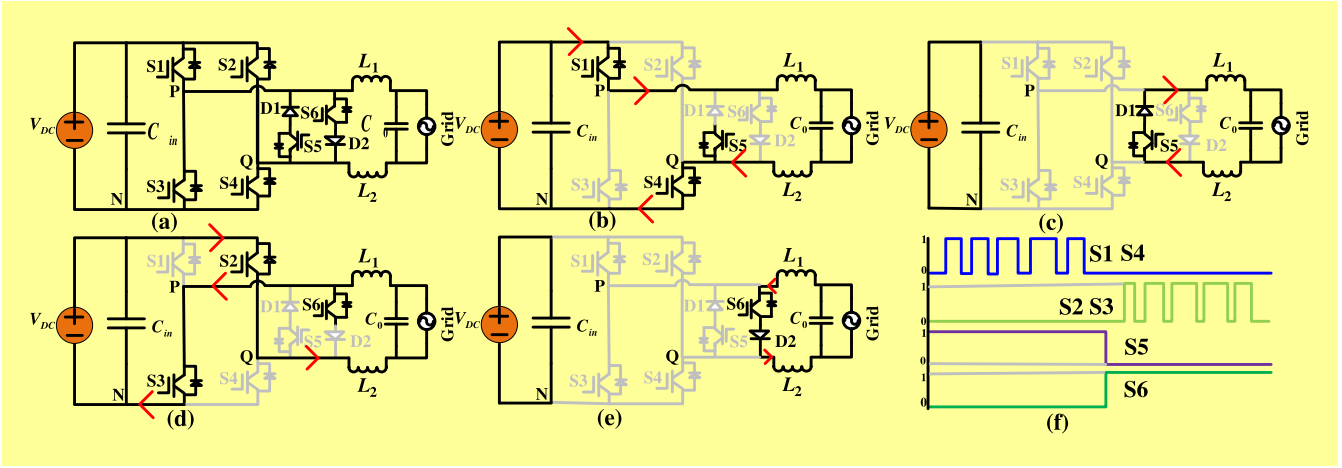


FIGURE 4. Operating modes of HERIC-I topology.

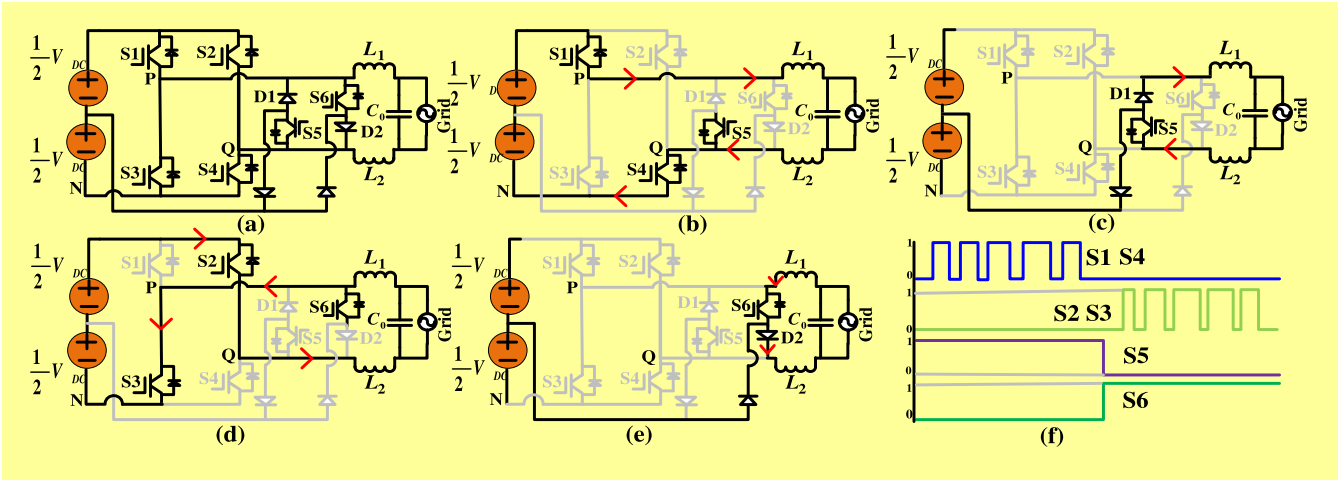


FIGURE 5. Operating modes of HERIC-I-PNPC topology.

mode (both negative and positive half cycles) [15], [16], [30], [43]–[45]. This little fluctuation of CM voltage produces the leakage current.

A. H5 TOPOLOGY

The H5 topology [15], [46] is the modified version of full bridge inverter structure where an extra switch is added as shown in Fig. 3(a). This extra switch increases the efficiency and eliminates the high-frequency component of CM voltage as no exchange of reactive power between DC side to the grid during freewheeling modes. It reduces the core losses by using unipolar voltage distribution. But the switch junction capacitor will create leakage current due to it's assymmetric structure in practical applications [47]. Moreover, high conduction losses are visualized due to the continuous conduction mode of three switches in all active modes.

The operation modes of this topology are summarized in Table 2, which shows the CM voltage varies between $\frac{V_{DC}}{2}$ to $\approx \frac{V_{DC}}{2}$ for every active to freewheeling mode (both negative and positive half cycles). This slight variation of CM voltage is responsible for the leakage current.

B. HERIC-I TOPOLOGY

Two extra switches with two diodes on AC side are employed in the HERIC-I topology [29], [43] as shown in Fig. 4(a). Those extra switches with diodes create an alternative path for inductor current during both positive and negative freewheeling states and helps to isolate the grid side from the DC source, that prevents the reactive power exchange between LCL filter and input capacitor C_{in} during freewheeling modes [29]. This topology also reduces the conduction loss [45]. The CM voltage of this topology is not constant in all operating modes, that is the evident of increasing the leakage current.

C. HERIC-I-PNPC TOPOLOGY

The HERIC-I-PNPC [15], [16] employs two diodes with bidirectional switches on the grid side as shown in Fig. 5(a).

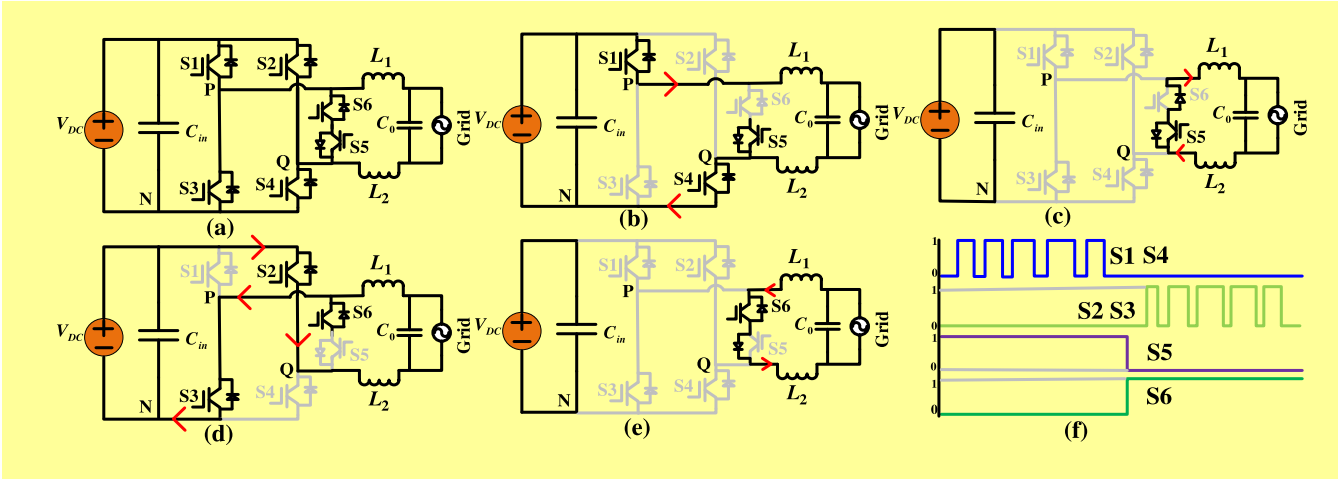


FIGURE 6. Operating modes of HERIC-II topology.

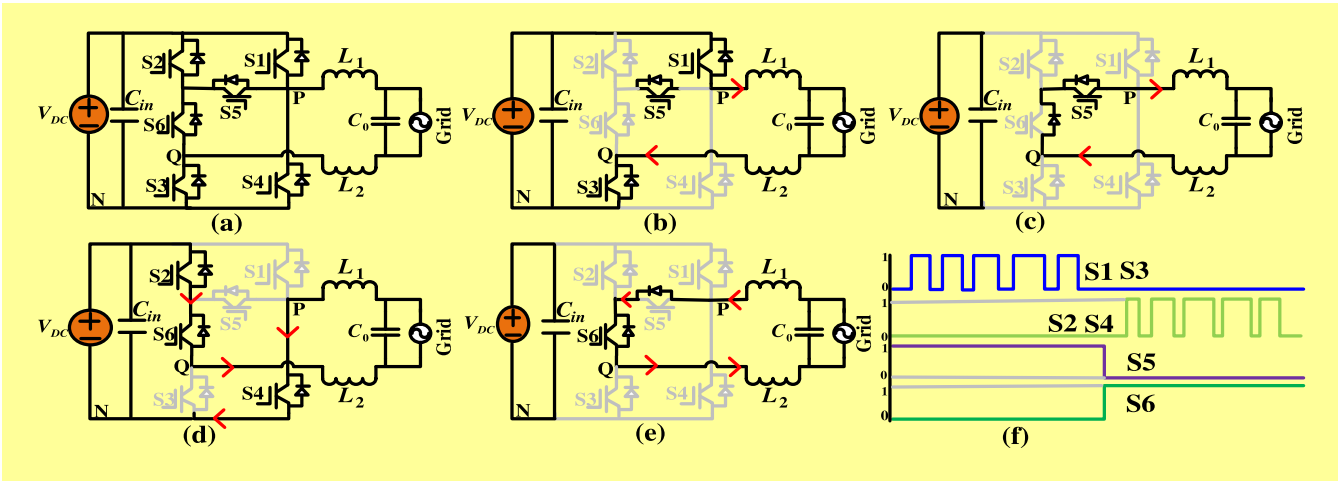


FIGURE 7. Operating modes of HERIC-III topology.

This topology inserts a passive neutral point clamped network which keeps the CM voltage almost constant and reduces the high frequency component of CM voltage [45]. So, the r.m.s value of leakage current would be very small in this topology.

D. HERIC-II TOPOLOGY

The HERIC-I and the HERIC-II are similiar in operation and therefor the characteristics of the CM voltage is almost identical. The HERIC-II [26], [44] employs two back to back switches on the grid side as shown in Fig. 6(a). These additional switches help to isolate the grid side from the DC source and preventing the reactive power exchange between LCL filter and input capacitor C_{in} during freewheeling modes [26]. But the requirement of these extra switches increase the size and cost of this inverter.

E. HERIC-III TOPOLOGY

The HERIC-III [27], [45] is the modification of basic HERIC structure, where two extra switches are used between the points P and Q as shown in Fig. 7(a). That kind of arrangement creates an alternative path for flowing the inductor current during freewheeling modes. Three switches are in conduction state during active mode of negative half cycle and eliminates the need of PWM dead time [45]. The presence of high conduction loss is the main limitation of this topology.

F. HERIC-IV TOPOLOGY

The HERIC-IV [28], [48] is the modified version of half bridge inverters, where two extra switches are employed on the filter side as shown in Fig. 8(a). Two back to back diodes are connected between these two switches and point Q which have two functions such as, creating an alternative path to flow the inductor current and isolating the DC source from the grid during freewheeling modes [28]. In this topology, three switches are in conduction in all active modes that having maximum conduction loss among the HERIC family.

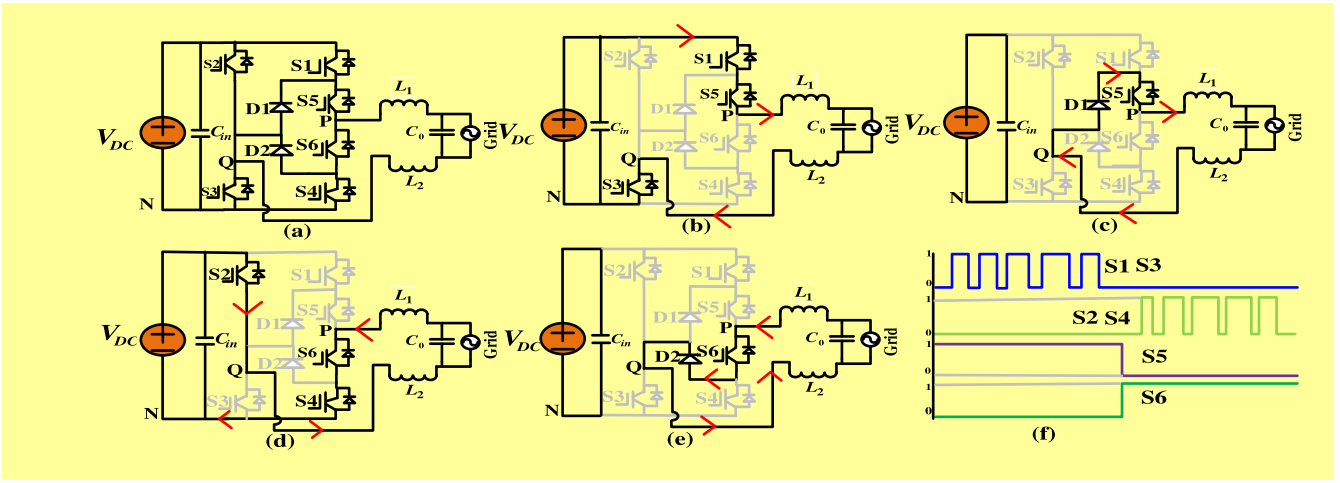


FIGURE 8. Operating modes of HERIC-IV topology.

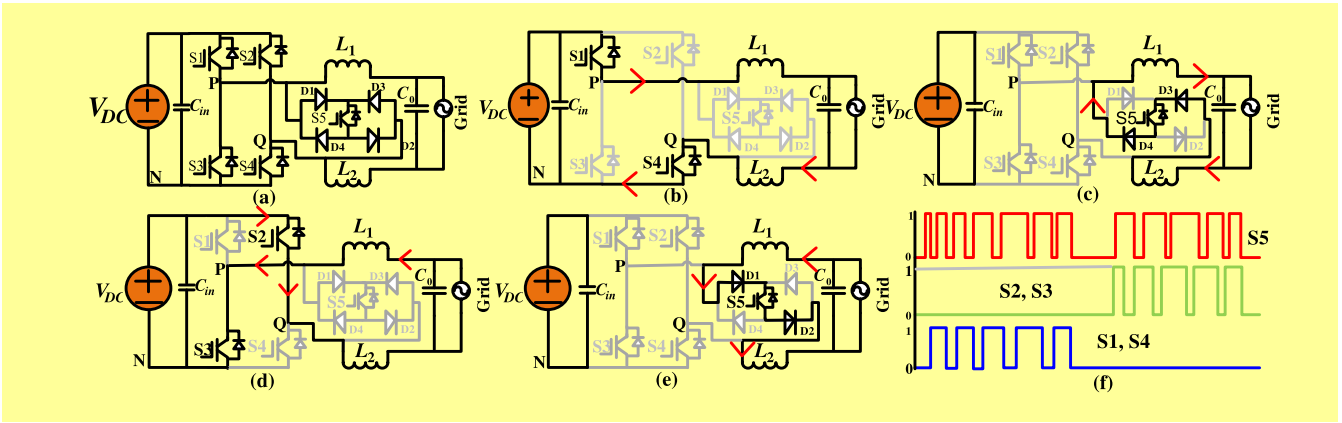


FIGURE 9. Operating modes of HERIC-V topology.

G. HERIC-V TOPOLOGY

The HERIC-V [16], [20] topology has a switch that can operate in high frequency all the time. This topology employs a single switch and four diodes on the grid side as shown in Fig. 9(a). This topology overcomes the limitation of HERIC-IV topology by reducing the conduction loss. But the high switching loss is the main disadvantage of this topology.

H. HERIC-V-PNPC TOPOLOGY

Another modified version of the HERIC family is the HERIC-V-PNPC [29], [45], consisting of a clamping cell on the DC side as shown in Fig. 10(a). This clamping cell helps to keep the CM voltage constant. As a result leakage current would be reduced in this topology. Extra switches and diodes are required to eliminate the high frequency component of grid voltage that increases the cost and the size of this topology.

I. H6 TOPOLOGY

The H6 topology [30], [44] employs two switches between the terminal (P) and the negative terminal of the DC source (N), another two switches between the terminal (Q) and the negative terminal of the DC source (N) as shown in Fig. 11(a). The inductor current is flowing through three switches in all modes of H6 topology. Diodes D1 and D2 are added to reduce the conduction loss and disconnect the AC and DC side during freewheeling modes. The presence of the unipolar distribution current between switches keep the loss of the inverter balanced [30]. But the conduction and switching losses are high of this topology.

J. H6-ANPC TOPOLOGY

The H6 inverter topology lacks the ability to reduce leakage current due to the transistors' junction capacitance. The H6-ANPC [45], [49] employs a clamping cell on the DC side, that overcomes the limitation of the H6 topology and helps to keep the CM voltage constant. Thus, the leakage current would be small after adding the clamping cell. But the requirement of large number of gate driver signals is the main limitation of this topology.

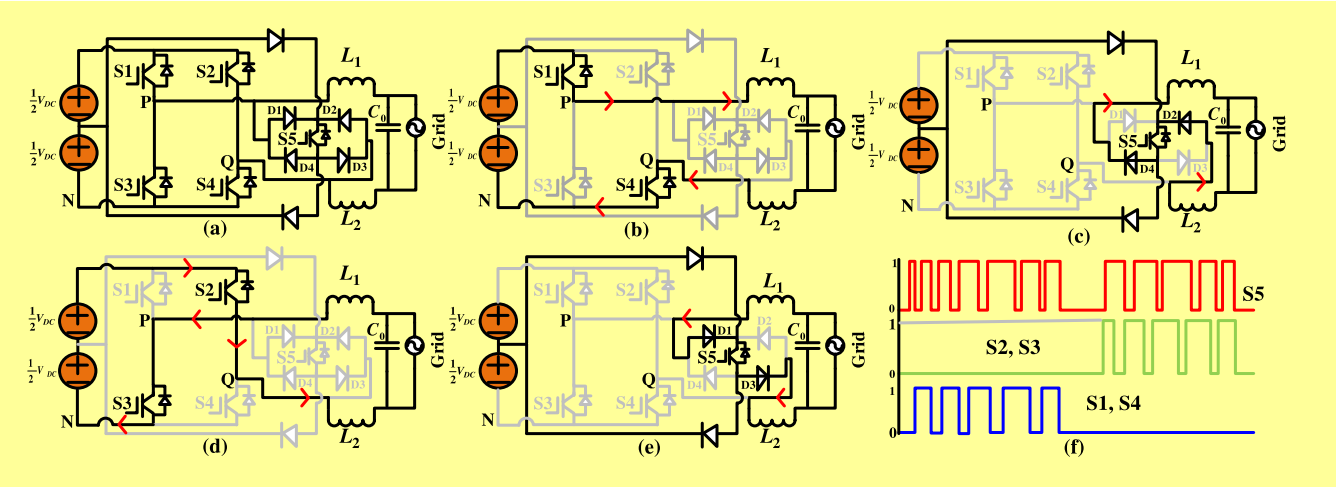


FIGURE 10. Operating modes of HERIC-V-PNPC topology.

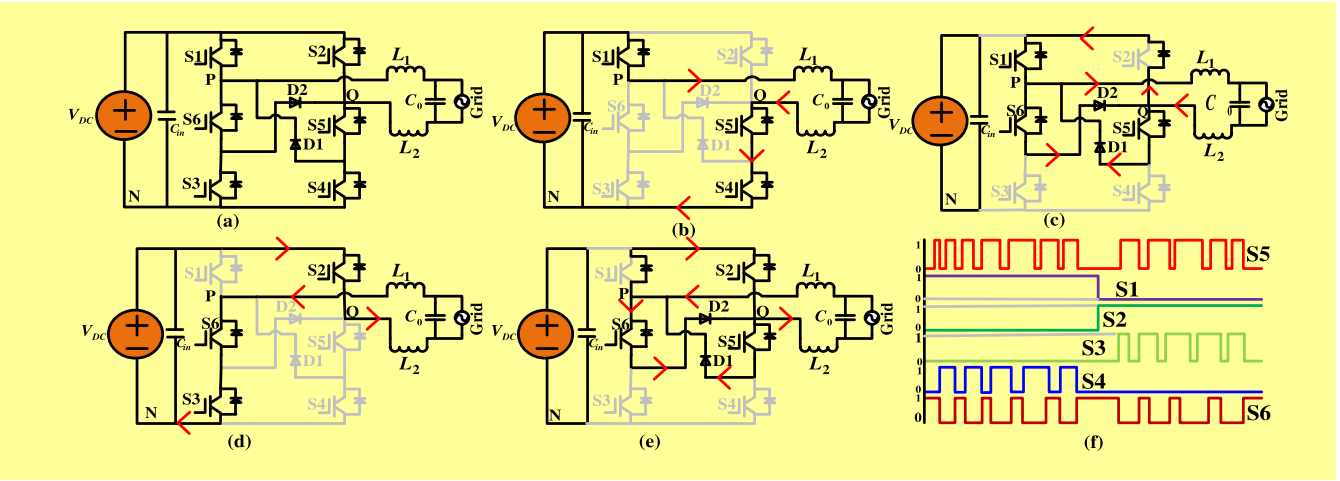


FIGURE 11. Operating modes of H6 topology.

K. H6-PNPC TOPOLOGY

The H6-PNPC [20], [31] employs two switches between the DC side and full bridge inverter structure and two diodes are added between these extra two switches. At freewheeling modes, these two switches help to disconnect the DC side from the grid. The H6-PNPC also employs a clamping cell which reduces the effect of switch junction capacitance [45]. Four switches are in conduction mode in all active modes, so conduction loss is very high for this topology compared to the H6.

L. IMPROVED H6 TOPOLOGY

To reduce the effect of switch junction capacitance, another H6 topology is proposed called improved H6 [44], [50]. An extra switch is added into the H5 topology between the point Q and the DC side as shown in Fig. 14(a). This switch prevents power exchange from grid side to the DC side and form an alternative path to flow the inductor current during freewheeling modes. Improved H6 topology reduces the conduction loss compared to the H5 topology, as only two switches are in conduction mode during active mode of negative half cycle. This topology is also able to reduce the leakage current and THD of grid voltage and current. But the main limitation of this topology is that it has higher conduction loss than any HERIC family member [44].

VI. DESIGN OF IMPROVED H5 TOPOLOGY

The variation of the CM voltage is the main reason of the leakage current which reduces the performance of the MG by increasing the THD of grid voltage and current. It is evident from all of the discussed topologies have varying CM voltage that causes the leakage current of the inverter. The main contribution of this paper is to design an improved H5 topology [34] with ILQG controller for MG application in order to reduce the leakage current. This improved H5 topology is consisted of five switches and one clamping diode D_c, as shown in Fig.15(a), where a passive clamped circuit is constituted by C_{in1}, C_{in2} and D_c.

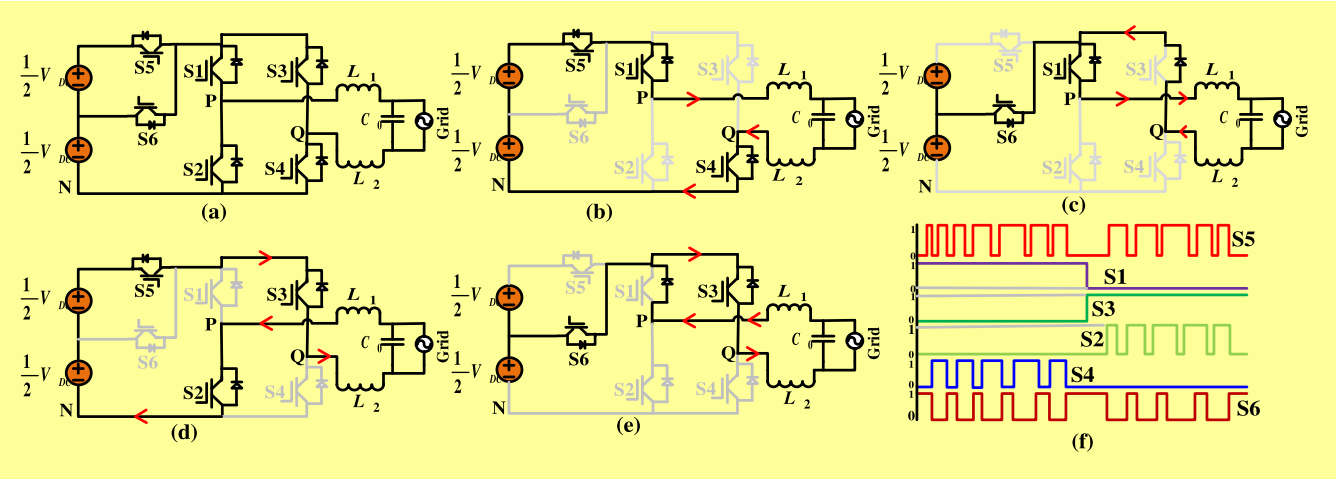


FIGURE 12. Operating modes of H6-ANPC topology.

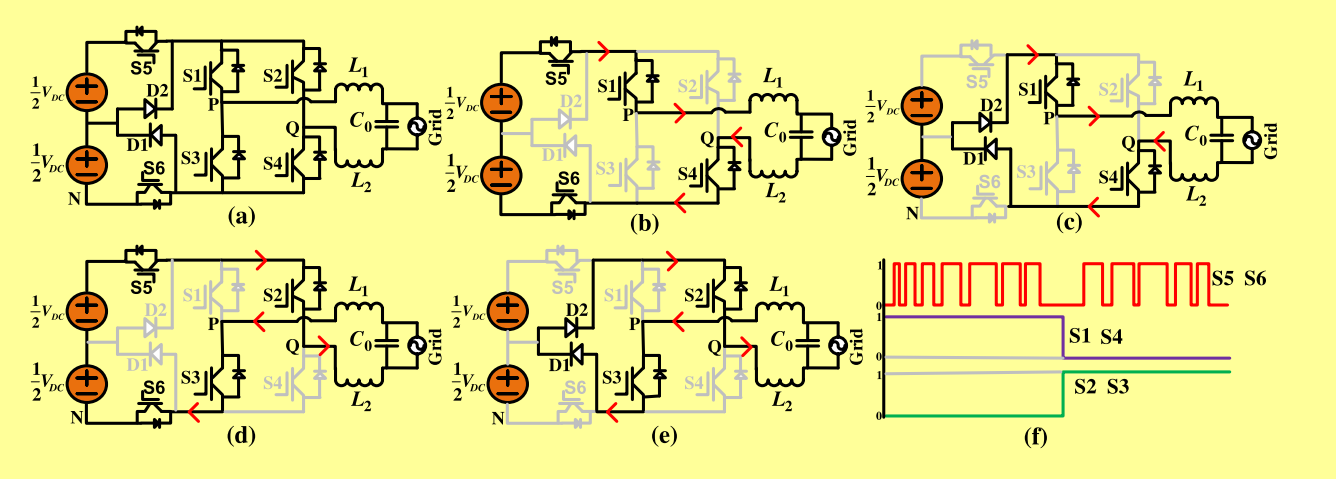


FIGURE 13. Operating modes of H6-PNPC topology.

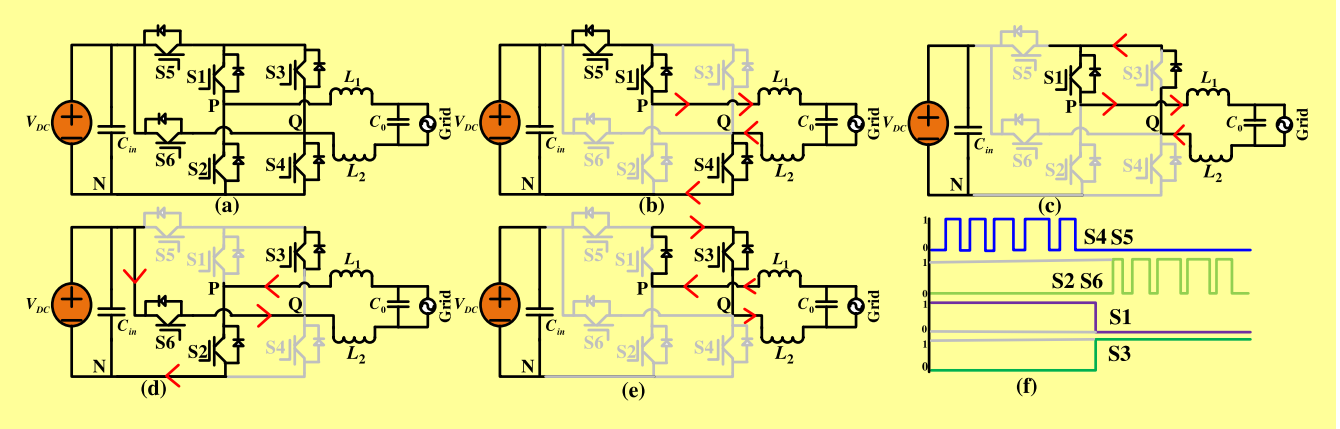


FIGURE 14. Operating modes of improved H6 topology.

A. OPERATING MODES ANALYSIS

Mode 1: S1, S4 and S5 are turned on during the active mode of the positive half cycle as shown in Fig. 15(b), which makes $V_{PM} = V_{QN} = 0$ and $V_{MN} = V_{DC}$. Thus the CM voltage can be found as,

$$V_{CM} = \frac{V_{PN} + V_{QN}}{2} = \frac{V_{PM} + V_{QN} + V_{MN}}{2} = \frac{V_{DC}}{2}$$

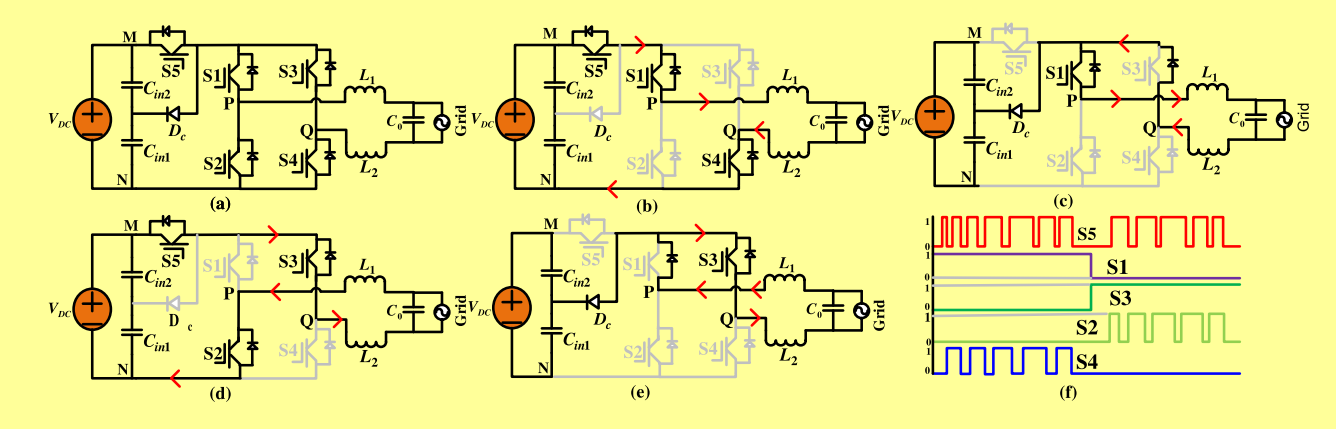


FIGURE 15. Operating modes of improved H5 topology.

TABLE 3. Highlights of different topologies.

Topology	Semiconductor Switches Used	Switches in Conduction Mode	Diode Used	Input Capacitor Used	Reversed Recovery Diode	Advantages	Limitations
H5	5	3	2	1	1	Lower core losses	Higher conduction losses
HERIC-I	6	2	2	1	1	Lower conduction losses and leakage current	Requirement of the dead time to eliminate the leakage current
HERIC-I-PNPC	6	2	4	0	1	Lower conduction losses and leakage current	Requirement of the dead time for bi-directional switches
HERIC-II	6	2	2	1	1	Lower switching losses and leakage current	Requirement of the dead time to eliminate the leakage current
HERIC-III	6	3	2	1	1	No requirement of the dead time to eliminate the leakage current	Higher conduction losses
HERIC-IV	6	3	2	1	1	Lower leakage current	Higher conduction losses
HERIC-V	5	2	4	1	2	Lower conduction losses	Higher switching losses
HERIC-V-PNPC	5	2	6	0	2	Lower conduction losses and leakage current	Requirement of the extra switches and diode to eliminate the higher frequency of the grid voltage that makes the system costly and bulky
H6	6	3	4	1	3	Balanced losses	Higher switching and conduction losses
H6-ANPC	6	3	2	0	1	Lower leakage current	Requirement of the large number of gate driver signal
H6-PNPC	6	4	2	0	2	Lower leakage current, no exchange of the reactive power between the input capacitor and filter inductor	Higher switching and conduction losses
Improved H6	6	3	2	1	1	Lower THD of the grid connected current and leakage current	Higher conduction losses
Improved H5	5	3	3	2	1	Maintain the constant CM voltage that reduces the leakage current of the inverter, lower THD of the grid voltage and current	-

Mode 2: Mode 2 is the freewheeling mode for positive half cycle where only S1 is turned on and other switches are turned off as shown in Fig. 15(c), where the inductor current is flowing through S1 and the anti-parallel diode of S3. So $V_{PN} = V_{QN} = \frac{V_{DC}}{2}$, which suggests $V_{PQ} = 0$. Then the CM voltage is,

$$V_{CM} = \frac{V_{PN} + V_{QN}}{2} = \frac{V_{DC}}{2}$$

Mode 3: Switches S2, S3 and S5 are turned on during the active mode for negative half cycle and the other switches are turned off. It is shown from the Fig. 15(d), the inductor current is flowing through S5, S3 and S2. So $V_{PN} = 0$, $V_{QM} = 0$ and $V_{MN} = V_{DC}$, which makes the CM voltage,

$$V_{CM} = \frac{V_{PN} + V_{QN}}{2} = \frac{V_{PN} + V_{QM} + V_{MN}}{2} = \frac{V_{DC}}{2}$$

Mode 4: Mode 4 is the freewheeling mode for negative half period where only S3 is turned on and the other switches of this topology are turned off. According to Fig. 15(e), the inductor current is flowing through S3 and the anti-parallel diode of S1. So $V_{PN} = V_{QN} = \frac{V_{DC}}{2}$, $V_{PQ} = 0$. Thus the CM voltage can be presented as,

$$V_{CM} = \frac{V_{PN} + V_{QN}}{2} = \frac{V_{DC}}{2}$$

This improved H5 topology is able to keep the CM voltage constant that allows the reduction of the leakage current and the THD of grid voltage and current. It is important to note that the direction of the clamping diode, D_c is mighty important here. The direction shown in Fig. 15(a) makes it in conduction state during both freewheeling modes, which eventually produces the voltages of V_{PN} and V_{QN} equal to exact $\frac{V_{DC}}{2}$. Otherwise, if the direction of that diode would be reversed, D_c will not be in conduction. That means those two voltages would not be exact $\frac{V_{DC}}{2}$, rather tends to $\frac{V_{DC}}{2}$ during freewheeling modes. Which actually indicates a variation in V_{CM} voltage and creates much more leakage current.

VII. CONTROLLER DESIGN

A pure sinusoidal signal is required to deliver the inverter gate pulse. It is difficult to produce due to unwanted oscillation in the grid connected MG that affects the production of the inverter gate pulse. To control this oscillation and produce a pure sinusoidal signal, an ILQG controller is designed which has been proposed in [11], [51]. The LQG controller along with integral controller provides the highly tracking performance as compared to LQG or integral controller itself. This control methodology has been done by using H_2 norm technique that is responsible to increase the gain and phase margin of the system.

The system can be represented as follows to design the controller,

$$\dot{x}_t = A_t x_t + B_t u_t + D_t \phi_t \tag{16}$$
$$y_t = C_t x_t + \bar{D}_t \bar{\phi}_t \tag{17}$$

where, A_t, B_t and C_t represent the matrices of the system, input and output respectively with state vector x_t and output y_t. The parameters ϕ_t and D_t are the process and measurement noise matrices respectively. A better selection of the quadratic cost function J_t increases the robustness of the control system to optimize the control input such as,

$$J_t = \Xi\Big\{\lim_{T\to\infty}\frac{1}{T}\int_0^T [x_t^T Q_t x_t + u_t^T R_t u_t]dt\Big\} \tag{18}$$

where, Q_t and R_t represent weighting matrices of the symmetric constant as such $Q_t = Q_t^T \geq 0$ and $R_t = R_t^T > 0$. The basic block diagram of the ILQG controller is presented in Fig. 16 with plant transfer function $P(s)$, integral action $\frac{1}{s}$ and LQG controller $L(s)$. The new plant model corresponding to the ILQG controller can be represented as,

$$\dot{x}_{t1} = A_{t1} x_{t1} + B_{t1} u_{t1} + B_{t1} \phi_{t1} \tag{19}$$

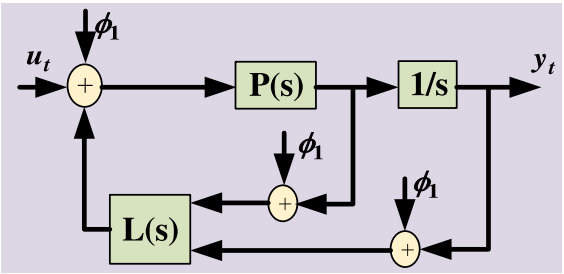


FIGURE 16. Control structure of ILQG controller.

$$y_{t1} = C_{t1} x_{t1}(t) + \vartheta_{t1} \tag{20}$$

where A_{t1}, B_{t1} and C_{t1} can be represented as,
$A_{t1} = \begin{bmatrix} A_t & 0 \\ C_t & 0 \end{bmatrix}$, $B_{t1} = \begin{bmatrix} B_t \\ 0 \end{bmatrix}$, and $C_{t1} = \begin{bmatrix} C_t & 0 \\ C_t & I \end{bmatrix}$
x_{t1} and y_{t1} are the augmented vector that can be represented as, $x_{t1} = [x_t \ \int y_t dt]^T$, $y_{t1} = [y_1 \ y_2]^T$. If the system noise is ω_1, sensor noise is ω_2 and added integral noise is ω_3, then $\vartheta_{t1} = [\omega_2 \ \omega_3]^T$. The cost function will be updated for the system with ILQG controller that can be represented as,

$$J_{t1} = \Xi\Big\{\lim_{T\to\infty}\frac{1}{T}\int_0^T [x_{t1}^T Q_{t1} x_{t1} + w_{t1}^T Q'' w_{t1} + u_{t1}^T R_{t1} u_{t1}]dt\Big\} \tag{21}$$

where, w_{t1} is the weighting matrices as $w_{t1} = \int_0^T y_{t1}(\tau)d\tau$. Q_{t1} and Q'' are the state and integral state matrices, and R_{t1} represents the control input matrix such as $Q_{t1} = Q_{t1}^T \geq 0$, $Q'' \geq 0$, and $R_{t1} = R_{t1}^T > 0$.

The complete modelling of the ILQG controller with Kalman filter and LQR controller can be represented as,

$$\dot{x}_{t1} = A_{t1} x_{t1} + B_{t1} u_{t1} + K_{t1}(y_{t1} - C_{t1} x_{t1}) \tag{22}$$
$$u_{t1} = -K_{t2} \bar{x}_{t1} \tag{23}$$

where K_{t1} is the kalman gain that can be represented as,

$$K_{t1} = P_{t1} C_{t1}^T R_{t1}^{-1} \tag{24}$$

where P_{t1} is the Riccati equation solution as,

$$P = A_{t1}^T P_{t1} + P_{t1} A_{t1} - P_{t1} C_{t1}^T R_{t1}^{-1} C_{t1} P_{t1} + Q_{t1} \tag{25}$$
$$Q_{t1} = \nu_1^2 \quad R_1 = \begin{bmatrix} \nu_2^2 & 0 \\ 0 & \nu_3^2 \end{bmatrix} \tag{26}$$

where, ν represents the standard deviation with sensor and measurement noise. And K_{t2} is the feedback gain that can be represented as

$$K_{t2} = R_{t1}^{-1} B_{t1} P_{t2} \tag{27}$$

where P_{t2} can be represented by

$$\bar{P} = A_{t1}^T P_{t2} + P_{t2} A_{t1} - P_{t2} C_{t1}^T R_{t2}^{-1} C_{t1} P_{t2} + Q_{t2} \tag{28}$$

where

$$Q_{t2} = C_{t1}^T \begin{bmatrix} 1 & 0 \\ 0 & q \end{bmatrix} C_{t1} \quad R_{t2} = r \tag{29}$$

The proper selection of the parameters Q_{t1}, Q_{t2}, R_{t1} and R_{t2}, are essential to track the reference signal properly that helps

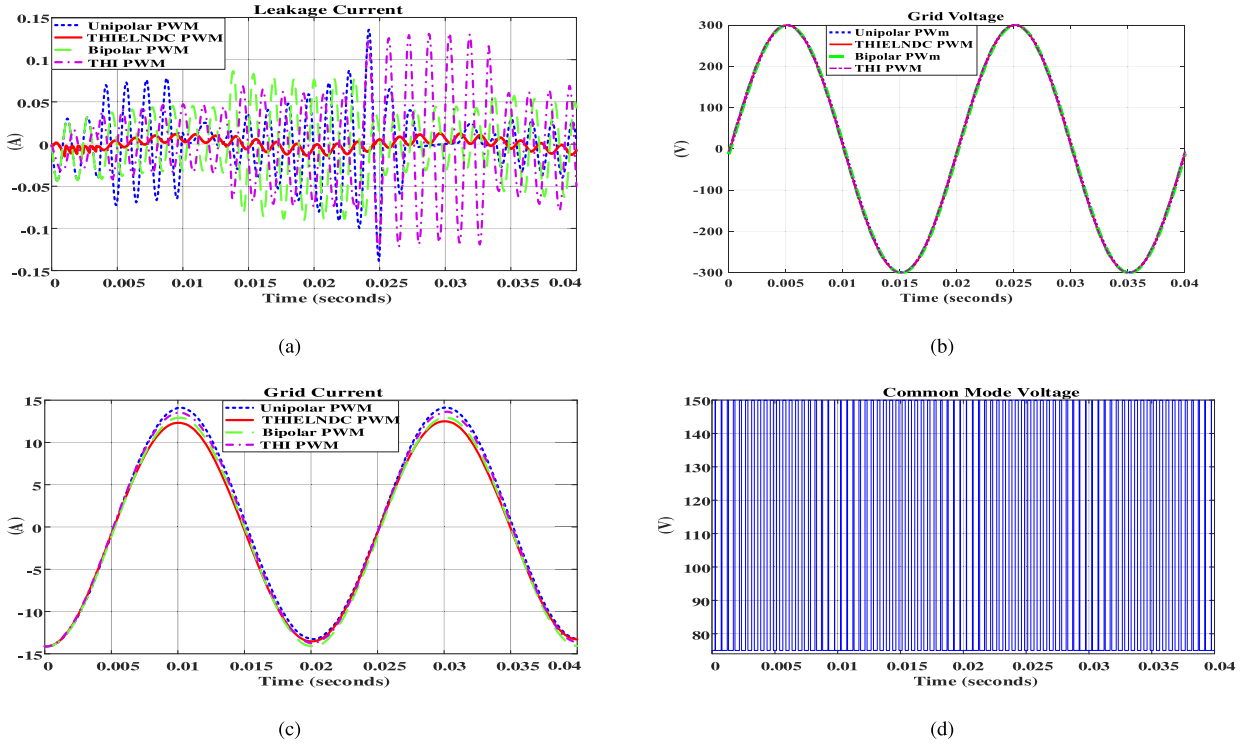


FIGURE 17. (a) Leakage Current, (b) Grid voltage, (c) Grid current and (d) CM voltage of H5 topology with ILQG controller.

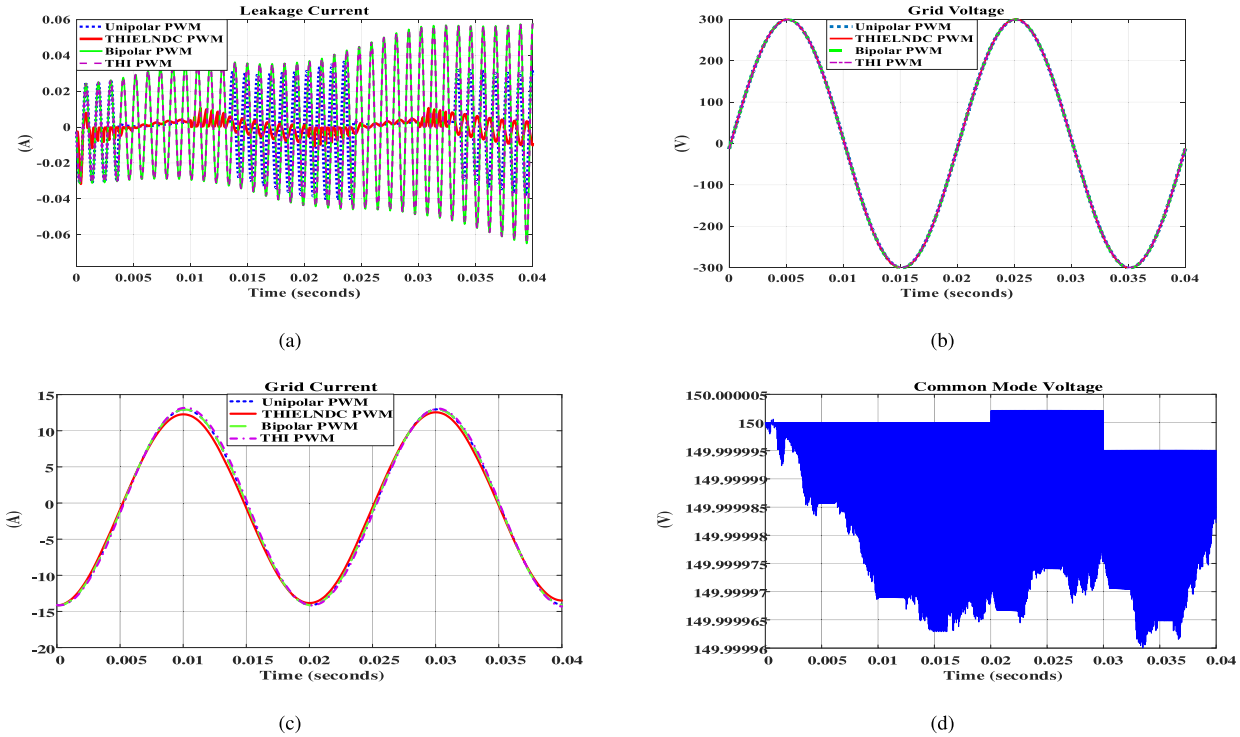


FIGURE 18. (a) Leakage Current, (b) Grid voltage (c) Grid current and (d) CM voltage of HERIC-I topology with ILQG controller.

to increase the bandwidth, gain and phase margin of the system and efficiently produce the gate signal for controlling the leakage current of the transformerless inverters. The parameters to design an ILQG controller has been listed in Table 4.

VIII. PERFORMANCE ANALYSIS

The performances of the MG with different topologies and methodologies have been investigated in this section. The variation of the CM voltage is responsible to increase the

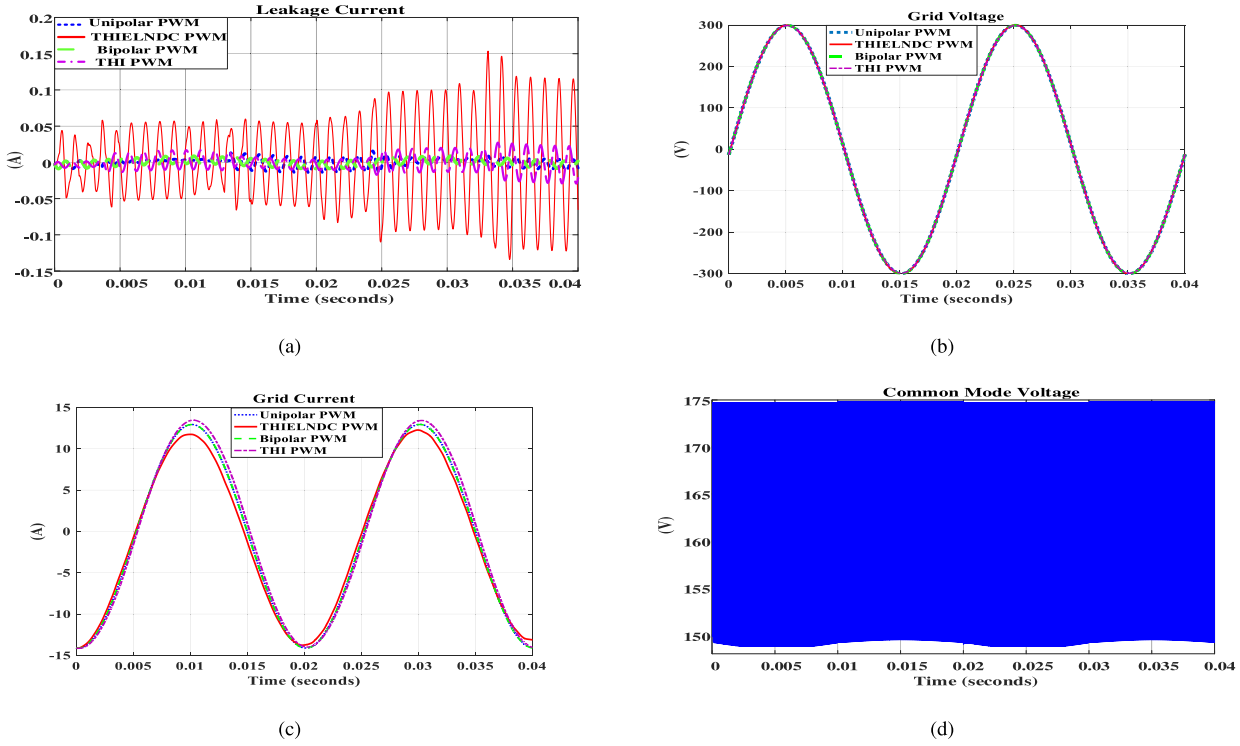


FIGURE 19. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of HERIC-I-PNPC topology with ILQG controller.

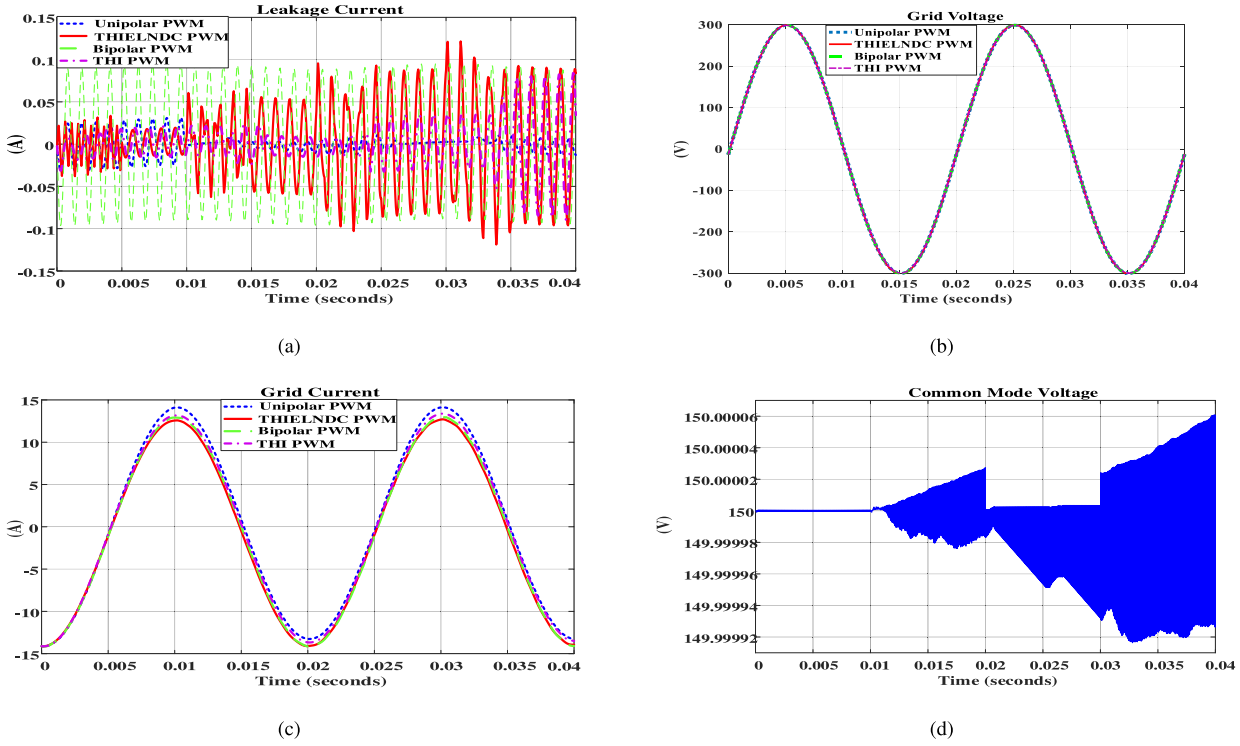


FIGURE 20. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of HERIC-II topology with ILQG controller.

leakage current of the inverter that hampers the performance of the MG, thus the THD of grid voltage and current increases. It is seen from the Table 2 that the existing topologies exhibit the variation of the CM voltage which varies from $V_{DC}/2$ to tends to $V_{DC}/2$. This little variation in the CM voltage increases the leakage current.

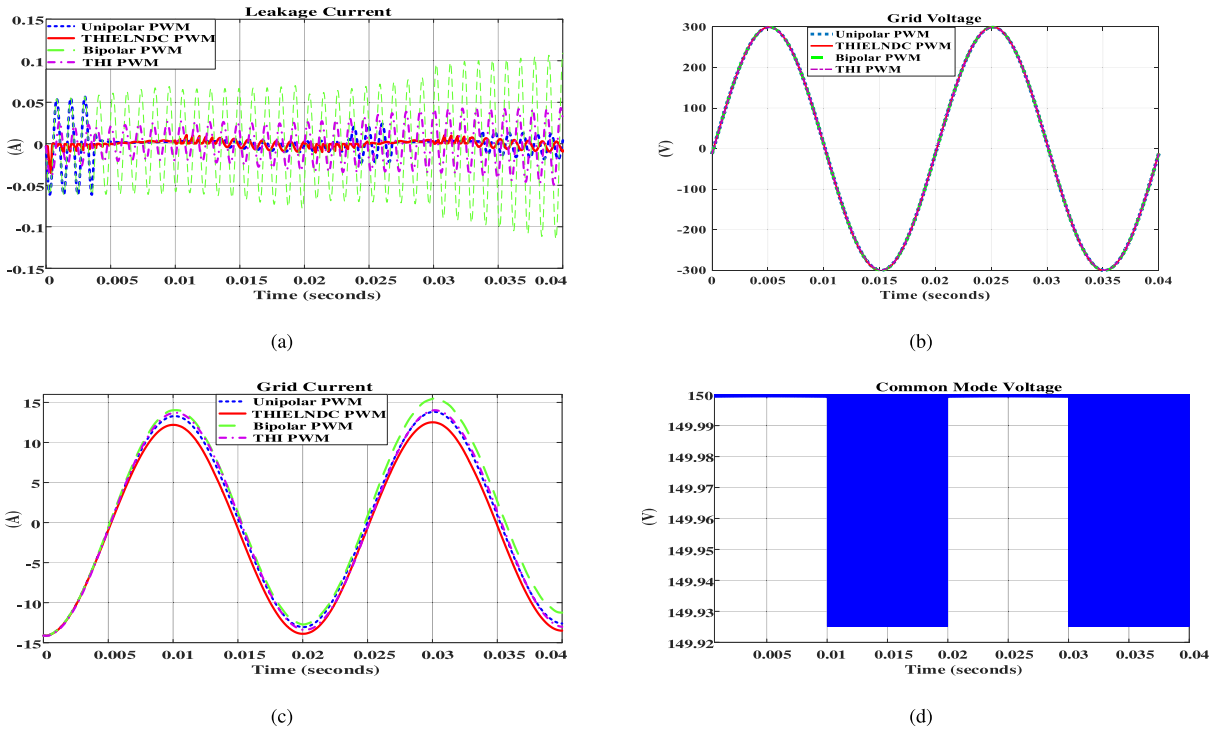


FIGURE 21. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of HERIC-III topology with ILQG controller.

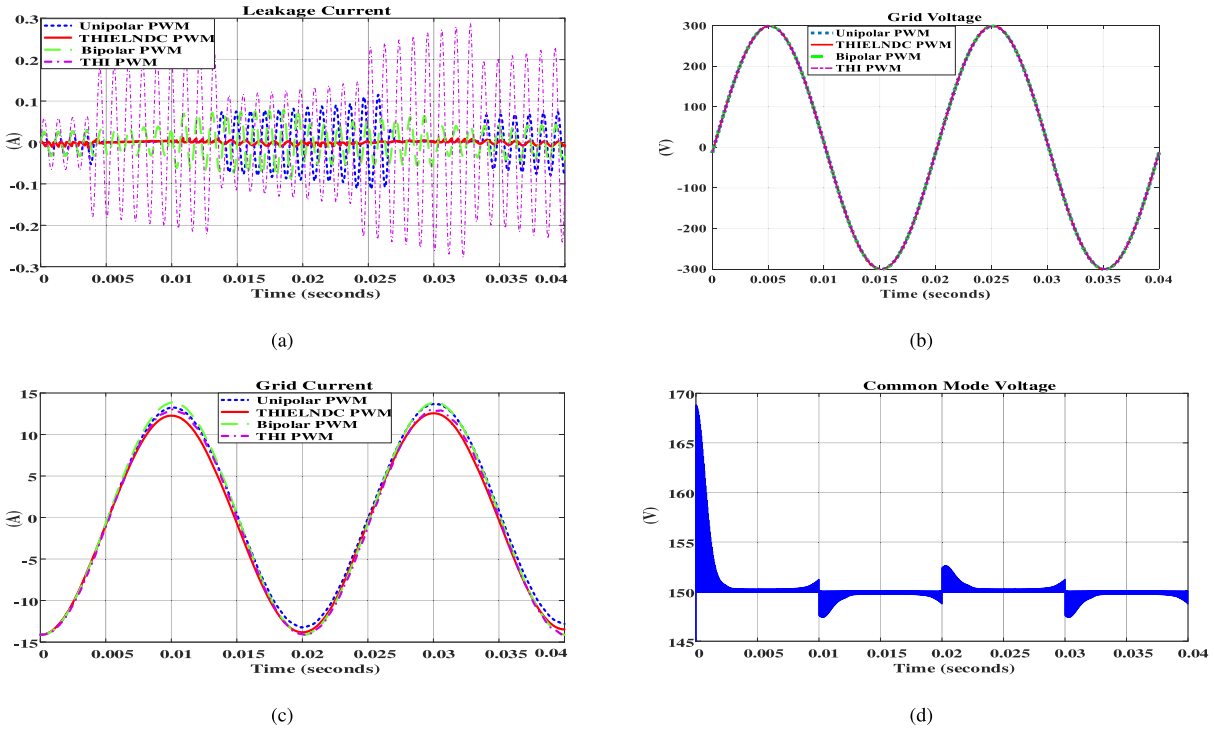


FIGURE 22. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of HERIC-IV topology with ILQG controller.

The performance of the designed topology has been compared in this section to find out the optimum modulation technique to reduce the leakage current with ILQG controller.

The leakage currents of the existing topologies with ILQG controller are shown in Figs. 17(a)- 28(a) which indicate the variation of the leakage current with different modulation techniques. The control method of gate drive signal for different modulation techniques is responsible for higher or lower THD of grid voltage and current. Figs. 17(b)- 28(b) exhibit the grid voltage under different modulation techniques using

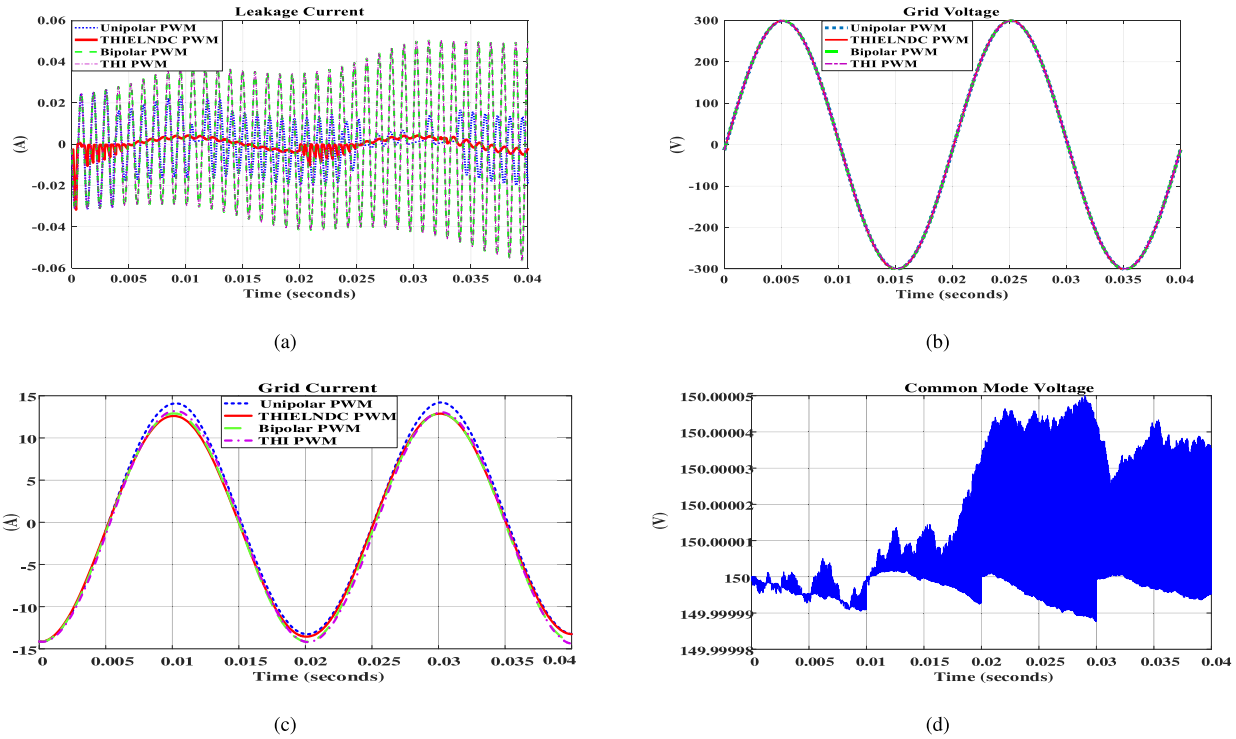


FIGURE 23. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of HERIC-V topology with ILQG controller.

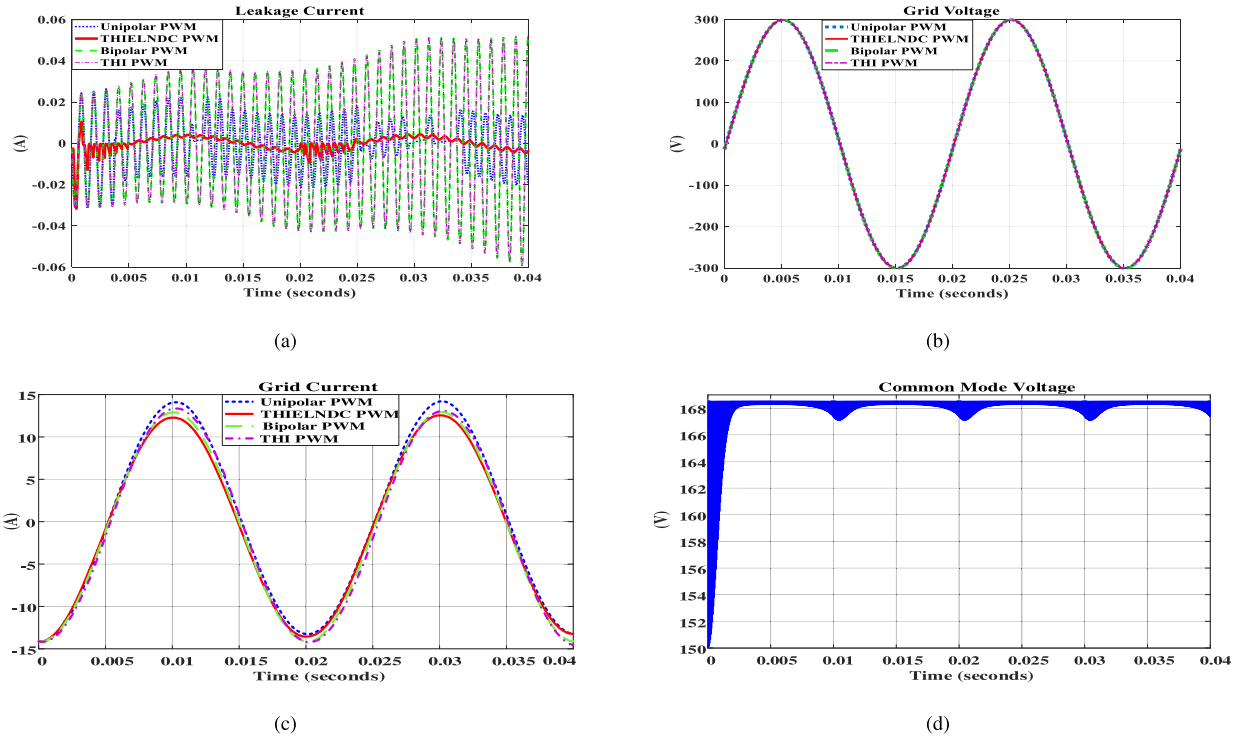


FIGURE 24. (a) Leakage Current, (b) Grid voltage, (c) Grid current and (d) CM voltage of HERIC-V-PNPC topology with ILQG controller.

ILQG controller. It is depicted from the Table 5 that all modulation techniques keep the grid voltage's THD almost same with a lower value which is possible because of using ILQG controller to produce the gate drive signal of inverters. Again, the grid current of the existing topologies are represented in Figs. 17(c)- 28(c).

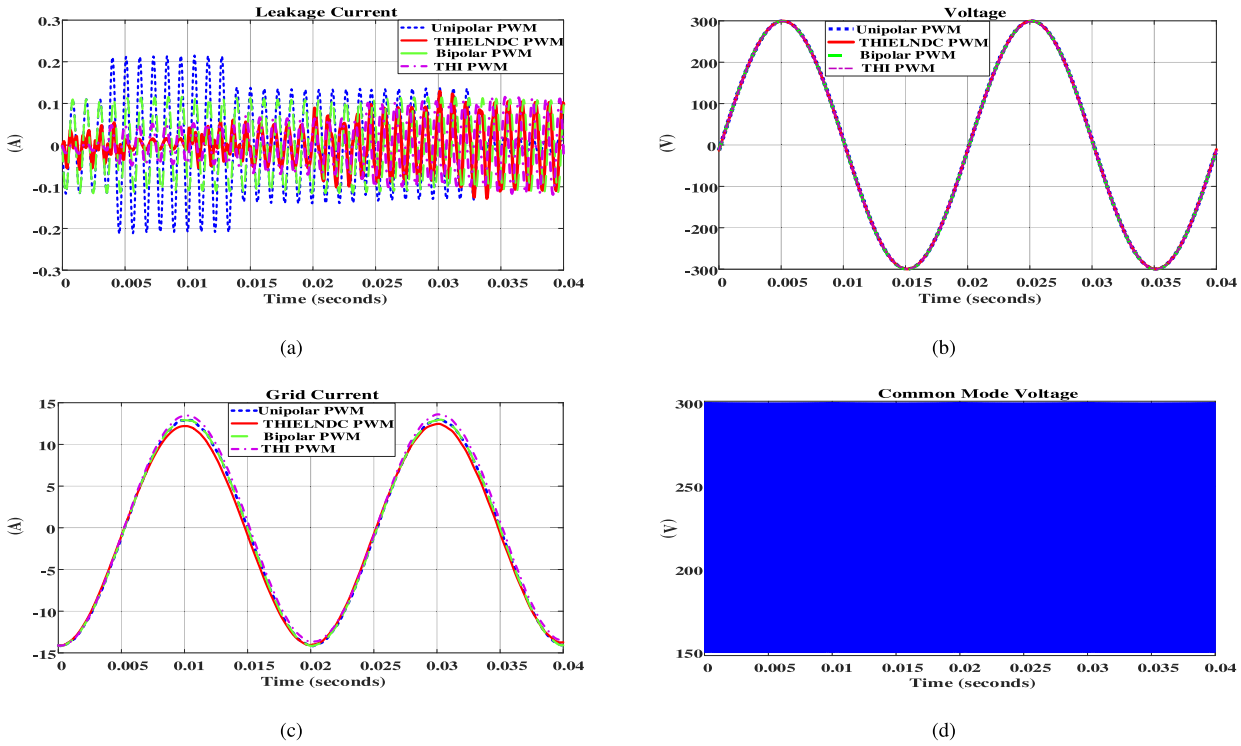


FIGURE 25. (a) Leakage Current, (b) Grid voltage, (c) Grid current and (d) CM voltage of H6 topology with ILQG controller.

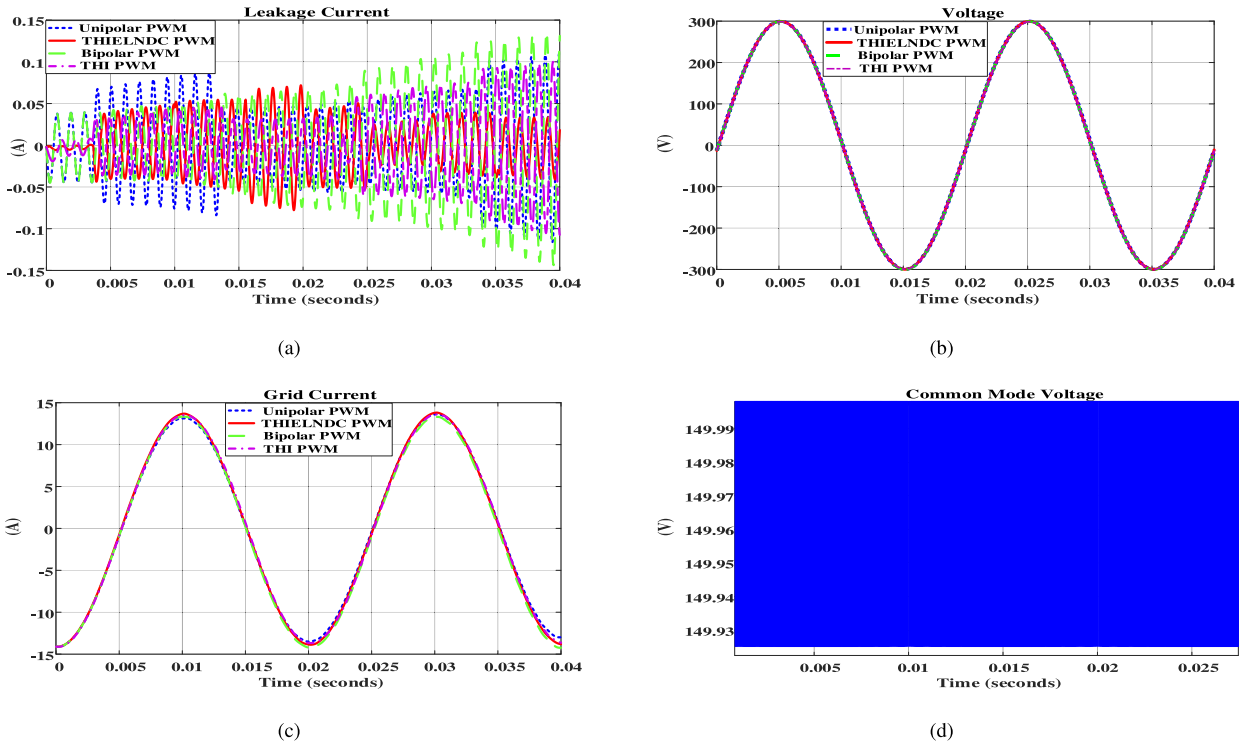


FIGURE 26. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of H6-ANPC topology with ILQG controller.

It is noticeable from the Table 5 that the r.m.s value of leakage current with H5 topology is very low for THIELNDC-PWM and the THD of grid current is much higher for THI-PWM as compared to other modulation techniques. The r.m.s value of leakage current with HERIC-I, HERIC-III, HERIC-IV, HERIC-V, HERIC-V-PNPC, H6-ANPC, H6-PNPC and improved H6 topologies is lowest for THIELNDC-PWM and for other topologies it is true for

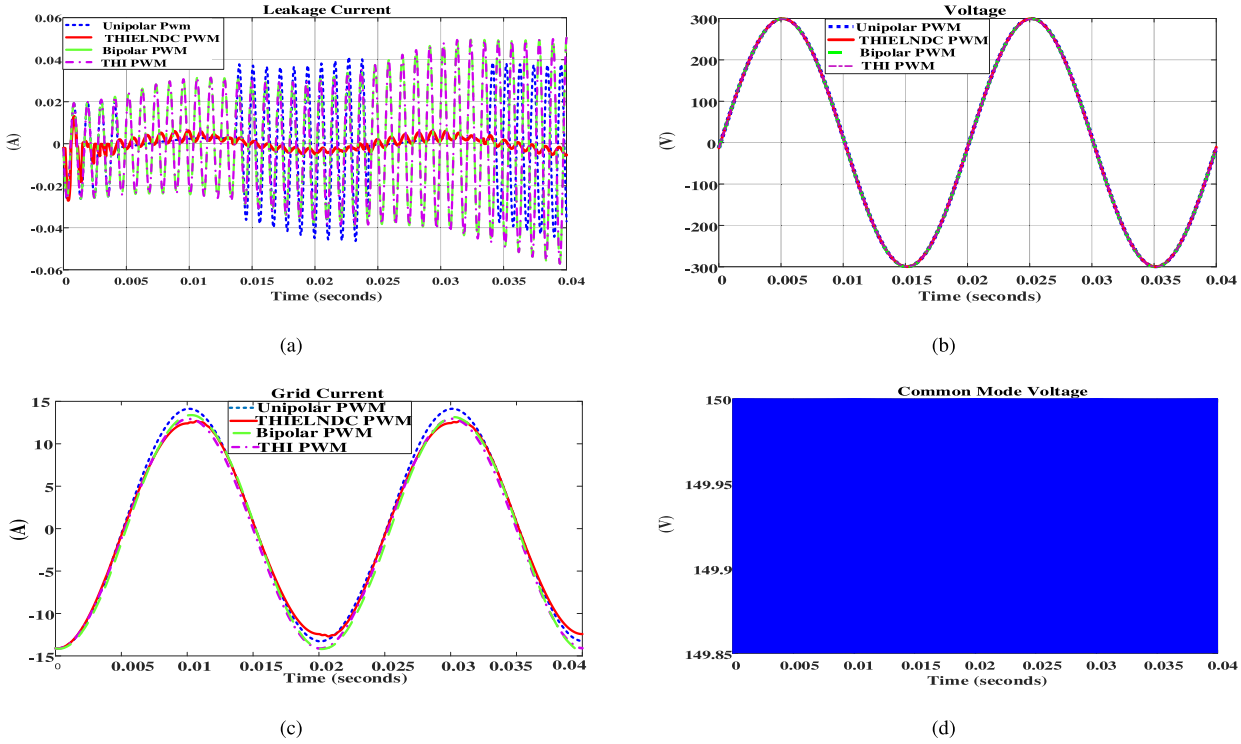


FIGURE 27. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of H6-PNPC topology with ILQG controller.

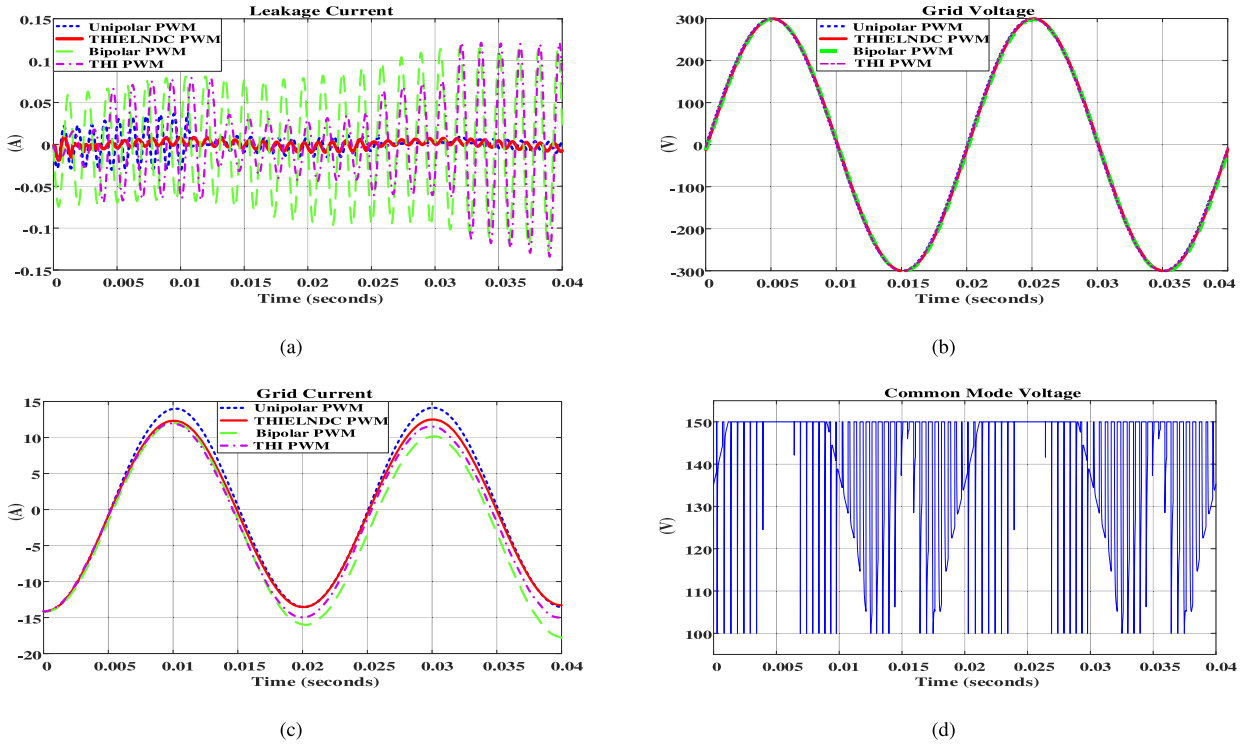


FIGURE 28. (a) Leakage current, (b) Grid voltage, (c) Grid current and (d) CM voltage of Improved H6 topology with ILQG controller.

unipolar PWM. The THD of grid voltage and grid current for all the existing topologies are good enough, which indicates the usefulness of the inclusion of ILGQ controller. The THD of grid voltage is extremely satisfactory for all the modulation techniques, though the THD of grid current is more reliable for unipolar-PWM technique.

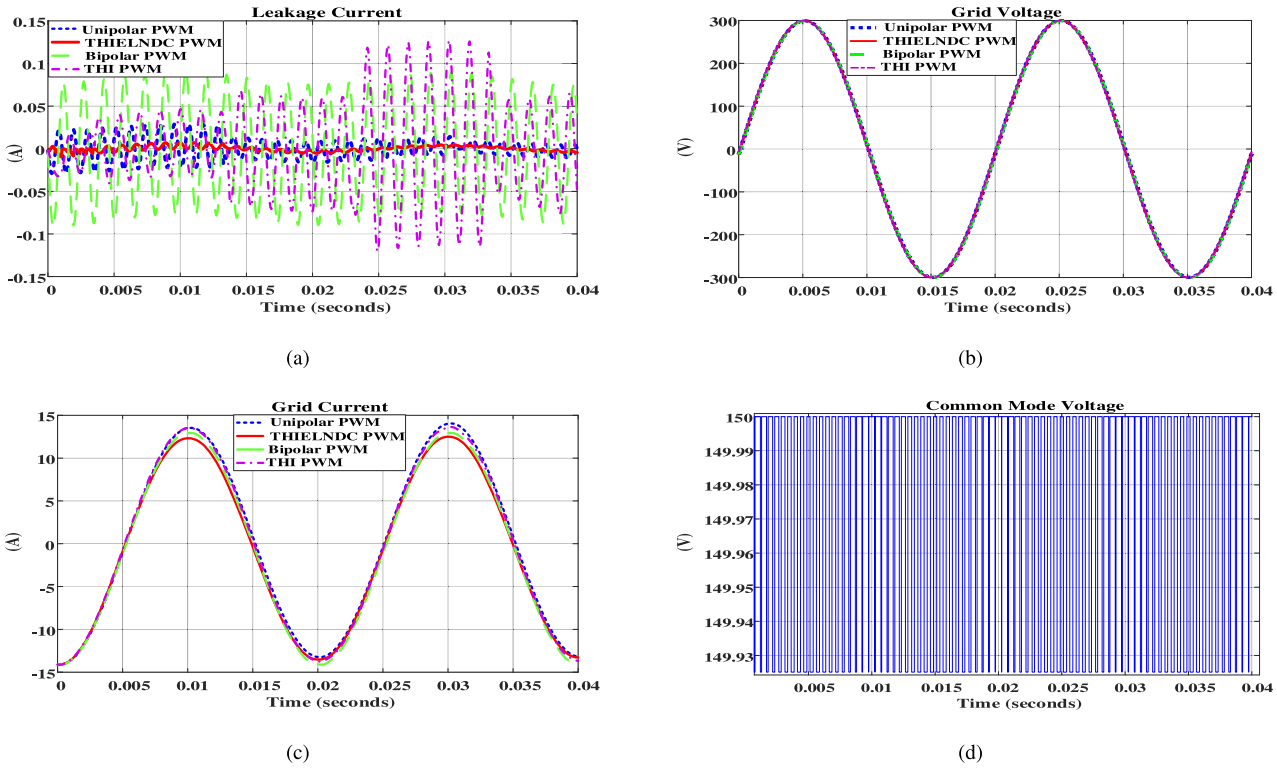


FIGURE 29. (a) Leakage current, (b) Grid voltage,(c) Grid current and (d) CM voltage of Improved H5 topology with ILQG controller.

TABLE 4. Design parameter values for ILQG.

Design parameter	ν_1	ν_2	ν_3	q	r
ILQG Controller	1×10^8	1×10^4	1×10^{-2}	1×10^5	1×10^{-2}

A. OUTPUT PERFORMANCE FOR DESIGNED H5 TOPOLOGY

To improve the CM characteristics, designed H5 topology employs a passive clamping circuit which is able to reduce the high frequency component in CM voltage and keeps it almost constant (149.925V to 150 V) as shown in Fig. 29(d). This constant CM voltage is able to reduce the leakage current to a great amount. Comparing with all those methodologies, the designed H5 with ILQG controller provides satisfactory result as shown in Fig. 29(a). Among them unipolar PWM exhibits the lowest leakage current of just 0.935 mA as shown in Table 5. It is worth mentioning that, in this work, we tried to find how much affects the direction of clamping diode, D_c has, and found that the revised direction of D_c gave worse results in every aspect with compare to the designed one. For example, with unipolar PWM modulation technique, its leakage current was 18.26 mA, while the designed one considers only 0.935 mA.

IX. COMPARATIVE ANALYSIS

This section presents a comparison of the designed H5 topology with the existing topologies with different modulation techniques in presence of ILQG controller to reduce the leakage current. This comparative analysis is important to find out the most optimum modulation technique for the inverter to reduce the leakage current as well as the THD of grid voltage and current. The design of ILQG controller is presented in this paper to produce the gate drive signal efficiently which is fed to the inverter to stabilize the voltage. The performances of the ILQG controller with different topologies and modulation techniques have been investigated in the MATLAB/Simulink environment. Table 3 highlights the different topologies in detail with different parameters. The r.m.s value of the leakage current and percentage of the THD of grid voltage and current have been reported in Table 5. This table and the simulated results are the evidents that the designed H5 topology with ILQG controller shows the satisfactory result as compared to the other topologies. The proposed blended technique with unipolar PWM reduces the leakage current to a lowest value as compared to other topologies with other modulation techniques. This unipolar PWM with ILQG controller provides the most optimum control performance to reduce the leakage current of the inverter as well as the THD of the grid voltage and current and stabilize its performance.

TABLE 5. Comparison of different performance parameters for various topologies with different modulation techniques including ILQG controller.

Topology	THI			Bipolar-PWM			Unipolar-PWM			THELNDCPWM		
	THD of Voltage (%)	THD of Current (%)	Leakage Current (A)	THD of Voltage (%)	THD of Current (%)	Leakage Current (A)	THD of Voltage (%)	THD of Current (%)	Leakage Current (A)	THD of Voltage (%)	THD of Current (%)	Leakage Current (A)
H5	0.09	0.07	0.03224	0.04	0.11	0.01804	0.08	0.05	0.02079	0.09	0.95	0.004669
HERIC-I	0.12	1.61	0.02674	0.1	2.36	0.02384	0.03	0.11	0.009586	0.04	1.88	0.00226
HERIC-I-PNPC	0.29	0.81	0.02187	0.19	1.92	0.03199	0.03	0.07	0.0128	0.04	1.72	0.01915
HERIC-II	0.28	1.5	0.05086	0.03	1.32	0.07271	0.01	0.48	0.003494	0.04	1.04	0.1676
HERIC-III	0.10	2.35	0.004857	0.35	9.01	0.3307	0.04	1.12	0.009413	0.07	1.83	0.003677
HERIC-IV	0.05	1.3	0.6496	0.02	0.56	0.08689	0.06	1.03	0.06244	0.03	0.81	0.00271
HERIC-V	0.17	4.2	0.1054	0.04	0.86	0.1054	0.06	1.47	0.005399	0.02	0.41	0.003794
HERIC-V-PNPC	0.28	6.81	0.1283	0.31	2.77	0.02424	0.06	1.49	0.05888	0.03	0.65	0.001966
H6	0.34	0.76	0.02948	0.05	0.17	0.04718	0.06	0.51	0.003503	0.06	0.97	0.009191
H6-ANPC	0.01	0.59	0.09844	0.06	1.53	0.5646	0.04	0.95	0.07838	0.02	0.58	0.01354
H6-PNPC	0.18	4.43	0.1417	0.15	3.42	0.04904	0.05	1.65	0.02271	0.1	2.65	0.005344
Improved H6	0.04	2.12	0.0289	0.35	3.81	0.01509	0.03	1.67	0.006971	0.05	0.95	0.006868
Improved H5	0.03	0.68	0.05664	0.03	0.08	0.001336	0.01	0.08	0.000935	0.06	0.95	0.003558

X. CONCLUSION

The better performance of MG largely depends on the proper control of the voltage source inverter. The production of the leakage current through the parasitic capacitance is the main limitation of the transformerless inverter that hampers the safe operation. This paper presents an improved H5 inverter topology with ILQG controller to reduce the leakage current by maintaining a constant CM voltage. Thus, it reduces the THD of the grid voltage and current. The design of ILQG controller produces the gate signal of the inverter efficiently and stabilize the voltage of the MG. This paper presents a comparative analysis among the improved H5 topology with the H5 topology, HERIC family and H6 family topologies and shows their performances with ILQG controller for different types of modulation techniques. It is clear from Table 5 that the blended technique of improved H5 topology including ILQG controller with unipolar PWM provides the most optimum performance in the case of reduction of leakage current, as well as the THD of grid voltage and current. This work will be extended for the three-phase MG to investigate its performance with ILQG controller under different modulation techniques.

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