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Comparison of Two Design Methods of EMI Filter for High Voltage Power Supply in DC-DC Converter of Electric Vehicle

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ABSTRACT In order to solve the problem that the conducted interference voltage of a high voltage/low voltage (HV/LV) DC-DC converter for vehicles exceeds the standard CISPR25-2016, two different design methods of EMI filter for HV power supply were proposed. The first method is to design a wide-band EMI filter at the high-voltage input port of the DC-DC converter. It can achieve the insertion loss of 60dB within 150kHz-108MHz. Another proposed method is to design a PCB-level EMI filter based on the resonance peaks suppression. During the PCB-level EMI filter design process, a high frequency equivalent circuit model of HV/LV DC-DC converter of EV considering the parasitic parameters was established, and by establishing the transfer functions at key frequencies of 200 kHz and 2 MHz, the dominated parameters responsible for the over-standard points were determined. From simulation and experiment results, the filters designed by above two methods can effectively reduce the conducted disturbance and comply with the limits requirements in 150kHz-108MHz. What's more, the PCB-level filter designed by the second method is smaller in size, only 1/5 of the filter size designed by the first method, lower in cost,and easy to be engineering.

INDEX TERMS Electric vehicle (EV), DC-DC converter, conducted electromagnetic interference (EMI), EMI filter, EMI suppression.

I. INTRODUCTION

As an energy-saving and environmentally-friendly new energy product, EVs have developed rapidly in the world in recent years [1], [2]. Unlike conventional internal combustion engine vehicles (ICEV), EVs use a large number of high-voltage components, like drive motor, DC-AC inverter, DC-DC converter, on-board charger, power battery, etc. In addition, many low-voltage electrical components such as battery management systems (BMS), vehicle control units (VCU), and Telematics BOX (TBOX) etc. are also used in EV. Therefore, the electromagnetic environment of EVs has become more complicated, and electromagnetic compatibility (EMC) of EVs has become more and more important. In order to protect the on-board and off-board receivers from disturbances produced by conducted and radiated emissions arising in EVs, some international standards like SAE J551-5, CISPR12-2009, CISPR25-2016, and some Chinese standards like GB/T 18387-2017, GB/T 14023-2011 and GB/T 18655-2018 are proposed and they set the limits for conducted and radiated emissions from EVs and components. So EMC design has become a key technology for EVs.

Unlike conventional ICEVs, low voltage power supply of 12V or 24V is need to be provided by the HV/LV DC-DC converter in EVs. The HV/LV DC-DC converter in EV is used to convert hundreds of volts of high-voltage direct current of power battery into low-voltage direct current to charge on-board low-voltage batteries, and supply power to low-voltage on-board electrical components [3]. The DC-DC converter typically uses power semiconductor devices (such as IGBTs, MOSFETs, etc.) to implement pulse width modulation (PWM) control to regulate the output low voltage [4], [5]. Fast switching on and off of the power semiconductor devices generates high current change rate *di/dt* and voltage

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change rate *du/dt*, which forms electromagnetic disturbance signal and propagates outward through the parasitic parameters [6]–[8], forming undesirable conducted and radiated disturbances. It would not only interfere with the on-board and off-board receivers, but also interfere with the on-board high-voltage and low-voltage components through the conducted interference coupling path, such as DC-AC inverter, BMS, VCU, etc., [6], and even affect the safety of the vehicle. In particular, the conducted EMI generated by the HV/LV DC-DC converter may cause the radiated emission of the HV/LV DC-DC converter to exceed the standard limits, and even cause the radiated emission of the vehicle to fail to meet the requirements of the EMC standards.

In order to finally ensure the electromagnetic compatibility of EV and make the electromagnetic emission of the whole vehicle meet the standard requirements, the international standard CISPR25-2016 and the Chinese standard GB/T18655-2018 provide conducted disturbance limits of the high and low voltage components of the EV in the frequency range of 150 kHz-108 MHz. A large number of test results show that HV/LV DC-DC converters without EMC design can hardly meet the requirements of the standard limits level 3 [4]. Thus, additional EMI filters are added to pass the test. However, the rectification of EMI suppression during the test phase would increase the cost of product development and extend the development cycle.

Although DC-DC converters are also used in switching power supply for industrial applications, a lot of research has mainly studied the EMI analysis and filter design of PCB level DC-DC converters [9]–[12]. However, the topology, voltage type and level, and load characteristics of DC-DC converters for switching power supply are different from those of HV/LV DC-DC converters for EV. In addition, the applicable EMC standards and EMI suppression frequency band requirements are also different. Therefore, the EMI generation mechanism and suppression method of switching power supplies for industrial applications are not suitable for the HV/LV DC-DC converters of EV.

At present, in the field of electric vehicles, most of the research of EMI from DC-DC converter is mostly focused on low-voltage PCB board-level DC-DC converters [13], [14]. Based on the dual-port network theory, the effects of PCB parasitic parameters, DC-DC switching techniques and layout topology optimization on the EMI from the switching of DC-DC device on PCB boards are analyzed in [15], [16]. The HV/LV DC-DC converter of EV is different from the DC-DC converter of low-voltage PCB, and there are the following differences: First, the input DC voltage range of the HV/LV DC-DC converter is 200V∼900V, not DC12V∼24V of the low voltage DC-DC converter. Second, the HV positive and negative power supply lines of HV/LV DC-DC converters are isolated from ground, while the negative line of the low-voltage DC-DC converter is grounded, so their EMI propagation paths are different. Third, the HV/LV DC-DC converter supplies power to all the low voltage components of the EV. Due to the characteristics of high input voltage, large output current and dynamic load changes, the power devices need to be adjusted in real time [3], [17]. Finally, because the output low-voltage power supply harness of the HV/LV DC-DC converter is more and longer, the conducted emission is easier to form radiation emission. Therefore, the EMI suppression methods of LV DC-DC converters are not suitable for HV/LV DC-DC converters.

At present, there are few studies on the formation mechanism and suppression method of conducted EMI in HV/LV DC-DC converters of EVs. The EMI suppression of the HV DC power supply still adopts the industrial classic filter design methods, and its EMI suppression frequency band is lower than 30MHz. At present, the design theory and method of EMI filters for high-voltage DC power systems in the frequency band of 150kHz-108MHz are lacking. When the conducted emission of the DC-DC converter appears to exceed the standard, an EMI filter is usually installed at the DC HV input port of the HV/LV DC-DC converter. The EMI filter had to need several rectifications to make the HV/LV DC-DC converter pass the standard test. This type of filter can only be installed in the later stages of product design, which results in high costs and long cycles in research and development, and it is not easy to implement in engineering. In addition, these HV port filters are designed based on the interference source impedance of 50Ω, without considering the actual source impedance of HV/LV DC-DC converter, resulting in the deviation between the actual value of the insertion loss of the filter and the expected value. Since the DM and CM components of conducted disturbance are not separated, the DM filter circuit and the CM filter circuit are required to have the same insertion loss. And since it is impossible to predict the frequency points or frequency bands that the conducted disturbance may beyond the standard value, the filter can only be required to have the same insertion loss in the whole frequency band of 150kHz-108MHz. The above two reasons lead to the over design of filter insertion loss, resulting in the increase of filter volume. In addition, the EMI filter cannot be added into the actual DC-DC converter system for on-load operation to verify the actual effective insertion loss of the filter.

In order to effectively suppress the conducted disturbance on the DC HV power lines of the HV/LV DC-DC converter, it is very important for the filter design to predict the CM and DM components of the conducted disturbance. EMI prediction usually uses simulation and experimental measurement methods. Because the conducted disturbance values obtained by the test measurement method are the sum of the CM and the DM disturbance components, the coupling paths and key parasitic parameters of CM and DM EMI can not be determined. In recent years, the modeling and simulation method have become a research focus of EMI prediction. Most of the previous modeling and prediction of conducted EMI for the HV/LV DC-DC converters of EVs are based on port network theory and black box theory, where the HV input ports of the converter are equivalent to EMI sources to analyze the relationship between interference

sources and electromagnetic noise. The influence of internal circuit parasitic parameters on the coupling path is not considered [12], [14]. In some researches, the ideal trapezoidal wave is equivalent to the interference source, without considering the parasitic parameters of MOSFETs and other switching devices, which cannot reflect the real signal characteristics of the interference source. The MOSFET interference source and the propagation path of CM and DM interference of the isolated full-bridge DC-DC converter for EV with input voltage of 120-160V and 200W is proposed in [19]. However, the influence of high frequency parasitic parameters on EMI propagation paths has not been fully considered. On the basis of considering the influence of parasitic parameters of power switching devices, cables and transformers, a conducted EMI prediction model for the HV/LV DC-DC converter system of hybrid EV was established, and only qualitative analysis of EMI propagation was proposed in [20]. Although some scholars have studied the influence of parasitic parameters such as MOSFET lead inductance on CM interference [13]–[15], no quantitative analysis has been made on conducted EMI of the system. Because the high-frequency circuit composed of parasitic parameters of the DC-DC converter is not modeled, the propagation paths of CM and DM conducted EMI can not be accurately determined, and the parasitic elements inside the DC-DC converter responsible for CM and DM conducted disturbance resonance can not be determined. Therefore, it is impossible to guide the design of DC-DC converter HV power EMI filters at the early stage of product design [4], [22]–[24].

The highlights of the paper is described as follows:

(1) A high-frequency equivalent circuit model of the HV/LV DC-DC converters with zero-voltage switching (ZVS) considering parasitic parameters of MOSFET is established to predict conducted EMI. Since through the model the actual EMI source impedance can be simulated, it provides a simulation platform for the prediction and suppression of conducted EMI.

(2) The transfer functions of CM interference and DM interference are established to predict the CM component and DM component of conducted disturbance in high voltage power lines, and the dominated circuit parameters responsible for the conducted disturbance voltage exceeding the standard limits at key frequencies are determined.

(3) In order to effectively suppress the conducted EMI and comply with the limits requirements by CISPR25-2016 in the wide frequency range of 150kHz∼108MHz, a design method of high-voltage filter with insertion loss of 60dB is proposed, considering three typical interferences from the HV/LV DC-DC converter of EV, i.e. switching frequency harmonic, low-frequency DM interference and high-frequency CM interference.

(4) Based on the harmonic and resonance peaks exceeding-standard limits, a PCB-level filter circuit design method is proposed. It is characterized by small size, low cost and high efficiency, which can be realized in different development stages of products.

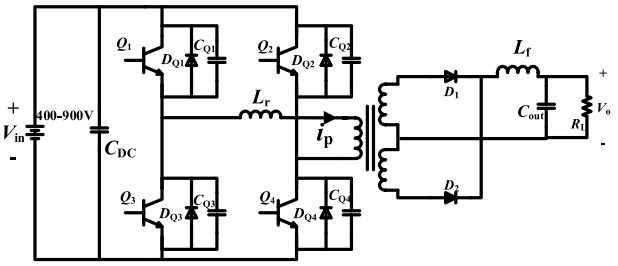


FIGURE 1. Topology of ZVS isolated full-bridge DC-DC converter.

The organization of this paper is as follows: Section 2 builds a HV/LV DC-DC converter system and its high-voltage system conducted EMI test platform. Section 3 presents the design method of a general wide-band HV input port EMI filter for DC-DC converter. In Section 4, by analyzing the generation mechanism of conducted interference in HV/LV DCDC converter, an internal PCB board-level filter circuit based on resonance point suppression is proposed. And Section 5 verifies and compares the effects of the filters through simulation and experiment. Finally, Section 6 explains the conclusions.

II. CONDUCTED EMI TEST PLATFORM

A. STRUCTURE OF THE DC-DC CONVERTER

A HV/LV DC-DC converter for commercial EV usually uses isolated full bridge topology. As shown in Fig.1, the HV/LV DC-DC converts DC high voltage of power batteries into DC low voltage to supply power for on-board low voltage electrical components. When the HV/LV DC-DC converter is controlled by PWM mode, the MOSFET operates in the hard switching mode, which causes a large switching loss. The phase-shifted PWM control mode utilizes the resonance between transformer leakage inductance and MOSFET junction capacitance to realize zero voltage switching (ZVS) of the MOSFET, which is beneficial to improve efficiency and switching frequency, while reducing EMI caused by the switching-on and-off of the MOSFET.

A prototype of the 3.6 kW DC-DC converter is used to test with the input voltage range of DC 400∼900V. The rated output voltage is 27V, the peak value of the input current is 10A, and the maximum output current can reach 119A. Four MOSFETs with 100 kHz switching frequency are used in the isolated full bridge topology of the DC-DC converter, as shown in Fig.1. Where, C_{DC} is the filter capacitor on the high-voltage input side, and D_{Q1}∼D_{Q4} are the anti-parallel diodes of the MOSFETs Q_1∼Q_4, C_{Q1}∼C_{Q4} is the resonant capacitor corresponding to each MOSFET, L_r is the resonant inductor, L_p is the leakage inductance of the transformer, L_f and C_{out} are the filtering inductor and filtering capacitor on the low voltage side respectively, R_L is the equivalent load resistance on the low voltage side, and D_1 and D_2 are rectifier diodes of the secondary side of transformer T_r.

B. TEST SETUP FOR THE CONDUCTED EMI

According to CISPR25-2016 (GB/T 18655-2018), the test arrangement of the conducted disturbances-voltage method

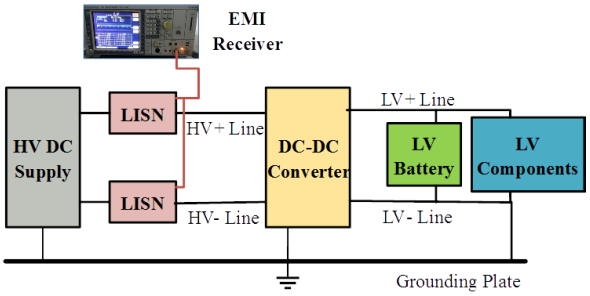


FIGURE 2. Conducted EMI test layout.

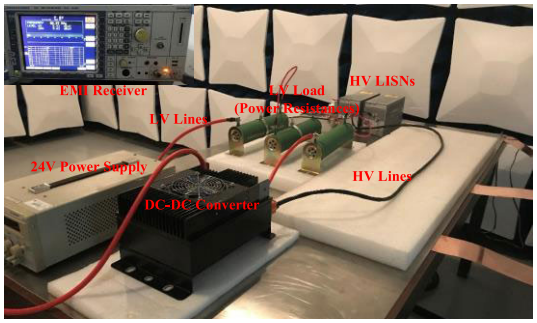


FIGURE 3. Conducted disturbances-voltage method test platform.

for the HV/LV DC-DC converter is shown in Fig.2. It mainly consists of a high voltage DC power supply, two line impedance stabilization networks (LISNs), the high voltage DC power supply lines with a standard length of 1.5m, the HV/LV DC-DC converter, two low voltage power supply lines with a standard length of 1m, a low voltage resistive load and a EMI receiver. The conducted voltage of the high-voltage positive bus and the negative bus in the frequency bands of 150kHz-108MHz should meet the limit level defined by CISPR25-2016. Fig. 3 shows the prototype layout of the test platform on a grounded copper plate in a shielding room.

Under the normal operation with 20% of the peak current, Fig.4 shows the experimental results of the conducted voltage with the limit lines in the frequency bands of 0.15-0.30 MHz, 0.53-1.8 MHz, 5.9-6.2 MHz, 30-54 MHz, 48.5-72.5 MHz, 68-87 MHz and 76-108 MHz required by the standard CISPR25-2016.

It can be found that the conducted voltages of the high voltage positive line exceed the average level of 5 standard limits.

There are couple of obvious conducted voltage values exceeding the standard limits at 800 kHz, 900 kHz, 1.2 MHz, 1.3 MHz, 1.4 MHz, 1.5 MHz, 1.6 MHz, 1.7 MHz, 1.8 MHz, 5.9-6.2 MHz, and 72 MHz, etc.

III. WIDE-BAND HV INPUT PORT FILTER DESIGN

There are two methods for EMI filter of high voltage power supply proposed to reduce the conducted disturbance in the frequency range of 150kHz∼108MHz by standard CISPR25-2016.

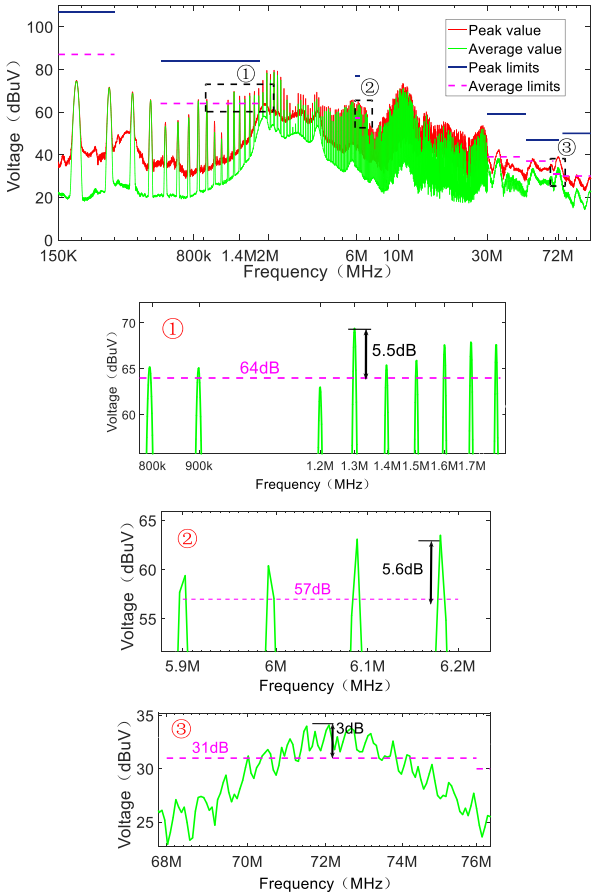


FIGURE 4. Experimental results of the conducted voltage.

Method 1: the EMI filter design of HV power supply input port of the HV/LV DC-DC converter is adopted in the case of unclear knowing the EMI source and propagation path. This method is suitable for EMC rectification in the later stage of product design.

A. TOPOLOGY OF THE FILTER

The source impedance and load impedance should be considered in the topology design of the filter. The input of the filter is connected to the high voltage DC power supply port of the DC-DC converter, where the high voltage port has been equipped with a large capacitor for absorbing voltage ripple, its impedance is low. The output of the filter is connected to the high-voltage power battery, which shows capacitance and low impedance. Since the source impedance and the load impedance of the filter are both low impedance, a T-type circuit was selected as the basic circuit of the DM EMI filter. Based on the T-type circuit, a CM EMI filter is designed by adding a CM choke coil and a Y capacitor.

B. DETERMINATION OF FILTER SERIES AND CUTOFF FREQUENCY

The series n of filters and the cutoff frequency f_0 of each stage are primarily related to the frequency range and insertion loss

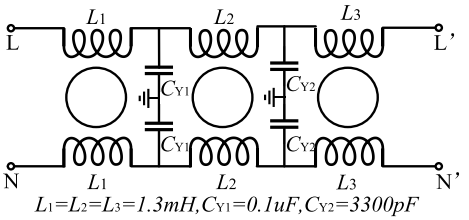


FIGURE 5. Filter topology.

requirements. In general, the slope of insertion loss curve of a single-stage filter will basically follow 20*n* dB/10dec between the cutoff frequency and the 10 times the cutoff frequency. The filter is required suppress EMI in the full frequency range of 150k-108MHz and insertion loss requirement is at least greater than 20 dB. However, the insertion loss curve will gradually deviate from the theoretical curve between 10-100 times the cutoff frequency, but it can still maintain 20*n* dB insertion loss. After 100 times the frequency, the suppression effect will gradually deteriorate until there is no filtering effect. Therefore, the requirement of insertion loss of the filter is 60 dB in the wide frequency range of 150k-108MHz. In general, single-stage filters cannot meet the requirements of insertion loss 60dB. Although the insertion loss will be improved as the number of filter series increases, it will cause the filter volume to multiply, so the filter is initially designed as a two stages LC filter, as shown in Fig. 5. The CM filter circuit consists of three same CM chokes with inductance L_1, L_2, L_3 respectively and two pairs of Y capacitors (2 C_{y1} and 2 C_{y2}) to suppress the CM EMI current. The leakage inductance of the CM choke and the two connected Y capacitors are connected in series to form a DM filter circuit to suppress the DM EMI current. Since the basic circuit is a T-shaped circuit, the number of components is 3, and the slope of the insertion loss curve below 10 times the cutoff frequency can satisfy 60 dB/10 decade. Therefore, the cutoff frequency of the first-stage *LCL* filter circuit needs to be lower than 15 kHz, so that the filter circuit can meet the 60 dB insertion loss requirement at 150 kHz, and finally the first cutoff frequency is selected to be 10 kHz. The second stage filter is designed to supplement the first stage filter when the suppression effect become worse after 100 times the first cutoff frequency. Therefore, the second cutoff frequency should be below 1MHz, and the final determination is 400kHz considering the parameter variation and load effects. As the frequency increases, the influence of the parasitic parameters of the filter elements will cause the filtering effect to decrease. After 10MHz, the CM choke L_3 is used to suppress the high frequency EMI.

C. DETERMINATION OF FILTER PARAMETER

The leakage current of the filter is mainly determined by the value of the common-mode capacitance of the filter. Compared with C_{Y1}, the value of C_{Y2} is much smaller, which means that the leakage current is mainly determined by C_{Y1}. Therefore, the value of CY1 was determined according to the limit of the leakage current, $C_{Y1} = 0.1\ \mu$F.

And the value of the inductor L_1 was calculated according to (1), $L_1 = 1.3$mH.

$$L_1 = \frac{1}{8\pi^2 C_{Y1} f_1^2} \tag{1}$$

In order to simplify the design process, the three CM chokes $L_1L_2L_3$ was chosen to have the same value, 1.3mH.

Then the value of C_{Y2} can be calculated according to (2), $C_{Y2} = 3300$pF.

$$C_{Y2} = \frac{1}{8\pi^2 L_2 f_2^2} \tag{2}$$

According to (3), the CM choke core is selected as Mn-Zn ferrite. Its magnetic permeability is low at low frequencies, but as the frequency increases, its magnetic permeability changes little, so it has excellent performance in high frequency.

$$L = \frac{k\mu_0\mu_r N^2 S}{l} \tag{3}$$

where, L is the inductance of the coil, taken as 1.3mH, l is the length of the coil along the magnetic ring, taken as 30mm, N is the number of turns of the coil, S is the cross-sectional area of the coil, taken as 60mm^2, and u_0 is the air permeability, taken as $4\pi^*10^{-7}$ H/m, u_r is the relative magnetic permeability of the core, taken as 5000, k is the long-haze coefficient, determined by the ratio of the radius of the winding to the length, here is 0.7.

$$N = \sqrt{\frac{Ll}{k\mu_0\mu_r S}} = \sqrt{\frac{1.3\times10^{-3}\times30\times10^{-3}}{0.7\times5000\times4\pi\times10^{-7}\times60\times10^{-6}}} = 12.12 \tag{4}$$

Based on (4), $N = 12$ can be obtained. The leakage inductance of a CM chock coil is 13 uH, which is 1% of the CM inductance.

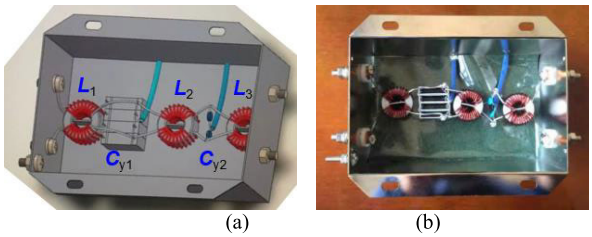
D. 3D LAYOUT AND PROTOTYPE

Since the operating voltage of the high-voltage DC port filter is 400∼1000V, the withstand AC voltage of the general safety capacitor is 275 V, equivalent to a DC voltage of about 600V. Therefore, each of C_{y1} and C_{y2} needs two capacitors in series. The actual 3D layout and prototype of the filter are shown in Fig.6.

E. INSERTION LOSS MEASUREMENT

According to Fig. 5 and the standard CISPR17-2011 for filter insertion loss measurement, the CM insertion loss and DM insertion loss of the filter are obtained by modeling and simulation in the software ADS, as shown in Fig. 7.

From the simulation results in Fig.7, it can be seen that the CM insertion loss of the filter with the source impedance and the load impedance of 50 ohms meets the requirement of 60 dB in the full frequency range of 150k-108MHz. Although the DM insertion loss can not meet the requirement



(a) (b)

FIGURE 6. High-voltage port filter. (a) Filter model. (b) Experimental prototype.

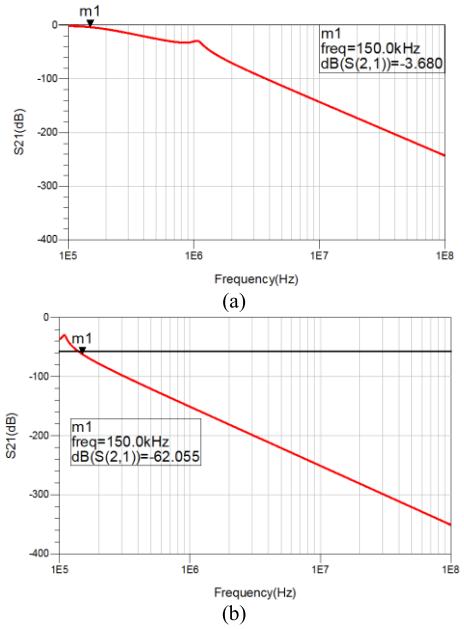


FIGURE 7. Insertion loss simulation results of the high voltage port filter. (a) DM insertion loss simulation and results. (b) CM insertion loss simulation and results.

of 60dB at low frequency, the low frequency DM EMI can be suppressed by using the filter capacitor C_{DC} inside the DC-DC controller.

Due to electromagnetic coupling between the input and output cables of the filter at high frequencies, the accuracy of measurement results of insertion loss will be affected. Then the measurement of insertion loss is not implemented. In order to verify the actual suppression effect of the filter, the filter was added to the HV/LV DC-DC converter system in Section 5.

IV. DESIGN METHOD OF FILTER CIRCUIT BASED ON EMI SUPPRESSION AT RESONANCE FREQUENCY

According to the experimental results of the conducted voltage based on CISPR25-2016, the CM and DM current propagation path and the mainly dominated element parameters responsible for EMI noise at the two key frequencies of 200 kHz and 2 MHz were analyzed. The filter circuit on PCB was proposed as the other design method, which is the mainly innovation of this paper.

TABLE 1. The main technical parameters of MOSFET (SiHG17N80E).

Parameters	Typical value	Unit	Condition
V_{DS}	850	V	T_J=25°C
$R_{DS(on)}$	0.25	Ω	T_J=25°C
C_{iss}	2408	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
C_{oss}	81	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
C_{rss}	9	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
t_r	24	ns	V_{DD} = 480 V, I_D = 8.5 A, V_{GS} = 10 V, Rg = 9.1 Ω
t_f	26	ns	

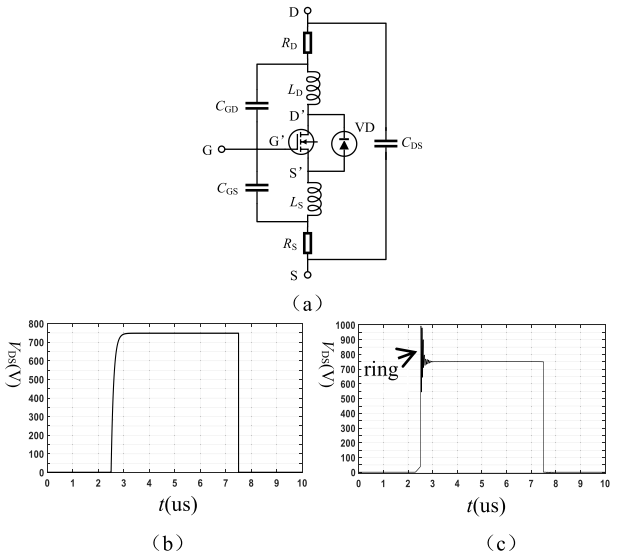


FIGURE 8. MOSFET equivalent circuit and drain-source voltage V_{DS}. (a) Equivalent circuit model of MOSFET (b) Ideal voltage waveform of V_{DS} (c) Actual voltage waveform of V_{DS}.

A. EMI SOURCE

SiHG17N80E MOSFET for automobile is used in the HV/LV DC-DC converter, and its switching frequency is 100 kHz. The main technical parameters of the MOSFET are shown in Table 1.

As shown in Fig.8(a), an equivalent circuit model of MOSFET considering parasitic parameters was established. Where V_D is a parasitic diode; the three junction capacitors of the MOSFET are respectively the inter-electrode capacitance C_{GS} between the gate and the source, the inter-electrode capacitance C_{GD} between the gate and the drain, and the inter-electrode capacitance C_{DS} between the source and the drain; and $C_{iss} = C_{GS} + C_{GD}$, $C_{oss} = C_{DS} + C_{GD}$, $C_{rss} = C_{GD}$; L_S and L_D are the lead inductors of the source and drain; R_S and R_D are the resistances of the corresponding leads. The voltage waveform obtained between the drain D' and the source S' of MOSFET in ideal case and considering the parasitic parameters are respectively shown in Fig.8(b) and 8(c). Fig.9 shows the spectrum of the voltage waveform V_{DS} in Fig.8(b), from which the effect of turn-on time t_{on} and rise time t_r of MOSFET, and ringing at the rising edge on V_{DS} spectrum can be seen. It can be seen from Fig. 9 that

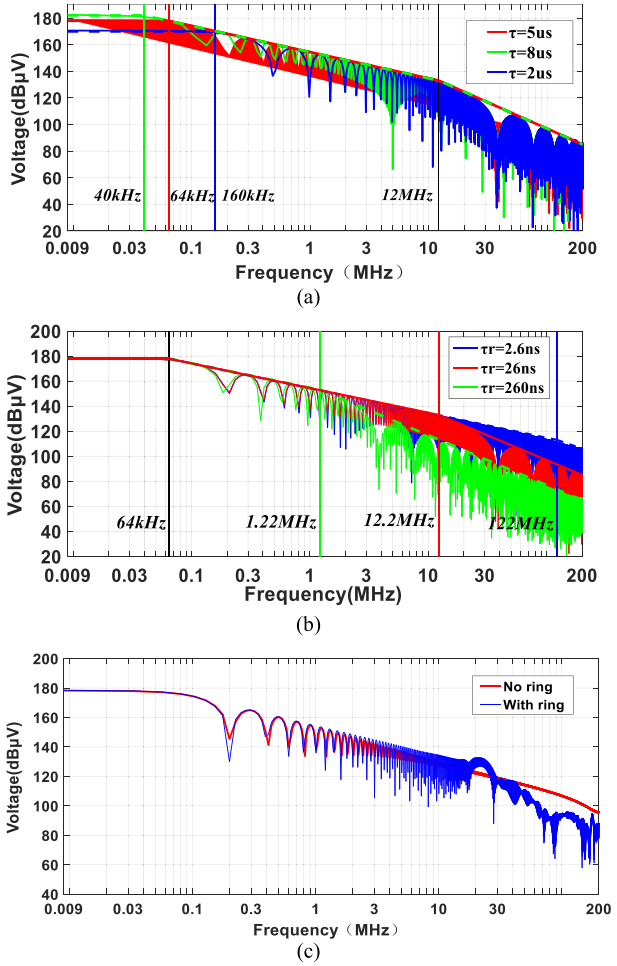


FIGURE 9. Spectrum of V_{DS}. (a) Influence of t_on. (b) Influence of t_r. (c) Influence of ring.

the longer the t_{on} is, the lower the first cutoff frequency is, and the higher the amplitude of V_{DS} in the low frequency band is. While the shorter the t_r is, and the higher the second cutoff frequency is, the higher the amplitude of V_{DS} in the high frequency band is.

The ringing at the rising edge of the pulse of V_{DS} causes a resonance point in the spectrum of V_{DS} around 20MHz, and then the amplitude of V_{DS} decreases as the frequency increases.

Due to the high amplitude of V_{DS}, the disturbance current in the wider frequency range of 150kHz-108MHz is easily formed by parasitic parameters, and finally causes conducted EMI on the high voltage power supply cables. For bench test conditions, the switching frequency, t_{on} and t_r of the MOSFET are usually constant, so the conducted EMI voltage is mainly related to the disturbance current propagation paths.

B. HIGH-FREQUENCY EQUIVALENT CIRCUIT MODEL OF THE HV/LV DC-DC CONVERTER SYSTEM

The spectrum of V_{DC} as EMI source signal is analyzed in Fig. 9. As shown in Fig.10, the high frequency equivalent

TABLE 2. The main parasitic parameters of the system.

Parameters	Description	Value
C_{DC}	HV side filter capacitor	0.4μF
C_{Q1},C_{Q2}, C_{Q3},C_{Q4}	Resonant capacitors	8nF
L_r	Resonant inductor	30μH
L_f	LV output filter inductor	50μH
R_L	Load resistance	0.48Ω
C_{out}	LV output filter capacitor	200μF
R_1、R_2	Standard resistances of LISN	50Ω
L_1、L_2	Standard inductors of LISN	50μH
C_1、C_2	Input side capacitors of LISN	5μF
C_3、C_4	Output side capacitors of LISN	470nF
C_{p1}、C_{p2}	Bridge arm midpoint to chassis distribution capacitors	26pF
C_{ps1}、C_{ps2}	Transformer parasitic capacitance	60pF
C_L	Load-to-chassis distributed capacitance	80pF
L_s	HV side filter capacitor parasitic inductance	0.4μH
R_s	HV side filter capacitor parasitic resistance	0.1Ω
L_{p1}、L_{p2}	HV DC cable inductance	10nH

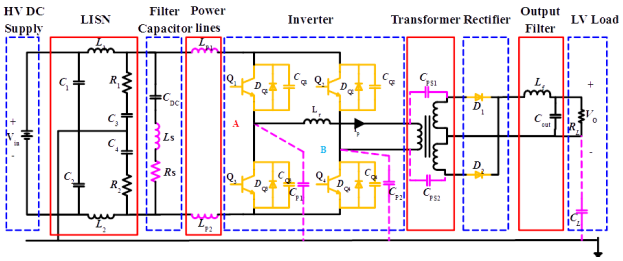


FIGURE 10. High-frequency equivalent circuit model.

circuit model of the HV/LV DC-DC converter system is established. Where the parasitic parameters of Q_1 and Q_4 are shown in Table 1. The values of the main parasitic parameters of the system are shown in Table 2, obtained by measurement or theoretical calculation [17].

C. EMI PATH ANALYSIS

It can be seen from Fig.4 that the conducted voltage of the high-voltage positive power supply line exceeding the standard limits mainly distributes in three frequency bands:

① Region 1 (0.53-1.8 MHz): In the frequency bands 0.15-0.30MHz, 0.53-1.8 MHz, the peaks of the conducted voltage are distributed at intervals of 100 kHz, such as 200 kHz, 300 kHz, ... 1.8 MHz. This is due to the harmonics generated by the trapezoidal pulse trains of the MOSFETs operating at a switching frequency of 100 kHz. Theoretically, the harmonic amplitude at 200 kHz is the largest, and the amplitude of the harmonics decreases as the frequency increases, and the conducted voltage in the

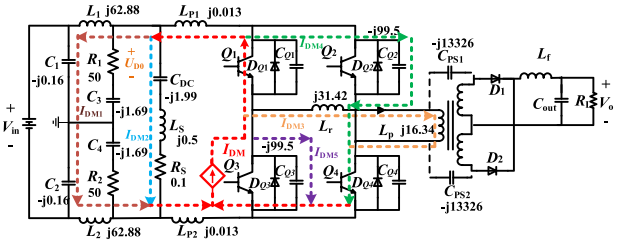


FIGURE 11. DM EMI current path at 200 kHz.

0.53-1.8 MHz band would not exceed the standard limits. However, at 800 kHz, 900 kHz, 1.2 MHz, 1.3 MHz, 1.4 MHz, 1.5 MHz, 1.6 MHz, 1.7 MHz, 1.8 MHz, the harmonic voltage amplitude increases and exceeds the limits. Due to the existence of parasitic parameters of the system, the resonance voltage is generated at 2 MHz, resulting in the increase of the harmonic peak voltage at 2 MHz. Therefore, the conducted voltage exceeding the standard limits in this region is related to the harmonics of the switching frequency 100 kHz of the MOSFETs and the resonance generated at 2 MHz. Thus, it is important to analyze the common mode (CM) interference paths and differential mode (DM) interference paths of the disturbance current at two frequencies of 200 kHz and 2 MHz, and determine the circuit parameters responsible for the conducted voltage exceeding the standard limits.

② Region 2: In the frequency band 5.9-6.2 MHz, the conducted voltage exceeds the limits by 6 dB, mainly due to the harmonics generated by the switching frequency 100 kHz of the MOSFET and the resonance at 2 MHz.

③ Region 3: The conducted voltage exceeded the standard limits at 72MHz, mainly due to the resonance caused by the low frequency harmonics and resonance of the system under the influence of high frequency parasitic parameters.

In summary, in order to reduce the conducted EMI of the high-voltage positive power line to meet the standard limits, it is only necessary to quantitatively analyze the factors responsible for the conducted EMI at two typical frequency points of 200 kHz and 2 MHz. Since the exceeding standard limits around 72MHz are mainly caused by high frequency parasitic parameters, it is difficult to perform accurate quantitative analysis.

The DC-DC converter operates with four switching modes: (1, 0), (0, 1), (0, 0) and (1, 1).Among them,the EMI source and the EMI propagation paths formed under the two working modes (1, 0) and (0, 1) are dual. Therefore, the switch of MOSFET can be equivalent to a CM EMI source and a DM EMI source on each bridge arm. Since the disturbance current paths generated by the two bridge arm DM EMI sources are completely identical, the actual DM EMI voltage is twice the voltage U_{R1} of the resistance R_1 measured by LISNs. However, the disturbance current paths generated by the two CM EMI sources are symmetrically complementary. In order to simplify the analysis, the (1,0) mode is taken as an example to analyze the propagation paths of CM and DM disturbance currents.

1) DM EMI ANALYSIS AT 200 kHz

The impedance values of the equivalent circuit parameters at 200 kHz are calculated, as shown in Fig.11. The EMI source caused by the switching of the MOSFET is equivalent to a constant current source I_{DM}. Then the following five DM current paths are formed in the high frequency circuit of the system.

① DM current path 1:

$$I_{DM1} \rightarrow L_{p1} \rightarrow \left(\begin{matrix}L_1\rightarrow C_1\\R_1\rightarrow C_3\end{matrix}\right) \rightarrow \left(\begin{matrix}C_2\rightarrow L_2\\C_4\rightarrow R_2\end{matrix}\right) \rightarrow L_{p2}$$

② DM current path 2: $I_{DM2} \rightarrow L_{p1} \rightarrow C_{DC} \rightarrow L_s \rightarrow R_s \rightarrow L_{p2}$

③ DM current path 3: $I_{DM3} \rightarrow L_r \rightarrow L_p$

④ DM current path 4: $I_{DM4} \rightarrow C_{Q2}$

⑤ DM current path 5: $I_{DM5} \rightarrow C_{Q3}$

Among them, only the DM current I_{DM1} of path 1 flows through R_1 to form the DM conducted voltage U_{R1} of the positive high voltage power line. In fact, two switching modes are considered simultaneously, $U_{DM} = 2U_{R1} = 2{*}50{*}I_{DM1}$. The relationship between U_{DM} and I_{DM} of the DC-DC converter is analyzed below. Suppose

$$Z_1 = j\omega(L_{P1} + L_{P2}) \tag{5}$$

$$Z_2 = -j\frac{1}{\omega C_{DC}} + j\omega L_S + R_S \tag{6}$$

$$Z_3 = 2(R_1 - j\frac{1}{\omega C_3})//(L_1 - j\frac{1}{\omega C_1}) \tag{7}$$

$$Z_4 = -j\frac{1}{\omega(C_{Q3} + C_{Q4})} \tag{8}$$

$$Z_5 = j\omega(L_R + L_P) \tag{9}$$

$$Z = (Z_1 + Z_2//Z_3)//Z_4//Z_5 \tag{10}$$

$$\begin{aligned} U_{DM} &= 2U_{R1} \\ &= 2 \times I_{DM} \times (Z_1 + Z_2//Z3)//Z_4//Z_5 \times \frac{Z_2//Z_3}{Z_1 + Z_2//Z_3} \\ &\quad \times \frac{1}{2}\frac{R_1}{Z_{C3} + R_1} \\ &= 2 \times I_{DM} \times \frac{(Z_1 + Z_2//Z3) \times Z_4 \times Z_5}{(Z_1 + Z_2//Z3) + Z_4 + Z_5} \\ &\quad \times \frac{Z_2//Z_3}{Z_1 + Z_2//Z_3} \times \frac{1}{2}\frac{R_1}{Z_{C3} + R_1} \\ &= \frac{I_{DM}R_1}{Z_{C3} + R_1} \times \frac{Z_4 \times Z_5 \times Z_2//Z_3}{(Z_1 + Z_2//Z3) + Z_4 + Z_5} \\ &= \frac{I_{DM}R_1Z_3Z_4Z_5}{Z_{C3} + R_1} \times \frac{1}{(Z_1 + Z_4 + Z_5)(1 + \frac{Z_3}{Z_2}) + Z_3} \end{aligned} \tag{11}$$

It can be seen from (11) that both of U_{DM} and I_{DM1} are related to multiple parameters. The method of reducing U_{DM} and I_{DM1} is to increase the branch impedance of the DM current I_{DM1} or reduce the impedance of the other four DM current paths.

2) CM EMI ANALYSIS AT 200 kHz

The CM EMI source caused by the switching of the MOSFET can be equivalent to a constant voltage source U_{CM}. The

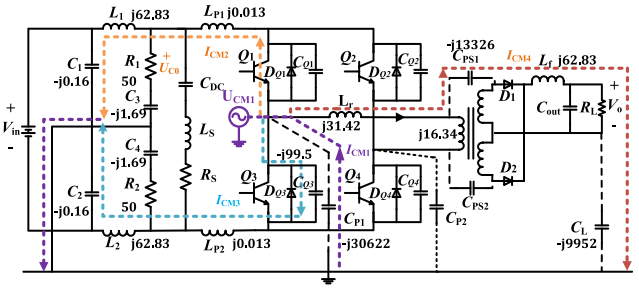


FIGURE 12. CM EMI current path at 200 kHz.

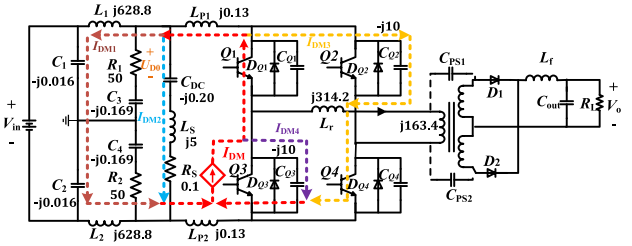


FIGURE 13. DM EMI current path at 2MHz.

following four CM current propagation paths are formed in the high frequency circuit as shown in Fig.12.

① CM current I_{CM1} path 1: $U_{CM1} \rightarrow C_{p1} \rightarrow U_{CM1}$

② CM current I_{CM2} path 2: $U_{CM1} \rightarrow L_{p1} \rightarrow (^{C_3 \rightarrow R_1}_{C_1 \rightarrow L_1}) \rightarrow U_{CM1}$

③ CM current I_{CM3} path 3:

$$U_{CM1} \rightarrow C_{Q3} \rightarrow L_{p2} \rightarrow (^{C_2 \rightarrow L_2}_{C_4 \rightarrow R_2}) \rightarrow U_{CM1}$$

④ CM current I_{CM4} path 4:

$$U_{CM1} \rightarrow L_r \rightarrow C_{ps1} \rightarrow L_f \rightarrow (^{C_{out}}_{R_L}) \rightarrow C_L \rightarrow U_{CM1}$$

Among them, only the CM current I_{CM2} of the path 2 flows through R_1. In fact, considering the two switching modes at the same time, the CM conducted voltage U_{CM} of the positive high voltage power line is formed by the composed of the conducted voltage generated by the CM EMI sources of the two bridge arms, so they need to be considered simultaneously during calculation. The current path of the conducted voltage $U_{R1'}$ at R_1 generated by the CM EMI source of the other bridge arm is:

$$U_{CM2} \rightarrow C_{Q2} \rightarrow L_{p1} \rightarrow (^{C_3 \rightarrow R_1}_{C_1 \rightarrow L_1}) \rightarrow U_{CM2}.$$

It can be seen from (12) that both of U_{R1} and U_{R2} are related to the parameters L_{p1}, C_3, R_1, C_1, L_1, C_{Q2} in path 2. The method of reducing the value of U_{CM} and I_{CM2} is to increase the impedance of CM current I_{CM2} path 2.

$$\begin{aligned} U_{CM} &= U_{R1} + U'_{R1} \\ &= U_{CM1} \times \frac{(R_1 + \frac{1}{j\omega C_3})//(j\omega L_1 + \frac{1}{j\omega C_1})}{(R_1 + \frac{1}{j\omega C_3})//(j\omega L_1 + \frac{1}{j\omega C_1}) + j\omega L_{P1}} \\ &\quad \times \frac{R_1}{R_1 + \frac{1}{j\omega C_3}} + U_{CM2} \\ &\quad \times \frac{(R_1 + \frac{1}{j\omega C_3})//(j\omega L_1 + \frac{1}{j\omega C_1})}{(R_1 + \frac{1}{j\omega C_3})//(j\omega L_1 + \frac{1}{j\omega C_1}) + j\omega L_{P1} + \frac{1}{j\omega C_{Q2}}} \\ &\quad \times \frac{R_1}{R_1 + \frac{1}{j\omega C_3}}) \end{aligned} \tag{12}$$

3) DM EMI ANALYSIS AT 2MHz

The impedance values of the equivalent circuit parameters at 2 MHz are calculated, as shown in Fig.13. It can be seen that only the DM current I_{DM1} of the path 1 flows through R_1 to form U_{R1}, and the relationship between U_{DM} and the I_{DM} of the DC-DC converter is analyzed below.

Suppose

$$\begin{aligned} U_{DM} &= 2U_{R1} \\ &= 2 \times I_{DM} \times (Z_1 + Z_2//Z_3)//Z_4 \times \frac{Z_2//Z_3}{Z_1 + Z_2//Z_3} \\ &\quad \times \frac{1}{2}\frac{R_1}{Z_{C3} + R_1} \\ &= 2 \times I_{DM} \times \frac{(Z_1 + Z_2//Z_3) \times Z_4}{(Z_1 + Z_2//Z_3) + Z_4} \times \frac{Z_2//Z_3}{Z_1 + Z_2//Z_3} \\ &\quad \times \frac{1}{2}\frac{R_1}{Z_{C3} + R_1} \\ &= \frac{I_{DM}R_1}{Z_{C3} + R_1} \times \frac{Z_4 \times Z_2//Z_3}{(Z_1 + Z_2//Z_3) + Z_4} \end{aligned} \tag{13}$$

In (13), since R_1, Z_3,and Z_{C3} are fixed values and the DM EMI source I_{DM} is a constant current source, so the main variables determining U_{R1} are Z_1 and Z_2, and increasing the amplitude of Z_1 and decreasing Z_2 can effectively reduce U_{R1}. Since $Z_1 + Z_2//Z_3 + Z_4 = 0.3267 + 5j + (-5j) = 0.3267$, it can be seen that L_s, C_{DC}, C_{Q3}, C_{Q4} produce parallel resonance, and the imaginary part of $Z_1 + Z_2//Z_3 + Z_4$ is 0, so U_{R1} appears a peak near 2M.

In fact, there are two different ways to reduce U_{DM} by changing the amplitudes of Z_1 and Z_2. Changing the amplitude of Z_1 is to reduce the impedance value of the path1 in the circuit, that is, the value of the real part of $Z_1 + Z_2//Z_3 + Z_4$, so that the peak value of U_{DM} at the resonance point is decreased, thereby lowering U_{DM}. However, since L_s and C_{DC} in Z_2 are the most important components that resonate with C_{Q3} and C_{Q4} in Z_3, changing the amplitude of Z_2 is essentially shifting the resonance point from 2MHz to a high-frequency point where there is no standard limit requirement, thereby reducing the amplitude of U_{DM} at the 2MHz.

4) CM EMI ANALYSIS AT 2MHz

The following three CM current paths are formed in the high frequency circuit as shown in Fig.14.

It can be seen that only the CM current I_{CM2} of path 2 flows through R_1. Similarly, The current path through R_1 to form the

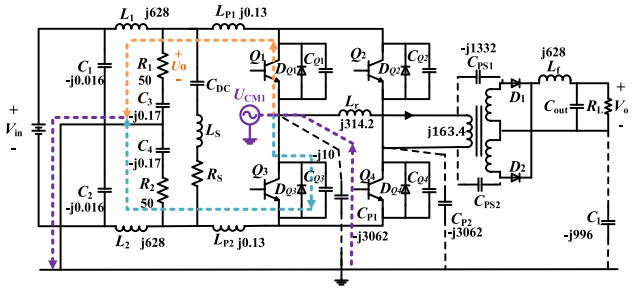


FIGURE 14. CM EMI current path at 2MHz.

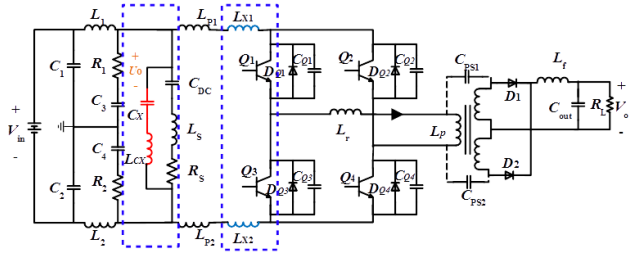


FIGURE 15. Filter circuit to reduce the peak of the resonance point at 2MHz.

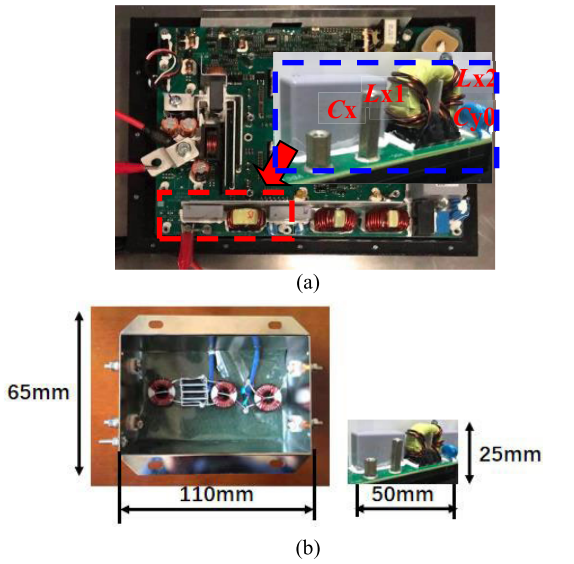


FIGURE 16. Filter circuit on the PCB. (a) Filter components on PCB in the DC-DC converter. (b) Comparison of two filter sizes.

conducted voltage U'_{R1} generated by the CM EMI source of the other bridge arm is as follow:

$$U_{CM2} \rightarrow C_{Q2} \rightarrow L_{p1} \rightarrow R_1 \rightarrow C_3 \rightarrow U_{CM2}.$$

So we can obtain:

$$\begin{aligned} U_{CM} &= U_{R1} + U'_{R1} \\ &= U_{CM1} \times \frac{R1}{R_1 + \frac{1}{j\omega C_3} + j\omega L_{P1}} + U_{CM2} \\ &\quad \times \frac{R1}{R1 + \frac{1}{j\omega C_3} + j\omega L_{P1} + \frac{1}{j\omega C_{Q2}}} \end{aligned} \tag{14}$$

It can be seen from (14) that U_{CM} is related to the parameters L_{p1}, C_3, R_1, and C_{Q2} in path 2. The method of reducing U_{CM} and I_{CM2} is to increase the impedance of I_{CM2} in path 2.

D. FILTER CIRCUIT ON PCB BOARD FOR DC-DC CONVERTER

According to Fig.4, it can be seen that the conducted voltage of the positive high voltage power supply line exceed the standard limits at 800 kHz, 900 kHz, 1.2 MHz, 1.3 MHz, 1.4 MHz, 1.5 MHz, 1.6 MHz, 1.7 MHz, 1.8 MHz, 5.9-6.2 MHz, which is mainly caused by the generated resonance at 2 MHz. Therefore, eliminating the resonance at the 2 MHz or reducing the amplitude of the 2 MHz conducted current can effectively reduce the amplitude of the conducted voltage below limits. According to the dominated parameters of the DM and the CM EMI current propagation paths at 2MHz, as shown in Fig.13 and Fig.14, the filter circuit can be directly designed on the PCB board inside the DC-DC converter. There are two main methods, as described below.

Method 1: The equivalent parasitic inductance L_s of the DC filter capacitor C_{DC} is reduced, so that the resonance point is shifted from 2MHz to the high frequency band around 10MHz, because there are no specified limits around 10MHz. In this paper, we choose to connect 1uF X capacitor C_x in parallel with C_{DC}, and its parasitic inductance L cx is 10nH, as shown in Figure 15 and Figure 16. In addition, from (13), since the capacitance C_x is connected in parallel, the impedance value Z_2 of the path 2 is reduced, and the DM current through the branch of the path 2 is increased, thereby reducing the DM current flowing on the positive high voltage power line and the conducted voltage measured on the LISN.

Method 2: According to (13), increasing the parasitic inductance L_{P1} and L_{P2} of the DC bus can increase the amplitude of Z_1, thereby reducing the resonance peak of the conducted voltage at 2MHz. In this paper, we added the DM inductors L_{x1} and L_{x2} to the positive and negative high voltage traces on the PCB of the DC-DC converter. The parameter matching calculation is carried out using (13). The inductance value is finally set to 1μH, as shown in Fig.15. By this way, the values of L_{P1} and L_{P2} can be effective increased.

For the conducted voltage exceeding limits near the high frequency of 72MHz, a pair of Y capacitors C_{y0} can be added between the high voltage positive and negative bus traces and the ground on the PCB, and the capacitance value of C_{y0} is 3300pF.

Designing the filter circuit on the PCB board inside the DC-DC converter has the following advantages: smaller size, only 1/5 of the high voltage filter (as shown in Fig.16); low in cost; easy to be engineering; and can eliminate the electromagnetic coupling between the input and output cables of the filter. In addition, it can be implemented in the early stage of product design.

V. SIMULATION AND MEASUREMENT

A. SIMULATION OF CONDUCTED EMI

According to the Fig.10, the high-frequency circuit model of the HV/LV DC-DC converter system is established by

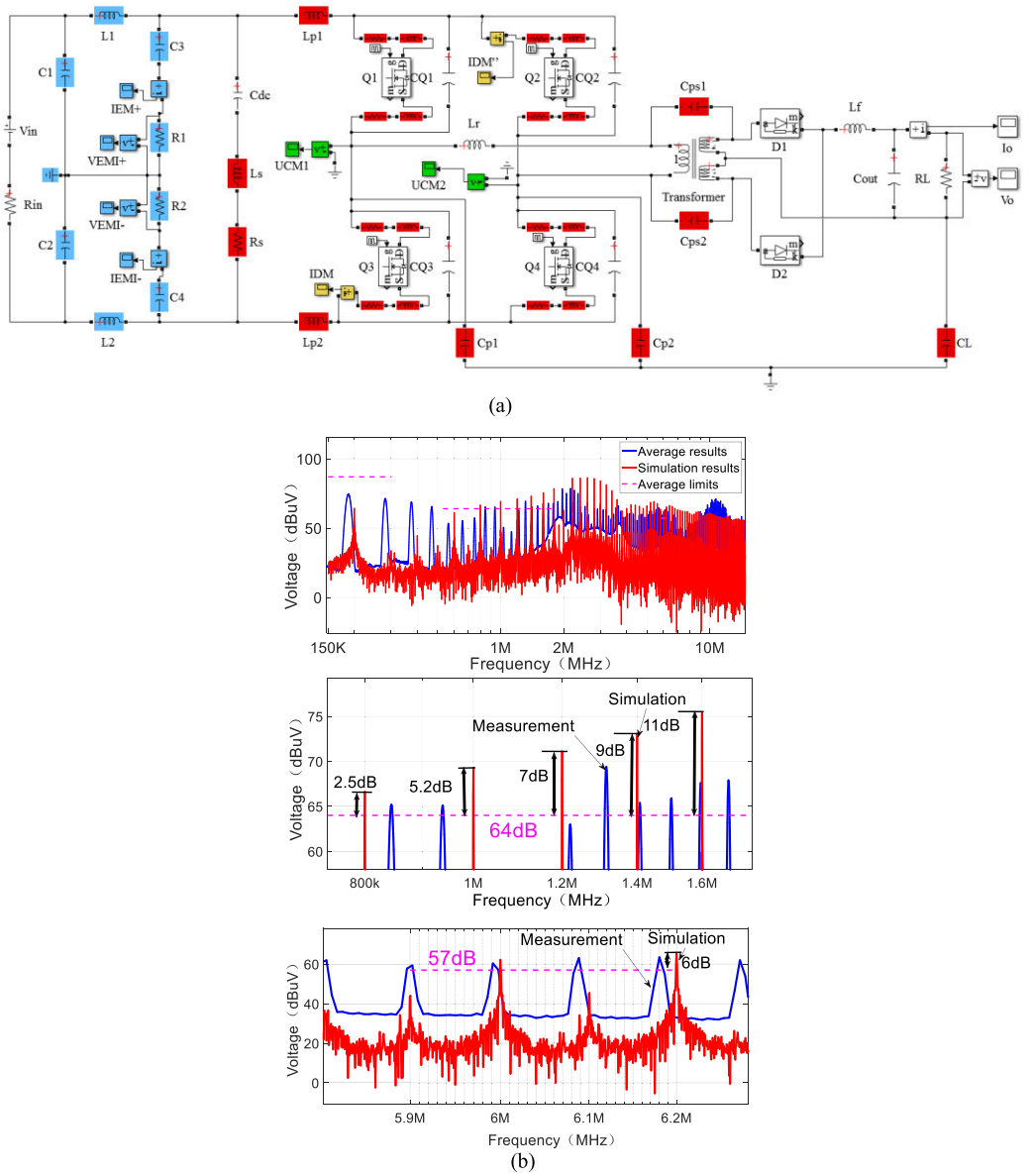


FIGURE 17. Modeling and simulation of the DC-DC converters for EMI analysis. (b) Comparison of simulation and experimental results of the conducted voltage.

MATLAB/Simulink, as shown in Fig. 17(a), to obtain the conducted voltage. The simulation and experimental results are compared, as shown in 17(b), and the difference is mainly due to the simplification of the model and the error of the parameter values. Similar to the experimental results, the conducted disturbance voltage exceeds the standard limit in the frequency band 1 (0.53-1.8 MHz), and forms resonance near 2 MHz, resulting in higher resonance peak voltage.

So the model can be used to design and verify the conducted EMI filter.

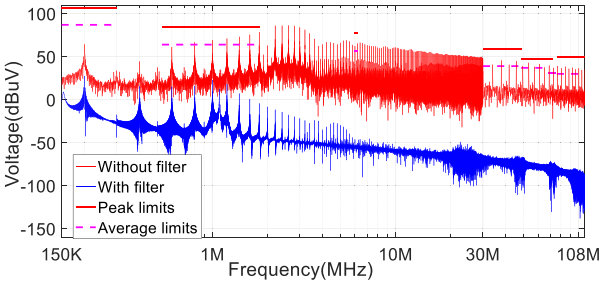


FIGURE 18. Simulation results of conducted voltage.

B. SIMULATION OF INSERTION LOSS OF THE FILTER IN DC-DC CONVERTER SYSTEM

According to CISPR25-2016, after adding the EMI filter to the DC-DC converter, the simulation of conducted emission from the high-voltage positive power line are carried out.

The simulation results of the EMI filter for HV input port are shown in Fig.18. It can be seen that the conducted voltage is greatly reduced and finally meet the requirements of the standard limit after adding the filter.

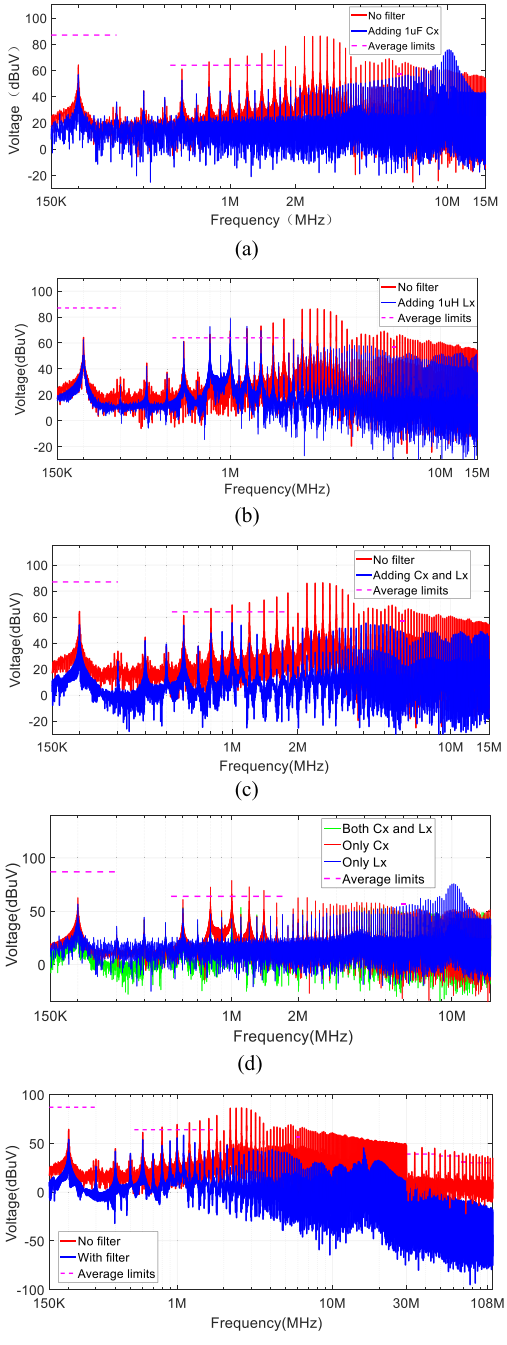


FIGURE 19. Simulation results of conduction voltage after adding filter circuit on PCB in the DC-DC converter. (a) Adding 1uF and 10nH X capacitors in parallel. (b) Adding LX1 and LX2 in series. (c) Adding 1uF and 10nH X capacitors in parallel, and LX1 and LX2 in series. (d) Comparison of the three methods. (e) Simulation results for the full frequency band.

According to Fig.15, the EMI filter circuit based on the resonance peaks is added into the high-frequency circuit model in Fig.17. The simulation results of the conducted voltage of the positive high-voltage power supply line are shown in Fig.19.

Fig.19(a) shows the simulation results after adding 1uF Cx with 10 nH Lcx. It can be seen that the resonance peak at the 2MHz disappears and the resonance moves to 10MHz with

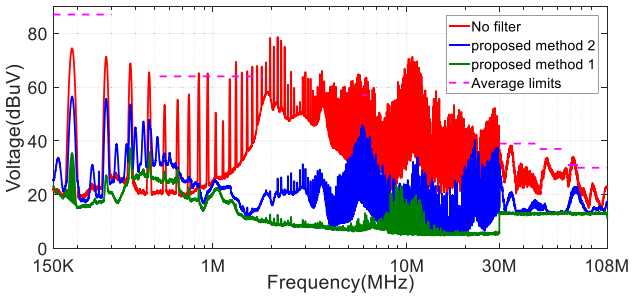


FIGURE 20. Measurement results of the conducted voltage after adding a filter circuit on the PCB.

no requirement of the standard limit. It can also be found that the conducted voltage at 800 kHz, 1.0 MHz, 1.2 MHz, 1.4 MHz, 1.6 MHz, and 1.8 MHz decreases significantly, meeting the standard limits requirements. In addition, due to the shifting of the resonance point, the conducted voltage at 5.9-6.2 MHz is also reduced, which is complied with the limits requirement.

Fig.19(b) shows the simulation results after adding L_{x1} and L_{x2}. It can be seen that the amplitude of the conducted voltage near the resonance point at 2MHz is reduced to meet the standard limit requirement, as well as the conducted voltage at 5.9-6.2 MHz. However, there are still some points exceeding standard limits at 800 kHz, 1.0 MHz, 1.2 MHz, and 1.4 MHz.

Fig. 19(c) shows the simulation results after adding C_x, L_{x1} and L_{x2}. It can be seen that the filter circuit has a good EMI suppression effect, and the conduction voltage between 150 kHz and 15 MHz satisfies the standard requirements. Figure 19(d) shows the comparison of the three methods. Fig.19(e) shows the simulation results after adding C_x and C_{DC} in parallel, L_{x1} and L_{x2} in series, and a pair of C_{y0}. It can be seen that after adding the filter circuit on the PCB, the conducted voltage comply with the limit requirements in the 150kHz-108MHz frequency band.

C. MEASUREMENT

Based on CISPR25-2016, the experiment for the conducted voltage of the positive high voltage power line is implemented at the test platform in Fig.3. Fig.20 shows the measurement results of the conducted voltage after adding C_x in parallel with C_{DC}, L_{x1} and L_{x2} in series, and a pair of C_{y0}. It can be seen that the conducted voltage exceeding standard limits drops significantly and comply with the standard limit requirements. Comparing the effective insertion loss of the filter circuit on the PCB with that of the high-voltage port filter, it can also be seen that although the insertion loss in some frequency bands is lower than that of the high-voltage port filter in some bands, it still meets the standard requirements, which can simplify the structure of filter and reduce size and cost.

VI. CONCLUSION

In order to solve the problem that the conducted interference voltage of a HV/LV DC-DC converter for vehicles exceeds

the standard CISPR25-2016, two different design methods of EMI filter for HV power supply were proposed: the design method of wide-band HV input port filter and the design method of PCB-level filter circuit based on the resonance peaks suppression. During the PCB-level EMI filter design process, by establishing the transfer functions at key frequencies of 200 kHz and 2 MHz, the dominated parameters responsible for the over-standard points were determined. Through analysis and experimental results, a few conclusions can be obtained:

(1) By connecting 1uF X capacitor with 10nF parasitic inductance in parallel with C_{DC}, the resonance peak can be shifted from 2MHz to the high frequency band around 10MHz, where there is no limits.

(2) Increasing the parasitic inductance L_{P1} and L_{P2} of the DC bus can reduce the resonance peak of the conducted voltage at 2MHz.

(3) The combination of an X capacitor with a small parasitic inductance, a pair of inductors, and a pair of Y capacitors can effectively suppress conducted voltage in the 150kHz-108MHz range.

(4) The filters designed by above two methods can effectively reduce the conducted EMI and comply with the limits requirements by CISPR25-2016 in 150kHz∼108MHz.

(5) The PCB-level filter designed by the second method is smaller in size, only 1/5 of the filter size designed by the first method, lower in cost,and easy to be engineering.

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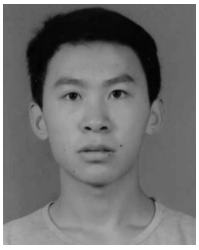

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