IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 4, 2020, accepted March 26, 2020, date of publication April 2, 2020, date of current version April 20, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2985256

Power Efficient Simple Technique to Convert a Reset-and-Hold Into a True-Sample-and-Hold Using an Auxiliary Output Stage

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This work was supported by a Grant TEC2016-80396-C2 (AEI/FEDER). The work of Hector Daniel Rico-Aniles was supported by the Mexican Consejo Nacional de Ciencia y Tecnologia (CONACYT) through an academic scholarship under Grant 408946.

ABSTRACT A technique to implement true-sample-and-hold circuits that hold the output for almost the entire clock cycle without resetting to zero is introduced, alleviating the slew rate requirement on the op-amp. It is based on a Miller op-amp with an auxiliary output stage that increases power dissipation by only 1.3%. The circuit is offset-compensated and has close to rail-to-rail swing. Experimental results of a test chip prototype in 130nm CMOS technology with 0.3mW power dissipation are provided, which validate the proposed technique.

INDEX TERMS Amplifiers, mixed-signal circuits, offset compensation, track-and-hold, sample-and-hold (S/H), switched capacitor.

I. INTRODUCTION

Sample-and-hold circuits are one of the most important building blocks in mixed signal IC design. They are required in analog to digital and digital to analog converters. In this paper, following definitions are used: a ''true-sample-and-hold'' (TSH) denotes a circuit that maintains the sampled output constant during the entire clock cycle; a ''reset-and-hold'' (RH) denotes a circuit that holds the output during one phase and resets it to a constant value during a non-overlapping phase and a ''track-and-hold'' (TH) denotes a circuit where the output tracks the input during one phase and holds its last value during the non-overlapping phase.

The offset and the slew rate requirements are two critical problems that affect accuracy and speed of sample-and-hold circuits. An approach to compensate offset is the well-known switched capacitor circuit shown in Fig. 1 [1]. In this circuit the offset is stored in C and C' during phase ϕ. During the non-overlapping phase ϕ_{no} the offset is subtracted, providing an offset-free output of value $V_{out} = V_{in}$.

The circuit has the drawback that it holds the output value during ϕ_{no} and then resets to the offset voltage (V_{os}) during ϕ, as shown in the simulation of Fig. 2. In this scheme the op-amp is required to have a high slew rate so that it can provide periodically large output variations within a brief period of time ($\tau << T_{clk}/2$). In practice the circuit is a RH circuit.

Several efforts have been done to mitigate the high slew rate requirement. In [2], Temes referenced an approach, shown in Fig. 3, consisting of placing an extra capacitor C_1, which is charged to the output value during phase ϕ_{no} and is connected in the feedback path during phase ϕ. In this circuit, the output changes during phase ϕ are given by:

$$\Delta V_{out} = V_{os} + \left(\frac{C_1}{C_{in}}\right) V_{in} \tag{1}$$

The output change during the reset phase ϕ is reduced at the expense of utilizing a large capacitance ratio C_1/C_{in} which translates into large silicon area and slower speed. In practice,

The associate editor coordinating the review of this manuscript and approving it for publication was Cihun-Siyong Gong.

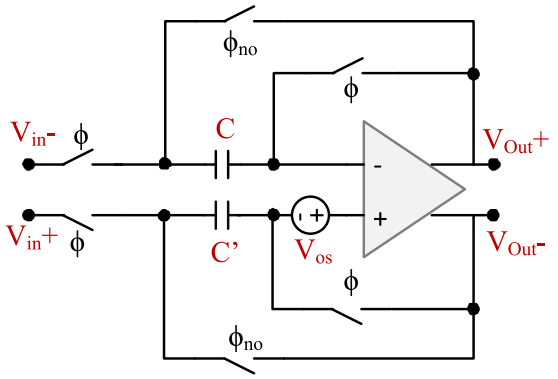

FIGURE 1. Conventional switched capacitor fully differential reset and hold circuit.

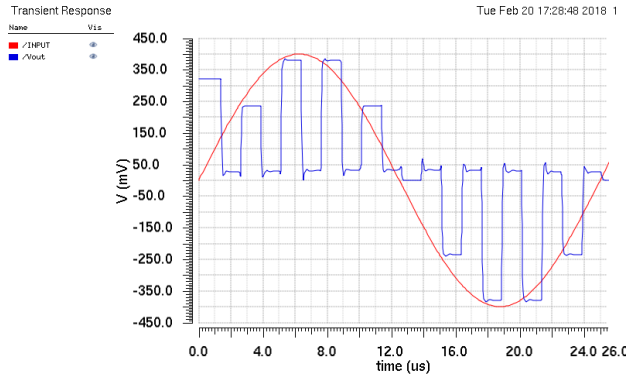

FIGURE 2. Conventional reset and hold output.

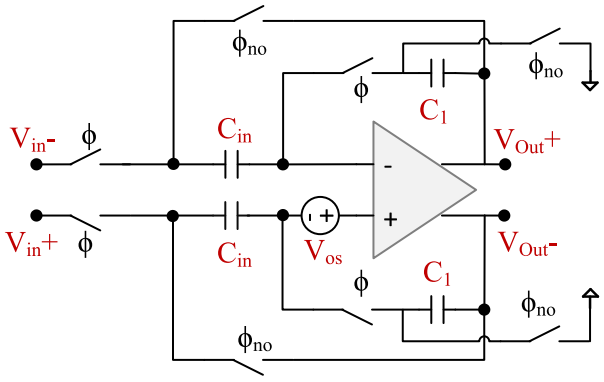

FIGURE 3. Proposal referenced in [2] of a pseudo-RH.

the circuit performs as a pseudo RH circuit because it also resets but not to a constant value.

Utilization of Track-and-Hold circuits is another approach to alleviate slew rate requirements [3]. A common method to implement a track-and-hold circuit that solves the slew rate issue is the Miller hold capacitance method [4], [5]. It uses the op-amp as a voltage follower during the tracking phase and the Miller capacitor to hold the output during the hold phase. However, it has various drawbacks: 1) It performs as a TH circuit (two stages in cascade with complementary phases can be used to implement a sample-and-hold circuit but speed is reduced by a factor two and power dissipation is increased by the same factor two); 2) It does not compensate DC offset, and 3) The input signal range is reduced by the headroom of the differential pair since during the track phase the positive input terminal of the op-amp operating as a voltage follower is directly connected to the input signal. This latter issue is of special concern in modern technologies with very low supply voltages in which case an essential reduction of the signal range can result.

A method to implement TSH circuits is the "ping-pong" technique [6], [7]. In this technique, two TH circuits are connected in parallel and the output is switched between the two TH outputs, in a "ping-pong" manner. During phase ϕ, one TH is tracking while the other is holding, and in the next phase ϕ_{no} the TH circuits change roles. This technique allows offset compensation and reduced slew rate requirements, but power dissipation and silicon area are doubled. Moreover, the reduction of the input signal range remains.

In this paper, an alternative simpler approach to implement a fully differential TSH circuit with offset compensation is presented. It uses a Miller op-amp with an auxiliary output stage that slightly increases the required silicon area and power dissipation (by approximately 1.3%) and has close to rail to rail input signal range. None of the outputs (main amplifier and auxiliary stage) are reset during a clock phase or experience large voltage variations. For this reason, the speed limitation that the slew rate imposes to conventional RH circuits like the one in Fig. 1 is essentially reduced.

The paper is organized as follows: Section II describes the proposed scheme. Section III discusses simulation and measurement results that validate the proposal. Conclusions are given in Section IV.

II. CIRCUIT DESCRIPTION

The proposed circuit is shown in Fig. 4. It is a pseudo rail-to-rail fully-differential, offset compensated TSH circuit that maintains the output voltage $V_{Out} = V_{oP} - V_{oN}$ constant during almost the entire clock period without switching between different output terminals. It can be considered as the combination of a switched capacitor and an integrating (Miller Hold capacitance) sample-and-hold circuit.

The circuit is based on a Miller op-amp with an additional low power auxiliary output stage. Both output stages use Miller capacitors as hold elements. The operation of the circuit is described in the next subsections.

A. SAMPLING PHASE, Φ_{no}

During the sampling phase (ϕ_{no}), switches S_1, S_1', S_2, S_2', S_3, S_3' are closed while S_4, S_4', S_5, S_5'are open. The circuit has a unity gain negative feedback loop formed by the input stage and the auxiliary amplifier as shown in Fig. 5. The outputs of the auxiliary amplifier are set to values defined by equations (2) and (3) with a *zero* common-mode output voltage. The capacitors C and C' are connected to the input signals (V_{iP}, V_{iN}) and are charged to voltages given

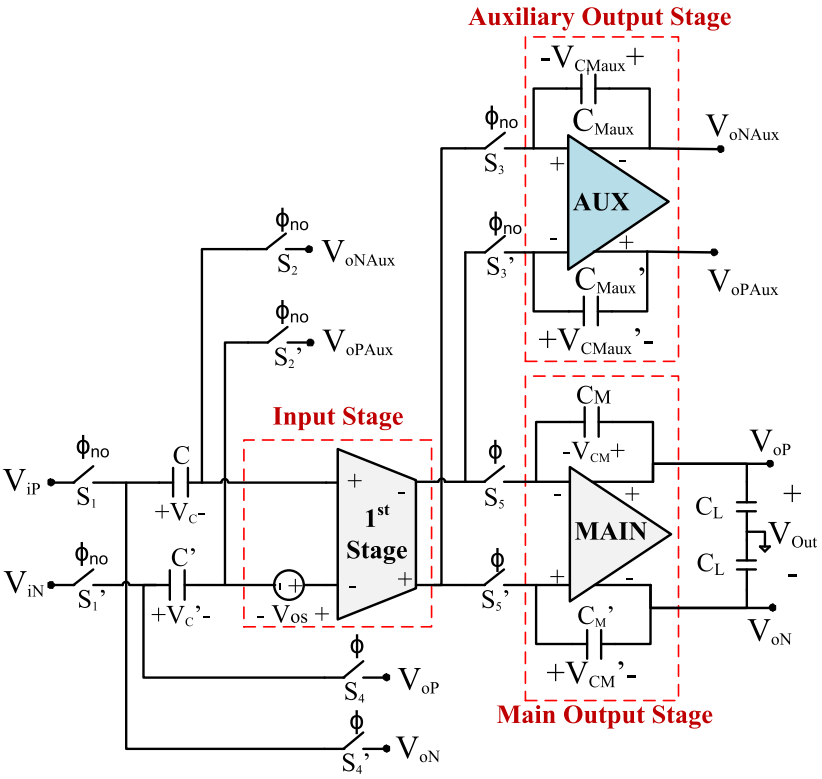

FIGURE 4. Scheme of proposed TSH using an auxiliary amplifier output stage.

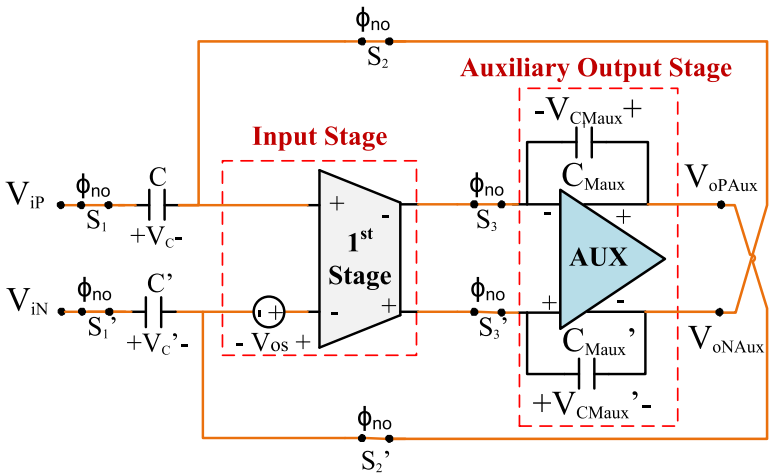

FIGURE 5. Circuit configuration during the sampling phase ϕ_{no}.

by equation (4) and (5).

$$V_{oPaux} = \frac{V_{os}}{2} \tag{2}$$

$$V_{oNaux} = -\frac{V_{os}}{2} \tag{3}$$

$$V_C = V_{iP} - \left(\frac{V_{os}}{2}\right) \tag{4}$$

$$V'_C = V_{iN} + \left(\frac{V_{os}}{2}\right) \tag{5}$$

B. HOLD PHASE, ϕ

During phase ϕ, switches S_4, S_4', S_5, S_5' are closed and the rest of the switches are open. In this case the negative feedback loop around the auxiliary output stage is open and the Miller capacitors C_{Maux}, C'_{Maux} hold the output values of the auxiliary amplifier at the constant values given by (2) and (3).

At the same time there is unity gain negative feedback around the main output stage through capacitors C, C', which

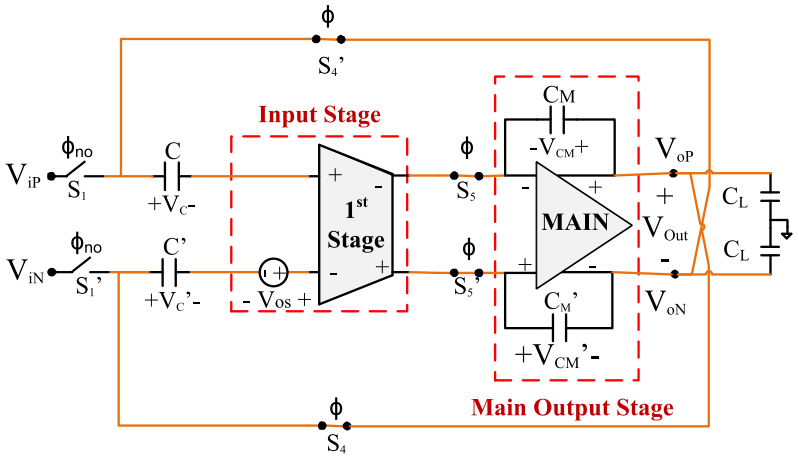

FIGURE 6. Circuit configuration during the hold phase ϕ.

act as floating batteries with values V_C and V'_C, as shown in Fig. 6. These capacitors cannot change their charge leading to the offset-free output voltages given by (6) and (7).

$$V_{oN} = \frac{(V_{iP} - V_{iN})}{2} \tag{6}$$

$$V_{oP} = \frac{(V_{iN} - V_{iP})}{2} \tag{7}$$

The output voltages (V_{oP}, V_{oN}) are held by the Miller capacitors C_M, C'_M during both phases (ϕ_{no} and ϕ) until the next sampled value is transferred to the output at the beginning of phase ϕ. The output voltage changes are given by (8) and (9).

$$\Delta V_{oN} = \frac{\Delta(V_{iP} - V_{iN})}{2} \tag{8}$$

$$\Delta V_{oP} = \frac{\Delta(V_{iN} - V_{iP})}{2} \tag{9}$$

C. TSH BUILDING BLOCKS

The op-amp used for the proposed TSH is a fully differential class AB Miller op-amp with a high gain telescopic input stage and a class AB main output stage. The op-amp has been divided into input and output stages that are depicted in Fig. 7 and Fig. 8, respectively. The main output stage is the free class AB amplifier [8] shown in Fig. 8. Class AB operation is achieved by means of capacitors C_{Bat}, which transfer high-speed changes in V_{o1p} and V_{o1n} to nodes X and X' respectively. This allows the NMOS output transistors to deliver negative output currents that are not limited by the bias current of the output stage. Therefore, both output transistors become active leading to a symmetrical slew rate [8]. The auxiliary output stage is a conventional class A common-source stage, as shown in Fig. 8.

The common mode feedback network (CMFN) used for the op-amp is also based on a telescopic differential stage, which is depicted in Fig. 9. The reference voltage V_{refCM} corresponds to the mid supply voltage, $V_{refCM} = V_{MS} = (V_{DD} + V_{SS})/2$. The auxiliary output stage provides negative

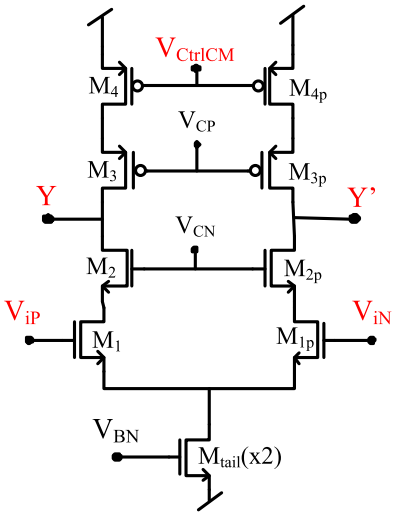

FIGURE 7. Telescopic op-amp input stage.

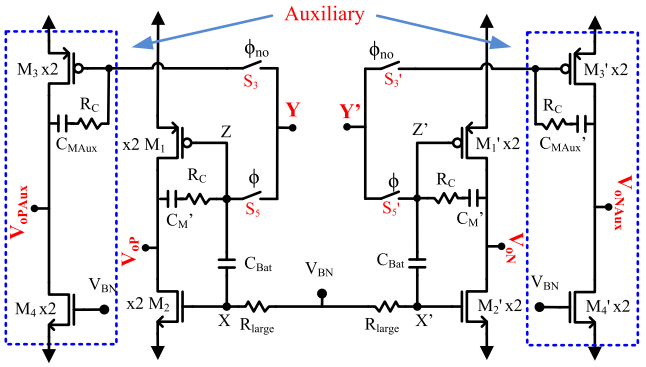

FIGURE 8. Op-amp free class AB main output stage and class A auxiliary output stage.

feedback during the sampling phase ϕ_{no} while the main output stage provides negative feedback during the hold phase ϕ. Since there are two independent output stages that are switch-

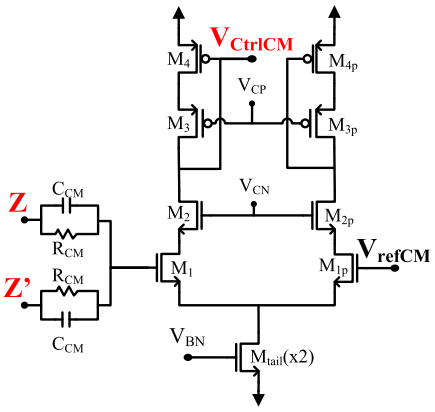

FIGURE 9. Common mode feedback network (CMFN).

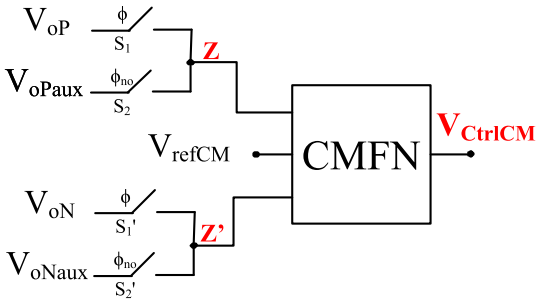

FIGURE 10. CMFN switching connection between main and auxiliary outputs.

ing with the control signals (ϕ_{no} and ϕ), the inputs of the common mode feedback network CMFN are switched alternatively between the outputs of the main and the auxiliary op-amp output stages as shown in Fig. 10. During phase ϕ, the inputs of the CMFN are connected to V_{oP}, V_{oN} while during phase ϕ_{no}, they connect to the auxiliary amplifier outputs V_{oPaux}, V_{oNaux}.

The input offset voltage V_{os} of the proposed TSH circuit corresponds mainly to the offset voltage of the input stage, which is common during both phases. A small contribution to the input offset voltage corresponds to the offset voltage of the output stage(s) reflected to the input divided by the high gain of the input stage ($A_{inp} \sim 1000$V/V), thus, although this component is not canceled, it can be neglected since it is very small (in the μV range). Due to this, the proposed scheme is effective in cancelling V_{os}.

D. REMARKS

1) Note that the auxiliary output stage does not have load capacitances and operates with constant output voltages $V_{os}/2$ and $--V_{os}/2$. For this reason, it does not require class AB operation and it is able to operate with a fraction of the biasing current used for the rest of the circuit; in the example discussed here, it operates with 1/30 of the bias current, I_b. It uses smaller Miller capacitors C_{Maux}, C'_{Maux}, which in the presented example are 1/5 of the Miller capacitors used in the main output stage. The auxiliary output stage leads only to a slight increase on power dissipation and Silicon area when compared to the conventional approach with only one output stage.
2) In addition, given that the main outputs V_{oP}, V_{oN} only change their values every clock cycle and since they do not reset to zero (or to another constant value), the slew rate requirement is greatly mitigated which allows to achieve higher speed.

E. OPERATIONS AT LOW SAMPLING RATES

Considering a given sampling period kT_s (with k integer) the TSH only requires a transition in the output voltage at the end of this period with value $\Delta V = V_{in}((k+1)T_s) - V_{in}(kT_s)$. Hence if consecutive samples $V_{in}((k+1)T_s)$ and $V_{in}(kT_s)$ are highly correlated (which is typically done with a sampling frequency $f_s = 1/T_s$ much larger than the Nyquist frequency $f_{Nyquist} = 2f_{in}$) then ΔV is very small and SR requirements are highly relaxed.

However, a conventional RH resets the output to the offset voltage V_{os}, so it requires an output voltage transition within the sampling period with value $\Delta V = V_{os} - V_{in}(kT_s)$ and another transition at the end of the sampling period with value $\Delta V = V_{in}((k+1)T_s) - V_{os}$. Hence even for highly correlated consecutive samples, the RH slews back and forth twice during each sampling period with voltage changes that may become large. This in general leads to stricter SR requirements than for the proposed TSH, allowing the TSH to work at sampling frequencies close to the op-amp gain bandwidth product GB.

However, when the condition $f_s >> f_{in}$ is not met this may not be the case. For instance, when $f_s = f_{Nyquist} = 2f_{in}$, there are only 2 samples per period of the input signal $T_{in} = 1/f_{in}$ which are separated by $T_{in}/2$. In the worst case these samples are at the maximum and minimum value of the input, so that ΔV in the TSH has the maximum value, corresponding to the peak-to-peak input amplitude. For this case, the RH only requires half the SR since ΔV is halved due to the reset, while the TSH changes from the maximum to the minimum value of the input signal. Fig. 11 and Fig. 12 show simulations illustrating this case, corresponding to the TSH and RH sampling at the Nyquist rate. In practice the SR requirements will be lower for the TSH for approximately $f_s > 2f_{Nyquist}$.

III. SIMULATION AND MEASUREMENT RESULTS

In order to validate the proposed technique the circuits of Fig. 4 (proposed TSH) and Fig. 1 (conventional RH) were fabricated on the same chip in a 130 nm CMOS n-well process with nominal NMOS and PMOS threshold voltages $V_{THn} = |V_{Thp}| \approx 0.4$ V. A microphotograph of the circuits is shown in Fig. 13.

The proposed and conventional circuits used the same op-amp topology (the conventional RH used an op amp with only one free class AB output stage), transistor sizes, C_C values and bias current (I_{bias}). They were tested under the

TABLE 1. Op-amp characterization for $C_L = 25$pF.

Parameters	Value
L (nm)	360
W_n (µm)	2
W_p (µm)	12
C_c (pF)	5
R_c (kΩ)	5
I_{bias} (µA)	30
C_L (pF)	25
A_{OL} (dB)	72.54
f_{3dB} (kHz)	2.6
GB (MHz)	10.88
PM (°)	94

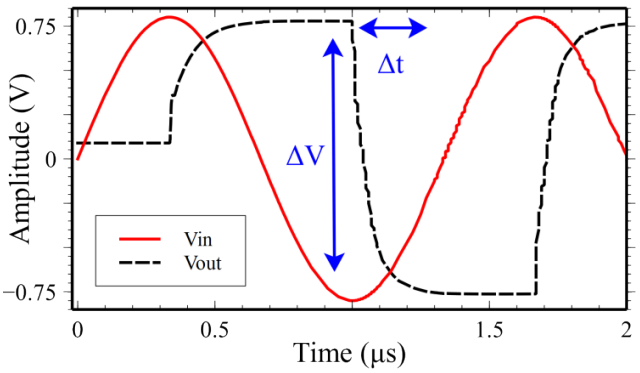

FIGURE 11. Proposed TSH circuit sampling at the Nyquist rate with a sinusoidal input signal ($V_{in} = \pm 800$ mV and $f_{in} = 750$ kHz).

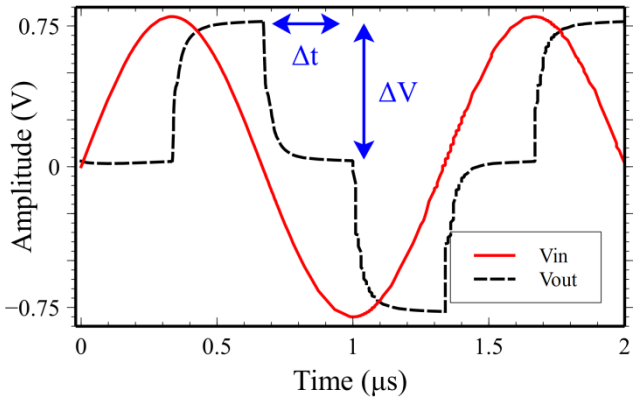

FIGURE 12. Conventional RH circuit sampling at the Nyquist rate with a sinusoidal input signal ($V_{in} = \pm 800$ mV and $f_{in} = 750$ kHz).

same conditions. Table 1 summarizes the simulated op-amp parameters and AC response. The op-amp was designed to drive an off-chip capacitive load of 25 pF, smaller load values give the freedom to reduce the compensation capacitor C_C, thus increasing the working speed with the same power dissipation. The supply voltage and biasing currents employed were $V_{DD} = -V_{SS} = 600$ mV and $I_{bias} = 30\mu$A. With this supply voltage and bias current, all transistors operate in strong inversion.

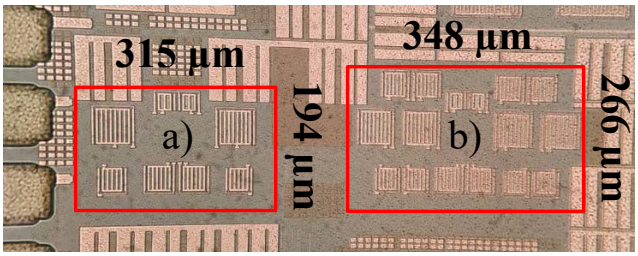

FIGURE 13. Microphotograph of the fabricated chip. (a) Conventional. (b) proposed.

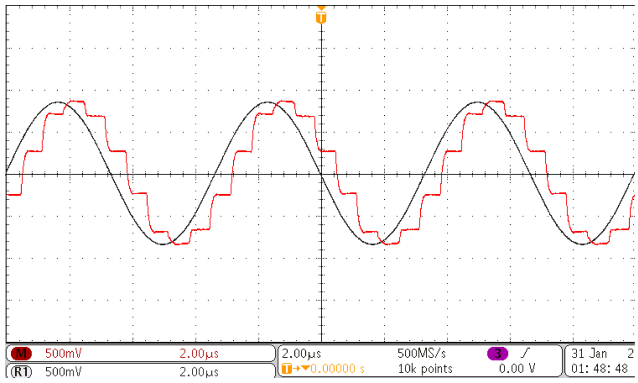

FIGURE 14. Experimental results of the proposed TSH with an 800 mV 150 kHz sinusoidal input and a 1.5 MHz clock.

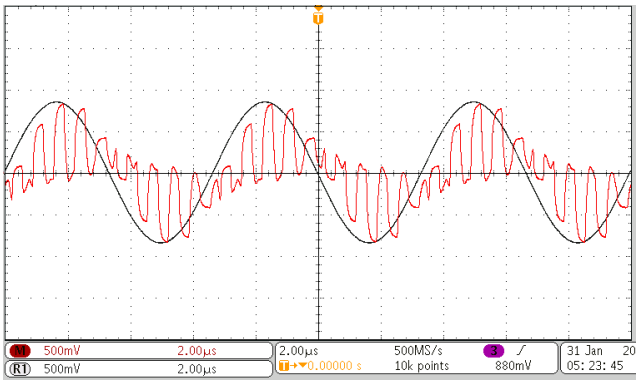

FIGURE 15. Experimental results of the conventional RH with an 800 mVp 150 kHz sinusoidal input signal and a 1.5 MHz clock.

The conventional RH circuit has a power dissipation of 288 μW. The auxiliary output stage works with 1 μA, this yields to a power consumption of the proposed TSH of 293 μW, which represents an increase of only 1.3% when compared to the conventional RH.

The proposed (TSH) and the conventional (RH) were both measured employing an 800mVp 150 kHz input signal and a sampling rate of 1.5 MS/s. The measured outputs of the TSH and the RH are shown in Fig. 14 and Fig. 15, respectively. As expected, the proposed architecture holds the sampled values during approximately the entire clock period, while the conventional RH resets to approximately zero, which leads to significant slew rate distortion in the output signal. This in

TABLE 2. Op-amp characterization for $C_L = 2$pF.

Parameters	Value
L (nm)	360
W_n (μm)	2
W_p (μm)	12
C_c (pF)	1
R_c (kΩ)	2
I_{bias} (μA)	30
C_L (pF)	2
A_{OL} (dB)	71.7
f_{-3dB} (kHz)	12
GB (MHz)	42
PM (°)	80

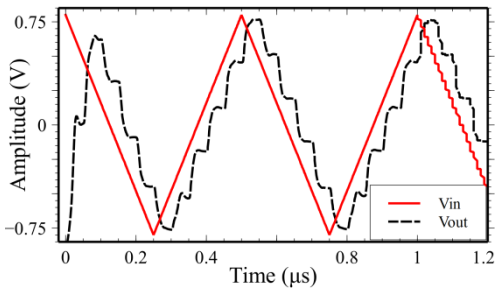

FIGURE 16. Simulated results of the proposed TSH with an 800 mV_p 2 MHz triangular input signal and 20 MHz clock.

spite of the fact that the conventional RH also uses a class AB op-amp.

Due to the reduced slew rate requirement of this technique, the proposed circuit exhibits an improved THD in spite of the fact that it works at a higher input signal frequency and sampling rate. Table 2 summarizes a comparison with other published SH circuits.

The design was simulated for a smaller load capacitance $C_L = 2$ pF so that the compensation capacitance could be reduced, $C_c = 1$ pF, this was done in order to increase the speed of the circuit. The compensation resistance was also reduced to $R_c = 2k\Omega$. The op-amp parameters and AC response are summarized in Table 3. The simulated output of the proposed TSH when sampling at $f_s = 20$ MHz is shown in Fig. 16. It can be seen that the TSH circuit can easily follow the input signal. Conversely, as shown in Fig.17 the conventional RH is no longer able to properly follow the input signal at this rate, despite of using the same design and simulation conditions as the TSH. The SR limitation on the conventional RH is dependent on the amplitude of V_{in}. This limitation is alleviated by the TSH at sampling frequencies $f_s >= 4\, f_{in} = 2\, f_{Nyquist}$ where V_{in} does not impose any SR limitation on the TSH circuit. In the case of $f_s = 4$ only 4 samples are taken per signal period. The worst scenario is faced when those four samples include the minimum and maximum values of V_{in}, so that the maximum output step is $V_{in}/2$, being the same for both TSH and RH circuits.

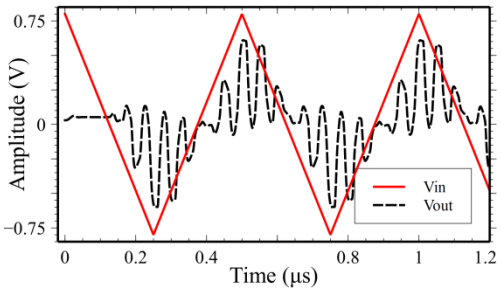

FIGURE 17. Simulated results of the conventional RH with a 800 mV_p 2 MHz triangular input signal and 20 MHz clock.

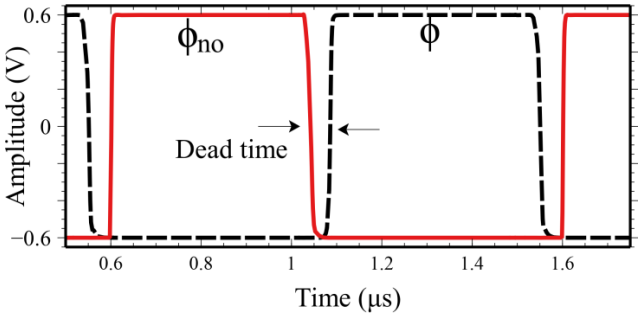

FIGURE 18. Simulated non-overlapping clock signals at 1 MHz.

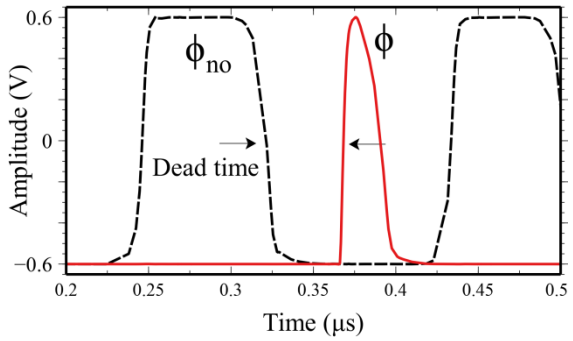

FIGURE 19. Simulated non-overlapping clock signals at 5 MHz.

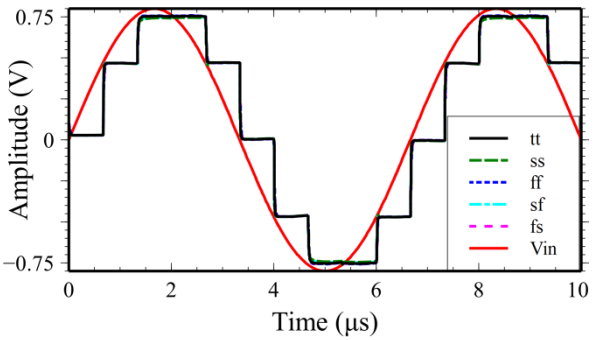

FIGURE 20. Process corners simulation of the TSH circuit with a 800 mV_p 150 kHz sinusoidal input signal and 1.5 MHz clock.

The fabricated chip was used to verify the proposed scheme of implementing a TSH using a Miller op-amp with an auxiliary output stage. In the fabricated chip the maximum

TABLE 3. Sample and hold experimental comparison.

Parameters	This work	[9]	[10]	[11]	[12]
Technology (µm)	0.13	0.25	0.18	0.13	0.18
Supply voltage (V)	±0.6	0.5	5	0.8	±0.9
Bandwidth (MHz)	1.5*	5	8	--	10
Sampling rate (MS/s)	1.5	1	0.25	1	1
Full-scale input range (V)	±0.4	--	0.6-3.4	--	±0.85
Pedestal error (mV)	5	0.8	--	--	6
DC offset (mV)	0.6	--	4	--	2
THD (dB)	-72**	--	--	-40	-60
Input signal frequency (kHz)	150	50	--	50 k	50
Power consumption (mW)	0.3	0.3	1	1.84	0.014

* limited by the clock generation circuit.
** 0.8 V_{pp} 150 kHz input signal and fs =1.5 MHz

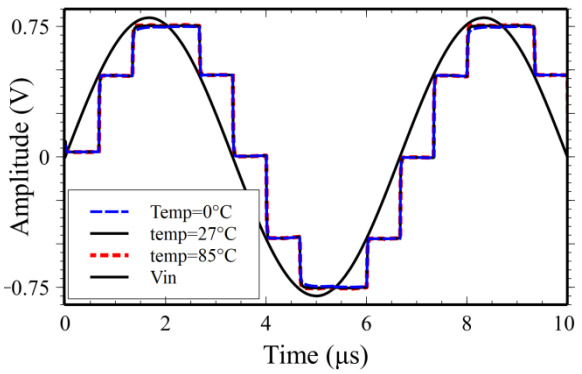

FIGURE 21. Temperature simulation of the TSH circuit with a 800 mV_p 150 kHz sinusoidal input signal and 1.5 MHz clock.

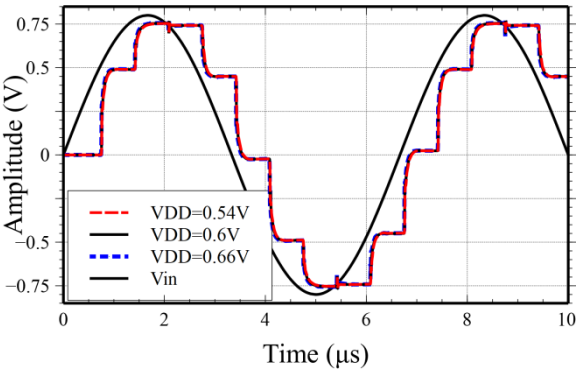

FIGURE 22. Voltage corners simulation of the TSH circuit with a 800 mV_p 150 kHz sinusoidal input signal and 1.5 MHz clock.

sampling frequency ($f_s = 3$ MHz) was limited in practice by the on-chip non-overlapping clock circuit generator and by the large load capacitance. The non-overlapping clock signals ϕ_{no} and ϕ shown in Fig. 18 had a fixed dead time between ϕ_{no} and ϕ of approximately $t_{dead} = 50$ ns. Moreover, as f_s increases, the time that ϕ is high shrinks in comparison to the time that ϕ_{no} is high as depicted in Fig.19. At this point, the clock signals are not able to control the circuit. A simulation using modified clock signals with lower dead time, $C_L = 25$pF and $C_c = 5$ pF showed that the proposed TSH can work at a sampling rate of $f_s \approx 8$ MHz as opposed to the measured $f_s \approx 3$ MHz. On the other hand, the conventional RH maximum sampling rate was maintained at $f_s \approx 1.5$ MHz because of the SR limitation and not because of the clock. Corners simulations were performed to evaluate the robustness of the proposal against PVT variations. Fig. 20 shows the simulation for the process corners tt, ss, ff, sf, fs. The simulation for temperature values 0°C, 27°C and 85 °C is depicted in Fig. 21. Supply voltage $V_{DD} = -V_{SS} = 0.54$ V, 0.6 V and 0.66 V equivalent to ±5% were simulated and are shown in Fig. 22. The results show that the design is robust against process, voltage or temperature variations.

IV. CONCLUSION

A simple method to transform a switched capacitor reset-and-hold circuit into a true-sample-and-hold circuit was introduced. The proposed circuit holds the output for an entire clock cycle, it does not reset to an offset value neither tracks the input signal during half of the clock period. The method greatly mitigates the op-amp slew rate requirements since it does not reset during one phase. This improves the THD compared to the conventional RH. The proposed scheme has offset compensation and almost rail to rail input range and just requires an auxiliary output stage that slightly increases (∼1.3%) power dissipation and silicon area. The scheme was experimentally validated with a fully differential sample-and-hold circuit fabricated in 130nm CMOS technology.

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