

Received February 26, 2020, accepted March 23, 2020, date of publication April 2, 2020, date of current version April 17, 2020. Digital Object Identifier 10.1109/ACCESS.2020.2985105

Dynamic Slingshot Operation for Low-Operation-Voltage Nanoelectromechanical (NEM) Memory Switches

MIN HEE KANG[®], (Student Member, IEEE), AND WOO YOUNG CHOI[®], (Senior Member, IEEE)

Department of Electronic Engineering, Sogang University, Seoul 04107, South Korea

Corresponding author: Woo Young Choi (wchoi@sogang.ac.kr)

This work was supported in part by the National Research Foundation (NRF) of Korea funded by the Ministry of Science and ICT (MSIT) through the Intelligent Semiconductor Technology Development Program under Grant NRF-2019M3F3A1A02072089, in part by the Mid-Career Researcher Program under Grant NRF-2018R1A2A2A05019651, in part by the Fundamental Technology Program under Grant NRF-2015M3A7B7046617, in part by the Nano-Material Technology Development Program under Grant NRF-2016M3A7B4909668, in part by the Institute for Information and Communications Technology Planning and Evaluation (IITP) funded by the MSIT through the Information Technology Research Center Program under Grant IITP-2020-2018-0-01421, and in part by the Ministry of Trade, Industry and Energy/Korea Semiconductor Research Consortium (MOTIE/KSRC) through the Technology Innovation Program under Grant 10080575.

ABSTRACT A dynamic slingshot pull-in operation is presented by using the influence of inertia and damping on the nanoelectromechanical (NEM) memory switch operation. To confirm the validity of the proposed idea, a finite element analysis (FEA) simulation, that reflects the actual cantilever beam structure, is performed, and an analytical one-dimensional (1D), the parallel plate model is tested. According to the analytical and FEA data, the dynamic slingshot pull-in voltage can be achieved ~0.78 times and ~0.73 times lower than conventional pull-in voltage under near-vacuum conditions, respectively. It is also shown that the proposed dynamic slingshot operation is more effective for lowering operation voltage (V_{DD}) and boosting the chip density of complementary-metal-oxide-semiconductor (CMOS)- NEM hybrid reconfigurable logic (RL) circuits than the static slingshot operation.

INDEX TERMS Complementary-metal-oxide-semiconductor-nanoelectromechanical (CMOS-NEM) hybrid reconfigurable logic (RL) circuits, operation voltage (V_{DD}), and dynamic slingshot pull-in.

I. INTRODUCTION

Conventional complementary-metal-oxide-semiconductoronly (CMOS-only) reconfigurable logic (RL) circuits, a well-known example of which is a field-programmable gate array (FPGA), suffer from some fundamental limitations including, low chip density, high energy consumption, and low speed [1], [2]. These limitations mainly stem from the fact that routing blocks (RBs) that determine data signal paths consist of CMOS devices horizontally integrated on a silicon substrate suffering from high leakage current and high resistance. To address these issues, researchers have tried to replace CMOS devices with novel routing devices such as nanoelectromechanical (NEM) memory switches [3]–[6]. Fig. 1 shows the conceptual view of our previously proposed monolithic-three-dimensional (M3D) CMOS-NEM hybrid RL circuit and NEM memory switch [7], [8]. As NEM memory switches can be integrated with metal interconnection layers using the CMOS backend process, CMOS-NEM hybrid RL circuits achieve higher chip density, higher performance, and lower power consumption than CMOS-only circuits [7]–[12]. These merits make the NEM memory switch as attractive as the routing switch.

Fig. 1(b) shows the conceptual view of a NEM memory switch whose movable cantilever beam length, width, and thickness are expressed as L_{beam} , W_{beam} , and t_{beam} , respectively. Conventionally, as shown in Figs. 1(b) and 2(a), the movable beam is separated from the two metal electrodes, called selection lines (L1 and L2), by air gaps (t_{gap}) in the pristine state. Pull-in occurs if the voltage applied between the beam and selection line is greater than the pull-in voltage (V_p): the movable beam becomes stuck to either L1 (State 1) or L2 (State 2) due to electrostatic force. The voltages applied to L1 and L2 are called V_{L1} and V_{L2} , respectively. Subsequently, to toggle between states 1 and 2, the applied voltage should exceed the switching voltage (V_s). More details on the conventional operation of NEM memory switches have been presented in prior studies [7].

The associate editor coordinating the review of this manuscript and approving it for publication was Chaitanya U. Kshirsagar.



FIGURE 1. (a) Schematic of the proposed M3D CMOS-NEM hybrid RL circuit and (b) NEM memory switch.

One of the most critical problems of M3D CMOS–NEM hybrid RL circuits is the high operation voltage (V_{DD}) of the NEM memory switches [8], [13]. This is challenging because if the V_{DD} of the NEM memory switch is higher than that of the CMOS logic circuits, the overall V_{DD} of M3D CMOS-NEM hybrid RL circuits will increase. According to prior studies, the V_{DD} of the NEM memory switches is determined by V_p when the L_{beam} is optimized to achieve minimum V_{DD} [13]. The V_p reduction of NEM memory switches is thus the key to lowering the overall V_{DD} of M3D CMOS-NEM hybrid RL circuits. Conventionally, V_p is reduced by introducing new structures and materials [15]–[17]. However, they have limitations in terms of CMOS-process compatibility and chip density.

Slingshot operation has recently been proposed as a novel pull-in method for lowering V_p while maintaining structures and materials [18]. The feature of the slingshot is to perform a pull-back operation before the pull-in operation to store elastic potential energy (E_{pot}), which reduces the electrical energy (E_{elec}) required for the pull-in operation following the energy conservation law. It is noteworthy that the slingshot pull-in operation of NEM memory switches. Thus, the latency and



FIGURE 2. NEM memory switch operations using three kinds of pull-in operation methods: (a) conventional pull-in operation, (b) the static and (c) the proposed dynamic slingshot pull-in operation. Note that the switching operation between State 1 and 2 is the same in the three cases. NEM memory switches store higher potential energy in the case of the dynamic slingshot operation than in the case of the static slingshot operation during their pull-back operation.

energy consumption originated from the pull-back step of the slingshot pull-in operation due is not critical. It has been proven, in a prior study, that V_p using static slingshot operation ($V_{p,sling,st}$) is theoretically ~0.84 times lower than conventional V_p without slingshot operation ($V_{p,conv}$), assuming an analytical parallel plate model [18]. $V_{p,conv}$ is written as

$$V_{p,conv} = \sqrt{\frac{8kt_{gap}^3}{27\varepsilon_0 L_{beam} W_{beam}}}.$$
 (1)

where k is the beam spring constant, and ε_0 is the vacuum permittivity.

The study, however, is limited to static analysis and a onedimensional parallel plate model. In the case of the static analysis, the time-dependent terms, such as inertia and damping, affecting the actual beam operation are ignored. This means that $V_{p,sling}$, derived by static analysis, can be different from that derived by dynamic analysis [19]. Additionally, the one-dimensional (1D) parallel plate model may lead to error, as it does not reflect the actual beam structure [20]. This study thus proposes a dynamic slingshot operation for further reduction of V_p , which eventually lowers the overall V_{DD} of M3D CMOS-NEM hybrid RL circuits. Furthermore, the study accurately evaluates the value of V_p using dynamic slingshot operation $(V_{p,sling,dy})$ using the dynamic analytical model and 3D finite element analysis (FEA) simulation, and compares it with the previously proposed static slingshot operation case.

II. RESULTS AND DISCUSSION

Figs. 2(b) and 2(c) compare the proposed dynamic slingshot operation with the previous static one of a NEM memory switch. Following the pristine state, it is assumed that pull-back occurs toward L2, and pull-in occurs onto L1. The absolute values of $x_{r,st}$ and $x_{r,dy}$, which have negative values in the coordinate system, are defined as the static and dynamic pull-back distances, respectively. In the case of the static slingshot operation, the optimized static pull-back position $(x_{r,st,opt})$ that minimizes V_p is $-t_{gap}/7$ and the optimized $V_{p,sling,st}$ ($V_{p,sling,st,opt}$) becomes ~0.84 times lower than $V_{p,conv}$, as shown in previous research [18]. On the contrary, in the case of the proposed dynamic slingshot operation, the optimized $x_{r,dy}$ ($x_{r,dy,opt}$) can be made larger than $x_{r,st,opt}$, indicating that more E_{pot} can be stored in the movable beam owing to the inertia effect. Assuming a vacuum environment in which the quality factor (Q) is infinite, using the dynamicmode d'Alembert's equation, the V_{L2} required to pull the movable beam back to x is derived as [21],

$$V_{L2} = \sqrt{\frac{kt_{gap} |x| (t_{gap} + x)}{\varepsilon_0 L_{beam} W_{beam}}} \quad (x \le 0).$$
(2)

Then, by replacing x with $x_{r,dy}$, the pull-back voltage ($V_{p,back}$) in the dynamic slingshot operation ($V_{p,back,dy}$) is determined by,

$$V_{p,back,dy} = \sqrt{\frac{kt_{gap} \left| x_{r,dy} \right| (t_{gap} + x_{r,dy})}{\varepsilon_0 L_{beam} W_{beam}}}.$$
 (3)

When $V_{p,back,dy}$ is applied to L2, the beam is pulled back to $x_{r,dy}$, which means that the movable beam stores $E_{pot}(x = x_{r,dy})$. Once the pull-back operation is completed, 0 V is applied to L2, and V_{L1} is applied to L1 to add E_{elec} to $E_{pot}(x = x_{r,dy})$. Subsequently, the beam moves towards L1, making $x = x_{f,dy}.x_{f,dy}$ is defined as the pull-in distance under the dynamic slingshot operation. When the movable beam reaches $x = x_{f,dy}$, following the energy conservation law, it stores $E_{pot}(x = x_{f,dy})$ as follows:

$$E_{pot}(x = x_{f,dy}) = E_{pot}(x = x_{r,dy}) + E_{elec}.$$
 (4)

 E_{elec} is derived as,

$$E_{elec} = \int_{x_{r,dy}}^{x_{f,dy}} \frac{\varepsilon_0 L_{beam} W_{beam} V_{L1}^2}{2(t_{gap} - x)^2} dx$$

= $\frac{\varepsilon_0 L_{beam} W_{beam} V_{L1}^2(x_{r,dy} - x_{f,dy})}{2(t_{gap} - x_{r,dy})(t_{gap} - x_{f,dy})},$ (5)

Each term in (4) is expressed as follows:

$$E_{pot}(x = x_{r,dy}) = kx_{r,dy}^2/2,$$
 (6)

$$E_{pot}(x = x_{f,dy}) = k x_{f,dy}^2 / 2.$$
 (7)

Combining (4)–(7), the V_{L1} required to move the beam from $x_{r,dy}$ to $x_{f,dy}$ ($V_{L1}(x_{r,dy} > x_{f,dy})$) is calculated as,

$$V_{L1}(x_{r,dy} \to x_{f,dy}) = \sqrt{\frac{k(x_{f,dy} + x_{r,dy})(t_{gap} - x_{f,dy})(t_{gap} - x_{r,dy})}{\varepsilon_0 L_{beam} W_{beam}}}.$$
 (8)

- -

The maximum value of $x_{f,dy}$ ($x_{f,dy,max}$) is calculated by applying the following condition:

$$\frac{dV_{L1}(x_{r,dy} \to x_{f,dy})}{dx_{f,dy}} = 0.$$
(9)

Then,

$$x_{f,dy,\max} = (t_{gap} - x_{r,dy})/2.$$
 (10)

which represents the pull-in location. By combining (8) and (10), $V_{p,sling,dy}$ is calculated as

$$V_{p,sling,dy} = \sqrt{\frac{k(t_{gap} + x_{r,dy})^2(t_{gap} - x_{r,dy})}{4\varepsilon_0 L_{beam} W_{beam}}}.$$
 (11)

For the minimization of the total voltage required to pull in the movable beam, $V_{p,sling,dy}$ should be equal to $V_{p,back,dy}$. To meet this condition, $x_{r,dy}$ becomes $-0.236t_{gap}$, which is called the optimized $x_{r,dy}$ ($x_{r,dy,opt}$). It has been proved that the movable beam can store more E_{pot} under the dynamic pull-back operation than under the static one as $x_{r,dy,opt}$ is larger than $x_{r,st,opt}$. The optimized $V_{p,sling,dy}$ ($V_{p,sling,dy,opt$) becomes,

$$V_{p,sling,dy,opt} = \sqrt{\frac{9kt_{gap}^3}{50\varepsilon_0 L_{beam} W_{beam}}}.$$
 (12)

The three V_p 's including $V_{p,conv}$, $V_{p,sling,st,opt}$, and $V_{p,sling,dy,opt}$ are compared as follows:

$$\frac{V_{p,sling,dy,opt}}{V_{p,conv}} = \sqrt{\frac{243}{400}} \approx 0.78,$$
(13)

$$\frac{V_{p,sling,dy,opt}}{V_{p,sling,st,opt}} = \sqrt{\frac{343}{400}} \approx 0.92.$$
(14)

This confirms that the proposed dynamic slingshot operation makes V_p 0.78 times and 0.92 times lower than conventional pull-in and static slingshot operations, respectively. However, it should be noted that the above-shown results are derived assuming the ideal vacuum condition and 1D parallel plate model.

The proposed dynamic slingshot operation is reevaluated, reflecting a finite Q and the actual cantilever beam shape. FEA simulation was performed in comparison with the 1D parallel plate model, referring to the simulation parameters summarized in Table 1. Fig. 3 compares the proposed dynamic slingshot operation with the previously proposed static operation in terms of $V_{p,sling,dy,opt}/V_{p,conv}$,

TABLE 1. Summarized simulation parameters.

Parameters	Values
Beam material	Cu
Young's modulus (E)	110 Gpa
Initial gap (g_0)	65 nm
Beam thickness (t _{beam})	65 nm
Beam width (W_{beam})	900 nm
Beam length (L_{beam})	3 µm



FIGURE 3. (a) $V_{p,sling,dy,opt}/V_{p,conv}$ and $x_{r,dy,opt}$ (dynamic slingshot operation) and (b) $V_{p,sling,st,opt}/V_{p,conv}$ and $x_{r,st,opt}$ (static slingshot operation) calculated by the analytical and FEA method with the variation of Q.

 $V_{p,sling,st,opt}/V_{p,conv}$, $x_{r,dy,opt}$, and $x_{r,st,opt}$, with the variation of Q. Q is known to be inversely proportional to damping [22]. A high Q case is discussed as NEM memory switches are generally operated under near-vacuum environments in CMOS metal interconnection layers [23]. According to the analytical model, when Q is $\sim 10^4 V_{p,sling,dy,opt}/V_{p,conv}$ is ~ 0.78 as predicted in (13), $V_{p,sling,st,opt}/V_{p,conv}$ is ~ 0.84 , as shown in our previous work [18]. In contrast, the FEA model shows that the slingshot operation is more effective than the analytical model because the movable beam stores more E_{pot} during pull-back operation in the case of the FEA model than in the case of the analytical model considering different $x_{r,dy,opt}$ values. According to the FEA simulation, $V_{p,sling,dy,opt}/V_{p,conv}$ is ~ 0.73 , and $V_{p,sling,st,opt}/V_{p,conv}$ is ~ 0.80 when Q is $\sim 10^4$. This highlights that the proposed dynamic slingshot operation is more advantageous in actual cases than predicted in (13) and (14) as the FEA model is generally more accurate than the analytical model [20]. Subsequently, as Q decreases, both $V_{p,sling,dy,opt}/V_{p,conv}$ and $V_{p,sling,st,opt}/V_{p,conv}$ increase. This is because the movable beam loses more energy during both pull-back and pull-in operation due to higher damping. This can be explained by observing that both $x_{r,dy,opt}$, and $x_{r,st,opt}$ increase as Q decreases. Thus, as the damping increases, it lowers the advantages of the slingshot operation over conventional pull-in operation. However, even when Qis ~10, $V_{p,sling,dy,opt}/V_{p,conv}$ is ~0.77, which is better than $V_{p,sling,st,opt}/V_{p,conv}$ under infinite Q.

Sophisticated timing control is required to take full advantage of the proposed dynamic slingshot operation. The pull-back operation should be converted into the pull-in operation when the movable beam reaches $x_{r,dy,opt}$. This may be difficult to implement in the actual beam operation owing to the variation issues such as mechanical delay and signal propagation delay [24], [25]. Fig. 4 shows the influence of the timing error (τ_{er}) on $V_{p,sling,dy,opt}/V_{p,conv}$ as a function of Q predicted by the analytical and FEA models. τ_{er} is defined as the difference between the time when the pullback operation is converted into the pull-in operation and the time when the movable beam reaches $x_{r,dy,opt}$. For example, zero $\tau_{\rm er}$ corresponds to the ideal case, while negative or positive τ_{er} indicates that the conversion from the pull-back into pull-in operation before and after the beam reaches $x_{r,dv,opt}$. A smaller τ_{er} is desirable to store a higher E_{pot} in the movable beam to maximize the merit of the proposed dynamic slingshot operation. As shown in Fig. 4, as Qbecomes smaller, V_{p,sling,dy,opt}/V_{p,conv} becomes less sensitive to τ_{er} . It is because that the difference between $x_{r,dy,opt}$ under the non-zero τ_{er} case and $x_{r,dy,opt}$ under the zero τ_{er} case is very small during τ_{er} as Q decreases. However, even when Q reaches 10⁴, $V_{p,sling,dy,opt}/V_{p,conv}$ is still insensitive to τ_{er} . A ± 30 ns deviation in τ_{er} leads to only 1.4% and 1.3% variation in $V_{p,sling,dy,opt}$, according to the analytical and FEA results, respectively. Notably, according to the FEA results, even if Q is reduced to 100 and $\tau_{\rm er}$ is ± 30 ns, $V_{\rm p,sling,dy,opt}/V_{\rm p,conv}$ continues to remain ~0.74, indicating that the proposed dynamic slingshot operation is reliable and immune to process and timing variation issues.

Finally, the influence of the dynamic and static slingshot operation on the V_{DD} of NEM memory switches is compared. As mentioned in an earlier study, the V_{DD} of the NEM memory switch is determined as $max(V_p, V_s)$, which is equal to V_p in the case of a small L_{beam} [14]. Fig. 5 shows the analytical $V_{p,conv}$, $V_{p,sling,st,opt}$, $V_{p,sling,dy,opt}$, V_s , and FEA $V_{p,sling,dy,opt}$ as a function of L_{beam} of NEM memory switch, whose W_{beam} , t_{beam} , and t_{gap} are 900 nm, 65 nm, and 65 nm, respectively. According to [14], V_s is derived in (15), as shown at the top of the next page, where p is the surface adhesion force per unit area, α is the length of the beam part that is not affected by p, β is the ratio of the capacitance calculated by the actual beam shape to that calculated by the parallel-plate model, and d_{vdw} is the van der Waals distance. Values for these have

$$V_s = \sqrt{\frac{2(2\beta t_{beam})^2}{\varepsilon_0} \left(p(1 - \frac{4\alpha^3}{3L_{beam}^3} + \frac{\alpha^4}{3L_{beam}^4}) - \frac{k(t_{beam} - d_{vdw})}{L_{beam}} \right)}.$$
(15)



FIGURE 4. Ratio of $V_{p, sling, dy, opt}$ to $V_{p, conv}$ calculated by (a) the analytical and (b) FEA methods with the variation of τ_{er} and Q. Zero τ_{er} represents the ideal dynamic slingshot operation case.



FIGURE 5. Comparison of V_{DD}'s and V_p's using conventional, static, and dynamic pull-in operation as a function of L_{beam} based on the analytical and FEA methods.

been calculated as $p = 0.450 \ \mu \text{N}/\mu\text{m}^2$, $\beta = 0.655$ and $d_{\text{vdw}} = 1.5 \text{ nm} [14]$.

In summary, among the three kinds of NEM memory switch operations, the proposed dynamic slingshot operation achieves the lowest $V_{\rm DD}$ as well as the smallest $L_{\rm beam}$. The analytical model predicts that the minimal $V_{\rm DD}$ and $L_{\rm beam}$ are 1.56 V and 2.97 μ m in the case of conventional operation, 1.31 V, and 2.95 μ m in the case of the static slingshot operation, and 1.22 V and 2.94 μ m in the case of the dynamic slingshot operation. Furthermore, the FEA model predicts that the minimum V_{DD} and L_{beam} using the proposed dynamic slingshot operation are 1 V and 2.93 μ m, respectively. It should be noted that the V_{DD} of the NEM memory switch reaches the sub-1 V region, which is lower than the V_{DD} of the 65 nm CMOS node using the proposed dynamic slingshot operation.

III. CONCLUSION

A dynamic slingshot operation has been proposed. According to the FEA results, the proposed dynamic slingshot operation shows ~0.73 times lower V_p than conventional pull-in operation. Even when exposed to ±30 ns τ_{er} , the $V_{p,sling,dy,opt}$ varies by < 2%. Therefore, it is confirmed that the proposed dynamic slingshot operation is superior to conventional pull-in and static slingshot operations in terms of V_{DD} and size reduction. The proposed dynamic slingshot operation is also expected to be helpful for implementing low-operation voltage and high chip density of M3D CMOS-NEM hybrid RL circuits.

REFERENCES

- I. Kuon, R. Tessier, and J. Rose, "FPGA architecture: Survey and challenges," *Found. Trends Electron. Des. Autom.*, vol. 2, no. 2, pp. 135–253, 2007, doi: 10.1561/1000000005.
- [2] C. Chen, H.-S.-P. Wong, S. Mitra, R. Parsa, N. Patil, S. Chong, K. Akarvardar, J. Provine, D. Lewis, J. Watt, and R. T. Howe, "Efficient FPGAs using nanoelectromechanical relays," in *Proc. 18th Annu. ACM/SIGDA Int. Symp. Field Program. Gate Arrays (FPGA)*, New York, NY, USA, 2010, pp. 273–282, doi: 10.1145/1723112.1723158.
- [3] J. O. Lee, Y.-H. Song, M.-W. Kim, M.-H. Kang, J.-S. Oh, H.-H. Yang, and J.-B. Yoon, "A sub-1-volt nanoelectromechanical switching device," *Nature Nanotechnol.*, vol. 8, no. 1, pp. 36–40, Jan. 2013, doi: 10.1038/nnano.2012.208.
- [4] S. Chong, K. Akarvardar, R. Parsa, J.-B. Yoon, R. T. Howe, S. Mitra, and H.-S.-P. Wong, "Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage," in *Proc. Int. Conf. Comput.-Aided Design (ICCAD)*, San Jose, CA, USA2009, pp. 478–484, doi: 10.1145/1687399.1687490.
- [5] N. Xu, J. Sun, I.-R. Chen, L. Hutin, Y. Chen, J. Fujiki, C. Qian, and T.-J.-K. Liu, "Hybrid CMOS/BEOL-NEMS technology for ultra-lowpower IC applications," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2014, p. 28, doi: 10.1109/IEDM.2014.7047130.
- [6] T. Qin, S. J. Bleiker, S. Rana, F. Niklaus, and D. Pamunuwa, "Performance analysis of nanoelectromechanical relay-based fieldprogrammable gate arrays," *IEEE Access*, vol. 6, pp. 15997–16009, 2018, doi: 10.1109/ACCESS.2018.2816781.
- [7] Y. J. Kim and W. Y. Choi, "Nonvolatile nanoelectromechanical memory switches for low-power and high-speed field-programmable gate arrays," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 673–679, Feb. 2015, doi: 10.1109/TED.2014.2380992.
- [8] H. S. Kwon, S. K. Kim, and W. Y. Choi, "Monolithic three-dimensional 65-nm CMOS-nanoelectromechanical reconfigurable logic for Sub-1.2-V operation," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1317–1320, Sep. 2017, doi: 10.1109/LED.2017.2726685.

- [9] A. Peschot, C. Qian, and T.-J. Liu, "Nanoelectromechanical switches for low-power digital computing," *Micromachines*, vol. 6, no. 8, pp. 1046–1065, Aug. 2015, doi: 10.3390/mi6081046.
- [10] Y. Zhou, S. Thekkel, and S. Bhunia, "Low power FPGA design using hybrid CMOS-NEMS approach," in *Proc. Int. Symp. Low power Electron. Design (ISLPED)*, 2007, pp. 14–19, doi: 10.1145/1283780.1283785.
- [11] R. Venkatasubramanian, S. K. Manohar, and P. T. Balsara, "NEM relay-based sequential logic circuits for low-power design," *IEEE Trans. Nanotechnol.*, vol. 12, no. 3, pp. 386–398, May 2013, doi: 10.1109/TNANO.2013.2252923.
- [12] T.-J.-K. Liu, N. Xu, I.-R. Chen, C. Qian, and J. Fujiki, "NEM relay design for compact, ultra-low-power digital logic circuits," in *IEDM Tech. Dig.*, Dec. 2014, p. 13, doi: 10.1109/IEDM.2014.7047042.
- [13] J. Rubin, R. Sundararaman, M. Kim, and S. Tiwari, "A low-voltage torsion nanorelay," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 414–416, Mar. 2011, doi: 10.1109/LED.2010.2099199.
- [14] H. M. Lee, H. C. Jo, H. S. Kwon, and W. Y. Choi, "Switching voltage analysis of nanoelectromechanical memory switches for monolithic 3-D CMOS-NEM hybrid reconfigurable logic circuits," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3780–3785, Jun. 2018, doi: 10.1109/TED.2858775.
- [15] Y. Qian, L. Lou, M. J. Tsai, and C. Lee, "A dual-silicon-nanowires based U-shape nanoelectromechanical switch with low pull-in voltage," *Appl. Phys. Lett.*, vol. 100, no. 11, Mar. 2012, Art. no. 113102, doi: 10.1063/1.3693382.
- [16] X. L. Feng, M. H. Matheny, C. A. Zorman, M. Mehregany, and M. L. Roukes, "Low voltage nanoelectromechanical switches based on silicon carbide nanowires," *Nano Lett.*, vol. 10, no. 8, pp. 2891–2896, Aug. 2010, doi: 10.1021/nl1009734.
- [17] J. E. Jang, S. N. Cha, Y. Choi, T. P. Butler, D. J. Kang, D. G. Hasko, J. E. Jung, Y. W. Jin, J. M. Kim, and G. A. J. Amaratunga, "Nanoelectromechanical switch with low voltage drive," *Appl. Phys. Lett.*, vol. 93, no. 11, Sep. 2008, Art. no. 113105, doi: 10.1063/1.2983743.
- [18] W. Y. Choi and H. S. Kwon, "Slingshot pull-in operation for low-voltage nanoelectromechanical memory switches," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2040–2043, Apr. 2019, doi: 10.1109/TED.2019.2899888.
- [19] R. Sattler, F. Plotz, G. Fattinger, and G. Wachutka, "Modeling of an electrostatic torsional actuator: Demonstrated with an RF MEMS switch," *Sens. Actuators A, Phys.*, vols. 97–98, pp. 337–346, Apr. 2002, doi: 10.1016/S0924-4247(01)00852-4.
- [20] S. H. Roh, K. Kim, and W. Y. Choi, "Scaling trend of nanoelectromechanical (NEM) nonvolatile memory cells based on finite element analysis (FEA)," *IEEE Trans. Nanotechnol.*, vol. 10, no. 3, pp. 647–651, May 2011, doi: 10.1109/TNANO.2010.2068056.
- [21] G. N. Nielson and G. Barbastathis, "Dynamic pull-in of parallel-plate and torsional electrostatic MEMS actuators," J. *Microelectromech. Syst.*, vol. 15, no. 4, pp. 811–821, Aug. 2006, doi: 10.1109/JMEMS.2006.879121.

- [22] G. M. Rebeiz, "Mechanical modeling of MEMS devices: Dynamic analysis," in *RF MEMS Theory, Design, and Technology*, vol. 3, 1st ed. Hoboken, NJ, USA: Wiley, 2003, ch. 3, sec. 3, pp. 62–64.
- [23] H. C. Jo and W. Y. Choi, "Encapsulation of NEM memory switches for monolithic-three-dimensional (M3D) CMOS–NEM hybrid circuits," *Micromachines*, vol. 9, no. 7, p. 317, Jul. 2018, doi: 10.3390/mi9070317.
- [24] F. Chen, H. Kam, D. Markovic, T. J. K. Liu, V. Stojanovic, and E. Alon, "Integrated circuit design with NEM relays," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design*, San Jose, CA, USA, Nov. 2008, pp. 750–757, doi: 10.1109/ICCAD.2008.4681660.
- [25] U. Sikder, G. Usai, T.-T. Yen, K. Horace-Herron, L. Hutin, and T.-J.-K. Liu, "Back-End-of-Line Nano-Electro-Mechanical switches for reconfigurable interconnects," *IEEE Electron Device Lett.*, vol. 41, no. 4, pp. 625–628, Apr. 2020, doi: 10.1109/LED.2020.2974473.



MIN HEE KANG (Student Member, IEEE) was born in Suwon, in 1995. She received the B.S. degree in nanotechnology and advanced materials engineering from Sejong University, Seoul, South Korea, in 2018. She is currently pursuing the M.S. degree with the Department of Electronic Engineering, Sogang University, Seoul. Her current research interests include nanoelectromechanical (NEM) relays/memory cell.



WOO YOUNG CHOI (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Seoul National University, Seoul, South Korea, in 2000, 2002, and 2006, respectively. From 2006 to 2008, he held a postdoctoral position with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, USA. Since 2008, he has been a Faculty Member with Sogang University, Seoul,

where he is currently a Professor with the Department of Electronic Engineering. He has authored or coauthored 284 articles in international journals and conference proceedings. He holds 47 Korean patents. His current research interests include fabrication, modeling, characterization and measurement of CMOS, emerging devices, and memory.