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Design Guidelines for Gate-Normal Hetero-Gate-Dielectric (GHG) Tunnel Field-Effect Transistors (TFETs)

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ABSTRACT A gate-normal hetero-gate-dielectric (GHG) tunnel field-effect transistor (TFET) and the guidelines for its design are proposed. The introduction of the HG structure into gate-normal TFETs improves device performance by lowering subthreshold swing (SS). It is confirmed that the SS of the proposed GHG TFET is successfully enhanced by suppressing the gate-diagonal tunneling current. Compared with conventional gate-normal TFETs, the final optimized GHG TFET improves the values of the point SS, effective SS, and on-current by 71 %, 15 %, and 2.4 times, respectively.

INDEX TERMS Band-to-band tunneling (BTBT), gate-normal hetero-gate-dielectric tunnel field-effect transistor (GHG TFET), subthreshold swing (SS).

I. INTRODUCTION

State-of-the-art metal-oxide-semiconductor field-effect transistors (MOSFETs) are faced with the two major problems of size and power reduction, both of which are related to fundamental physical limits [1]. As an alternative to MOSFETs, tunnel field-effect transistors (TFETs) have recently been studied [2], [3]. It is because TFETs have short-channel-effect (SCE) immunity and low supply voltage (V_{DD}), which stem from the band-to-band tunneling (BTBT) operation [4], [5]. However, their low on-current (I_{on}) has been problematic because the subthreshold swing (*SS*) becomes degraded as drain current (I_D) increases [6], [7]. To obtain higher I_{on}, several ideas have been proposed: pocket doping [8], bandgap engineering [9] and a hetero-gate-dielectric (HG) structure [10]. In addition, gate-normal tunneling (also referred to vertical [11] or line tunneling [12]) has been considered potential solutions [13] for the following reasons. First, I_{on} could be boosted by increasing the gate-source overlap region, which leads to the BTBT area. Second, gate-normal tunneling shows abrupt on-off transition [11]–[17]. In spite of these advantages, gate-normal TFETs suffer from gate-diagonal tunneling current [13], [18]. Because the gate-diagonal tunneling originates from the corner of the source edge, it degrades the on-off transition abruptness of gate-normal TFETs. Specifically, the BTBT direction gradually changes from the gate-parallel to gate-normal direction as the gate-overdrive voltage (V_{ov}) increases as shown in Fig. 1a. It means that the gate-diagonal tunneling current is dominant before the complete turn-on of the gate-normal tunneling. Thus, an abrupt switch from gate-parallel tunneling to gate-normal tunneling while minimizing gate-diagonal tunneling is necessary to improve the *SS* of gate-normal TFETs. To achieve this, some pioneering research results have been reported [19]–[21]. However, there remains room for the further suppression of gate-diagonal tunneling and its underlying physics have not been discussed in detail.

In this manuscript, Si-based gate-normal hetero-gate-dielectric (GHG) TFETs are proposed to improve the *SS* of gate-normal TFETs by suppressing the gate-diagonal tunneling current. The proposed GHG TFETs feature a low-k gate dielectric layer at the gate-channel overlap region and a high-k dielectric layer at the gate-source overlap region as shown in Fig. 1b. Figure 1 compares our proposed GHG TFETs

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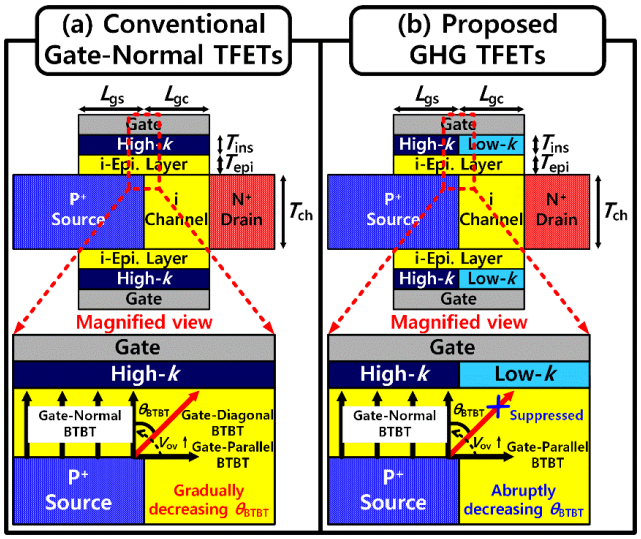

FIGURE 1. Schematic views of the (a) conventional gate-normal TFETs and (b) GHG TFETs. Magnified views of the dotted red boxes illustrate the dominant BTBT direction (red) with respect to the Vov for both devices. The dominant BTBT direction changes from gate-parallel to gate-normal direction as Vov increases. In addition, θBTBT is defined as the angle between the gate-normal direction and the dominant BTBT direction. In this case, the θBTBT of GHG TFETs is bigger than that of the conventional gate-normal TFETs due to the suppression of gate-diagonal tunneling.

with conventional gate-normal TFETs using only a high-k gate dielectric layer. GHG TFETs should have a smaller SS than conventional gate-normal TFETs because the low-k dielectric layer suppresses gate-diagonal BTBT current. To obtain a theoretical explanation of the benefits of GHG TFETs, a quantitative analysis is performed by introducing the dominant BTBT path angle (θ_{BTBT}). A detailed discussion is presented in Section III.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

To compare the proposed GHG TFETs with conventional gate-normal TFETs, the two-carrier and two-dimensional device simulation were performed using Synopsys Sentaurus technology computer-aided design (TCAD) simulator [22]. The dynamic nonlocal BTBT, Shockley-Read-Hall recombination, Philips unified mobility model and Fermi distribution were used in our simulation. In addition, theoretically calculated A and B parameters of Kane's model for dynamic nonlocal BTBT are used [23]. Quantization effects were neglected and semi-classical approach is adapted for the simplicity of the simulation without losing the essential properties of TFETs. Also, gate-diagonal tunneling is a two-dimensional phenomenon as shown in Fig. 1, which causes self-consistency issues in TCAD simulation [22], [24], [25].

Gate length is defined as the sum of the gate-source overlap length (L_{gs}) and gate-channel overlap length (L_{gc}). In addition, HfO_2 and SiO_2 are used for high-k and low-k dielectric regions whose relative dielectric constant (k) values are 22.0, and 3.9, respectively. The lengths of high-k and low-k dielectric regions are assumed to be the same as L_{gs} and L_{gc}, respectively. Parameters T_{epi}, T_{ins}, and T_{ch} represent epitaxial layer thickness, gate dielectric thickness and channel thickness, respectively. Detailed simulation parameters are given in Table 1.

TABLE 1. Summarized simulation parameters.

Parameters	Values
L_{gs}	30 nm
L_{gc}	30 nm
T_{epi}	5 nm
T_{ins}	4 nm
T_{ch}	20 nm
Source doping concentration	1×10^{20} cm^{-3} (p-type)
Drain doping concentration	1×10^{20} cm^{-3} (n-type)
Dynamic nonlocal BTBT, A	1.64×10^{15} cm^{-3}/s
Dynamic nonlocal BTBT, B	23.8 MV/cm

For the quantitative analysis, V_{ov} is calculated as $V_{\mathrm{G}} - V_{\mathrm{off}}$. V_{G} and V_{off} indicate the gate voltage and off-state voltage, respectively. When $V_{\mathrm{G}} = V_{\mathrm{off}}$, the drain current ($I_{\mathrm{D}}$) is equal to the off-current (I_{off}): 0.1 fA/μm reflecting low I_{off} of Si-based TFETs [11], [17]. The on-current (I_{on}) is defined as I_{D} when $V_{\mathrm{ov}} = V_{\mathrm{D}} = 0.7$ V. Point SS (SS_{point}) is measured around V_{off} over 1 order of magnitude change in I_{D} while effective SS (SS_{eff}) is calculated as the average SS when I_{D} ranges from I_{off} to $I_{\mathrm{D}}(V_{\mathrm{G}} = 0.35$ V, $V_{\mathrm{D}} = 0.7$ V) [26].

III. DEVICE FABRICATION STEP

Figure 2 shows the key process steps of the proposed GHG TFETs. First, the oxide hard mask is formed on the prepared SOI wafer by using sidewall spacer patterning. Second, the SOI layer is etched to define the fin active regions. Third, source/drain regions are formed by masked boron/arsenic tilted ion implantation followed by rapid thermal annealing (RTA). Subsequently, the epitaxial layer for abrupt tunnel junctions is formed by selective epitaxial growth. The most important process step is the formation of the HG metal-gate (MG) stack. To avoid the dopant diffusion from the heavily doped source into the epitaxial layer, materials such as HfO_2, SiO_2 for HG and TiN for MG should be formed by atomic layer deposition (ALD). After the growth of epitaxial layers, SiO_2/TiN gate-stacks are formed and patterned. Then, the SiO_2 layer on the gate-source overlap region is removed by using hydrogen fluoride (HF) vapor. On the other hand, drain-side gate dielectric is protected by the photoresist mask which was used for source ion implantation. Thus, no additional photo mask is needed to form the HG. After a HfO_2 layer is formed on the gate-source overlap region, a HGMG stack is formed following the removal of residual HfO_2 by using HfO_2 dry etch. Finally, BEOL steps are performed.

IV. SIMULATION RESULTS AND DISCUSSION

A. CONCEPT OF SUPPRESSING GATE-DIAGONAL BTBT

For the implementation of ideal gate-normal TFETs, gate-diagonal tunneling, which appears during the on-off transition, should be suppressed effectively. In other words,

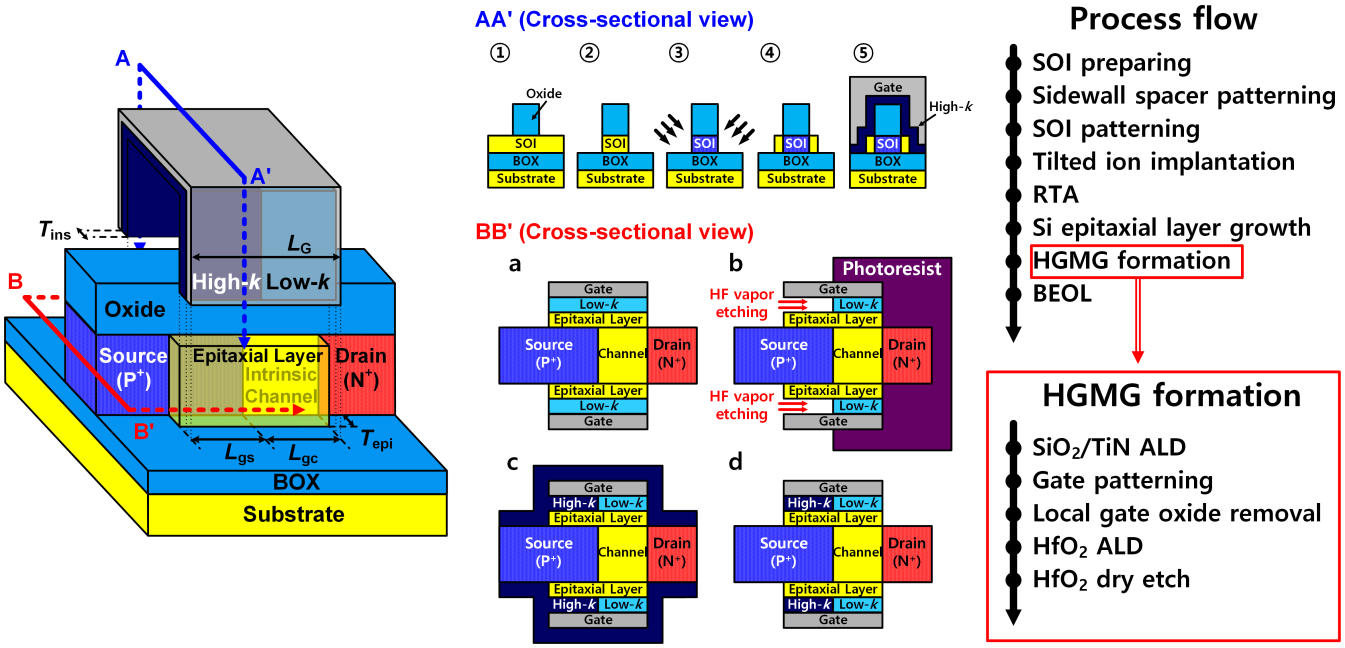

FIGURE 2. Bird's eye view of the proposed three-dimensional (3D) GHG TFET, its key process steps, and cross-sectional views following of AA' and BB' lines. Also, cross-sectional views of AA' and BB' show overall process flow and HGMG formation, respectively.

the *SS* reduction of gate-normal TFETs is feasible when the off-state, dominated by gate-parallel tunneling current, is abruptly changed to the on-state, dominated by gate-normal tunneling current without experiencing gate-diagonal tunneling current [11]–[17]. Note that gate-parallel tunneling current stems from the reverse-biased PIN diode. Thus, we propose the use of GHG TFETs to suppress the gate-diagonal tunneling and improve the *SS* of gate-normal TFETs. Figure 3 compares the simulated transfer curves of conventional gate-normal TFETs and our proposed GHG TFETs. As predicted, the latter show steeper *SS* than the former. Because GHG TFETs have a low-k dielectric layer on the gate-channel overlap region, the surface potential under this region is maintained at a low level. Additionally, the low-k dielectric region is helpful for suppressing the ambipolar behavior [10]. To explain the role of the low-k dielectric layer clearly, the electron BTBT generation rates of the conventional gate-normal TFETs and GHG TFETs in the off- and on-states are shown in Fig. 4. In the off-state, shown in Fig. 4a, gate-diagonal tunneling is the dominant tunneling mechanism in the case of conventional gate-normal TFETs whereas GHG TFETs show suppressed leakage at the same value of $V_{ov} = -50$ mV. In addition, the energy band diagrams of the conventional gate-normal TFET and GHG TFET are extracted in the gate-diagonal direction along the gradient of the valence band energy at the source where the maximum BTBT generation rate occurs, which is parallel with the electric field [22], [25]. Moreover, as shown in Fig. 4, dominant BTBT path is defined from the point A where maximum hole BTBT generation rate occurs to the point A' where maximum electron BTBT generation rate occurs. Also, it follows the gradient of valence band energy.

For quantitative analysis, θ_{BTBT} is introduced, which is defined as the angle between the gate-normal and maximum BTBT direction (*A*-*A*' line). Unlike conventional gate-normal TFETs, gate-diagonal tunneling is suppressed. It is because the valence band energy of the source is not aligned with the conduction band energy of the channel in the case of GHG TFETs. In contrast, in the on-state shown in Fig. 4b, gate-normal tunneling becomes dominant for both kinds of TFETs. It is observed that the maximum electron BTBT generation rate of GHG TFETs is higher than that of conventional gate-normal TFETs. According to the energy band diagrams extracted in the gate-normal direction from the middle of gate-source overlap with $\theta_{BTBT} = 0°$ (*A*-*A*' line), the conduction and valence energy band edges of GHG TFETs are located lower than those of conventional gate-normal TFETs. Thus, suppressing the gate-diagonal tunneling makes the on-off transition more abrupt in GHG TFETs.

B. DEVICE OPTIMIZATION

As mentioned before, the direction of the dominant BTBT path varies as a function of V_{ov}. In this manuscript, the direction is investigated quantitatively by introducing the dominant BTBT angle (θ_{BTBT}) which is defined as the angle between the gate-normal direction and the dominant BTBT direction as shown in Fig. 1. The dominant BTBT direction is calculated as the gradient of the valence band energy at the source where the maximum BTBT generation rate is obtained. To calculate the θ_{BTBT}, the dot product of the vector calculation is used as below

$$\cos\theta_{BTBT} = \frac{u_{GN} \cdot u_{BTBT}}{\|u_{GN}\| \|u_{BTBT}\|} \quad (1)$$

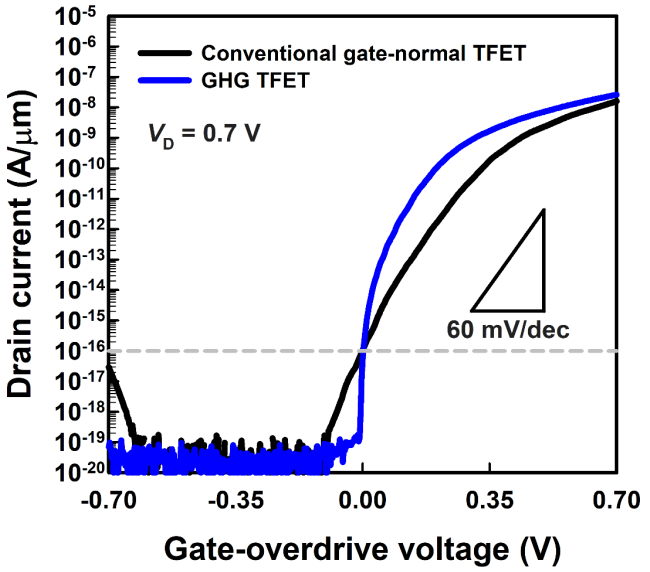

FIGURE 3. Transfer characteristics of the conventional gate-normal TFETs and the GHG TFETs. The SSeff's of conventional gate-normal and GHG TFETs are 56.00 mV/dec and 46.49 mV/dec, respectively. The minimum SSpoint's of conventional gate-normal and GHG TFETs are 38.31 mV/dec and 8.75 mV/dec, respectively.

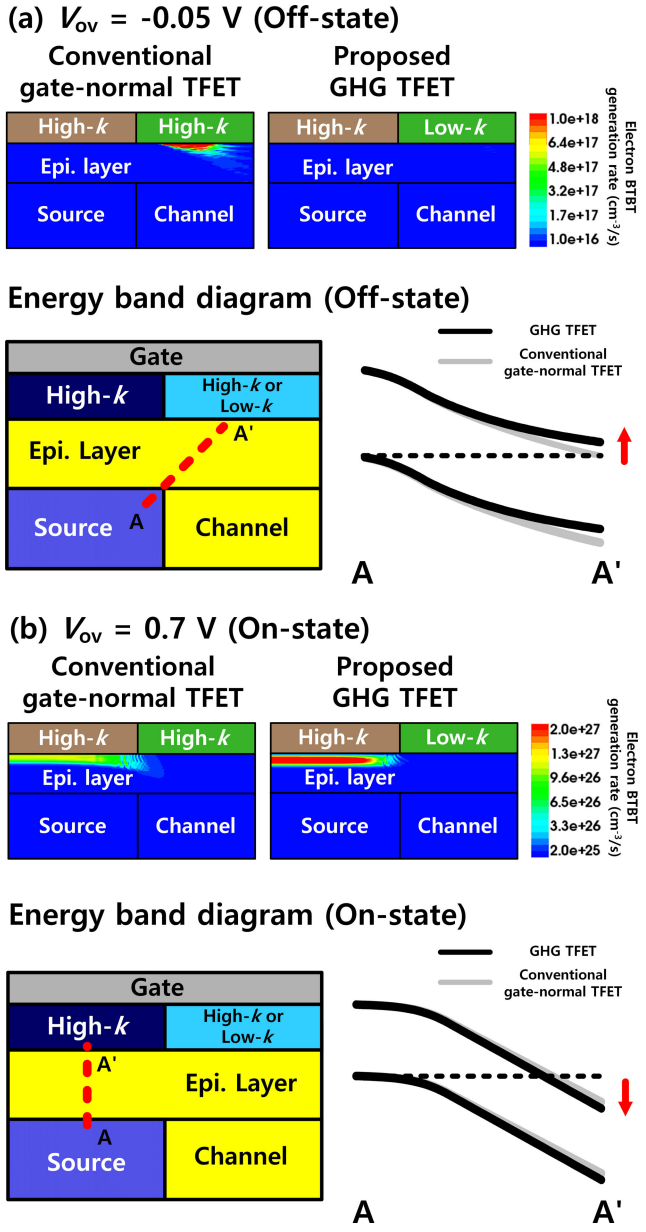

FIGURE 4. Electron BTBT generation rates and energy band diagrams of conventional gate-normal TFETs and proposed GHG TFETs in the (a) off- and (b) on-states. In addition, the off- and on-states of both devices are at the same Vov. These contours are the simulation results of the magnified views in Fig. 1. Energy band diagrams are extracted following A-A' lines, which is the gradient of valence band energy. Also, the points A and A' mean the locations where maximum hole and electron generation rate occur, respectively.

where u_{GN} and u_{BTBT} mean the unit vector of gate-normal direction and the unit vector of the electric field.

Figure 5 shows θ_{BTBT} as a function of V_{ov}. When V_{ov} is around 0 V, gate-parallel BTBT is dominant: $\theta_{BTBT} = 90°$. Then, as V_{ov} increases during on-off switching operation, gate-diagonal BTBT becomes stronger: $0° < \theta_{BTBT} < 90°$. Finally, when V_{ov} becomes so high that the surface potential at the gate-source overlap region is saturated, gate-normal BTBT is dominant: $\theta_{BTBT} = 0°$. The k values of the low-k dielectric layer (k_{low}) varies between 1 and 22 while those of the high-k dielectric layer (k_{high}) is fixed at 22 to show the validity of GHG TFETs for the suppression of gate-diagonal BTBT. When k_{low} is equal to 22, which corresponds to conventional gate-normal TFETs, as shown in Fig. 5a, θ_{BTBT} gradually decreases as V_{ov} increases. On the contrary, as k_{low} decreases, GHG TFETs show a more abrupt decrease in θ_{BTBT} as V_{ov} increases, as shown in Figs. 5b-5d. This means that GHG TFETs suppress the gate-diagonal BTBT more effectively as k_{low} decreases by making the on-off transition more abrupt. This is because the surface potential on the gate-channel overlap region decreases as k_{low} decreases, which suppresses gate-diagonal BTBT. In contrast, the reduction of k_{low} may decrease I_{on} by increasing channel resistance. Thus, it is necessary to optimize k_{low} in terms of both SS_{point} and I_{on}.

Figure 6 shows the influence of varying k_{low} on the electrical characteristics of GHG TFETs. From the transfer curves of Fig. 6a, SS_{point} and $I_{on}/I_{on,max}$ are extracted and shown in Fig. 6b. Here, $I_{on,max}$ is the maximum I_{on} that is obtained at $k_{low} = 7$. In this work, the optimized k_{low} ranges between 5 and 10, meeting the requirement that $I_{on}/I_{on,max} > 0.9$. If k_{low} decreases below 5, I_{on} decreases because channel resistance increases while SS_{point} reduction remains saturated, as shown in Fig. 6b. In contrast, if k_{low} exceeds 10, I_{on} also decreases because the gate-diagonal BTBT becomes stronger, which makes SS_{point} worse, as shown in Fig. 6b. Furthermore, V_{off} and $I_{on}/I_{on,max}$ with respect to various values of k_{low} are examined in Fig. 6c. When k_{low}increases, V_{off} decreases, as shown in Fig. 6c. This results from the revealed gate-diagonal tunneling current. Moreover, V_{off} shows a small change at a small cost to SS_{point} when k_{low} is increased in the optimized k_{low} range of 5 to 10. In contrast, if k_{low} is higher than 15,

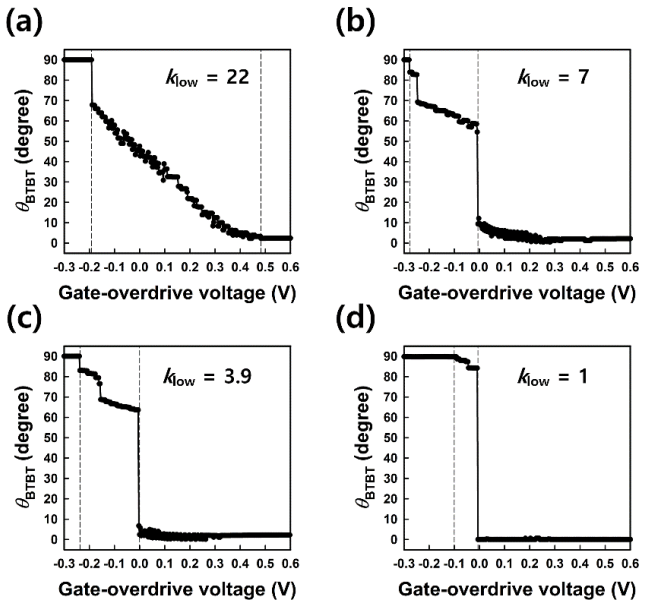

FIGURE 5. Calculated θBTBT as a function of Vov with respect to the value of k of the gate-dielectric on the gate-channel overlap region: (a) k = 22, (b) k = 7, (c) k = 3.9, and (d) k = 1. The value of k = 22 indicates the conventional gate-normal TFET whereas other values of k are for GHG TFETs. The interval marked by the dashed lines for Vov indicates where gate-diagonal tunneling occurs.

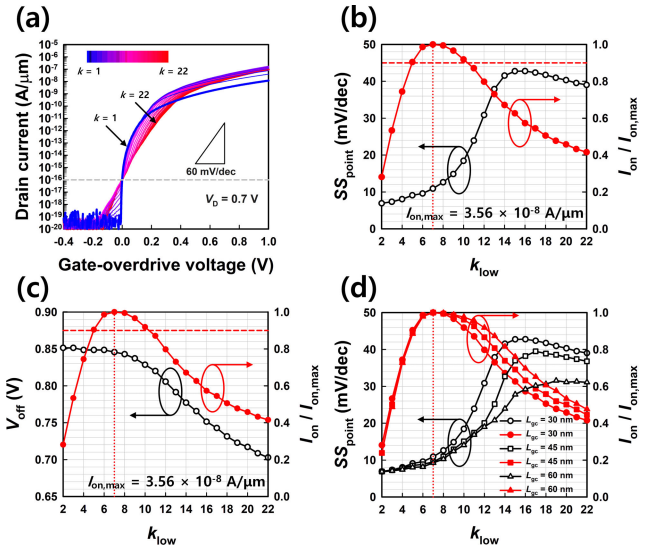

FIGURE 6. (a) ID-Vov characteristic of GHG TFETs for various values of klow. The blue and red curves represent klow = 1 and klow = 22, respectively. (b) SSpoint and Ion/Ion,max with respect to klow. (c) Voff and Ion/Ion,max with respect to klow. (d) SSpoint and Ion/Ion,max as a function of Lgc for various values of klow. The red dashed-line in (b)-(d) indicates Ion / Ion,max = 0.9 while the red dotted-line indicates the optimized value of klow (= 7). Also, the Ion,max of GHG TFETs with Lgc = 30, 45, and 60 nm are 3.56 × 10-8, 3.37 × 10-8, and 3.30 × 10-8 A/μm, respectively. Ion,max is obtained at klow = 7 for all Lgc's.

SS_{point} is enhanced while V_{off} is still decreased as shown in Figs. 6b and 6c. This is due to the enhanced SCE immunity in GHG TFETs owing to the increased k_{low}. To verify the SCE of GHG TFETs, SS_{point} and I_{on} as functions of L_{gc} for various values of k_{low} are shown in Fig. 6d. It is clear in Fig. 6d

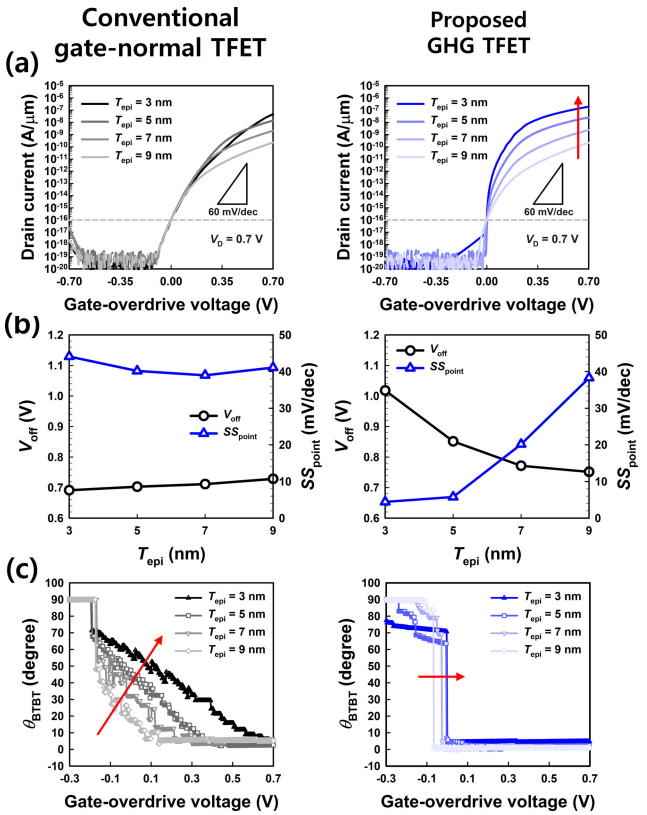

FIGURE 7. (a) ID-Vov characteristics of conventional gate-normal TFETs (left) and GHG TFETs (right). (b) SSpoint and Voff for various values of Tepi for conventional gate-normal TFETs (left) and GHG TFETs (right). (c) θBTBT with respect to Vov as a function of Tepi of conventional gate-normal TFETs (left) and GHG TFETs (right). The red arrows in (a) and (c) imply the direction of change as Tepi decreases. From (a), the Ion of conventional gate-normal TFETs as Tepi increases are 4.587 × 10-8, 1.390 × 10-8, 2.045 × 10-9, and 2.243 × 10-10 A/μm respectively. In addition, the Ion of GHG TFETs as Tepi increments are 19.342 × 10-8, 2.533 × 10-8, 2.338 × 10-9, and 2.131 × 10-10 A/μm, respectively. From (c), the onsets of gate-normal tunneling in conventional gate-normal TFETs with respect to the Tepi = 3, 5, 7, and 9 nm are Vov = 0.640 V, 0.391 V, 0.300 V, and 0.137 V, respectively. In addition, the onsets of gate-normal tunneling in GHG TFETs with respect to the values Tepi = 3, 5, 7, and 9 nm are Vov = 0.000 V, -0.003 V, -0.026 V, and -0.066 V, respectively.

that both SS_{point} and I_{on} deteriorate as L_{gc} decreases when k_{low} exceeds 15. Furthermore, the slight SS_{point} improvement fades away with respect to the increase of L_{gc}. This is because SCE is mitigated as L_{gc} increases [14], [27]. Also, the electric field in the gate-parallel direction becomes stronger as L_{gc} decreases. Thus, gate-diagonal tunneling degrades SS_{point} and I_{on} more substantially for a smaller value of L_{gc}. Furthermore, GHG TFETs with k_{low} around the optimized value of 7 show better SS_{point} and I_{on} than conventional gate-normal TFETs (k_{low} = 22) as shown in Fig. 6d. Moreover, SS_{point} at k_{low} =~7 shows little difference with the variation of L_{gc} which is contrast to conventional gate-normal TFETs. It is because k_{low} lowering weakens the gate-parallel electric field. Thus, GHG TFETs is superior to conventional gate-normal TFETs in terms of scalability if the gate-diagonal tunneling is effectively suppressed.

Figure 7 shows the influence of T_{epi} on conventional gate-normal and GHG TFETs. The transfer curves of conventional

gate-normal TFETs and GHG TFETs are depicted with respect to T_{epi} in Fig. 7a. In Fig. 7b, to examine the effect of T_{epi} variation, SS_{point} and V_{off} as a function of T_{epi} in both types of TFETs are extracted from Fig. 7a.

It has been reported that SS_{point} is enhanced whereas V_{off} is increased as T_{epi} decreases [28]. Thus, SS_{point} and V_{off} are in a trade-off relationship as T_{epi} varies. However, these results are dissimilar to those reported in [28] in the case of conventional gate-normal TFETs when considering gate-diagonal tunneling, as shown in Fig. 7b. For conventional gate-normal TFETs, constant SS_{point} and V_{off} with respect to T_{epi} are shown in Fig. 7b. This is due to the gate-diagonal tunneling which determines the value of SS_{point} and V_{off} regardless of the value of T_{epi}. In contrast, GHG TFETs show the aforementioned trade-off relationship in SS_{point} and V_{off}, as depicted in Fig. 7b. This is because gate-diagonal tunneling is successfully suppressed for GHG TFETs.

To further investigate the effect of gate-diagonal tunneling as a function of T_{epi}, θ_{BTBT} for both types of TFETs is plotted in Fig. 7c. As T_{epi} decreases, gate-diagonal tunneling degrades the switching characteristic of conventional gate-normal TFETs. In addition, the average slope of θ_{BTBT} where gate-diagonal tunneling occurs ($0° < \theta_{BTBT} < 90°$) decreases as T_{epi} becomes thinner. This implies that the surface potential changes more slowly as T_{epi} decreases. This results in an increased onset of gate-normal tunneling, where θ_{BTBT} reaches 0° as T_{epi} is reduced. Therefore, hump effect appears in conventional gate-normal TFETs, as shown in Fig. 7a when T_{epi} decreases, especially for $T_{epi} = 3$ nm. Likewise, the average slope of θ_{BTBT} where gate-diagonal tunneling occurs ($0° < \theta_{BTBT} < 90°$) also decreases when T_{epi} is decreased for the GHG TFETs.

Furthermore, the onset of gate-normal tunneling increases as $T_{epi}$is reduced for GHG TFETs. However, the differences in the onset of gate-normal tunneling are small for GHG TFETs compared with those of conventional gate-normal TFETs, as shown in Fig. 7c. This is because of the suppressed gate-diagonal tunneling, which leads to further improvement in SS_{point} as T_{epi} decreases in the case of GHG TFETs. Overall, a T_{epi} of 5 nm is an optimal value for the GHG TFETs with little cost to SS_{point} and V_{off}.

In contrast, the I_{on} of both conventional gate-normal and GHG TFETs increases with respect to reductions in T_{epi}. This is due to shortened gate-normal tunnel distance. Note that the I_{on} of conventional gate-normal TFETs is slightly larger than that of GHG TFETs when T_{epi} is 9 nm. It is because the gate-normal tunnel distance is long enough to have a low tunneling probability for both types of TFETs. Thus, the currents of both gate-diagonal and gate-normal tunneling are similar. Whereas gate-diagonal tunneling current is added to the gate-normal tunneling current in conventional gate-normal TFETs, gate-diagonal tunneling is suppressed in GHG TFETs, which reverses I_{on} when T_{epi} is equal to 9 nm. Hence, the I_{on} and SS_{point} of conventional gate-normal and GHG TFETs show smaller differences as T_{epi} increases.

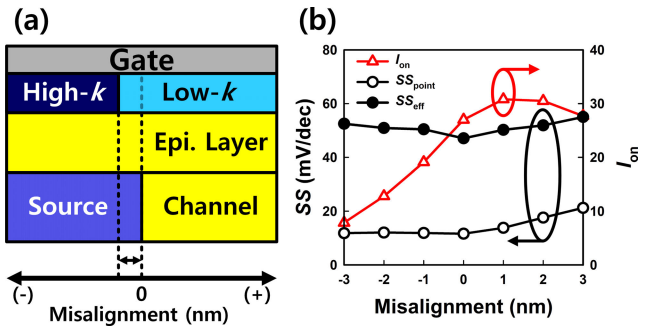

FIGURE 8. (a) Misalignment between the source-edge and HG structure of GHG TFETs. Positive (+) and negative (–) misalignment mean extended high-k dielectric and low-k dielectric, respectively. (b) SSpoint, SSeff, and Ion as functions of misalignment when klow is 3.9.

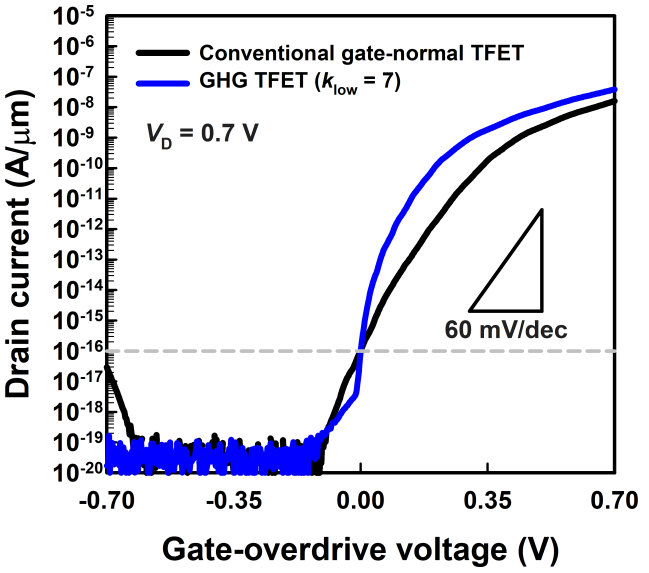

FIGURE 9. Transfer characteristics of the conventional gate-normal and optimized GHG TFETs. Here, klow = 7, Tepi = 5 nm for the optimized GHG TFETs. SSeff's are 56.00 mV/dec and 47.87 mV/dec for conventional gate-normal and optimized GHG TFETs, respectively. The minimum SSpoint's are 38.31 mV/dec and 11.27 mV/dec for conventional gate-normal and GHG TFETs, respectively. Furthermore, Ion's are 1.58 × 10-8 A/μm and 3.83 × 10-8 A/μm for conventional gate-normal and optimized GHG TFETs, respectively.

Figure 8 shows the effects of misalignment in GHG TFETs. Overall, it is observed that both SS_{point} and SS_{eff} are less sensitive to misalignment than I_{on}. For positive misalignment, SS_{point} and I_{on} are rarely degraded due to the revealed gate-diagonal tunneling. On the contrary, I_{on} is more sensitive to negative misalignment than positive one because the high-k dielectric affects the channel resistance. Thus, positive misalignment would be preferred for less severe process variation.

Figure 9 represents the transfer curves of the optimized conventional gate-normal and GHG TFETs. The optimized GHG TFETs use $k_{low} = 7$, and $T_{epi} = 5$ nm. This figure shows that the optimized GHG TFETs reduce the values of SS_{point} and SS_{eff}, by 71 % and 15 %, respectively, and

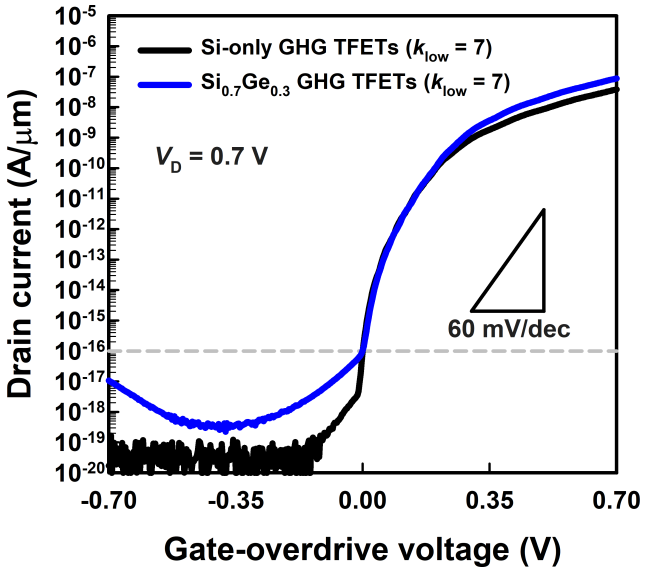

FIGURE 10. Transfer characteristics of Si-only GHG TFETs and SiGe GHG TFETs whose klow and Tepi are 7 and 5 nm, respectively. SSeff's are 47.87 mV/dec and 46.24 mV/dec for Si-only GHG TFETs and SiGe GHG TFETs, respectively. The minimum SSpoint's are 11.27 mV/dec and 15.81 mV/dec for Si-only GHG TFETs and SiGe GHG TFETs, respectively. The Ion's of Si-only and SiGe GHG TFETs are 3.83 × 10-8 A/μm and 8.77 × 10-8 A/μm, respectively.

increase I_{on} by 2.4 times when compared with conventional gate-normal TFETs.

Finally, it is still necessary to boost the I_{on} of GHG TFETs. Thus, SiGe homojunction GHG TFETs are introduced. Fig. 10 compares the transfer characteristics of Si-only GHG TFETs with those of SiGe GHG TFETs whose k_{low} and Tepi are 7 and 5 nm, respectively. Ge content is assumed to be 30% considering I_{off}. As shown in Fig. 10, SiGe GHG TFETs achieve 2.3x higher I_{on} than Si-only GHG TFETs. It is observed that the SS_{point} and SS_{eff} of SiGe GHG TFETs are 15.81 mV/dec and 46.24 mV/dec, respectively, which are analogous to those of Si-only GHG TFETs. Moreover, the transfer characteristic of SiGe homojunction GHG TFETs exhibits no hump effect compared with SiGe heterojunction TFETs owing to the absence of valence band offset around the source [20].

V. CONCLUSION

In this paper, GHG TFETs are proposed to improve the switching characteristics of conventional gate-normal TFETs. These TFETs feature as low *SS* by better suppressing the gate-diagonal tunneling current compared with conventional gate-normal TFETs. In addition, the device design is optimized by modulating k_{low} and T_{epi}. The optimized GHG TFETs exhibit an increase of 2.4 times for I_{on}, and decreases of 71 % and 15 % for SS_{point} and SS_{eff}, respectively, compared with conventional gate-normal TFETs. Moreover, the characteristics of the gate-diagonal tunneling are quantitatively analyzed in terms of the dominant BTBT direction by comparing the proposed GHG TFETs with conventional gate-normal TFETs. For further performance improvement of GHG TFETs, narrow bandgap materials such as SiGe or Ge can be introduced. The results of this study indicate that GHG TFETs are a promising option for ultralow-power applications.

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REFERENCES

[1] A. M. Ionescu, "Energy efficient computing and sensing in the Zettabyte era: From silicon to the cloud," in *IEDM Tech. Dig.*, Dec. 2017, pp. 1.2.1–1.2.8.

[2] K. Narimani, S. Glass, P. Bernardy, N. von den Driesch, Q. T. Zhao, and S. Mantl, "Silicon tunnel FET with average subthreshold slope of 55 mV/dec at low drain currents," *Solid-State Electron.*, vol. 143, pp. 62–68, May 2018.

[3] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[4] W. Cao, D. Sarkar, Y. Khatami, J. Kang, and K. Banerjee, "Subthreshold-swing physics of tunnel field-effect transistors," *AIP Adv.*, vol. 4, no. 6, Jun. 2014, Art. no. 067141.

[5] W. Young Choi, B.-G. Park, J. Duk Lee, and T.-J. King Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.

[6] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 88–95, May 2015.

[7] W. G. Vandenberghe, A. S. Verhulst, B. Soree, W. Magnus, G. Groeseneken, Q. Smets, M. Heyns, and M. V. Fischetti, "Figure of merit for and identification of sub-60 mV/decade devices," *Appl. Phys. Lett.*, vol. 102, no. 1, pp. 013510-1–013510-4, 2013.

[8] R. Jhaveri, V. Nagavarapu, and J. C. S. Woo, "Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 80–86, Jan. 2011.

[9] A. S. Verhulst, W. G. Vandenberghe, K. Maex, S. De Gendt, M. M. Heyns, and G. Groeseneken, "Complementary silicon-based heterostructure tunnel-FETs with high tunnel rates," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1398–1401, Dec. 2008.

[10] W. Y. Choi and W. Lee, "Hetero-gate-dielectric tunneling field-effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2317–2319, Sep. 2010.

[11] Y. Morita, T. Mori, S. Migita, W. Mizubayashi, A. Tanabe, K. Fukuta, and T. Matsukawa, "Synthetic electric field tunnel FETs: Drain current multiplication demonstrated by wrapped gate electrode around ultrathin epitaxial channel," in *VLSI Technol. Dig.*, Jun. 2013, pp. T236–T237.

[12] A. S. Verhulst, D. Leonelli, R. Rooyackers, and G. Groeseneken, "Drain voltage dependent analytical model of tunnel field-effect transistors," *J. Appl. Phys.*, vol. 110, no. 2, Jul. 2011, Art. no. 024510.

[13] W. Hsu, J. Mantey, L. F. Register, and S. K. Banerjee, "Strained-Si/strained-Ge type-II staggered heterojunction gate-normal-tunneling field-effect transistor," *Appl. Phys. Lett.*, vol. 103, no. 9, pp. 093510-1–093510-4, Aug. 2013.

[14] W. Hsu, J. Mantey, L. F. Register, and S. K. Banerjee, "On the electrostatic control of Gate-Normal-Tunneling field-effect transistors," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2292–2299, Jul. 2015.

[15] L. Lattanzio, L. De Michielis, and A. M. Ionescu, "Electron-hole bilayer tunnel FET for steep subthreshold swing and improved ON current," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2011, pp. 259–262.

[16] P.-Y. Wang and B.-Y. Tsui, "Experimental demonstration of p-channel germanium epitaxial tunnel layer (ETL) tunnel FET with high tunneling current and high ON/OFF ratio," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1264–1266, Dec. 2015.

[17] S. Wan Kim, J. Hyun Kim, T.-J. King Liu, W. Young Choi, and B.-G. Park, "Demonstration of L-Shaped tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1774–1778, Apr. 2016.

[18] J. T. Teherani, T. Yu, D. A. Antoniadis, and J. L. Hoyt, "Electrostatic design of vertical tunneling field-effect transistors," in *Proc. 3rd Berkeley Symp. Energy Efficient Electron. Syst. (E3S)*, Oct. 2013, pp. 1–2.
[19] S. Glass, N. von den Driesch, S. Strangio, C. Schulte-Braucks, T. Rieger, K. Narimani, D. Buca, S. Mantl, and Q. T. Zhao, "Experimental examination of tunneling paths in SiGe/Si gate-normal tunneling field-effect transistors," *Appl. Phys. Lett.*, vol. 111, no. 26, pp. 263504-1–263504-5, Dec. 2017.
[20] P.-Y. Wang and B.-Y. Tsui, "Band engineering to improve average subthreshold swing by suppressing low electric field Band-to-Band tunneling with epitaxial tunnel layer tunnel FET structure," *IEEE Trans. Nanotechnol.*, vol. 15, no. 1, pp. 74–79, Jan. 2016.
[21] H. Asai, T. Mori, T. Matsukawa, J. Hattori, K. Endo, and K. Fukuda, "Steep switching in trimmed-gate tunnel FET," *AIP Adv.*, vol. 8, no. 9, pp. 095103-1–095103-6, Sep. 2018.
[22] *TCAD Sentaurus Device Manual*, Synopsys, Inc., Mountain View, CA, USA, 2017, pp. 436–440.
[23] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. De Meyer, "Direct and indirect Band-to-Band tunneling in germanium-based TFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 292–301, Feb. 2012.
[24] G. Betti Beneventi, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Optimization of a pocketed dual-metal-gate TFET by means of TCAD simulations accounting for quantization-induced bandgap widening," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 44–51, Jan. 2015.
[25] P. Wisniewski and B. Majkusiak, "Modeling the tunnel field-effect transistor based on different tunneling path approaches," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2626–2631, Jun. 2018.
[26] I. Huh, S. Park, M. Shin, and W. Y. Choi, "An accurate drain current model of monolayer transition-metal dichalcogenide tunnel FETs," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3502–3507, Aug. 2017.
[27] L. Liu, D. Mohata, and S. Datta, "Scaling length theory of double-gate interband tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902–908, Apr. 2012.
[28] S. W. Kim, W. Y. Choi, M.-C. Sun, H. W. Kim, and B.-G. Park, "Design guideline of Si-based L-shaped tunneling field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 51, pp. 06FE09-1–06FE09-4, Jun. 2012.

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