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Output Filter Design for Grid-Tied Cascaded Multi-Level Inverters Based on Novel Mathematical Expressions

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ABSTRACT Renewable energy resources, which are widely used in modern power systems, require power electronic-based converters to couple with the external grid. The main impact of utilizing power electronic converters on the grid power quality is harmonic generation produced by their switching process. Multi-level inverters are outstanding solutions to significantly reduce the voltage stress and harmonics. In this paper, novel mathematical expressions are derived to calculate the maximum ripple of the inverter output current, which are used to size the inverter-side inductor for an output filter. Moreover, new analytical and simplified formulas are proposed to calculate the damping losses, which lead to optimum selection of the damping resistor of the output filter. Ultimately, a mathematical expression for the grid-side inductor is attained considering compatibility level for harmonics within the range of 2-150 kHz to cover electrical and electronics equipment, which currently are the most important issues in the international standardization committee (IEC, TC77A). The efficiency of the proposed approach is finally validated by the experimental and simulation results.

INDEX TERMS Cascaded multi-level inverter, current ripple, damping resistor, LCL filter, optimum damping, passive damping, pulse width modulation, renewable generation, resonance.

I. INTRODUCTION

Energy has become the most important concern of human beings since the dawn of industrial revolution. The galloping rate at which technology is thriving has had a significant effect on the pattern of energy consumption in the world demonstrating a dramatic increase especially during the last decade. Air pollution and irreversible environmental damages are the most tangible consequences of this eternal tendency to energy consumption [1], [2]. Therefore, a need to move towards sustainable and renewable energy resources is inevitable [3], [4]. Fortunately, there has been a major breakthrough on how to effectively utilize clean sources of energy like solar and wind for industrial and residential applications in recent years. Since the output power of these renewable resources are not compatible with distribution grids considering magnitude and frequency, they need to be connected to the grid through power electronics interfaces. However, the output current and voltage of these power electronics interfaces, which operate based on switching devices and Pulse Width Modulation (PWM), are highly pulsating and polluted with undesired harmonics [5]–[12].

There are different types of integrated power electronic equipment in a network which create harmonics within a wide range of frequencies. These ranges include frequencies below 2 kHz for conventional rectifiers and high-power and medium-voltage 3-phase Active-Front-End (AEF) converters, between 2 and 9 kHz such as Power Factor Correction (PFC) circuits and high-power and low-voltage 3-phase AEF, and above 9 kHz such as low-power single-phase AEF with an LCL filter. International standards exist to cover the frequency ranges of 0-2 kHz and above 150 kHz (IEEE 519 and 1547, IEC 61000-3-2, IEC 61000-3-12, and CISPR). However, there are no standard levels for harmonics within the range of 2-150 kHz, which currently are the most important

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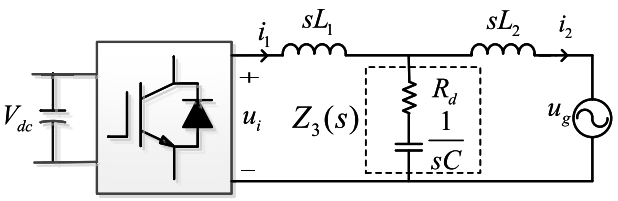

FIGURE 1. Equivalent circuit model of a grid-connected inverter with an LCL filter.

issues in the international standardization committee (IEC, TC77A) [8], [13], [14].

Typically, high-order filters are placed between inverters and distribution grids, which act as an effective barrier to impede harmonics flow to the main grid. The simplest structure for such filters is an inductor. In fact, a first-order simple L-filter was initially introduced to absorb the output current ripple of inverters. However, it suffers from poor harmonic attenuation capability. Additionally, to restrict the output harmonics of inverters in standard limits, a large amount of inductance is needed, which leads to considerable voltage drop across the filter [15], [16]. The poor performance of a standard L-filter can be improved by adding a capacitor and an extra inductor to the filter structure, which consequently leads to a higher order LCL filter [17]. In fact, the capacitor in the middle branch of LCL filters provides a path for current ripple to flow and helps to significantly cut down the size of the required inductor. Fig. 1 shows a general equivalent circuit of a grid-tied inverter with an output LCL filter.

Utilization of LCL filters for grid-connected inverters creates stability problems due to a resonance point located in the frequency response of the LCL filters. Therefore, a damping structure is required to ensure the stability of the control system and to mitigate the oscillatory behaviour of grid-connected inverter-based systems. To reduce the resonance peak of the filter transfer function, which causes the instability, both passive and active damping methods can be implemented [18]. However, utilizing the active damping methods, in most cases, yields to an increased number of sensors installed mostly to capture the capacitor voltage and current. The additional cost of these sensors, which are expensive components especially those with high bandwidth and accuracy, is a major limitation in employing active damping methods. Additionally, sensor-less active damping methods [19], [20] are quite complicated and need huge volume of mathematical and numerical calculations. Moreover, they are practically difficult and sometimes impossible to implement inside of a real-time microcontroller with limited cycle-time, especially for high switching frequency, which is being utilized in estate-of-the-art multi-level inverters. On the other hand, if the series passive damping resistor is placed in the filter topology, the damping becomes more robust and the stability of the system is guaranteed for a vast range of parameters variation [21]. A new trend in Power Electronics is to utilise fast and ultra-fast semiconductor switching devices in modern and high-power density converters based on high switching frequency. Moreover, it should be noted that the size of the passive damping resistor is proportional to the size of the inverter-side inductor, which its size is conversely proportional to the sampling frequency. Therefore, by utilizing multi-level inverters, which yields to an increased sampling frequency, the size of the damping resistor significantly diminishes and consequently the damping losses are reduced and can be limited within a desired range.

Various algorithms have been introduced in literature [22] to design an output filter for grid-tied inverters to enhance the power quality of the grid at the point of common coupling (PCC). Generally, these algorithms begin their flowchart by sizing the inverter-side inductor based on the maximum ripple of the inverter output current. In fact, the size of the inverter-side inductor is calculated based on its volume index, which is defined as $L * (I_{ave} + \Delta i_{ripple-max})^2$ [23]. Hence, using a precise mathematical expression for maximum ripple current calculation is an inevitable obligation in order to attain the accurate size of this inductor.

A comprehensive survey on previous studies demonstrates that almost all formulations to calculate the maximum ripple of an inverter output current are based on approximation and they are only valid for inverters with a simple L-filter and operating at a very high switching frequency [24], [25]. In other words, some important factors like the size of the capacitor in the middle branch of the filter, the type of the PWM used for switching, the number of phases, and the number of output voltage levels are totally neglected in the existing literature. In [22], a mathematical method is presented to calculate the maximum ripple of an inverter output current. However, this method is only valid for two-level inverters. Moreover, the numerical algorithm to obtain the required coefficient of the mentioned expression can be effectively enhanced, which will be considered in this paper.

Based on the fact that conventional two-level converters are less tolerable of high voltage stresses, multi-level converters are used for high power applications, which are able to significantly reduce the voltage stress by utilizing series connected switches [26], [27]. Cascaded configuration is one of the most renowned topologies for multi-level inverters [28], [29], which is the main focus of this paper. This type of multi-level inverters utilizes horizontal carrier waveform shifting method for performing the PWM. This topology and its general output voltage are depicted in Fig. 2. Since a more complicated PWM method is used for cascaded multi-level inverters (CMI) [30], compared to conventional two-level ones, the mathematical expressions to calculate the output current ripple become more complicated and difficult to achieve. Therefore, this paper will present a method to design a filter for a CMI, based on a novel expression for the maximum ripple of the inverter output current, which is calculated mathematically by considering all effective parameters.

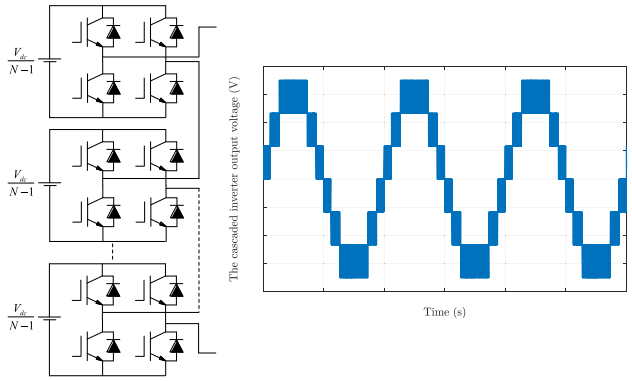

FIGURE 2. The topology of a cascaded inverter with its output voltage waveform.

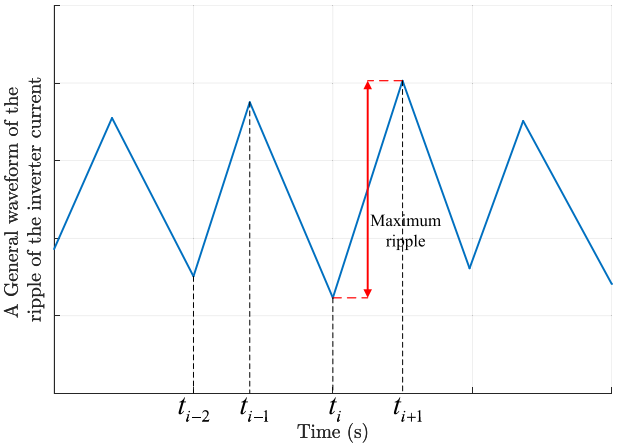

FIGURE 3. The ripple of the inverter-side current and its critical instants.

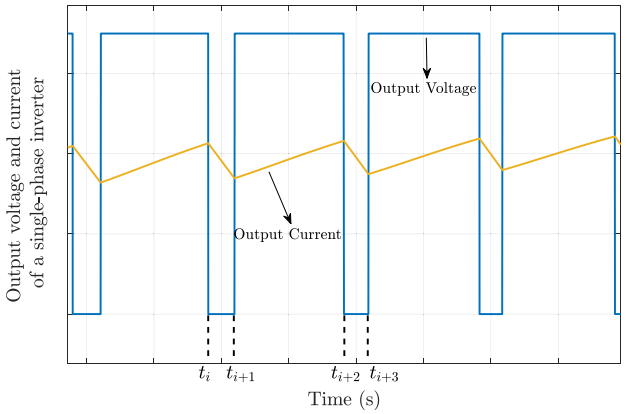

FIGURE 4. Output voltage and current of a single-phase inverter and the critical instants of the ripple current.

The main contributions of the paper can be summarized as follows:

- The mathematical definition of the ripple of a signal is explained and formulated. The equation is derived by simplifying a complex problem. Then, a comprehensive formulation is proposed to calculate the maximum ripple of inverters output current. To solve the associated problem, a very fast and simple numerical method is introduced in the next step to solve it.
- Novel compact formulas are proposed to obtain the maximum current ripple of CMIs. These mathematical expressions take the number of output voltage levels into account.
- A novel and significantly accurate formula is obtained to calculate the maximum active power losses across the damping resistor of LCL filters. This expression comprised of the fundamental and ripple losses of the damping resistor.
- The damping resistor of LCL filters is optimized by considering both stability of the system and limiting the damping active power losses.
- An analytical solution is obtained to calculate the size of the grid-side inductor of LCL filters to restrict the grid-side current harmonics within the standard intervals.
- Eventually, an algorithm is defined to design an LCL filter for CMIs with respect to all above considerations.

II. RIPPLE CALCULATION FOR CASCADED MULTI-LEVEL INVERTERS

The ripple of a signal is defined as the sum of all its harmonics except the fundamental one. Fig. 3 shows a general waveform of the current ripple flowing through the inverter inductor. Now, the maximum ripple of this signal is the maximum change of its value in one switching cycle, which can be mathematically expressed as follows:

$$\Delta i_{Rip-max} = \max_{\substack{k\in\mathbb{Z}^+ \\ kT_s\le t_i,\ t_{i+1}\le(k+1)T_s}} |i_{Rip}(t_{i+1}) - i_{rip}(t_i)| \qquad (1)$$

where $i_{Rip}(t)$ is the ripple of the inverter-side current, T_s is the switching period in seconds, and t_i and t_{i+1} are the times at which $i_{Rip(t)}$ is minimum and maximum at the k^{th} switching cycle.

The points at which the local minimum and maximum (known as critical instants in this paper) of the ripple current $i_{Rip}(t)$ occur must be mathematically obtained to evaluate (1). For a certain type of PWM algorithm, the inverter output current is the response of the filter and grid to the inverter output voltage. Since the output voltage of the inverter is a train of pulses, so, the critical instants of the current waveform are the times at which the inverter voltage alternates between two adjacent levels. This fact is demonstrated in Fig. 4. Furthermore, the instants at which the inverter output voltage pulsates are the intersection points between the reference and carrier signals of the PWM, which is shown in Fig. 5.

PWM methods with horizontally shifted carrier signals are utilized in cascaded N-level inverters where N is the number of non-negative voltage levels for v_{ab} and $N-1$ inverters are cascaded. This type of PWM for asymmetrical regular sampled reference signal (ARSRS) is depicted in Fig. 5. As mentioned above, the critical instants are located at the intersection points between the carrier and reference signals of the PWM algorithm. It should be noted that there are two

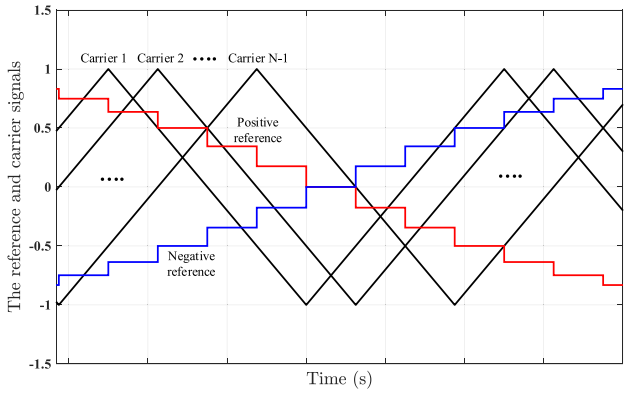

FIGURE 5. The reference and carrier signals in the horizontally shifted PWM method and regular-sampled reference signal.

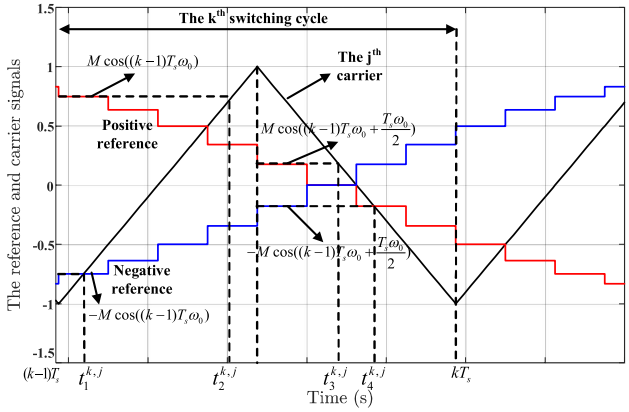

FIGURE 6. Intersection of the j^{th} carrier signal and the positive and negative reference signals in one switching cycle.

intersection points between the positive reference signal (leg a) and each carrier signal, and another two points between the negative reference signal (leg b) and each carrier signal. Additionally, in a real microcontroller in which the regular-sampled PWMs are implemented, the sampling of each carrier signal occurs just at the minimum and maximum of the corresponding triangular carrier signal. Fig. 6 demonstrates a detailed sketch of this fact for the j^{th} carrier signal in one switching cycle. In this paper, these critical instants are exactly determined, which is one of the main contributions of this paper. In fact, the analytical expressions for evaluating the critical instants in the case of asymmetrical regular sampled PWM and in the k^{th} switching cycle can be obtained as follows:

$$t_1^{k,j} = a^{k,j} + (\frac{T_s}{4})(1 - Mcos(\omega_0 a^{k,j})) \quad (2)$$

$$t_2^{k,j} = a^{k,j} + (\frac{T_s}{4})(1 + Mcos(\omega_0 a^{k,j})) \quad (3)$$

$$t_3^{k,j} = a^{k+1,j} - (\frac{T_s}{4})(1 + Mcos(\omega_0 b^{k,j})) \quad (4)$$

$$t_4^{k,j} = a^{k+1,j} - (\frac{T_s}{4})(1 - Mcos(\omega_0 b^{k,j})) \quad (5)$$

where T_s is the period of the carrier signal in seconds, M is the modulation factor, ω_0 is the frequency of the reference signal in radian per second, $t_2^{k,j}$ and $t_3^{k,j}$ are the time of intersections between the positive reference and the j^{th} carrier signals in the k^{th} switching cycle, and $t_1^{k,j}$ and $t_4^{k,j}$ are the corresponding instants for the negative reference signal. Additionally,

$$a^{k,j} = (k-1)T_s + (\frac{(j-1)T_s}{2(N-1)})$$
$$b^{k,j} = a^{k,j} + \frac{T_s}{2} \quad (6)$$

By using the same approach, the critical instants can be determined for the horizontally-shifted and naturally-sampled PWM method. However, the numerical methods must be employed to solve the corresponding equations.

Now, the inverter output current, in the frequency domain, can be simply obtained by dividing the inverter output voltage by the input impedance of the filter. The input impedance of the filter can be obtained as follows:

$$Z_i(\omega) = j\omega L_1 + (Z_3(\omega)||j\omega L_2) \quad (7)$$

where $j\omega L_1$, $j\omega L_2$, and $Z_3(\omega)$ are the impedance of the inverter-side inductor, grid-side inductor and middle branch of the filter, respectively. Equation (7) can be rewritten as follows:

$$Z_i(\omega) = j\omega L_1(1 + \frac{Z_3(\omega)||j\omega L_2}{j\omega L_1}) = j\omega L_1(1 + Z_3'(\omega)) \quad (8)$$

The Fourier series of the normalized output voltage of the inverter can be written as follows:

$$\frac{v_{ab}(t)}{V_{dc}} = M\cos(\omega_0 t) + \sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty} V_{mn}\cos(m\omega_s t + n\omega_0 t) \quad (9)$$

where V_{dc} is the input DC voltage, ω_s is the frequency of the carrier signals in radian per second, and V_{mn} is determined according to the modulation type by using the Bessel functions theories [30], [31].

Therefore, by using Ohm laws as well as superposition, the following equation for the inverter output ripple current can be derived from (8) and (9):

$$i_{Rip}(t) = \sum_{\substack{m=0\\ m=0\leftrightarrow n\neq 1}}^{\infty}\sum_{n=-\infty}^{\infty} \frac{V_{dc}V_{mn}\cos(q_{mn}\omega_s t - \angle Z_i(q_{mn}\omega_s))}{|Z_i(q_{mn}\omega_s)|}$$
$$= \sum_{\substack{m=0\\ m=0\leftrightarrow n\neq 1}}^{\infty}\sum_{n=-\infty}^{\infty} \frac{V_{dc}V_{mn}\cos(q_{mn}\omega_s t - \angle Z_i(q_{mn}\omega_s))}{q_{mn}\omega_s L_1|(1 + Z_3'(q_{mn}\omega_s))|} \quad (10)$$

where $q_{mn} = m + n\omega_0/\omega_s$. Equation (10) can be briefly written as follows:

$$i_{Rip}(t) = \frac{V_{dc}}{f_s L_1}\Psi(M, t, f_s, Z_3') \quad (11)$$

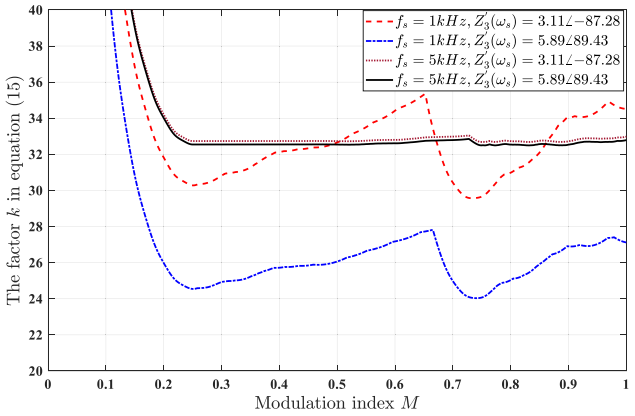

FIGURE 7. Variation of factor k in (15) as a function of the switching frequency and impedance $Z_3'(\omega_s)$ given by (8).

where

$$\Psi(M, t, f_s, Z_3') = \sum_{\substack{m=0 \\ m=0 \leftrightarrow n \neq 1}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{V_{mn} \cos(q_{mn}\omega_s t - \angle Z_i(q_{mn}\omega_s))}{2\pi q_{mn} |(1 + Z_3'(q_{mn}\omega_s))|} \tag{12}$$

Eventually, the maximum ripple is calculated according to the definition in (1) as follows:

$$\Delta i_{Rip-max} = \max_{t_i \in \mathbf{C}} |i_{Rip}(t_{i+1}) - i_{Rip}(t_i)| \tag{13}$$

$$\Delta i_{Rip-max} = \frac{V_{dc}}{f_s L_1} \max_{\substack{t_i \in C \\ 0<M<1}} |\Psi(M, t_{i+1}, Z_3') - \Psi(M, t_i, Z_3')| \tag{14}$$

where $\mathbf{C}$ is the set of successive critical instants determined by (2)-(6).

Since the number of critical instants is finite, evaluation of (14) takes a few seconds, even for extremely large switching frequencies (instead of solving the optimization problem on a continuous interval of infinitely many points). Generally, (14) can be written as follows:

$$\Delta i_{Rip-max} = \frac{V_{dc}}{k f_s L_1} \tag{15}$$

where k is a factor that depends on the modulation type and index, angular carrier signal frequency, filter middle branch impedance and the number of voltage levels. As an example, k factor variation with respect to the modulation index has been shown in Fig. 7 when the number of levels is $N = 3$, and the factor k is plotted for different values of switching frequency and impedance $Z_3'(\omega_s)$. As can be seen from this figure, the curve of factor k converges when the switching frequency increases. Examining the numerical values of the factor k for different values of N reveals that this factor is almost independent of the switching frequency and yields the following novel and simplified expression in this paper:

$$\Delta i_{Rip-max} = \frac{V_{dc}}{8(N-1)^2 f_s L_1} \tag{16}$$

It should be noted that the more accurate value of the factor k should be calculated by using (14), and (16) is useful to make an initial guess of the maximum ripple.

Lastly, after all above mathematical calculations, the inverter-side inductor can be designed by using (14) and based on the desired maximum current ripple. In order to limit the ripple and core losses of the inverter-side inductor and to avoid saturation problems, it is recommended restricting the maximum ripple of the inverter-side current to 20-30 % of the inverter rated current. In this paper, the maximum ripple of L_1 is considered to be 30% of the rated current.

III. DESIGN OF THE MIDDLE BRANCH

The middle branch of an LCL filter is comprised of a capacitor and a resistor. The role of the capacitor is to provide a path for the ripple current of L_1 to flow through. Besides, the resistor in series with this capacitor damps the resonant peak of the filter transfer function to achieve a stable control system. The larger the capacitor is, the lower the amount of the ripple is. However, the power factor of the inverter output current is an important constraint, which limits the size of the capacitor. Based on this constraint, it is suggested that the reactive power of this capacitor should not exceed 5% of the inverter rated power. This constraint can be mathematically expressed as follows:

$$Q_c = \omega_0 C |\frac{V_g + j\omega_0 L_2 I_g}{1 - jR_d C\omega_0}|^2 < 0.05 P_{rated} \tag{17}$$

where Q_c is the generated reactive power of the capacitor in VAR, V_g and I_g are the grid RMS voltage and current in Volts and Amps, respectively, and P_{rated} is the inverter rated power in Watts.

The series resistor in the middle branch of the filter must damp the resonance created by the inductors and capacitor of the filter. It should be sized in a way that minimizes the resonant peak of the filter transfer function. This transfer function in the frequency domain is as follows:

$$G(j\omega) = \frac{1}{L_T} \times \frac{1 + jR_d C\omega}{-R_d C\omega^2 + j(\omega - LC\omega^3)} \tag{18}$$

where $L_T = L_1 + L_2$ and $L = L_1 L_2/(L_T)$. Fig. 8 demonstrates the Bode diagram of the filter for different values of the damping resistor. As can be seen from this figure, the larger the resistor is, the lower the peak of the magnitude is.

However, the active power losses of the resistor limit its size. The active power across the damping resistor is comprised of the fundamental and ripple losses, which can be written as follows:

$$P_{damp} = R_d(\omega_0 C)^2 \times \frac{V_g^2 + (\omega_0 L_2 I_g)^2}{1 + (R_d \omega_0 C)^2} + \sum_{\substack{m=0 \\ m=0 \leftrightarrow n \neq 1}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{R_d (q_{mn}^2 \omega_s^2 L_2 C)^2}{(R_d q_{mn} \omega_s C)^2 + (q_{mn}^2 \omega_s^2 L_2 C - 1)^2} \times \frac{I_{mn}^2}{2} \tag{19}$$

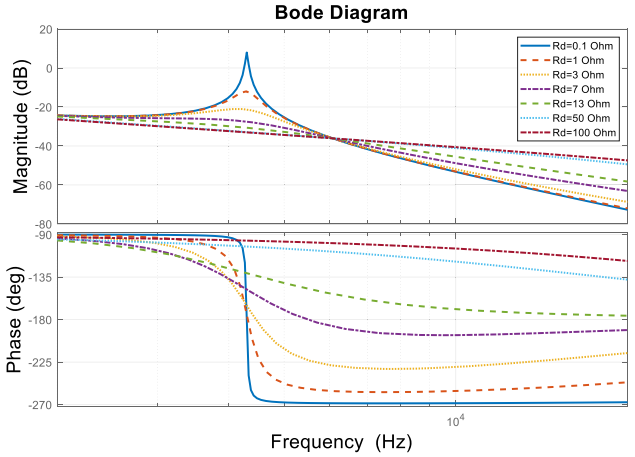

FIGURE 8. The Bode diagram of the LCL filter transfer function for different values of the damping resistor, $L_1 = 0.86$ mH, $L_2 = 0.8$ mH, $C = 3.3$ μF.

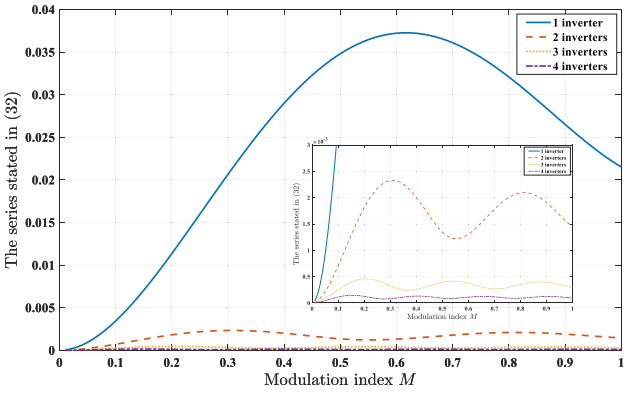

FIGURE 9. Variation the series stated in (21) as a function of the modulation index M for different numbers of cascaded inverters.

where

$$I_{mn} = \frac{V_{mn} \times V_{dc}}{|Z_i(jq_{mn}\omega_s)|} \tag{20}$$

The first term of (19) is the fundamental active power losses and the second one is the ripple losses. Apparently, the ripple active power expressed in (19) is very complicated and even impractical to calculate. To have a fairly exact estimation of this term, it can be assumed that $Z_i(j\omega) \approx j\omega L_1$ at high frequencies (In the order of the switching frequency), $f_s \gg f_0$, and $j\omega L_2 \gg 1/(j\omega C)$ again at high frequencies. The first assumption is almost accurate since the impedance of inductors are much higher than that of capacitors when the frequency increases. The second assumption is also reasonable due to the significant advancement in power electronics switches to work at quite high switching frequencies. Eventually, the last assumption is correct since the output current harmonics of the filter injected to the grid are almost zero at high frequencies, which means that the impedance of L_2 is much higher than the impedance of the capacitor at high frequencies. Therefore, the ripple active power losses of the damping resistor can be rewritten as follows:

$$P_{damp}^{ripple} = R_d(\frac{V_{dc}}{\omega_s L_1})^2 \sum_{\substack{m=0 \\ m=0 \leftrightarrow n \neq 1}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{V_{mn}^2}{q_{mn}^2} \tag{21}$$

The series appeared in (21) only depends on the modulation index M and the number of levels in the output voltage of the inverter N. Using numerical calculations, this paper proposes a new mathematical expression for the the maximum ripple power losses across the damping resistor, for horizontally shifted PWMs, as follows:

$$P_{damp-max}^{ripple} = R_d(\frac{0.193V_{dc}}{\omega_s L_1 (N-1)^2})^2 \tag{22}$$

Equation (22) is a novel expression which is extremely useful and accurate to calculate the maximum damping losses and design the damping resistor based on a constraint to limit the power losses of the filter. Fig. 9 shows the variation of the series stated in (21) as a function of the modulation index M for different numbers of cascaded inverters. Additionally, since the ripple current flows through the parasitic resistor of the inductor L_1, (22) can be modified as follows to consider the effect of this resistance on the total power losses of the filter:

$$P_{filter}^{ripple-max} = (R_d + r_1)(\frac{0.193V_{dc}}{\omega_s L_1 (N-1)^2})^2 \tag{23}$$

where r_1 is the equivalent resistance of the inverter-side inductor in ohms.

Considering the stability of the overall inverter system, it has been recommended [32] selecting the damping resistor for LCL filters by using the following equation:

$$R_d = \frac{1}{3}\sqrt{\frac{L_1 L_2}{(L_1 + L_2)C}} \tag{24}$$

However, it should be noted that if the damping losses exceed a specific predefined design value (for example 1% of the rated power in this paper), the resistance should be selected based on the criteria expressed in (22).

IV. DESIGN OF THE GRID-SIDE INDUCTOR

The grid-side inductor must be designed such that the values of injected current harmonics to the main grid fall into a predefined standard interval. However, these standards, e.g., IEEE 1547, IEEE 519 or IEC 61000-3-2, only consider harmonics up to 2-2.5 kHz. Since the switching frequency of PWM methods is steadily increasing by advancement in semiconductor technologies, the frequency of the current harmonics generated by inverters are being shifted to extremely higher ranges above the existing standards. In addition, another challenging issue with some current codes, e.g., IEEE 519, is that they consider harmonics level relative to demand current of the feeder where equipment is going to be installed. Therefore, design of equipment such as inverters cannot be unique. Fortunately, researchers are working on new codes for harmonics in the ranges 2-9 kHz and 9-150 kHz

which are based on equipment rated values [8], [13], [14]. In this paper, desired individual harmonic distortion level is considered as 0.3% of the inverter rated current for frequencies greater than 2.5 kHz (the fundamental frequency is 50 Hz), and for harmonics below 2.5 KHz, the latest IEEE 1547 standard is considered.

According to the above explanation, mathematical expressions to design the grid-side inductor are as follows:

$$|I_2(j\omega)| < x \times I_{rated} \quad \omega = m\omega_s + n\omega_0 \tag{25}$$

$$|I_2(j\omega)| = |G(j\omega) \times V_i(j\omega)| < x \times I_{rated} \tag{26}$$

where I_2 is the grid current, $G(j\omega)$ is the filter transfer function, V_i is the inverter output voltage, x is the desired percentage of the output current harmonics, and I_{rated} is the inverter rated current. Equation (26) is analytically solved in this paper as follows:

$$L_2^{min} = \max_{m,n} \frac{-B + \sqrt{\Delta}}{A} \tag{27}$$

where:

$$\begin{aligned} A &= R_d^2 C^2 \omega^4 + (\omega - L_1 C \omega^3)^2 \\ B &= R_d^2 C^2 \omega^4 L_1 + \omega L_1 (\omega - L_1 C \omega^3) \\ D &= R_d^2 C^2 \omega^4 L_1^2 + \omega^2 L_1^2 - \left(\frac{V_{m,n}}{x I_{rated}}\right)^2 (1 + R_d^2 C^2 \omega^2) \\ \Delta &= B^2 - AD \end{aligned} \tag{28}$$

Additionally, it should be noted that the most significant harmonics are located at the sampling frequency and around it. Hence, it is needed to solve (27) at the sampling frequency and at most three sidebands to ensure that it holds for all other harmonics, and select the maximum calculated value for L_2.

V. FILTER DESIGN ALGORITHM

The following steps describe the filter design algorithm:

1) The initial value of the inverter-side inductor is calculated by using (16) based on the maximum specified amount of the ripple (30% in this paper).

2) The total capacitance in the middle branch of the filter is initialized as follows:

$$C = \frac{0.05 P_{rated}}{\omega_0 V_g^2} \tag{29}$$

3) The initial values of L_2 and R_d can be simultaneously evaluated by solving the set of equations obtained from (24) and (27). This evaluation can be carried out by using iterative numerical methods in few steps.

4) Iteration starts at this step to obtain accurate values of the filter parameters. For this purpose, the filter capacitance is updated by using (17). Then, the value of impedance $Z_3(j\omega)$ is recalculated by using the updated capacitance of the filter. In the next step, the updated value of the inverter-side inductor is evaluated by using (14). Afterward, the size of the damping resistor and grid-side inductor is recalculated based on the new values for L_1 and C. This iterative process is carried on until the error becomes smaller than a specified value (1% in this paper).

5) The next step is to verify the required condition for the resonant frequency of the filter. It has been suggested in [24] that the resonant frequency lies between $10f_0$ and $f_{samp}/2$, where f_0 is the fundamental frequency and f_{samp} is the sampling frequency of the inverter control system. The resonant frequency of LCL filters without a passive damping resistor is equal to $\frac{1}{2\pi}\sqrt{\frac{L_1+L_2}{L_1 L_2 C}}$. Although introducing a passive damping resistor significantly reduces the value of the filter transfer function at the resonant point, the resonant frequency is roughly fixed and constant. Thus, the resonant frequency of LCL filters with a passive damping resistor of the size obtained by (24) is considered as follows:

$$f_{resLCL} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{30}$$

If the criterion for the resonant frequency is violated, the value of L_2 can be increased marginally to achieve a suitable value for the resonant frequency. It should be noticed that the damping resistor also needs to be recalculated after changing the value of L_2.

6) The last step is to calculate the damping losses. If the calculated damping losses by using (22) are greater than 1% of the rated power, the damping resistor must be restricted by using (22). Afterwards, the grid-side inductor must be updated by using (27).

The flowchart depicted in Fig. 10 summarizes the proposed design procedure.

VI. DESIGN EXAMPLE

In this section, the proposed method is applied to design an LCL filter for an inverter with this specification: a 4-level cascaded inverter (4 non-negative voltage levels) and a PWM with horizontally shifted carrier signals, rated power is 1 kW, frequency of the carrier signal is 5 kHz, asymmetrical regular-sampled PWM is utilized, the RMS voltage of the grid is 220 V, the DC link voltage is 350 V, the maximum ripple of the inverter-side current is 30% of the rated current, and the grid-side current is controlled by using a Proportional-Resonant (PR) controller. The design procedure is described step-by-step as follows:

1) Three full-bridge inverter unit must be cascaded to have a 4-level cascaded inverter. The initial value of the inverter-side inductor is calculated by using (16):

$$\begin{aligned} L_1 &= \frac{V_{dc}}{8(N-1)^2 f_s (0.3 \times I_{rated})} \\ &= \frac{350}{8 \times 9 \times 5000 \times 0.3 \times 6.43} = 505\ \mu\text{H} \end{aligned} \tag{31}$$

2) The total initial capacitance is evaluated by using (29) as below:

$$C = \frac{0.05 \times 1000}{2\pi \times 50 \times 220^2} = 3.3\mu\text{F} \tag{32}$$

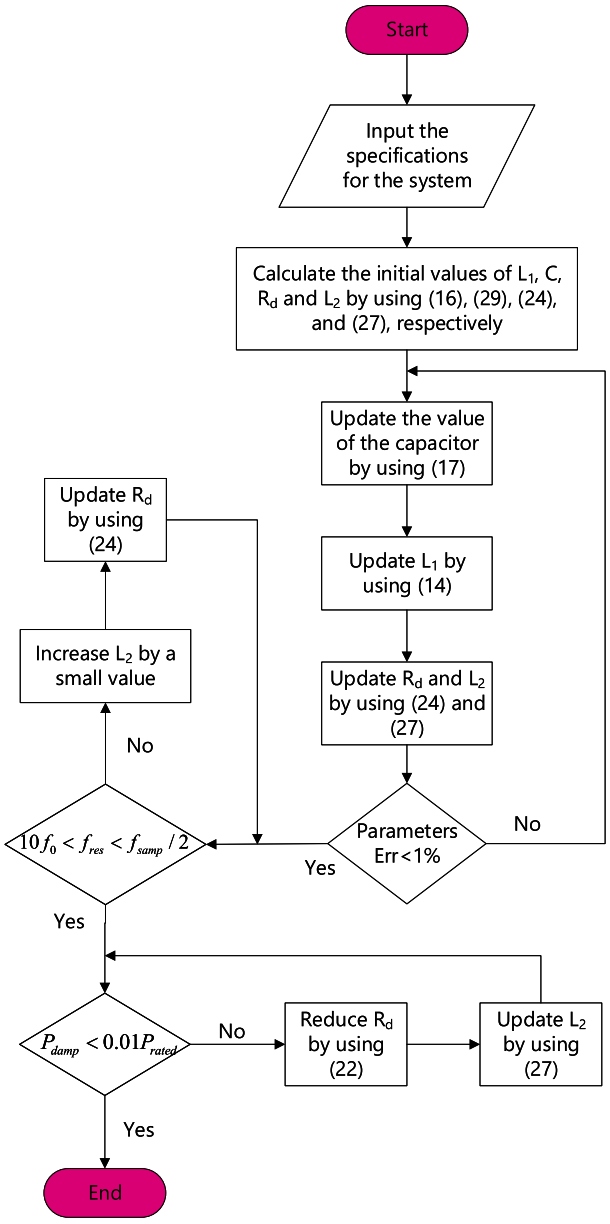

FIGURE 10. The flowchart of the proposed method for the filter design of CMIs.

3) In order to calculate R_d and L_2, the set of equations (24) and (27) must be solved. The results are as follows:

$$R_d = 2.77\ \Omega, \quad L_2 = 418\ \mu\text{H} \tag{33}$$

4) In this step, firstly, the size of the capacitor is recalculated by using (17). This calculation reveals that there is no significant change in the filter capacitance compared to the initial value. Therefore, the size of the capacitor can be considered fixed during the iteration. Then, the value of parameter k in (15) is updated by using (14) as well as the values obtained in the previous steps. The updated value of k is 72.67. Thus, L_1 is recalculated as $L_1 = 499\ \mu$H. Consequently, $R_d = 2.78\ \Omega$ and $L_2 = 422\ \mu$H are updated. The specified amount of error (1%) is attained at this step. Hence, the algorithm stops at this point. The final values are $L_1 = 499\ \mu$H, $L_2 = 422\ \mu$H, $R_d = 2.78\ \Omega$

5) The resonance frequency of the filter transfer function is then evaluated as $f_{resLCCL} = 5467$ Hz. As it can be seen, it is located in the recommended interval $[10f_0,\ \frac{f_{samp}}{2}] = [500\text{ Hz},\ 15\text{ kHz}]$.

6) The last step is to verify the damping losses constraint. This constraint is evaluated by using (19) and (22) as $P_{damp}^{fund} = 0.1436$ W, $P_{damp}^{ripple-max} = 0.6363$ W, which result in $P_{damp} = 0.7799$ W. Apparently, the total damping losses are much less than 1% of the rated power as desired.

The designed values are tabulated in Table. 1. Besides, in order to compare the results with a conventional two-level inverter, an LCL filter is designed by using the proposed method (considering $N = 2$ in the proposed method) and the method in [33]. The results are also tabulated in Table. 1. As can be seen from this table, increasing the number of levels significantly reduces the size of the filter and damping losses. Moreover, the proposed method yields to more optimized parameters for the filter even in the case $N = 2$.

TABLE 1. Designed parameters for the output filter design.

Configuration	4-Level cascaded	two-level proposed method	two-level method in [33]
L_1 mH	0.499	4.54	9.1
L_2 mH	0.422	3.82	9.1
$C\ \mu$F	3.29	3.29	3.29
$R_d\ \Omega$	2.78	8.36	37.14
f_{res} kHz	5.467	1.860	1.146
P_{damp}^{fund} W	0.1436	0.4329	1.9282
$P_{damp-max}^{ripple}$ W	0.6363	1.8804	2.0739
P_{damp} W	0.7799	2.3133	4.0029

VII. SIMULATION

In order to examine the proposed method for the filter design of CMIs, a simulation study is carried out for the filter designed in the previous section. A proportional-resonant (PR) controller with harmonics compensation is employed for the control purpose. The transfer function of the controller in the s-domain is given in (34). In a practical case, this continuous transfer function is discretized by using the "Tustin" method. The transformation between the continuous and discrete domains in this method is defined as $s = \frac{2}{T}\frac{z-1}{z+1}$, where $T = 1/f_{samp}$ is the sampling period in seconds.

$$G_c(s) = K_p + K_r \sum_{n=1,3,5,7,9} \frac{2\zeta n\omega_0 s}{s^2 + 2\zeta n\omega_0 s + (n\omega_0)^2} \tag{34}$$

where ζ is the damping parameter of the PR controller, which is considered as $\zeta = 0.0001$ in this design. Furthermore, parameters K_P and K_r are determined such that the gain and phase margin of the control system are $G.M > 10$ dB and $P.M > 40$ degrees. These criteria and considering a stiff grid condition, i.e $L_g = 0$ mH, yield to $K_p = 0.00996$ and $K_r = 19.9278$. Fig. 11 shows the Bode diagram of the open-loop transfer function of the overall system (filter, controller, PWM, and the processing delay) for the inverter under study.

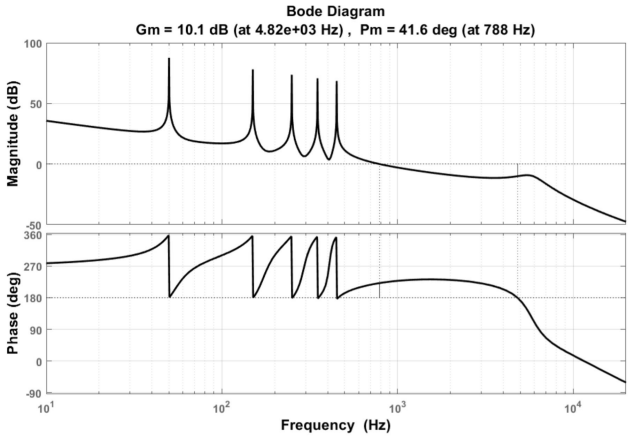

FIGURE 11. The Bode diagram of the open-loop transfer function of the overall system (filter, controller, PWM, and the processing delay) for the cascaded inverter under study.

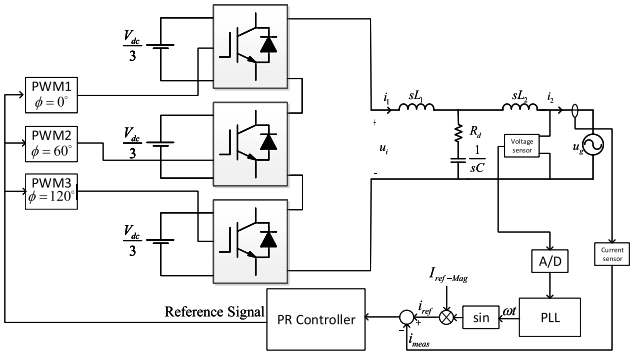

FIGURE 12. The inverter control system diagram.

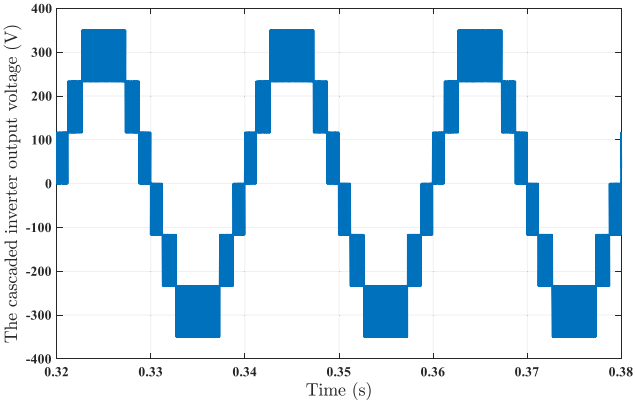

FIGURE 13. The output voltage of the inverter from the simulation study.

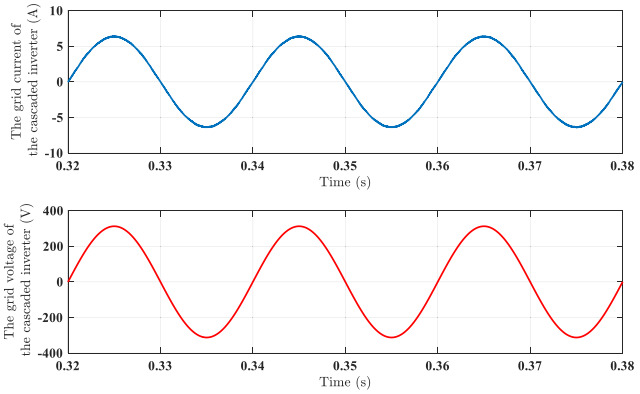

FIGURE 14. The grid current and voltage from the simulation study.

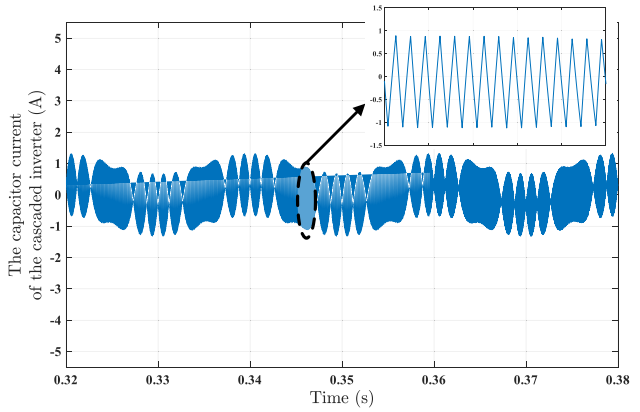

FIGURE 15. The capacitor current from the simulation study.

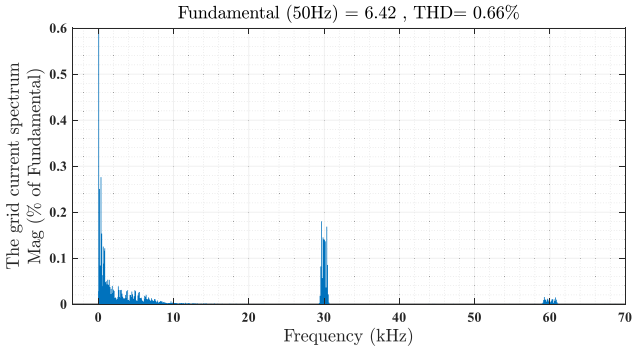

FIGURE 16. Harmonic spectrum of the grid current from the simulation study.

The control system block diagram is depicted in Fig. 12. As can be seen from this figure, the grid voltage is measured by using a voltage sensor and gets through the A/D conversion of the microcontroller to be digitalized. The digitalized voltage signal is fed to the Phase Lock Loop (PLL) to generate the synchronization signal for the reference current. The grid current is measured by using a current sensor and after digitalizing by using another A/D port of the microcontroller is subtracted from the generated reference current to create the error signal. Then, the error signal enters the designed PR controller. This controller generates the reference signal for the PWM blocks. The carrier signals of these PWM blocks have 60 degrees phase shift between. Eventually, the PWM blocks create the pulses for the switches of each cascaded inverter.

The waveform of the inverter output voltage, grid-side current and voltage, and the capacitor current (approximately equals the ripple current) obtained from the simulation are plotted in Fig. 13 to Fig. 15, respectively. Besides, the

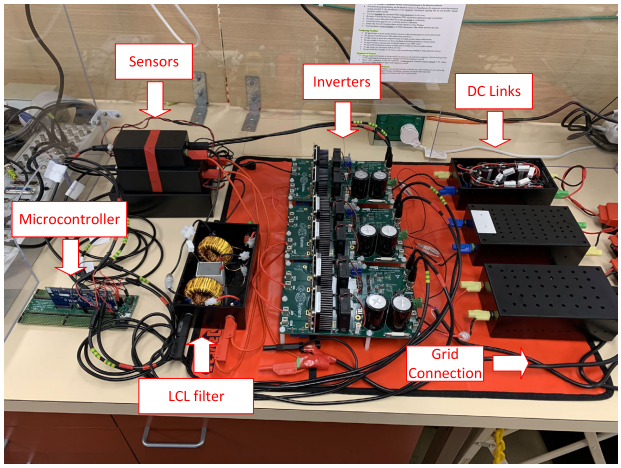

FIGURE 17. The practical circuit for the 4-level cascaded inverter with the designed LCL filter.

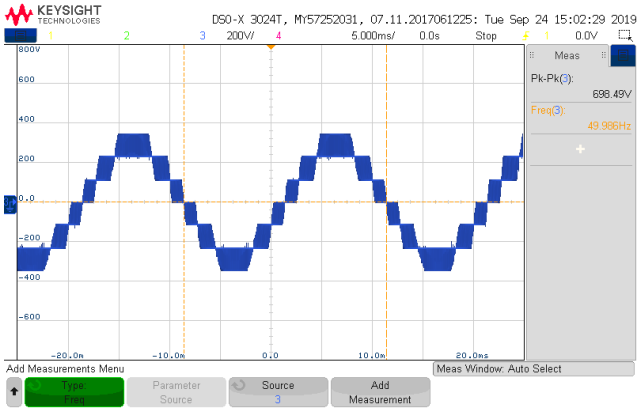

FIGURE 18. The output voltage of the inverter obtained from the experiment.

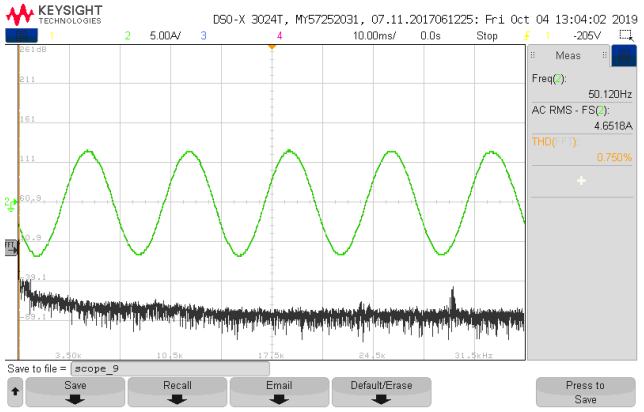

FIGURE 19. The grid current and its harmonic spectrum obtained from the experiment.

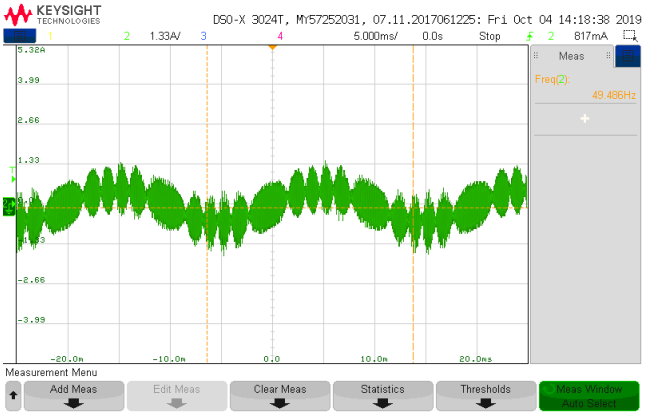

FIGURE 20. The capacitor current obtained from the experiment.

harmonics spectrum of the grid-side current is shown in Fig. 16. As it can be seen from Fig. 15, the ripple of the inverter-side current is about 1.9 A or 29% of the rated current (6.42 A), which is in accordance with the design specification. Additionally, Fig. 16 reveals that the individual harmonics of the grid-side current are less than 0.3% of the inverter rated current based on the design assumptions, and the total harmonic distortion is $THD = 0.66\%$.

VIII. EXPERIMENTAL RESULTS

In this section, an experimental setup is built based on the design parameters determined in section VI. This circuit comprises of three single-phase inverters in series, an LCL filter with the designed parameters, a DC and an AC source, a microcontroller, and current and voltage sensors as depicted in Fig. 17. The utilized switches for the inverters are based on GaN wide band gap technology. The discretized controller is implemented on a dual-core TI Delfino F28379D microcontroller. A robust and accurate Phase Lock Loop (PLL) based on average calculation is programmed and downloaded onto the cyclic routine of the microcontroller with a fixed frequency of 10 kHz. Furthermore, the controller is uploaded into an interrupt service routine, which is controlled by a PWM module of the frequency 30 kHz (the overall sampling frequency), and another three PWM modules with phase shift of $pi/3$ are employed to create the switching pulses for the cascaded inverters.

The capacitor current, which is approximately equivalent to the ripple current, is shown in Fig. 20. Furthermore, Fig. 21 demonstrates a magnified capture of the capacitor current, in a few switching cycles, and as can be seen from this figure, the peak to peak ripple is 1.99 A, which is about 30% of the rated current as desired.

The inverter output voltage is shown in Fig. 18. As can be seen, it has four non-negative levels (seven levels totally). Besides, the waveform of the grid current and its FFT waveform, captured from the oscilloscope, are shown in Fig. 19. This figure shows the appropriate filtering of the designed LCL filter. Moreover, it can be seen that the most significant switching harmonic located at 30 kHz is less than the desired value (0.3% of the rated current which is about -35 dB), and the total harmonic distortion of the grid current is reasonably

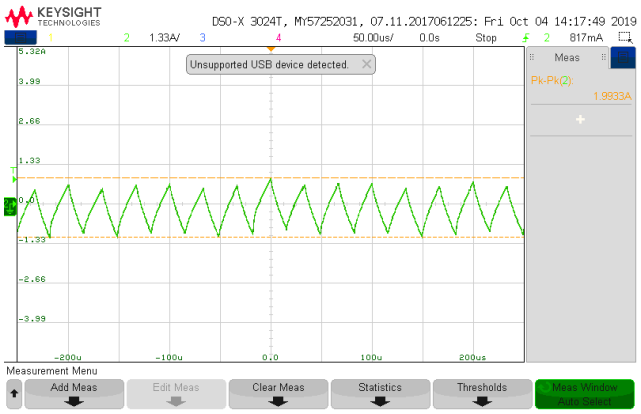

FIGURE 21. The magnified waveform of the capacitor current obtained from the experiment.

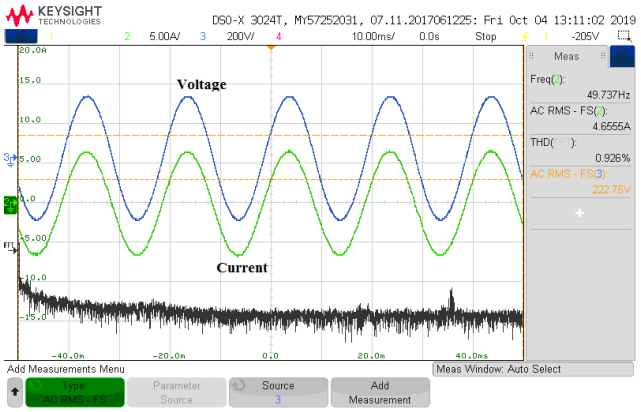

FIGURE 22. The grid and voltage current obtained from the experiment.

very small ($THD = 0.75$) and so close to the value obtained by the simulation ($THD_{simulation} = 0.66$).

Lastly, Fig. 22 shows the grid current and voltage together proving the excellent synchronization of the employed PLL. Moreover, the RMS value of the grid current is 4.65 A, which is so close to the rated current of 4.55 A (RMS). Therefore, the current tracking of the implemented controller is performed with high accuracy.

IX. CONCLUSION

Based on the fact that the mathematical expressions for the output voltage and current of CMIs are completely different from those of conventional two-level ones, there is a need to propose a specific filter design method for CMIs with horizontally shifted PWMs. In this paper, a novel comprehensive design algorithm to determine the optimum values of an LCL filter for a CMI has been introduced. One of the major contributions of this research is to present a precise mathematical equation to calculate the maximum value of the inverter output current ripple. This novelty, which is attained by identification of the intersection instants of the reference and carrier signals in each switching cycle, ultimately leads to estimating the optimum value of the inverter-side inductor. In the next steps, other filter parameters are assigned based on accurate mathematical formulations. In this regards, introducing a new formula to calculate the damping losses of LCL filters of CMIs is another significant contributions of this paper. Finally, a new comprehensive algorithm to find the optimum values of the output filter parameters has been presented. The efficiency of the design algorithm as well as the accuracy of the mathematical expressions in this study have been verified by various simulations and experiments.

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