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A -193.6 dBc/Hz FoM$_T$ 28.6-to-36.2 GHz Dual-Core CMOS VCO for 5G Applications

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ABSTRACT By combining the transformer feedback and VCO multi-core techniques, this paper presents a 0.5 V low voltage 28.6-to-36.2 GHz dual-core VCO for 5G applications. Based on the transformer feedback topology, with the power-ground interconnect inductor and embedded decouple capacitor, the second harmonic real impedance is achieved at the VCO cross-couple pair source terminal. Accordingly, the common-mode current path is reduced and the signal symmetry improved, suppressing the flicker noise up conversion. With a 4 bit switch capacitors and varactors, the proposed VCO achieves a 28.6-to-36.2 GHz (23.5 %) tuning range, and its flicker noise corner is from 250 to 980 kHz. Fabricated in a 65nm CMOS process, the VCO consumes 4.6mW from a 0.5 V supply voltage with a core area of about 0.24×0.5 mm^2. At 31 GHz, the proposed VCO achieves a phase noise of -103 dBc/Hz@1MHz offset, resulting in a figure-of-merit (FoM) of -186.2 dBc/Hz and tuning range figure-of-merit (FoM$_T$) of -193.6 dBc/Hz, respectively.

INDEX TERMS Dual core, low supply, transformer feedback, VCO.

I. INTRODUCTION

In WRC-19, 5G millimeter wave (mmWave) spectra have been selected, the mmWave RF front-end comes to the turning point from concept to implementation [1]. With wide bandwidth characteristics, the mmWave band, such as the 28 and 39 GHz, can be used to realize Gbps data rate with high-order modulation schemes [2], [3]. From the implementation point of view, this poses very challenging requirements for the VCO phase noise and tuning range. Moreover, for the portable wireless communication application, it is preferred to realize VCO with low voltage and low power consumption.

In response to above requirements, a transformer feedback VCO topology is proposed [3]–[5], improving the start-up gain and achieving low supply operation. However, to realize more than 20% tuning range, the ratio of the switch capacitor C_{max} to C_{min} is large. As a result, the tank quality-factor (Q-factor) and the tank impedance is limited, worsening the VCO phase noise. As an alternative solution, with the VCO multi-core techniques [6], the VCO phase noise can be improved by 10 logN dB, where N is the VCO core number. In addition, by doing so the VCO tuning range is increased due to less ratio of the buffer parasitic capacitor over the LC tank capacitor. Moreover the output signals of each VCO core are coupled with each other, improving the signal symmetry [6]. However, the VCO power consumption is enlarged as the VCO core number increases.

To address the low voltage, wide tuning range and low phase noise issues of mmWave VCOs, considering the trade-off between the VCO phase noise and power consumption [7], in this paper a dual-core transformer feedback VCO is proposed by combining the transformer feedback and VCO multi-core techniques. Based on the transformer feedback VCO topology, with the power-ground interconnect inductor and embedded decouple capacitor, the common-mode current return path is reduced, and the common-mode resonance is achieved at the VCO second harmonic frequency. Accordingly, the source tank impedance becomes real at the second

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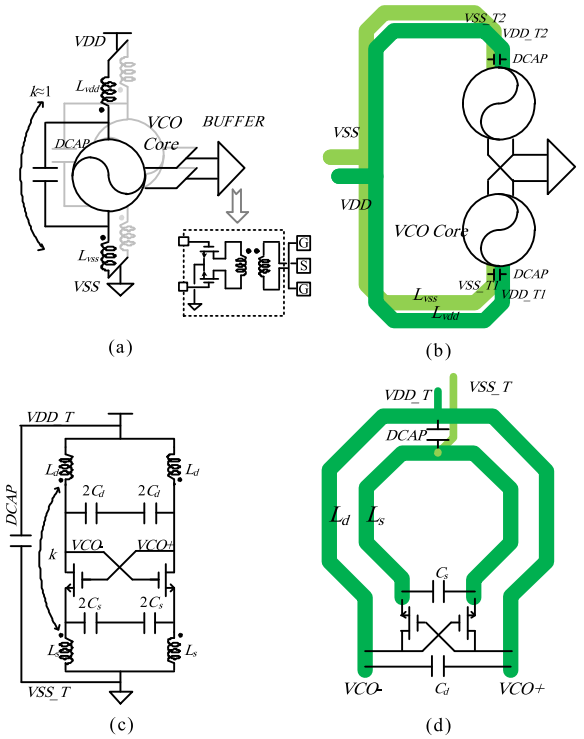

FIGURE 1. (a) Dual-core VCO topology, and (b) layout; (c) VCO cell topology, and (d) layout.

harmonic frequency, aligning the fundamental and the second harmonic phase and improving the signal symmetry and phase noise performance [8]–[9].

This paper is organized as follows. In Section II, the proposed dual-core VCO is discussed and simulated. Section III presents the VCO test results and performance comparison. Final conclusion is drawn in Section IV.

II. DESIGN AND ANALYSIS OF THE DUAL-CORE VCO

Fig. 1(a) and (b) presents the proposed dual-core VCO topology and its layout floorplan, in which the power-ground interconnect tail inductors, L_{vdd} and L_{vss}, are strongly coupled with each other with a coupling coefficient of about 1. With the decouple capacitor *DCAP,* the common-mode signal at each VCO power supply (such as *VDD_T1* and *VDD_T2*) is directly coupled to the ground (such as *VSS_T1* and *VSS_T2*). In this way, the VCO common-mode current return path is reduced, relaxing the outside parasitics effect and filtering the supply noise [9]. As to be explained shortly, the VCO common-mode resonance frequency is set at the second harmonic, thereby increasing the common-mode impedance for less second harmonics and improving the signal symmetry. For test purpose, the output buffer is required, which directly connects with the VCO output as close as possible to reduce the parasitic capacitor. As indicated in Fig. 1(b), with the dual-core topology the VCO layout can be realized in a symmetrical way, improving the VCO symmetry further. With less second harmonics and improved signal symmetry, the VCO flicker ($1/f$) noise up-conversion can be suppressed [10].

Fig. 1(c) shows the topology of the oscillator cell. As indicated, with a coupling coefficient of k, the transformer's primary and secondary inductors, L_d and L_s, are connected to the transistor drain and source terminals, respectively. With the 4 bit switch capacitors C_d and C_s, varactors and parasitic capacitance, the above two inductors realize an LC tank. Fig. 1(d) presents the detailed layout of the VCO cell, in which the embedded decoupling capacitor *DCAP* connects VCO core power and ground (*VDD_T* and *VSS_T*), resulting in a very compact layout.

According to [3]–[7], the transformer based VCO has two resonance frequencies:

$$\omega_{1,2} = \sqrt{\frac{(\omega_s^2+\omega_d^2) \pm \sqrt{(\omega_s^2+\omega_d^2)^2 - 4(1-k^2)\omega_s^2\omega_d^2}}{2(1-k^2)}} \tag{1}$$

where $\omega_d = 1/\sqrt{2L_dC_d}$ and $\omega_s = 1/\sqrt{2L_sC_s}$. Note that, the lower frequency ω_1 is the operating frequency and mainly determined by L_d and C_d. To achieve the aforementioned phase alignment of the fundamental and second harmonic for better signal symmetry [8], for initial design ω_2 is firstly set to be twice of the ω_1. In principle, the second harmonic frequency ω_2 should be calculated with the VCO common-mode model, whose inductor and capacitor values are different from that of the differential model. In this design, the VCO resonance frequency and design parameters are optimized with simulations.

For the VCO second harmonic impedance optimization, Fig. 2(a) and (b) present the common-mode return path schematic and layout of the transformer based VCO without the interconnect inductor and the embedded *DCAP*, respectively. As indicated, without the interconnect its common-mode resonance frequency will be affected by the outside decouple network parasitics, resulting in the inductor and the embedded *DCAP* the VCO power and ground are connected to the outside decouple network, and uncontrolled second harmonic frequency and worsening the signal symmetry. In contrast, as indicated in Fig. 2(c) and (d), with the *DCAP* and the strongly-coupled interconnect inductor, the VCO power and ground common-mode return path is reduced and well controlled. With optimizations, the VCO common-mode resonance frequency is set at the second harmonic frequency. Note that, in the common-mode model the equivalent inductor and capacitor values at the transistor drain and source terminals are represented as L_{d_CM}, L_{s_CM} and C_{d_CM}, C_{s_CM}, respectively.

To achieve good phase noise performance, the VCO tank loaded Q-factor is optimized by tuning L_d, L_s and k to achieve the transistor source to drain terminal voltage ratio of 0.5 at the operating frequency, which helps to increase the start-up gain at the same time [3]–[5]. To increase output power, the VCO tank impedance is optimized to match the input impedance of the output buffer by optimizing L_d and C_d. For this VCO, its design parameters are: $L_d = 110$pH, $L_s = 80$ pH, and $k = 0.6$. Fig. 3 shows the

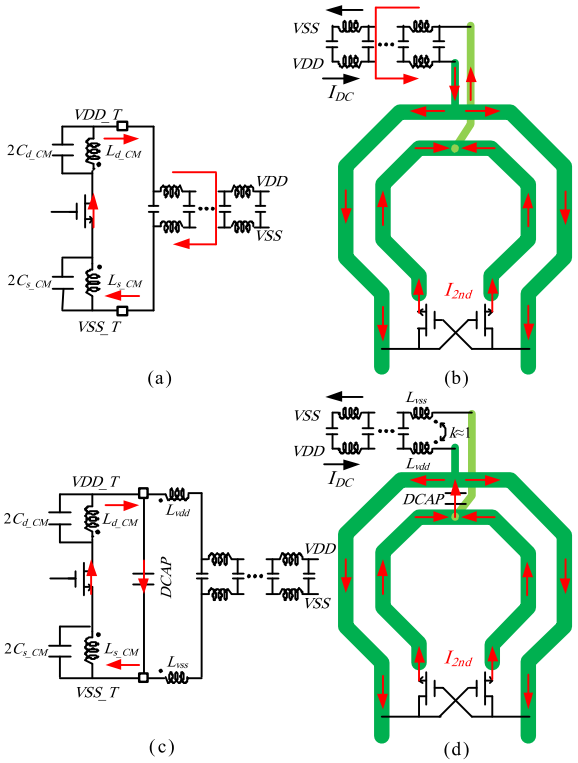

FIGURE 2. The common-mode return path of the transformer based VCO (a) schematic and (b) layout w/o the interconnect inductor and the embedded *DCAP*; (c) schematic and (d) layout w/ the interconnect inductor and the embedded *DCAP*.

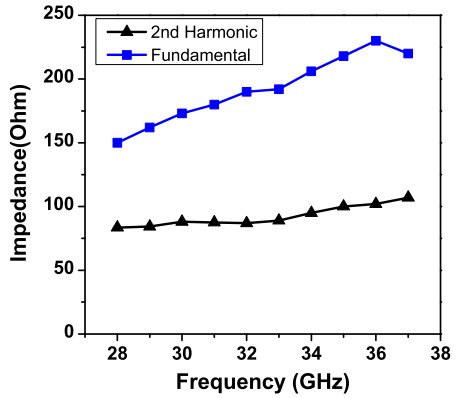

FIGURE 3. The fundamental and second harmonic impedances at the cross-coupled pair drain and source terminals, respectively.

tank fundamental and second harmonic impedances at the cross-couple pair drain and source terminals, respectively. Accordingly, the fundamental tank impedance at the drain is about 200 Ω. In this way, an impedance match is realized between the cross-couple pair and the output buffer, increasing the output power. As indicated, the VCO second harmonic tank impedance at the cross-couple pair source terminal is real, about 70 Ω, increasing the symmetry of the signal [7]–[12]. Moreover, with the source degeneration effect, the second harmonic current into the LC tank will be suppressed. With the improved signal symmetry and less second harmonics, the 1/*f* noise up-conversion is reduced.

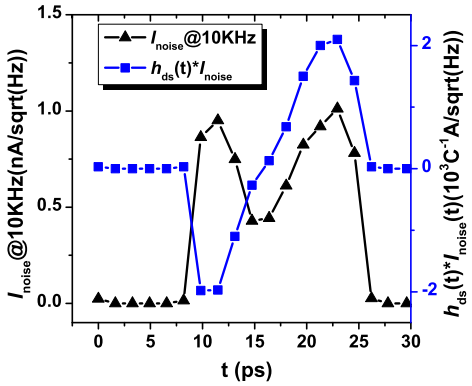

FIGURE 4. Simulation results of one period discrete I_{ds} noise (I_{noise}) at 10 kHz offset from 31 GHz and the effective non-normalized ISF.

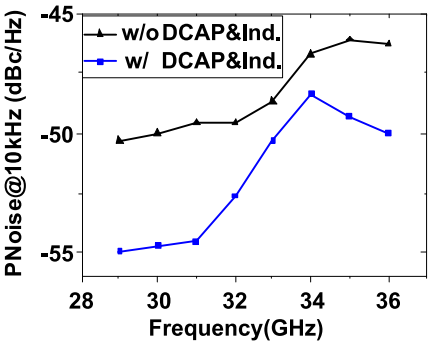

FIGURE 5. Phase noise simulation w/ and w/o the power-ground interconnect inductor and the *DCAP*.

To illustrate the improved signal symmetry, with the PSS and PXF simulations Fig. 4 shows the discrete I_{ds} noise at 10 kHz offset and the effective non-normalized impulse sensitivity function (ISF) which is the product of the non-normalized ISF, $h_{ds}(t)$, and I_{ds} noise, I_{noise} respectively [12]. As indicated, the VCO conduction angle is 180 degree, and benefiting from the physical symmetry and the improved signal symmetry, the proposed dual-core VCO ISF is symmetrical. With the ISF result, the VCO phase noise can be calculated as,

$$L(\Delta\omega) = \left(\frac{\sqrt{2}}{2\Delta\omega}\frac{1}{T}\int_0^T h_{ds}(t)I_{noise}(t)dt\right)^2 \qquad (2)$$

where T is the period of the VCO. Accordingly, the calculated phase noise is -54 dBc/Hz at 10 kHz offset from 31 GHz.

Fig. 5 shows the phase noise simulation results at 10 kHz offset with and without the power-ground interconnect inductor and the *DCAP*. As indicated, with the power-ground interconnect inductor and the *DCAP*, the VCO phase noise is lower, proving their advantages on the 1/*f* noise reduction. To be specific, the phase noise is about -54 dBc/Hz at 10 kHz offset from 31 GHz output frequency, which is the same as the above calculated results.

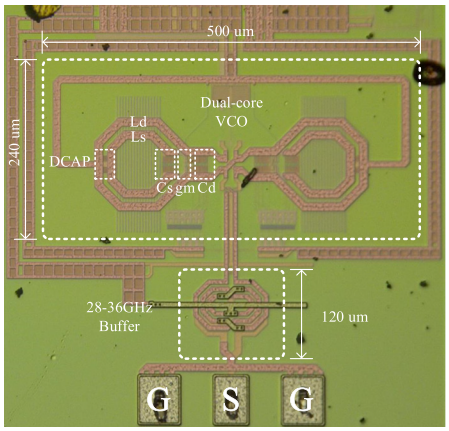

FIGURE 6. Chip micrograph.

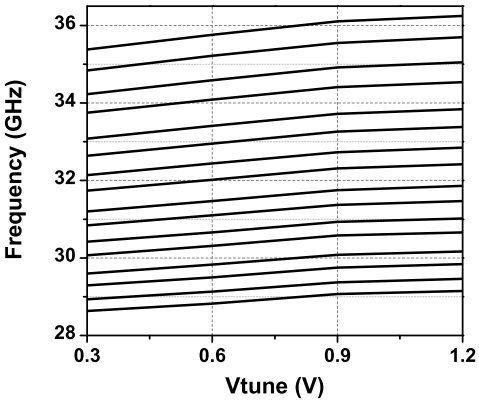

FIGURE 7. Tuning range with 4 bit switch capacitor.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

Fig. 6 shows the micrograph of the proposed VCO. Fabricated in a 65nm CMOS process, the dual-core VCO core area is 0.24 × 0.5 mm^2. Corresponding to the VCO structure, the inductors (L_d and L_s), capacitors (C_d and C_s) and transistors (g_m) are indicated. To reduce the substrate loss and to increase the tank Q-factor, the floating metal shield is used for the inductor. The VCO consumes a DC power of about 4.6 mW from a 0.5 V supply.

With the Rhode & Schwarz phase noise analyzer equipment, the oscillator tuning range, the output power and the phase noise are measured. As shown in Fig. 7, with a 4 bit switch capacitor, the VCO achieves a 28.6 to 36.2 GHz (23.5 %) tuning range. As indicated in Fig. 8, compared to the simulation results, due to the cable loss the VCO output power is about 1 dB lower.

Fig. 9 shows the VCO phase noise performance at 31 GHz. As indicated, the VCO achieves a phase noise of -103 and -124 dBc/Hz at 1 and 10 MHz offset, respectively, and the 1/f noise corner is about 400 kHz. Note that, as indicated in [8], the 1/f noise is very sensitive to the transformer coupling coefficient k and the VCO common-mode impedance. Suffering from the process PVT corner and the EM simulation accuracy, the tested phase noise at 10 kHz offset is about -48 dBc/Hz, which is 6 dB higher than the above calculation result. Accordingly, the 1/f noise corner frequency is about 1.5 times higher than the simulation results.

Versus the operating frequency, Fig. 10(a) shows the output phase noise at 1MHz offset and 1/f noise corner, while

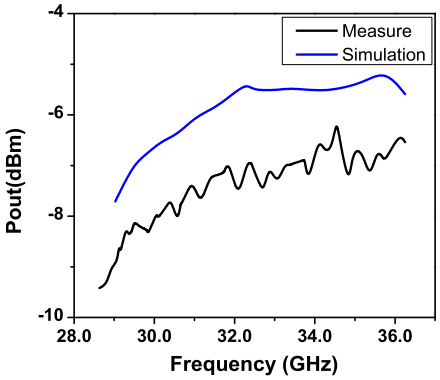

FIGURE 8. Output power comparison between simulations and measurements.

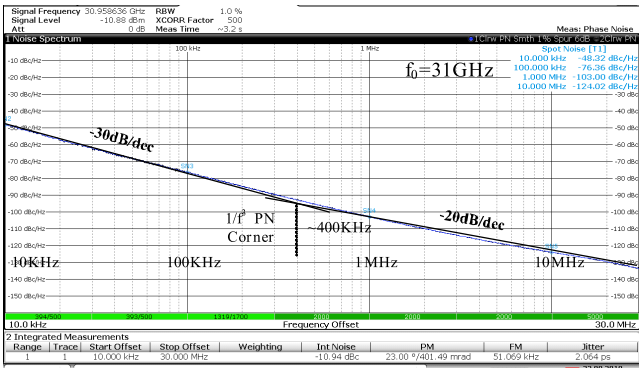

FIGURE 9. Phase noise measurement at 31 GHz.

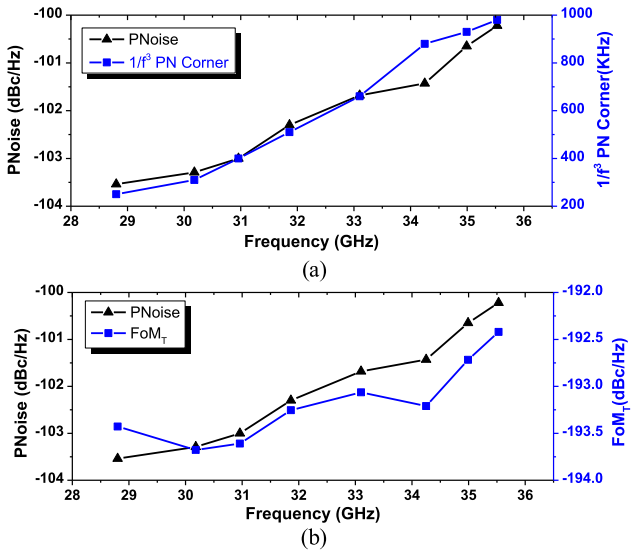

FIGURE 10. (a) Output phase noise and 1/f noise corner, (b) output phase noise and FoM$_T$ versus the operating frequency.

TABLE 1. Performance summary of state-of-the-art oscillators.

	This Work	VLSI 2019 [3]	TCSI 2018 [8]	JSSC 2018 [9]	ISSCC 2019 [13]	RFIC 2018 [14]
FO (GHz)	31	25.6	25	31.2	29.92	26
FTR (%)	23.5	14	12	17	16	42.3
PNoise @1MHz (dBc/Hz)	-103	-105.8	-110	-104	-112.3[c]	-102.6
Power (mW)	4.6	10.8	4.8	13	4	5.5
VDD (V)	0.5	0.9	0.6	1	0.48	0.9
FoM @1MHz (dBc/Hz)	-186.2	-184	-191.2	-183	-189.8	-183.3
FoM$_T$ @1MHz (dBc/Hz)	-193.6	-186.9	-192.8	-187.6	-193.9	-195.8
Process (CMOS)	65 nm	65 nm	65 nm	28 nm	65 nm	28 nm

a. FoM = PNoise- $20\log(f_0/\Delta f)+10\log(P_{DISS}/1mW)$

b. FoM$_T$ = PNoise- $20\log(f_0/\Delta f)+10\log(P_{DISS}/1mW)-20\log(FTR/10)$

c. Measured with divide-by-2 divider

Fig. 10(b) indicates the output phase noise and tuning range figure-of-merit (FoM$_T$). Over the 28.6-to-36.2 GHz tuning range, the phase noise is from -103.5 to 100.5 dBc/Hz at 1MHz offset, and the 1/*f* noise corner is from 250 to 980 kHz. At 31 GHz, the FoM$_T$ is about -193.6 dBc/Hz.

Table 1 summarizes the comparison with state-of-the-art results. With the proposed structure, this oscillator achieves a good tuning range and phase noise performance, resulting in a -193.6 dBc/Hz FOM$_T$ and -186.2 dBc/Hz FoM with a low supply voltage.

IV. CONCLUSION

This paper presents a low voltage 28.6-to-36.2GHz dual-core VCO in a 65nm CMOS process for 5G applications. Based on the transformer feedback topology, with the power-ground interconnect inductor and embedded decouple capacitor, the second harmonic real impedance is achieved at the VCO cross-couple pair source terminal. Accordingly, the common-mode current path is reduced and the signal symmetry improved, suppressing the flicker noise up conversion. With a 4 bit switch capacitor, the VCO achieves a 23.5 % tuning range from 28.6 to 36.2 GHz. At 31 GHz, the proposed VCO achieves phase noise of -103 dBc/Hz and FoM$_T$ of -193.6 dBc/Hz at 1 MHz offset.

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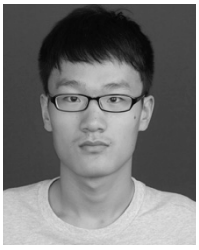

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