

# Novel Design Approach of Soft-Switching Resonant Converter With Performance Visualization Algorithm

SHOHEI SAITO<sup>1</sup>, (Student Member, IEEE), SHOHEI MITA<sup>1</sup>, (Student Member, IEEE), WENQI ZHU<sup>1</sup>, (Student Member, IEEE), HIROYUKI ONISHI<sup>2</sup>, SHINGO NAGAOKA<sup>2</sup>, TAKESHI UEMATSU<sup>2</sup>, KIEN NGUYEN<sup>1</sup>, (Senior Member, IEEE), AND HIROO SEKIYA<sup>1</sup>, (Senior Member, IEEE)

<sup>1</sup>Graduate School of Science and Engineering, Chiba University, Chiba 263-8522, Japan

<sup>2</sup>OMRON Corporation, Kyoto 600-8530, Japan

Corresponding author: Hiroo Sekiya (sekiya@faculty.chiba-u.jp)

**ABSTRACT** This paper presents a new design approach for the soft-switching resonant converter with satisfying the multiple design conditions. As an example, the FM controlled class-E resonant converter is designed. By applying the class-E inverter at the inverter part, the resonant converter works with high efficiency at high frequencies. The class-E inverter has, however, problems, which are the high peak value of the switch voltage and the difficulty of the zero-voltage switching continuation against the load variations. Additionally, there is a restriction on the peak value of the transformer voltage. In the proposed design approach, we can find the proper component values, which satisfy the multiple constraint conditions simultaneously, by full-use of the numerical computations of the converter-characteristic visualization on the parameter space. From the quantitative agreements between the experimental results and numerical predictions, the validity and effectiveness of the proposed design approach were confirmed.

**INDEX TERMS** Resonant converter, class-E inverter, push-pull class-E inverter, class-D full-wave rectifier, zero-voltage switching, frequency modulation control.

## NOMENCLATURE

$j$	Subscript expressing the inverter label.	$C_{ds}, C_{dsj}$	MOSFET drain-to-source parasitic capacitances.
$l$	Subscript expressing the rectifier label.	$C_S = C_{ds} + C_{ext}$	
$V_I, I_I, P_I$	Input voltage, current, and power, respectively.	$C_{Sj} = C_{dsj} + C_{extj}$	Shunt capacitances.
$V_o, P_o$	Output voltage and power, respectively.	$C_1$	Resonant capacitance of the inverter.
$L_I, L_{Ij}$	Input inductances.	$L_1, L_{2l}$	Primary and secondary inductances of the transformer, respectively.
$r_{Lj}$	Equivalent Series Resistances (ESRs) of the input inductance.	$r_{L1}, r_{L2l}$	ESRs of the transformer coil.
$S, S_j$	Switching devices of the inverter.	$k_1, k_2$	Coupling coefficients between the primary coil and the secondary one, and between the secondary coils, respectively.
$R_S, R_{Sj}$	ESRs of the switching device.	$D_l$	Rectifier diodes.
$r_S$	On-resistance of the MOSFET.	$R_{Dl}$	ESRs of the rectifier diode.
$V_{th1}$	Forward voltage of the MOSFET anti-parallel diode.	$r_D$	On-resistance of the rectifier diode.
$r_{SD}$	On-resistance of the MOSFET anti-parallel diode.	$V_{th2}$	Forward voltage of the rectifier diode.
$C_{ext}, C_{extj}$	External capacitances.	$C_{Dl}$	Rectifier diode anode-to-cathode parasitic capacitances.

The associate editor coordinating the review of this manuscript and approving it for publication was Yijie Wang<sup>1</sup>.

$C_f$	Filter capacitance of the rectifier.
$R_L$	Load resistance.
$R_{Lrated}$	Rated load resistance.
$f$	Operating frequency.
$f_{nom}$	Nominal operating frequency.
$f_0 = 1/2\pi\sqrt{C_1L_1}$	Resonant frequency.
$f_c = 1/2\pi C_f R_L$	Cutoff frequency.
$D$	Switch on-duty ratio of the MOSFETs.
$Q = 2\pi f_0 L_1 / R_L$	Loaded quality factor like parameter.
$A = f_0 / f$	Normalized resonant frequency.
$B = C_S / C_1$	Normalized shunt capacitance.
$H = L_1 / L_1$	Normalized input inductance.
$N = \sqrt{L_1 / L_2}$	Turn ratio of the transformer
$J_l = C_{Dl} / C_1$	Normalized rectifier diode parasitic capacitances.
$K = f_c / f$	Normalized cutoff frequency.
$v_{Smax}, v_{L1max}$	Maximum values of voltages across the MOSFET and primary coil of the transformer, respectively.
$\eta$	Power-conversion efficiency.

## I. INTRODUCTION

Next-generation semiconductor devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), realize high-speed switching, low conductance loss, and high-temperature operation [1]–[3]. With these characteristics, the SiC and GaN devices open new technological innovations for power converters. The high-frequency converter is one of such innovative technologies, which leads to compact volume and high power density. However, high-frequency converters suffer from the switching loss because the switching loss is proportional to the operating frequency. One of the well-known solutions for switching-loss reduction is to add the resonant mechanism to the circuit operation [4].

The LLC converter [5]–[9], which has already been in practical use, is a typical resonant converter. The LLC converter usually adopts the frequency modulation (FM) control to regulate the output voltage. Most, the LLC converters, including the commercial ones, use the operating frequencies in a hundred-kilohertz range [5]–[9]. With the appearances of SiC and GaN devices, it is expected to increase in the operating frequency range to a few megahertz ranges mainly. The LLC converter generally consists of the half or full-bridge inverter and full-wave rectifier, namely the class-D inverter [10]–[12], and the class-D rectifier [13]–[15]. The class-D inverter, however, has a difficulty of the driver design for the high-side switching devices at high frequencies, in particular.

The class-E inverter [16]–[22] is one of the high-frequency inverters without the floating switch in its circuit topology. Therefore, the burden of its driver-circuit design of the class-E inverter is lighter than that of the class-D inverter. In the class-E inverter, the soft-switching, namely the zero-voltage switching (ZVS) and/or the zero-derivative switching (ZDS),

is mandatory for obtaining high power-conversion efficiency [17]. The class-E inverter, however, has a problem that the peak voltage across the switch is 3.5 times as high as the input voltage [19]. There have been various studies to reduce the switch voltage stress in the resonant converters with class-E inverter [23]–[26]. These solutions, however, use additional components, which increase the circuit complexity. Besides, it is also a problem that the switching condition depends on load variations strongly.

The LLC converters are often designed by the first harmonic approximation (FHA) technique [5], [6]. From the gain characteristics for fixed load resistances in the frequency region, we can determine the frequency control range. Besides, it is regarded that the ZVS is satisfied when the resonant filter of the inverter is inductive. We cannot obtain the design accuracy with the FHA technique when the resonant current includes much high-harmonic components, for example, when the operating frequency is far from the resonant frequency, and the resonant filter has a low loaded quality factor. Additionally, this design method does not consider the peak value of the switch voltage and the transformer voltage, which become problems of the class-E converter designs.

In the traditional designs of the class-E converters, the inverter and the rectifier are designed individually with applying the FHA. After the individual designs, the resonant converter is built by connecting the inverter and the rectifier in series. The first stage of the class-E converter designs focused on how to satisfy the class-E ZVS/ZDS conditions at the rated operations [27], [28]. As the next stage, the class-E converters with achieving the soft switching against the load variations were designed [29]–[34]. The designs of the class-E converters in [29]–[34], however, do not consider the peak values of the switch voltage against the load variations. Additionally, it is difficult to obtain the design accuracy when the resonant current includes much high-harmonic components. If the converter needs to satisfy the multiple constraint conditions, we have to comprehend the numerous converter characteristics simultaneously for the entire load variations.

This paper proposes a new converter design approach for the resonant converter with multiple design constraint conditions. As an example, we show the detailed design process of the FM-controlled class-E converter for satisfying multiple design constraint conditions, namely rated output voltage, restrictions of the peak voltage across the switch and transformer, and ZVS achievement in the entire control range. By full-use of the converter-characteristic-visualization technique on the parameter space, it is possible to comprehend the converter performance for the entire load variations. The design accuracy of the proposed design method is not affected by the high-harmonic components of the resonant current. As a result, the proper circuit topology and the component values for satisfying the constraint conditions can be obtained. In the proposed converter,

- the peak value of the switch voltage is less than 2.5 times the input voltage by applying the 25% duty ratio,

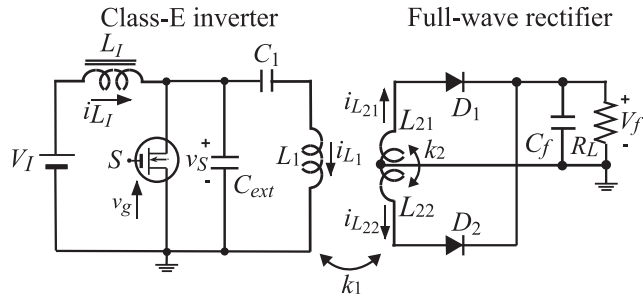


FIGURE 1. Circuit topology of the converter with the class-E inverter and the class-D full-wave rectifier.

- the peak voltage across the transformer is less than five times the input voltage by making the quality factor of the inverter resonant network low,
- the ZVS condition is ensured against the specified load variations by adopting the push-pull topology,
- the frequency-variation range for FM control is narrow in the entire control range by applying the large turn ratio of the transformer and the push-pull topology.

The validity and effectiveness of the proposed design method were confirmed from the quantitative agreements between the experimental results and the numerical predictions.

## II. DESCRIPTIONS OF RESONANT CONVERTER WITH CLASS-E INVERTER AND CLASS-D FULL-WAVE RECTIFIER

In this section, we consider the design of the resonant converter with the single class-E inverter and the class-D full-wave rectifier.

### A. CIRCUIT TOPOLOGY AND FUNDAMENTAL OPERATION

Figure 1 shows a circuit topology of the resonant converter with the single class-E inverter [16]–[22] and class-D full-wave rectifier [13]–[15]. The center-tapped transformer connects the inverter and the rectifier with a coupling coefficient of  $k$ . In the class-E inverter, the source terminal of the MOSFET is connected to the ground. Therefore, it is easy to design a driver circuit, which is suitable for high-frequency operations, compared with the bridge-type class-D inverter.

The MOSFET in the class-E inverter, as a switching device  $S$ , turns on and off by the driving voltage  $v_g$  with the operating frequency  $f$  and the on-duty ratio  $D$ . While the state of the switch is off, the pulse-shape voltage appears across the switch [16]. By applying the resonant filter  $C_1 - L_1$  to the switch voltage, the inverter has an AC current. In the class-E inverter, there is a special parameter set, which achieves the ZVS and the ZDS simultaneously at the switch turn-on instants, namely

$$v_S(2\pi) = 0 \tag{1}$$

$$\left. \frac{dv_S(\theta)}{d\theta} \right|_{\theta=2\pi} = 0. \tag{2}$$

(1) and (2) are called the class-E ZVS/ZDS conditions.

The rectifier diodes work as the half-wave rectification in each of the positive or the negative cycle. The voltages across

the diodes are converted into the DC voltage through the low-pass filter  $C_f - R_L$  [13]–[15]. Because the anode-to-cathode parasitic capacitance  $C_{Dj}$  exists on the actual diode device, the diode voltage  $v_{CDj}$  satisfies the class-E ZVS/ZDS conditions automatically at turn-off instant [15]. Because of the class-E ZVS/ZDS at both the inverter and the rectifier, the resonant converter in Fig. 1 achieves high power-conversion efficiency at high frequencies.

### B. ASSUMPTIONS

For the design of the converter in Fig. 1, we want to comprehend the converter characteristics. In this paper, we derive the converter waveforms numerically by solving the differential circuit equations and have the converter characteristics from the waveforms.

For simplifying the circuit operations, the following assumptions are given for the converter design.

- The MOSFET is expressed by the ideal switch, switch on-resistance, anti-parallel diode, and drain-to-source parasitic capacitance.
- The rectifier diode is modeled by the ideal switch, forward-voltage source, diode on-resistance, and anode-to-cathode parasitic capacitance.
- In the ideal switches, the infinite off-resistance and the zero switching time are assumed.
- The shunt capacitance  $C_S$ , which is the sum of the drain-to-source parasitic capacitance of the MOSFET  $C_{ds}$  and the external capacitance  $C_{ext}$ , works as a linear component.
- The secondary coils  $L_{21}$  and  $L_{22}$  has the same inductance value, namely,  $L_2 = L_{21} = L_{22}$ .
- The ESRs of the passive components are ignored.
- The inverter turns off and on at  $\theta = 2\pi D$  and  $\theta = 2\pi$ , respectively.

From the above assumptions, we have an equivalent circuit model of the resonant converter, as shown in Fig. 2.

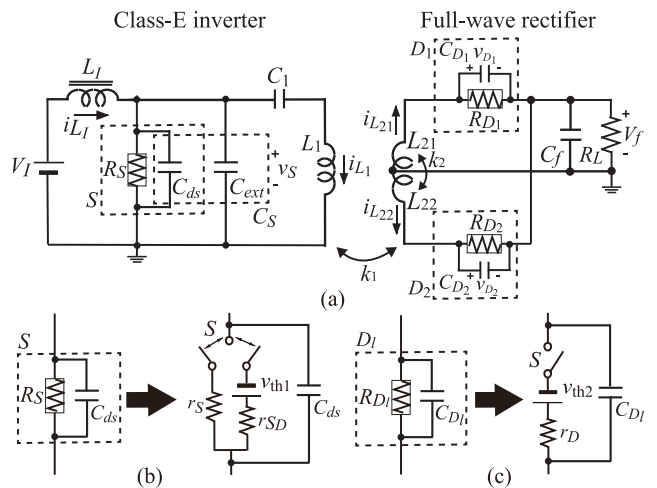


FIGURE 2. Equivalent models. (a) Equivalent model of the resonant converter in Fig. 1. (b) Equivalent model of the MOSFET. (c) Equivalent model of the rectifier diode.

### C. WAVEFORM DERIVATIONS

By adapting the above assumptions, the circuit equations are formulated as

$$\frac{dx}{d\theta} = f(\theta, \mathbf{x}, \boldsymbol{\lambda}), \quad (3)$$

where  $\mathbf{x} = [x_1, x_2, \dots, x_9] = [R_L i_{L1}/V_I, v_S/V_I, v_{C1}/V_I, R_L i_{L1}/V_I, R_L i_{L21}/V_I, R_L i_{L22}/V_I, v_{D1}/V_I, v_{D2}/V_I, v_f/V_I]^T \in \mathbf{R}^9$ , and  $\boldsymbol{\lambda} = [A, B, D, H, N, J_1, J_2, K, Q, V_{th1}/V_I, V_{th2}/V_I]^T \in \mathbf{R}^{11}$ .

Note that all the variations and parameters in (3) can be dimensionless. Therefore, general converter characteristics, which are independent of operating frequency, input voltage, and load resistance, can be obtained. Here, we omit to describe the detailed circuit equations because most of them overlap with the equations in (9)-(12).

We have transient waveforms by solving (3). In this paper, we use the Runge-Kutta method as a differential equation solver. The time step of the Runge-Kutta method is  $\pi/400000$ .

## III. DESIGN STRATEGY

### A. PROBLEM STATEMENT

The target application of the proposed resonant converter is the latter stage of an industrial AC/DC power supply connected in series with a power factor correction circuit. Therefore, the rated specifications are input voltage  $V_{I\text{rated}} = 200$  V, output voltage  $V_{o\text{rated}} = 48$  V and output power  $P_{o\text{rated}} = 240$  W. Besides, the nominal operating frequency is  $f_{\text{nom}} = 1$  MHz, in this paper. The proposed converter keeps the output voltage constant by applying FM control against the load variations, whose range is  $0.9 < R_L/R_{L\text{rated}} < 10$ . It is a mandatory condition for the design that the converter satisfies the ZVS condition in the entire control range. Additionally, the peak value of the switch voltage must be less than 500 V in the entire control range because of the permissible drain-to-source voltage of SiC MOSFET; we adopt SCT3120AL SiC MOSFET in the converter. It is also necessary that the peak values of the voltages across the inductances and transformer are less than 1 kV regardless of the load variations, because of the magnetic core constraint.

The purpose of this paper is to find the component-value set for satisfying all the design constraint conditions. For achieving the purpose, we make full use of the characteristic-visualization algorithm with the aid of a computer.

### B. SWITCHING PATTERNS IN CLASS-E INVERTER

In this paper, we consider three switching patterns at the turn-on instant in the class-E inverter [35].

Figure 3 shows examples of the switch voltage and current waveforms of the class-E inverter. Figure 3(a) shows that the switch voltage does not reach zero before the switch turns on, which is called ‘‘Case-1 switching’’ in this paper. In Fig. 3(b), the MOSFET anti-parallel body diode turns on at  $\theta = \theta_1$  and the switch turns on during the body diode is in the on-state, which is regarded as the ZVS. This switching pattern is the

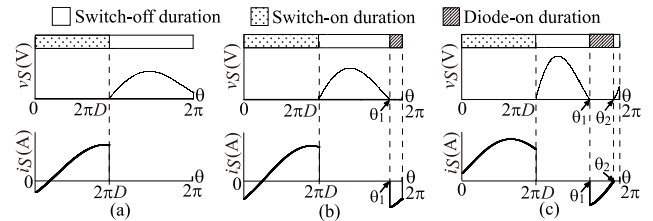


FIGURE 3. Waveforms of the switch voltage and current in the class-E inverter. (a) Case 1. (b) Case 2. (c) Case 3.

‘‘Case-2 switching’’. There is also a switching pattern that the body diode turns off at  $\theta = \theta_2$  again before the switch turns on, which is defined as the ‘‘Case-3 switching’’. In the Case-3 switching, both the turn-on switching loss and the conduction loss of the body diode occur.

It is a design constraint for the proposed converter to achieve the ZVS, namely the Case-2 switching, in the entire control range. It is well known that the inverter can satisfy the ZVS condition by making the resonant filter  $C_1 - L_1$  inductive [36]. When the inductive characteristic of the resonant filter is, however, too strong, the Case-3 switching appears in the class-E inverter. In the Case-3 switching pattern, the conduction losses at ESRs of each passive component also increase. That is because a strong inductivity of the resonant filter generates a large free-wheeling current.

The class-E ZVS/ZDS point is the switching-pattern boundary not only between Cases 1 and 2 but also between Cases 2 and 3. Therefore, it is possible to suppress both the power losses due to the diode-active duration and the free-wheeling current when the converter operates in the close parameter region of the class-E ZVS/ZDS point.

## IV. ALGORITHM OF CONVERTER CHARACTERISTIC VISUALIZATION ON PARAMETER SPACES

The purpose of this paper is to design the resonant converter for satisfying the design constraint conditions in the entire control range against the load variations. Because the FM control is adopted against the load variations in the proposed converter, it is useful to obtain the converter characteristics in the parameter space of the load resistance and the operating frequency.

### A. DERIVATION OF THE CLASS-E ZVS/ZDS POINT

High-efficiency operations against the load variations are expected around the class-E ZVS/ZDS point. Therefore, as the first step, the class-E converter, which satisfies the class-E ZVS/ZDS conditions in (1) and (2) at the rated condition, is designed. In the rated condition, the output voltage of the converter should be

$$\begin{aligned} \frac{V_o}{V_I} - \frac{V_{o\text{rated}}}{V_I} &= \int_0^{2\pi} \frac{v_f}{V_I} d\theta - \frac{V_{o\text{rated}}}{V_I} \\ &= \int_0^{2\pi} \frac{v_f}{V_I} d\theta - 0.24 = 0, \end{aligned} \quad (4)$$



This paper adopts the trapezoidal method for the numerical integration in this paper. By applying the algorithm in [37], we can numerically derive a parameter set for satisfying (1), (2) and (4).

**B. RESTRICTIONS OF THE PEAK VOLTAGES**

As the second step, we comprehend the states of the design constraint conditions of the converter, which is designed in the first step, in the entire control range. From the SiC MOSFET restriction, the permissible peak value of the switch voltage is expressed as

$$\left| \frac{v_{Smax}}{V_I} \right| - 2.5 = 0, \tag{5}$$

Similarly, the permissible peak value of the voltage across the transformer primary coil is given by

$$\left| \frac{v_{L1max}}{V_I} \right| - 5 = 0, \tag{6}$$

When the normalized load resistance  $R_L/R_{Lrated}$  is given, the normalized frequency  $f/f_{nom}$  for satisfying the above conditions can be obtained numerically.

**C. ZVS-REGION VISUALIZATION**

As the third step, it is necessary to consider the ZVS achievement in the control range. Only the Case-2 switching satisfies the ZVS condition. Therefore, the ZVS region on the parameter space of the load resistance and the operating frequency can be comprehended easily by visualizing the Case-2 switching region. Our idea for visualizing it is to draw the switching-pattern boundary curve between the Cases 1 and 2 and that between the Cases 2 and 3, which are expressed as

$$\frac{v_S(2\pi)}{V_I} = 0, \tag{7}$$

and

$$\frac{R_L i_S(2\pi)}{V_I} = \frac{d}{d\theta} \frac{v_S(\theta)}{V_I} \Big|_{\theta=2\pi} = 0, \tag{8}$$

respectively.

When the normalized load resistance is given, the value of the normalized frequency for satisfying the boundary condition is determined uniquely. The class-E ZVS/ZDS point is located on the intersection of these boundary curves. Therefore, both the boundary curves start from the class-E ZVS/ZDS point.

**D. CHARACTERISTICS OF FM CONTROL**

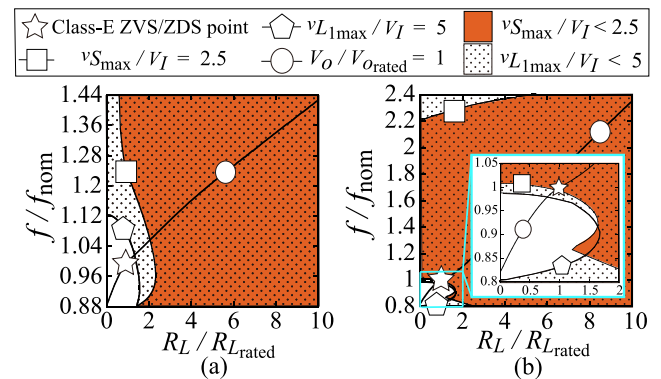
The resonant converter should keep the rated output voltage by varying the operating frequency against the load variations. Namely, when we solve (4) with given normalized load resistance for the normalized operating frequency, it is possible to predict the operating frequency for keeping the rated output voltage as a function of the load resistance.

**E. CHARACTERISTIC VISUALIZATION**

When all the solution curves, which are described in subsection IV - B and C, are superimposed on the parameter space of the normalized load resistance and the normalized operating frequency, it is possible to visualize the converter characteristics. By tracking the solution curve of (4), it is possible to comprehend the converter characteristics of the FM controlled converter intuitively and visually. The characteristic diagrams can be derived quickly with low computation cost by applying the numerical-computations proposed in [37]. It is a simple task to draw the diagram at a given parameter set. Therefore, we can confirm the converter characteristics at the many component-value sets.

**V. CHARACTERISTIC EVALUATIONS OF RESONANT CONVERTER WITH SINGLE CLASS-E INVERTER**

In the converter designs, three parameters  $A$ ,  $B$ , and  $N$  are adjusted for achieving the rated output voltage and the class-E ZVS/ZDS conditions. It is an important problem to make criteria to determine these parameters. In the design, the coupling coefficient values are set as  $k_1 = k_2 = 0.9$ . The other parameters are given from the design specifications.



**FIGURE 4. Characteristics diagram of the peak values of the switch and primary-coil voltages on the  $R_L/R_{Lrated} - f/f_{nom}$  space. (a) For  $D = 0.5$ ,  $H = 10$ , and  $Q = 100$ . (b) For  $D = 0.25$ ,  $H = 10$ , and  $Q = 20$ .**

Figure 4 shows the resonant converter characteristics on the normalized load resistance and the normalized frequency parameter space. The curves on the parameter space are solutions of (4) - (6). The dotted area satisfies the constraint condition of the primary-coil-voltage peak value, and the red area satisfies that of the switch-voltage peak value. From Fig. 4, we can investigate the effects of the duty ratio and the loaded quality factor on the peak voltage values across the switch and the transformer.

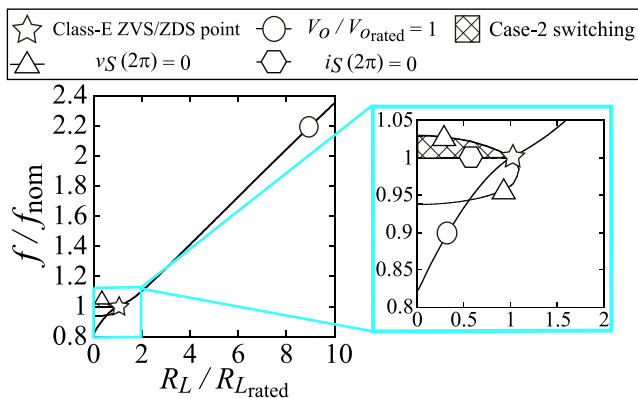
Figure 4(a) shows the peak-voltage characteristics for  $D = 0.5$ ,  $H = 10$ , and  $Q = 100$ . This parameter set provides a high  $Q$  resonant filter. By tracking the curve of  $V_O/V_{Orated} = 1$ , it is possible to comprehend the characteristics of the FM-controlled resonant converter against the load variation. It is seen from Fig. 4(a) that both the peak values of the switch and transformer voltages are higher than the permissible value around the rated conditions, namely in the range of

$0.9 < R_L/R_{Lrated} < 1.3$ . While, both the conditions are satisfied in the range of  $2.1 < R_L/R_{Lrated}$ . It is found from this result that we need to change the values of the parameters in the first step for achieving the design constraint conditions.

Figure 4(b) shows the peak-voltage characteristics for  $D = 0.25$ ,  $H = 10$ , and  $Q = 20$ . It can be confirmed from this figure that the peak values of the switch voltage in the range of  $1.0 < R_L/R_{Lrated}$ , and the transformer voltage in the entire control range are lower than the permissible values. From the result, we find that it is possible to satisfy the voltage restrictions by adapting the low  $Q$  and 25 % on-duty ratio. In the following designs, we adopt the duty ratio as  $D = 0.25$  and low  $Q$ .

**A. NECESSITY OF PUSH-PULL TOPOLOGY**

Figure 5 shows the Case-2 switching region for  $D = 0.25$ ,  $H = 10$ ,  $N = 1.21$  and  $Q = 20$  on the parameter space of the normalized operating frequency and the normalized load resistance. The meshed area, which is surrounded by the solution curves of (7) and (8), is the case-2 switching region. It is seen from this figure that the FM-controlled converter cannot achieve the Case-2 switching at all in the entire control range except the class-E ZVS/ZDS point.



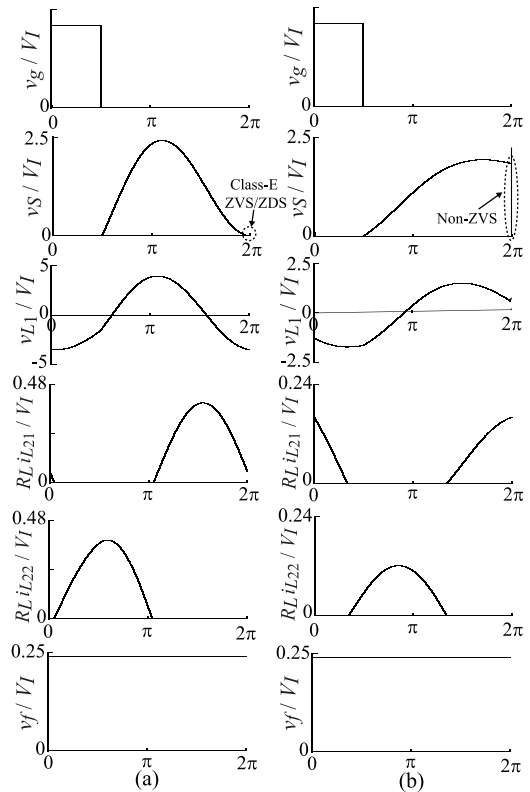
**FIGURE 5.** Case-2 switching region for  $D = 0.25$ ,  $H = 10$ ,  $N = 1.21$  and  $Q = 20$  on the  $R_L/R_{Lrated} - f/f_{nom}$  space.

Figure 6 shows waveforms of the converter with the single class-E inverter. It can be confirmed from Fig. 6(a) and (b) that all the peak values of the normalized voltages across the switch and the transformer satisfy the constraint conditions.

It is also confirmed from Fig. 6(a) that the switch voltage satisfies the class-E ZVS/ZDS conditions. The inverter, however, does not achieve the ZVS for  $R_L/R_{Lrated} = 3$  as shown in Fig. 6(b).

From the waveforms in Fig. 6(b), we see that the inverter resonant current includes much direct and high harmonic components. This makes that the operation of the class-D full-wave rectifier is asymmetric, which is a cause of the non-ZVS occurrence.

The push-pull topology may be effective against this asymmetric problem. By adopting the push-pull topology, the direct component and even-harmonic components of the



**FIGURE 6.** Waveforms of the resonant converter with single class-E inverter for  $D = 0.25$ ,  $H = 10$ ,  $N = 1.21$  and  $Q = 20$ . (a) For  $R_L/R_{Lrated} = 1$ . (b) For  $R_L/R_{Lrated} = 3$ .

inverter resonant current are canceled. As a result, it is expected that the full-wave rectifier works with the symmetry, which can expand the ZVS area. Additionally, the voltage stress across the resonant capacitance can be reduced by applying the push-pull topology because the direct voltage component across the resonant capacitance becomes zero.

**VI. EVALUATION AND DESIGN OF PUSH-PULL CLASS-E ZVS CONVERTER**

**A. DESCRIPTION OF PUSH-PULL CLASS-E INVERTER**

From the discussions in Section V, we determine to design the resonant converter with the push-pull class-E inverter and the class-D full-wave rectifier.

Figure 7 shows an equivalent circuit topology of the resonant converter with the push-pull class-E inverter. The push-pull class-E inverter is composed of two class-E inverters connected in parallel.

**B. CIRCUIT EQUATION FORMULATION**

The assumptions of (a) - (e) in Section II are also valid in the designs of the push-pull class-E converter. Additionally, the following assumptions are given

- (h) The duty ratio of  $S_1$  is the same as that of  $S_2$ . The switches  $S_1$  and  $S_2$  turn on at  $\theta = 2\pi$  and  $\theta = \pi$ , respectively.

(i) The push-pull inverter has symmetry, namely, the component values of the inverter 1 are the same as those of the inverter 2.

When we define  $L_l = L_{l1} = L_{l2}$  and  $C_s = C_{s1} = C_{s2}$  from the assumption (i), the circuit equations can be formulated as

$$\left\{ \begin{aligned} \frac{d}{d\theta} \frac{R_L i_{Llj}}{V_I} &= \frac{A}{HQ} \left( 1 - \frac{v_{Sj}}{V_I} - \frac{r_{Llj} i_{Llj}}{V_I} \right), \\ \frac{d}{d\theta} \frac{v_{Sj}}{V_I} &= \frac{AQ}{B} \left( \frac{R_L i_{Llj}}{V_I} - \frac{v_{Sj} R_L}{V_I R_{Sj}} - \frac{R_L i_{Ll1}}{V_I} \right), \\ \frac{d}{d\theta} \frac{v_{C1}}{V_I} &= AQ \frac{R_L i_{L1}}{V_I}, \\ \frac{d}{d\theta} \frac{R_L i_{L1}}{V_I} &= \frac{A[(1-k_2^2)v_{L1} - k_1(1-k_2)Nv_{L21} + k_1(1-k_2)Nv_{L22}]}{Q[1 - k_2^2 + 2k_1^2(k_2 - 1)]}, \\ \frac{d}{d\theta} \frac{R_L i_{L2l}}{V_I} &= \frac{A[(-1)^l k_1(1-k_2)Nv_{L1} - (1-k_1^2)N^2v_{L2l} - (k_2 - k_1^2)N^2v_{L2(3-l)}]}{Q[1 - k_2^2 + 2k_1^2(k_2 - 1)]}, \\ \frac{d}{d\theta} \frac{v_{Dl}}{V_I} &= \frac{AQ}{J_l} \left( \frac{R_L i_{L2l}}{V_I} - \frac{R_L v_{Dl}}{r_{Dl} V_I} \right), \\ \frac{d}{d\theta} \frac{v_f}{V_I} &= \frac{1}{K} \left( \frac{R_L i_{L21}}{V_I} + \frac{R_L i_{L22}}{V_I} - \frac{v_f}{V_I} \right), \end{aligned} \right. \quad (9)$$

( $j = 1$  and  $2$ ,  $l = 1$  and  $2$ )

where,

$$\left\{ \begin{aligned} v_{L1} &= \frac{v_{S1} - v_{S2} - v_{C1} - i_{L1} r_{L1}}{V_I}, \\ v_{L2l} &= \frac{v_{Dl} + v_f + i_{L2l} r_{L2l}}{V_I}, \end{aligned} \right. \quad (10)$$

are the normalized voltage across the transformer. Additionally, the normalized ESRs of the inverter switch and the rectifier diodes are expressed as

$$\frac{R_{Sj}}{R_L} = \begin{cases} \frac{r_S}{R_L}, & \text{for } (j-1)\pi < \theta \leq (j-1+2D)\pi, \\ \infty, & \text{for } (j-1+2D)\pi < \theta \leq (j+1)\pi \\ & \text{and } \frac{v_{Sj}}{V_I} \geq \frac{V_{th1}}{V_I}, \\ \frac{r_{SD}}{R_L}, & \text{for } (j-1+2D)\pi < \theta \leq (j+1)\pi \\ & \text{and } \frac{v_{Sj}}{V_I} < \frac{V_{th1}}{V_I}, \end{cases} \quad (11)$$

and

$$\frac{R_{Dl}}{R_L} = \begin{cases} \frac{r_D}{R_L}, & \text{for } \frac{v_{Dl}}{V_I} \geq \frac{V_{th2}}{V_I}, \\ \infty, & \text{for } \frac{v_{Dl}}{V_I} < \frac{V_{th2}}{V_I}, \end{cases} \quad (12)$$

respectively. The ESRs of the passive components are ignored in the converter design stage because they have little effect on the waveforms. The ESRs are considered only when we calculate the power-conversion efficiency.

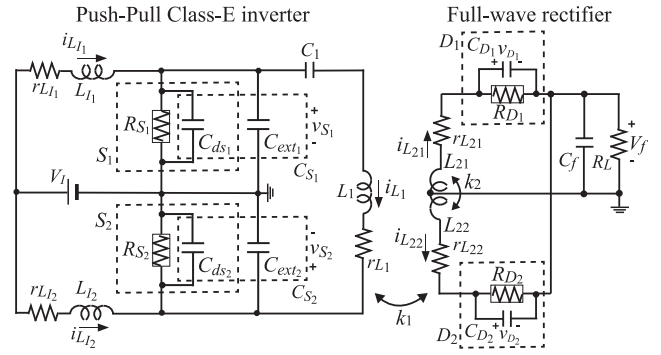


FIGURE 7. Equivalent model of the resonant converter with the push-pull class-E inverter.

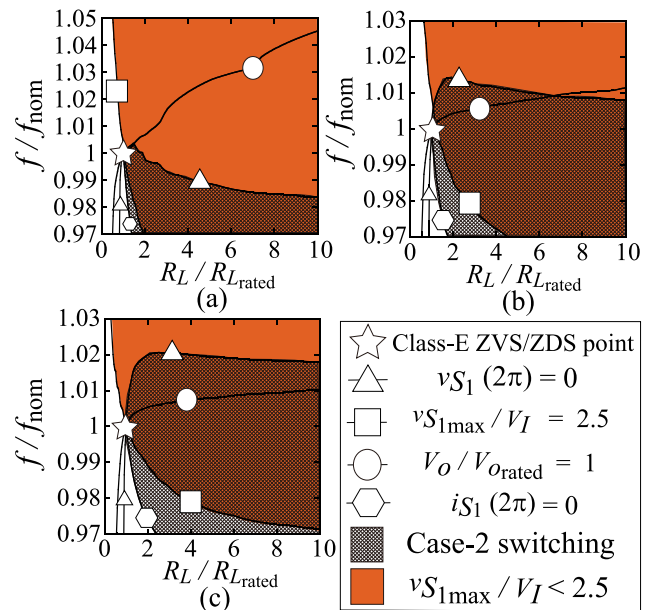


FIGURE 8. Converter characteristics with the push-pull class-E converter on the  $R_L/R_{Lrated} - f/f_{nom}$  space for  $D = 0.25$  and  $Q = 20$ . (a) For  $N = 8$ . (b) For  $N = 10$ . (c) For  $N = 12$ .

### C. TRANSFORMER DESIGN

From the results in Section V,  $D = 0.25$  and  $Q = 20$  are given for satisfying the peak voltage values in the design constraint conditions. Here, we consider the transformer, namely, it is necessary to determine the transformer turn ratio  $N$ . In this stage, the coupling coefficient values are assumed as  $k_1 = k_2 = 0.9$ .

Figure 8 shows the peak switch-voltage value characteristic and the ZVS region of the push-pull class-E converter, on the parameter space of the normalized load resistance and the normalized operating frequency. The condition of the peak value of the transformer voltage can be satisfied in all the regions of the parameter space of Fig. 8.

Figure 8(a) shows the characteristics of the converter for  $N = 8$ . It can be confirmed from Fig. 8(a) that the Case-2 switching region is expanded compared with Fig. 5 because

the push-pull topology is applied. However, the converter still cannot satisfy the ZVS in the control range.

Figure 8(b) shows a characteristic diagram for  $N = 10$ . It is seen from Fig. 8(b) that the range of the ZVS achievement is expanded to a higher frequency range. Besides, we see that the variation range of the frequency at light loads becomes narrow by the increase in  $N$ . As a result, the converter achieves the ZVS condition in the range of  $1.0 < R_L/R_{Lrated} < 6.6$  in Fig. 8(b). From this result, the increase in the transformer turn ratio contributes not only to the expansion of the Case-2 switching region but also to the reduction of the frequency variation range.

Figure 8(c) shows the characteristics diagram for  $N = 12$ . It can be confirmed Fig. 8(c) that the converter satisfies all the constraint conditions in the range of  $R_L/R_{Lrated} > 1.0$ .

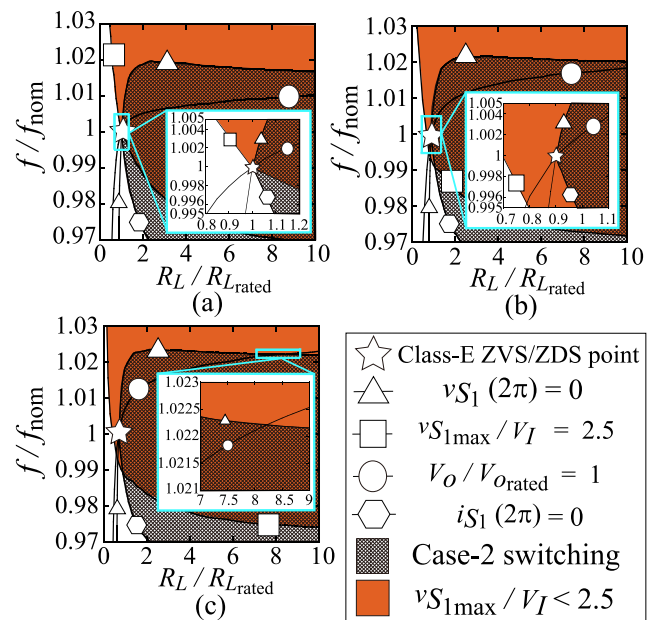
From the above results, we give  $N = 12$  for the transformer design. The transformer for the LLC-type converter needs to have sufficient leakage flux. We implemented the transformer with the leakage flux enhancement by the magnetic material [38]. In the implemented transformer, the winding turn number can be reduced because of the leakage flux enhancement. The turn numbers of the primary and secondary of the implemented transformer were twelve and one, respectively. The small winding turn number enabled the core-loss reduction. Besides, it was possible to turn the windings loosely due to the small turn number, which reduced the proximity effects. From the above ingenuity, it was possible to reduce the transformer loss. TOMITA ELECTRIC 2N5 core was adopted for the transformer core. The implemented transformer parameters were measured by the KEYSIGHT E4990A impedance analyzer as  $L_1 = 52.3 \mu\text{H}$ ,  $L_{21} = L_{22} = 0.39 \mu\text{H}$ ,  $k_1 = 0.91$ , and  $k_2 = 0.92$ . These values were used at the following converter designs.

The measured ESRs of the primary and secondary coils at 1 MHz are  $r_{L1} = 1.24 \Omega$ ,  $r_{L21} = 7.11 \text{ m}\Omega$ , and  $r_{L22} = 7.54 \text{ m}\Omega$ , which includes the effects of both the winding and core losses. Additionally, we confirmed that these ESR values were almost constant under the  $\pm 5\%$  variations of the nominal frequency.

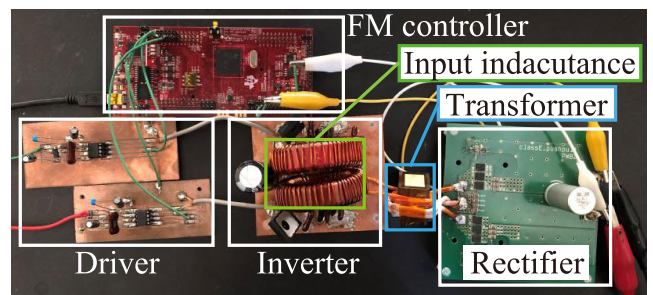
#### D. CONVERTER DESIGN WITH VISUALIZED CHARACTERISTIC DIAGRAM

From subsection VI - C, we had  $N = 11.6$ . At least three parameters are necessary for satisfying the class-E ZVS/ZDS conditions and the rated output voltage. In this section, three parameters  $A$ ,  $B$ , and  $H$  are used for converter designs.

Figure 9 shows the characteristic diagram of the push-pull class-E converter on the parameter space of the normalized load resistance and the normalized operating frequency. Figure 9(a) shows the characteristics of the converter, which satisfies the class-E ZVS/ZDS conditions at  $R_L/R_{Lrated} = 1.0$ . It can be seen from Fig. 9(a) that both the ZVS condition and the peak-value restrictions of the switch voltages cannot be achieved in the range of  $R_L/R_{Lrated} < 1.0$ . On the other hand, the converter satisfies all the design constraint conditions, including the Case-2 switching, in the range of



**FIGURE 9.** Characteristic diagrams of the push-pull class-E converter on the  $R_L/R_{Lrated} - f/f_{nom}$  space for  $D = 0.25$ ,  $Q = 20$ , and  $N = 11.6$ . The class-E ZVS/ZDS points are (a)  $R_L/R_{Lrated} = 1.0$ , (b)  $R_L/R_{Lrated} = 0.9$ , and (c)  $R_L/R_{Lrated} = 0.7$ .



**FIGURE 10.** Photo of the implemented circuit.

$R_L/R_{Lrated} \geq 1.0$ . From the result, it can be supposed that the converter satisfies all the constraint conditions by setting the class-E ZVS/ZDS point at  $R_L/R_{Lrated} \leq 0.9$ .

Figure 9(b) shows the characteristic diagram when the class-E ZVS/ZDS point is set at  $R_L/R_{Lrated} = 0.9$ . It is seen from Fig. 9(b) that all the constraint conditions are satisfied in the entire control range.

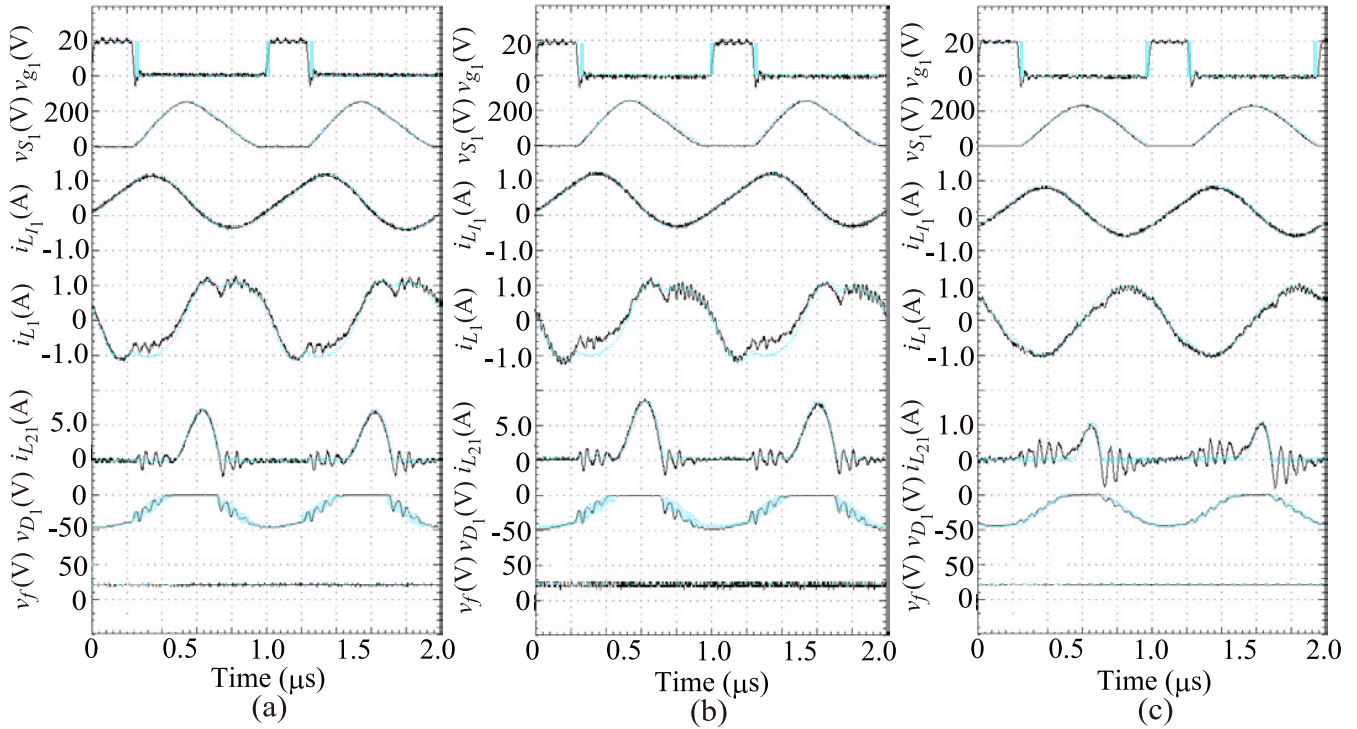
Figure 9(c) shows the characteristic diagram when the class-E ZVS/ZDS point is set at  $R_L/R_{Lrated} = 0.7$ . In this case, the Case-1 switching appears in the range of  $R_L/R_{Lrated} \geq 8.2$ .

By drawing and the investigating the characteristic diagrams, the proper component values, which satisfy all the constraint conditions in the entire control range, can be obtained by setting the class-E ZVS/ZDS point within  $0.78 < R_L/R_{Lrated} \leq 0.9$ .

#### VII. EXPERIMENTAL VERIFICATIONS

From the design process in Section VI, we can obtain all the parameters for satisfying the design constraint conditions.

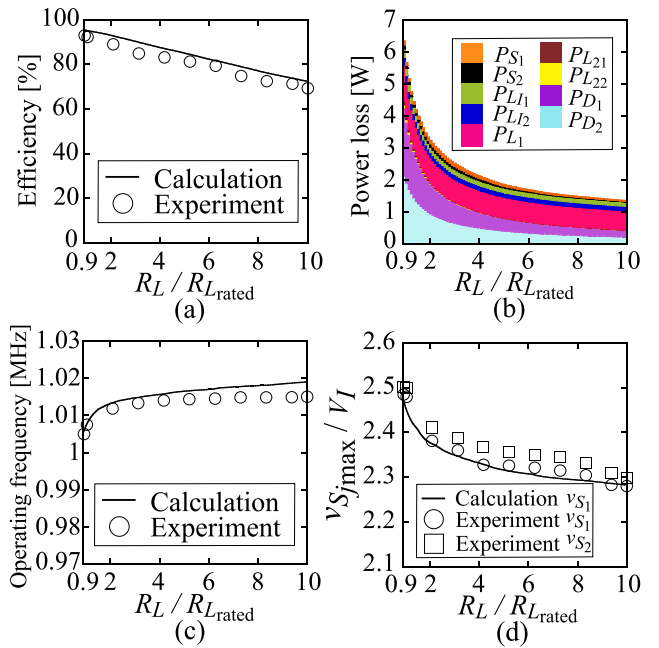




**FIGURE 11.** Experimental and numerical waveforms for the proposed converter for (a)  $R_L/R_{L_{rated}} = 1$ , (b)  $R_L/R_{L_{rated}} = 0.9$ , and (c)  $R_L/R_{L_{rated}} = 10$ . (Solid line: Experimental waveforms, Dashed blue line: Calculated waveforms).

**TABLE 1.** Design parameters and component values.

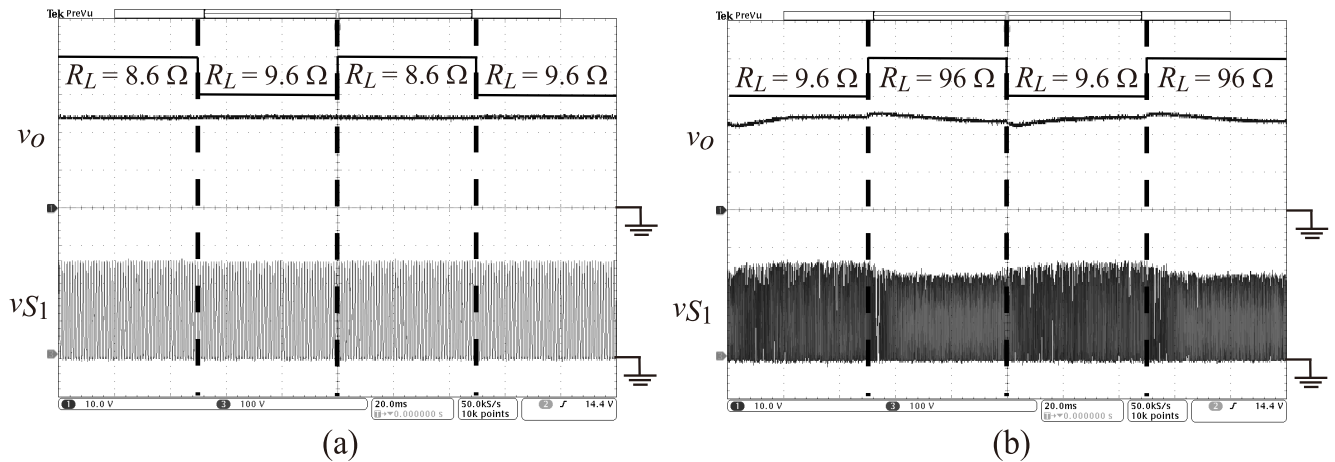
	Calculated	Measured	Difference
$f$	1.005 – 1.019 MHz	1.005 – 1.015 MHz	–
$R_{L_{rated}}$	9.6 $\Omega$	9.6 $\Omega$	–
$V_{I_{rated}}$	100 V	100 V	–
$D$	0.25	0.25	–
$L_{I1}$	27.8 $\mu$ H	27.4 $\mu$ H	1.4 %
$L_{I2}$	27.8 $\mu$ H	27.5 $\mu$ H	1.1 %
$r_{LI1}$	–	470 m $\Omega$	–
$r_{LI2}$	–	452 m $\Omega$	–
$L_1$	52.3 $\mu$ H	52.3 $\mu$ H	0.0 %
$r_{L1}$	–	1.24 $\Omega$	–
$L_{21}$	390 nH	390 nH	0.0 %
$L_{22}$	390 nH	390 nH	0.0 %
$r_{L21}$	–	7.11 m $\Omega$	–
$r_{L22}$	–	7.54 m $\Omega$	–
$C_{S1}$	1.98 nF	1.96 nF	2.1 %
$C_{S2}$	1.98 nF	1.96 nF	2.1 %
$C_1$	1.72 nF	1.71 nF	0.6 %
$C_{D1}$	70.0 pF	70.0 pF	0.0 %
$C_{D2}$	70.0 pF	70.0 pF	0.0 %
$C_f$	47.0 $\mu$ F	47.0 $\mu$ F	0.0 %
$r_S$	120 m $\Omega$	120 m $\Omega$	0.0 %
$r_{SD}$	250 m $\Omega$	250 m $\Omega$	0.0 %
$r_D$	5.00 m $\Omega$	5.00 m $\Omega$	0.0 %
$V_{th1}$	3.2 V	3.2 V	0.0 %
$V_{th2}$	0.61 V	0.61 V	0.0 %
$k_1$	0.91	0.91	0.0 %
$k_2$	0.92	0.92	0.0 %



**FIGURE 12.** The characteristics of the converter as functions of the normalized load resistance (a) Power conversion efficiency, (b) Numerical predictions of power-loss factors, (c) Operating frequency for keeping the rated output voltage, (d) Peak value of the normalized switch voltages.

Table 1 gives the design parameters and component values of the implemented converter, where all the measured component values were obtained from the KEYSIGHT E4990A

impedance analyzer. The measured ESRs of the passive components were considered for the numerical waveform derivations and efficiency predictions. Figure 10 shows a photo



**FIGURE 13.** Experimental waveforms of output voltage and switch voltage with sudden load variations. (a) Between  $R_L = 8.6 \Omega$  and  $R_L = 9.6 \Omega$ . (b) Between  $R_L = 9.6 \Omega$  and  $96 \Omega$ . Vertical :  $v_O$  10 V/div,  $v_{S1}$  100 V/div, Horizontal : 20 ms/div.

of the implemented circuit. In the converter implementation, SCT3120AL SiC MOSFETs of ROHM Semiconductor and STPS30120DJF Power Schottky diodes of STMicroelectronics were used as the switching devices, whose permissible voltages are 650 V and 120 V, respectively. Additionally, the IR2011 of Infineon Technologies was adopted as the MOSFET driver. For the input inductances implementations, we used the powder core #2 of Micrometals. Also, the FM controller was implemented in the TMS320F28379D Dual-Core Delfino Microcontroller of Texas Instruments.

Figure 11 shows the experimental and numerical waveforms. The waveforms were measured by the Tektronix MDO4014B-3 oscilloscope. From Fig. 11, it can be seen to agree on the experimental waveforms with the numerical waveforms quantitatively. Therefore, these results show the validities of the converter modeling in (9) and the numerical computations for the converter-characteristic visualizations. Additionally, it can also be confirmed from Fig. 11 that the peak value of the switch voltages was less than 2.5 times the input voltage, and the switch voltage satisfied the ZVS condition in all the cases.

Figure 12 shows efficiency, power-loss factors, operating frequency, and the normalized peak values of the switch voltages in the control range as functions of the normalized load resistance. Figure 12(a) shows the numerical and experimental power-conversion efficiency by considering the ESRs from Table 1, where the power-conversion efficiency is defined as

$$\eta = \frac{P_o}{P_I} = \frac{V_o^2}{R_L V_I I_I}, \quad (13)$$

In (13), the input current  $I_I$  is calculated as

$$I_I = \int_0^{2\pi} (i_{L11} + i_{L12}) d\theta, \quad (14)$$

In the experiments, the input voltage, input current, and the output voltage were measured by SANWA CD800a digital

multimeter. The power conversion efficiency was 92.2 % at 66.7 W and 1.01 MHz, which was the highest efficiency in the entire control range. In addition, we see from Fig. 12(b) that the dominant power-loss factor of the efficiency degradation at light loads is the power loss at ESRs of the primary coil. The narrow-range variations of the operating frequency in Fig. 12(c) meant that the output voltage was almost constant in spite of the load variations. Namely, the converter had a load-independent-like characteristic [39]. The waveform of the current flowing through the primary coil did not vary changed against the load variations because of this characteristic. Therefore, the absolute value of the power loss at the primary coil was kept at light loads. The power losses at the secondary coils could be ignored because the ESRs of the secondary coils are quite small compared with the other ESRs.

It is seen from Fig. 12(c) that the output voltage could be controlled with a slight frequency variations in all the control range. It can be confirmed from Fig. 12(d) that the peak values of the normalized switch voltages were less than 2.5 times the input voltage in the entire control range, which also agreed with the characteristic predictions in Fig. 9(b) well.

Figure 13 shows that the experimental waveforms of the output and switch voltages against the sudden load variations. We confirm from Fig. 13 that the output voltage did not show significant variations even though the load varied suddenly. That is because the implemented inverter had the load-independent-like characteristic. Additionally, it is seen that the converter could keep the rated output voltage by FM control.

## VIII. CONCLUSION

This paper has proposed a new design approach for the resonant converter with satisfying multiple conditions. As an example, we have shown the detailed design process of the FM-controlled resonant converter with the class-E inverter. By full-use the converter-characteristic-visualization

technique on the parameter space, we can design the converter with satisfying the multiple conditions, which are rated output voltage, restrictions of the peak voltage across the switch and transformer, and ZVS condition, in the entire control range. By comprehending the converter characteristics from the visualized characteristic diagrams, it is possible to obtain the proper circuit topology and component values for achieving the conditions. From the experimental results, which agreed with numerical predictions quantitatively, the validity and effectiveness of the proposed design method are shown.

## REFERENCES

- [1] E. Gurpinar and A. Castellazzi, "Single-phase T-type inverter performance benchmark using Si IGBTs, SiC MOSFETs, and GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7148–7160, Oct. 2016.
- [2] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett, and B. J. Blalock, "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, Feb. 2016.
- [3] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 v GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.
- [4] R. L. Steigerwald, "High-frequency resonant transistor DC–DC converters," *IEEE Trans. Ind. Electron.*, vols. IE–31, no. 2, pp. 181–191, May 1984.
- [5] M. K. Kazimierczuk and C. Wu, "Frequency-controlled series-resonant converter with synchronous rectifier," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 33, no. 3, pp. 939–948, Jul. 1997.
- [6] X. Xie, J. Zhang, C. Zhao, Z. Zhao, and Z. Qian, "Analysis and optimization of LLC resonant converter with a novel over-current protection circuit," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 435–443, Mar. 2007.
- [7] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle, and W. G. Dunford, "An LLC resonant DC–DC converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5437–5445, Dec. 2013.
- [8] G. Chen, H. Li, X. Sun, J. Zhou, and L. Bai, "Analysis and design of LLC converter based on SiC MOSFET," in *Proc. 13th IEEE Conf. Ind. Electron. Appl. (ICIEA)*, May 2018, pp. 2158–2297.
- [9] H. Wen, J. Gong, X. Zhao, C.-S. Yeh, and J.-S. Lai, "Analysis of diode reverse recovery effect on ZVS condition for GaN-based LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11952–11963, Dec. 2019.
- [10] M. K. Kazimierczuk, "Class-D voltage-switching MOSFET power amplifier," *IEE Proc. B Electr. Power Appl.*, vol. 138, no. 6, pp. 285–296, Nov. 1991.
- [11] X. Wei, H. Sekiya, T. Nagashima, M. K. Kazimierczuk, and T. Suetsugu, "Steady-state analysis and design of Class-D ZVS inverter at any duty ratio," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 394–405, Jan. 2016.
- [12] Y. Nagata, Y. Yamada, Y. Fukumoto, T. Ikenari, X. Wei, T. Suetsugu, and H. Sekiya, "The phase-controlled class-D ZVS inverter with current protection," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2017, pp. 2176–2183.
- [13] M. Mikotajewski, "Class d synchronous rectifiers," *IEEE Trans. Circuits Syst.*, vol. 38, no. 7, pp. 694–697, Jul. 1991.
- [14] C. Ekkaravarodome, V. Chunkag, K. Jirasereamornkul, and M. K. Kazimierczuk, "Class-D Zero-Current-Switching rectifier as power-factor corrector for lighting applications," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4938–4948, Sep. 2014.
- [15] S. Park and J. M. Rivas, "Design of a class-DE rectifier with shunt inductance and nonlinear capacitance for high-voltage conversion," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2282–2294, Mar. 2018.
- [16] N. O. Sokal and A. D. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 3, pp. 168–176, Jun. 1975.
- [17] T. Nagashima, X. Wei, H. Sekiya, and M. K. Kazimierczuk, "Power conversion efficiency of class-E power amplifier outside nominal operation," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 749–752.
- [18] L. Roslaniec, A. S. Jurkov, A. A. Bastami, and D. J. Perreault, "Design of single-switch inverters for variable Resistance/Load modulation operation," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3200–3214, Jun. 2015.
- [19] K. Peng and E. Santi, "Class e resonant inverter optimized design for high frequency (MHz) operation using eGaN HEMTs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2015, pp. 2469–2473.
- [20] S. Saito, S. Mita, H. Onishi, S. Nagaoka, T. Uematsu, and H. Sekiya, "Frequency-controlled resonant converter with push-pull Class-E inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2019, pp. 1635–1640.
- [21] D. Kawamoto, H. Sekiya, H. Koizumi, I. Sasase, and S. Mori, "Design of phase-controlled class E inverter with asymmetric circuit configuration," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 10, pp. 523–528, Oct. 2004.
- [22] T. Nagashima, X. Wei, T. Suetsugu, M. K. Kazimierczuk, and H. Sekiya, "Waveform equations, output power, and power conversion efficiency for Class-E inverter outside nominal operation," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1799–1810, Apr. 2014.
- [23] A. Mediano and N. O. Sokal, "A class-E RF power amplifier with a flat-top transistor-voltage waveform," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5215–5221, Nov. 2013.
- [24] S. Aldhaher, D. C. Yates, and P. D. Mitcheson, "Modeling and analysis of class EF and class E/F inverters with series-tuned resonant networks," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3415–3430, May 2016.
- [25] E. Chung, K.-H. Lee, Y. Han, and J.-I. Ha, "Single-switch high-frequency DC–DC converter using parasitic components," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3651–3661, May 2017.
- [26] Z. Zhang, X.-W. Zou, Z. Dong, Y. Zhou, and X. Ren, "A 10-MHz eGaN isolated class- $\phi_2$  DCX," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2029–2040, Mar. 2017.
- [27] R. Redl, B. Molnar, and N. O. Sokal, "Class e resonant regulated DC/DC power converters: Analysis of operations, and experimental results at 1.5 MHz," *IEEE Trans. Power Electron.*, vols. PE–1, no. 2, pp. 111–120, Apr. 1986.
- [28] K.-H. Liu and F. C. Y. Lee, "Zero-voltage switching technique in DC/DC converter," *IEEE Trans. Power Electron.*, vol. 5, no. 3, pp. 293–304, Feb. 1990.
- [29] W.-J. Gu and K. Harada, "A circuit model for the class e resonant DC-DC converter regulated at a fixed switching frequency," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 99–110, Jan. 1992.
- [30] I. Boonyaroonate and S. Mori, "Analysis and design of class e isolated DC/DC converter using class e low dv/dt PWM synchronous rectifier," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 514–521, Jul. 2001.
- [31] N. Bertoni, G. Frattini, R. G. Massolini, F. Pareschi, R. Rovatti, and G. Setti, "An analytical approach for the design of Class-E resonant DC–DC converters," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7701–7713, Nov. 2016.
- [32] S. Park and J. Rivas-Davila, "Duty cycle and frequency modulations in Class-E DC–DC converters for a wide range of input and output voltages," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10524–10538, Dec. 2018.
- [33] A. Ayachit, F. Corti, A. Reatti, and M. K. Kazimierczuk, "Zero-voltage switching operation of transformer Class-E inverter at any coupling coefficient," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1809–1819, Mar. 2019.
- [34] K.-H. Lee and J.-I. Ha, "Resonant switching cell model for high-frequency single-ended resonant converters," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11897–11911, Dec. 2019.
- [35] T. Nagashima, X. Wei, T. Kousaka, and H. Sekiya, "Bifurcation analysis of the class-E inverter for switching-pattern derivations," *IEICE Commun. Exp.*, vol. 1, no. 1, pp. 33–39, Jun. 2012.
- [36] F. Pareschi, N. Bertoni, M. Mangia, R. Rovatti, and G. Setti, "A unified design theory for Class-E resonant DC–DC converter topologies," *IEEE Access*, vol. 7, pp. 83825–83838, 2019.
- [37] H. Sekiya, T. Ezawa, and Y. Tanji, "Design procedure for class e switching circuits allowing implicit circuit equations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3688–3696, Dec. 2008.
- [38] Sanken Electric Co., "Switching power supply," U.S. Patent 015 725, Feb. 17, 2005.
- [39] D. S. Silvio, *LLC Resonant Half-Bridge Converter Design Guideline*. Coppell, TX. Disponivel: STMicroelectronic, 2007. [Online]. Available: [http://www.st.com/st-webui/static/active/en/resource/technical/document/application\\_note/CD001143244](http://www.st.com/st-webui/static/active/en/resource/technical/document/application_note/CD001143244)



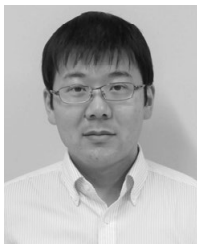
**SHOHEI SAITO** (Student Member, IEEE) was born in Chiba, Japan, in April 1995. He received the B.E. degree from Chiba University, Japan, in 2018. His research interests include class-E inverter and dc/dc converter.



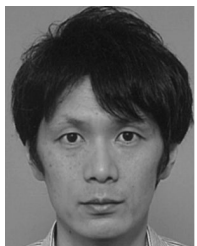
**SHOHEI MITA** (Student Member, IEEE) was born in Gunma, Japan, in November 1994. He received the B.E. and M.S. degrees from Chiba University, Japan, in 2017 and 2019, respectively. His research interests include dc/ac inverters, dc/dc converters, and wireless power transfer systems.



**WENQI ZHU** (Student Member, IEEE) received the B.E. degree from the School of Electric Engineering and Automation, Anhui University, China, in 2016. Since October 2018, he has been a Graduate Student with the Graduate School of Advanced Integration Science, Chiba University, Japan. His current research interests include dc/dc, ac/dc power converters, and wireless power transfer systems.



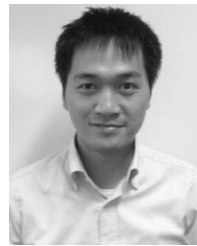
**HIROYUKI ONISHI** received the B.E. and M.S. degrees in engineering science from Osaka University, Japan, in 2007 and 2009, respectively. In 2009, he joined the OMRON Corporation. He is working on development and EMI analysis of ac/dc converter.



**SHINGO NAGAOKA** received the B.S. and M.S. degrees in engineering from the University of Tsukuba, Ibaraki, Japan, in 2001 and 2003, respectively. He is currently with OMRON Corporation, Kyoto, Japan.



**TAKESHI UEMATSU** received the B.E. degree in precision mechanical engineering from Tokyo Denki University, Japan, in 1986, the M.S. degree in electronics and computer science from Tsukuba University, Japan, in 1992, and the Ph.D. degree in information science and electrical engineering from Kyusyu University, Japan, in 2011. In 2017, he joined the OMRON Corporation. He has more than 30 years of experience in developing ac/dc and dc/dc converter.



**KIEN NGUYEN** (Senior Member, IEEE) received the B.E. degree in electronics and telecommunication from the Hanoi University of Science and Technology (HUST), Vietnam, in 2004, and the Ph.D. degree in informatics from the Graduate University for Advanced Studies, Japan, in 2012. He is currently an Assistant Professor with the Graduate School of Science and Engineering, Chiba University. His research covers a wide range of topics, including the Internet, the Internet of

Things technologies, and wired and wireless communication. He has published more than 80 publications in peer-reviewed journals and conferences, several submitted patents, and Internet drafts. He is a member of IEICE. He also involves in IETF activities.



**HIROO SEKIYA** (Senior Member, IEEE) was born in Tokyo, Japan, in July 1973. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Keio University, Yokohama, Japan, in 1996, 1998, and 2001, respectively. Since April 2001, he has been with Chiba University, Chiba, Japan, where he is currently a Professor with the Graduate School of Science and Engineering. His research interests include high-frequency high-efficiency tuned power amplifiers, resonant dc/dc power converters, dc/ac inverters, and digital signal processing for wireless communications. He is a Senior Member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan, and a member of Institute of Electronics, Information Processing Society of Japan (IPSJ) and the Research Institute of Signal Processing (RISP), Japan.

...