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A Low-Profile 36-Element K-Band Active Phased Array for Ultra-Small Aperture Application

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ABSTRACT This paper presents a 36-element low-profile half-duplex K-band T/R phased array as a solution for the platform with limited aperture and space for the phased array. With the solution of micro-assembly presented in this paper, the height of the array is only 12.3 mm. To improve the phased array's performance in ultra-small aperture, multi-channel GaAs MMICs have been applied in this work. The array's scan angle could achieve ±50° in both azimuth (H-plane) and elevation (E-plane). The EIRP and G/T of the array are 51dBm and -12.5dB/K respectively at the bandwidth from 21.5 GHz to 22 GHz.

INDEX TERMS GaAs, half-duplex, K-band, low-profile, micro-assembly, multi-channel MMIC, phased array, ultra-small aperture.

I. INTRODUCTION

Due to phased array's outstanding performance and its rapid development, the Active Electronically Scanned Array (AESA) has been widely utilized in advanced military equipment [1]–[6]. In recent years, with the development of Satcom and 5G communication technology, phased arrays have become a fundamental technology for commercial applications [7]–[13]. In modern communication systems, phased arrays operated in millimeter wave are required to be more compact in order to adapt to space-limited platforms, such as the QTM052 antenna module designed by Qualcomm for mobile devices [14]. The phased array based on CMOS or SiGe technology and multi-layer PCB technology has become one of the most popular solutions for compact sizing requirements [15]–[18]. In 2013, Phasor Solutions Ltd. demonstrated this approach in a Ku-band Satcom-on-the-move platform [19]. However, the phased array based on CMOS technology struggles to meet satisfactory performance when the aperture is limited. For example, the datalink of Unmanned Aerial Vehicles (UAVs) requires the phased array to not only be compact in size, but also process at high performance levels to establish long distance network. In order to avoid the drawbacks of CMOS, some scholars have applied both GaAs and CMOS technology in array design [20]–[22], which significantly increases the complexity and cost of the array design. In this paper, a low-profile phased array based on GaAs MMICs is presented as a solution for platform with limited aperture and space for antenna. The K-band phased array as shown in Fig. 1 can scan to ±50° and achieve an EIRP of 51 dBm.

Section II introduces the architecture of the phased array. Section III presents the package solution of phased array. Section IV presents the GaAs MMICs used in this work and their measurement result. Section V introduces the simulation results of element antenna and transition circuit in this array. Finally, Section VI thoroughly discusses the antenna's performance in Rx and Tx mode.

II. PHASED ARRAY ARCHITECTURE

As shown in Fig. 2, the phased array consists of four main units: The Array Antenna Unit (AAU), the RF Unit (RFU), the Antenna Control Unit (ACU) and the Power Supply Unit (PSU). The AAU is a microstrip antenna array made by RO5880 substrate, which is shown in Fig. 1.

The main functions of the RFU are RF signal amplification, phase and amplitude modulation and switching between Tx and Rx modes. As the radio architecture shows in Fig. 4, the RFU consists of 20 dual-channel transceiver chips, 9 quad-channel beamformer chips, a 36-way distribution feed network and a transition circuit for each channel. Particularly, two of the dual-channel transceiver chips are applied as driver amplifiers for both Tx and Rx modes. Because the number 36 is not a power of 2, the feed network is constructed by several different power dividers (PD). All the power dividers with their power division ratios (PDR) are

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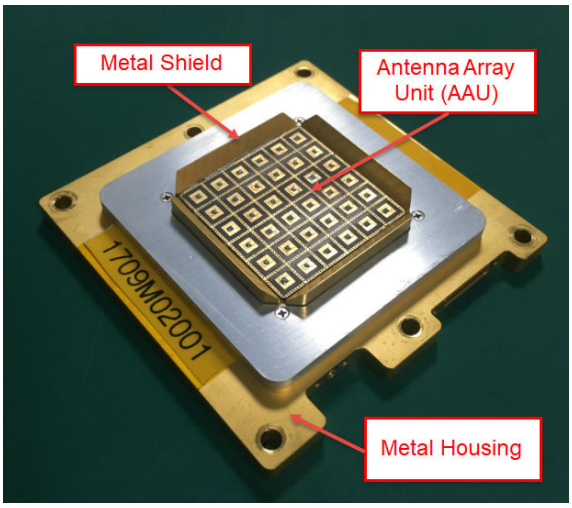

FIGURE 1. A K-band 36-element phased array.

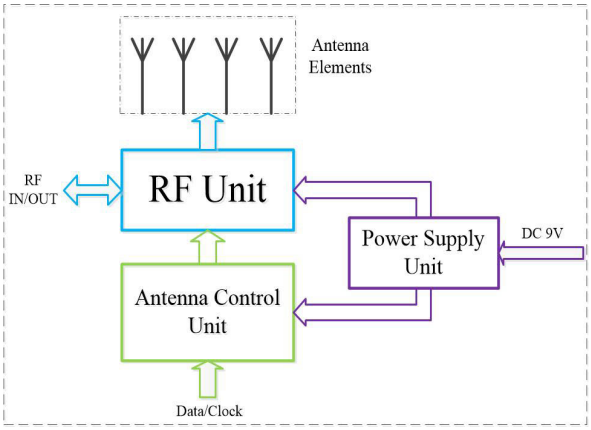

FIGURE 2. Block diagram of phased array.

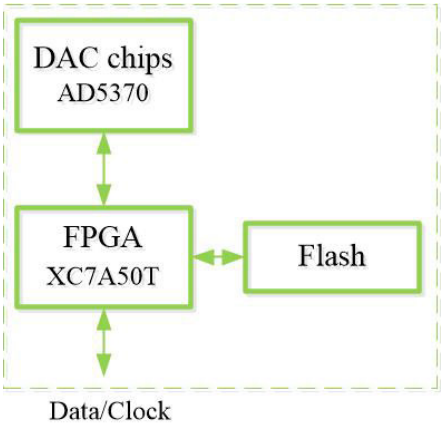

FIGURE 3. Block Diagram of Antenna Control Unit (ACU).

illustrated in Fig. 4. The PDR of two 2-way unequal dividers (PD1, PD3) are 4:5 and 3:2 respectively.

Fig. 3 shows the block diagram of the Antenna Control Unit (ACU). In this work, the ACU completes the beam scanning procedure as follow: first, the FPGA in the ACU calculates each channel's phase and amplitude; then it searches the value of the control voltage for each channel's VM from the database stored in FLASH, which saves data from the VM's response to different voltage; the FPGA sends commands to the DACs to output voltage to the quad-channel beamformer; finally, the VM in the quad-channel beamformer changes the phase or amplitude as expected.

The Power Supply Unit (PSU) is designed to convert the input 9V into the required DC voltage.

III. ASSEMBLY PROCESS OF PHASED ARRAY

The K-band phased array as shown in Fig. 1 is assembled mainly by micro-assembly technology. The first step of assembly, as shown in Fig. 5, involves attaching the MMICs chips, 36-way feed network and microstrip lines of transition circuit on metal housing with silver epoxy. The power dividers of feed network and microstrip lines of transition are all implemented by thin film circuit technology. The substrate of thin film circuit is Al_2O_3 of which relative permittivity is 9.8. And the thickness of substrate is 0.254 mm. Other 50ohm transmission lines of the feed network is made by 0.127 mm Roger 5880. The MMICs and all the passive devices are connected by bonding wire.

As shown in Fig. 6, the PCB, in which the ACU and PSU are integrated is attached above the RFU by silver epoxy. The MMICs and PCB are also interconnected by bonding wire, as shown in Fig. 7. According to this assembly method, no connectors for interconnection between different function units need to be applied. As a result, the height and weight of the array has been substantially decreased.

Furthermore, in order to adapt to harsh environments and to facilitate long-term storage, the phased array is hermetic. All the electronic devices are sealed inside the metal housing by laser welding. The passive antenna array is connected with MMICs by hermetic glass beads as shown in Fig. 8. The glass beads also act as a coaxial line for transmitting the signal vertically.

After assembly, the final height of the phased array is only 12.34 mm with a 1 mm Antenna Array Unit and 11.34 mm metal housing as shown in Fig. 9.

IV. MULTI-CHANNEL GaAs MMICs

This section describes the architecture and performance of two multi-channel GaAs MMICs applied in this work.

To achieve better performance in a limited aperture, applying a wide-bandgap (WBG) semiconductor such as GaAs or GaN is a reasonable solution. MMICs in this work are fabricated in the Win Semiconductor 0.15um GaAs process. Since the GaAs MMIC has lower integration than CMOS, multi-channel chips are proposed to improve the GaAs MMIC's integration, to some extent. For example, the extra space required for wafer dicing between two TR chips is not necessary. Furthermore, less chips need to be assembled, so the time spent in micro-assembly is reduced.

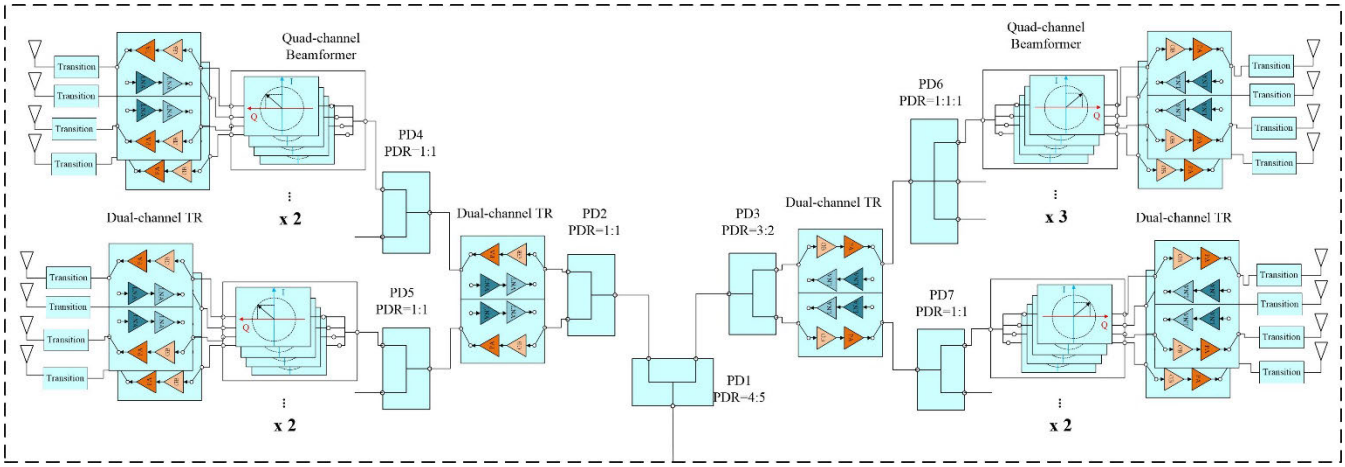

FIGURE 4. Radio Architecture of the phased array.

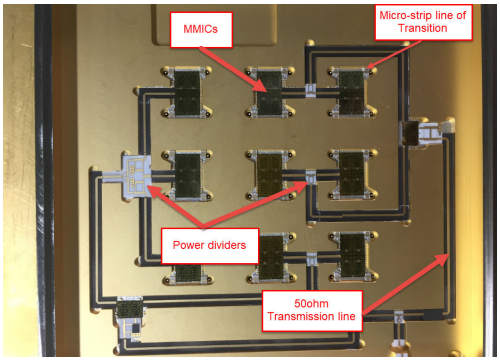

FIGURE 5. RF Unit attached on the bottom of metal housing.

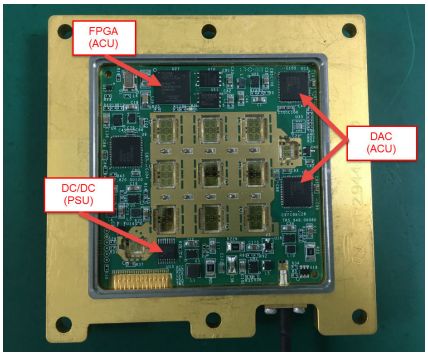

FIGURE 6. Inside view of the phased array.

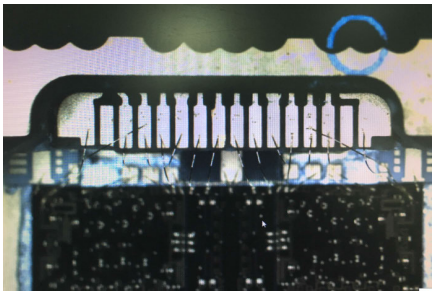

FIGURE 7. Gold bonding wire between PCB and MMICs.

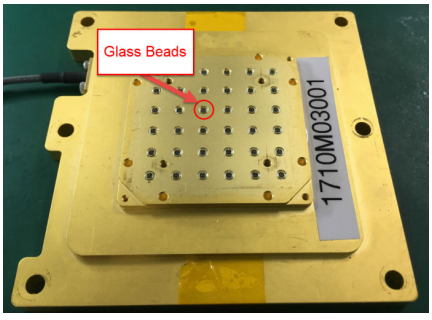

FIGURE 8. Glass beads for hermetic seal and interconnection.

The size of dual-channel transceiver and quad-channel beamformer chip are 4 mm × 2.7 mm and 4 mm × 1.6 mm respectively. Thus, the chip area for each TR channel is about 7 mm^2.

A. DUAL-CHANNEL TRANSCEIVER CHIP

The dual-channel TR chip shown in Fig. 10 has three basic function blocks: the Rx Low-Nosie Amplifier, the Tx Power Amplifier and the Rx/Tx switch.

As shown in Fig. 10, the dual-channel transceiver chip consists of one TR channel and its mirrored copy. The advantage of a mirrored copy is that the receiver circuit of two channels share the same pad of power supply, and the chip size is further reduced.

Figure 11 shows the measured S-parameters under Rx mode.

The Rx gain is higher than 22 dB from 21.5 GHz to 22 GHz. The S11 is below −13 dB and the S22 is below −8.5 dB in the band width of interest. The measured NF (noise figure) is below 4.5 dB, as shown in Fig. 12.

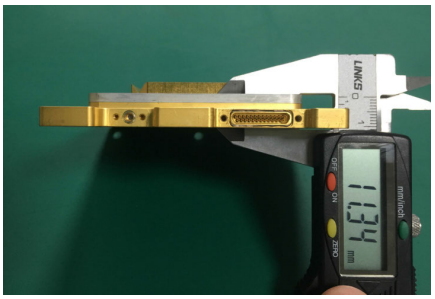

FIGURE 9. measured thickness of metal housing of phased array.

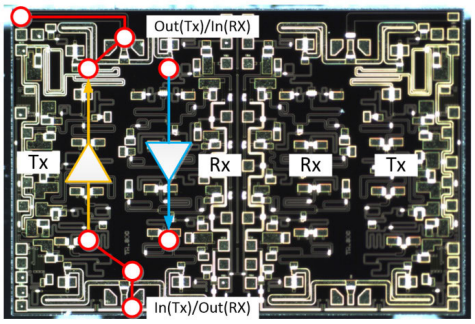

FIGURE 10. Dual-channel TR chip.

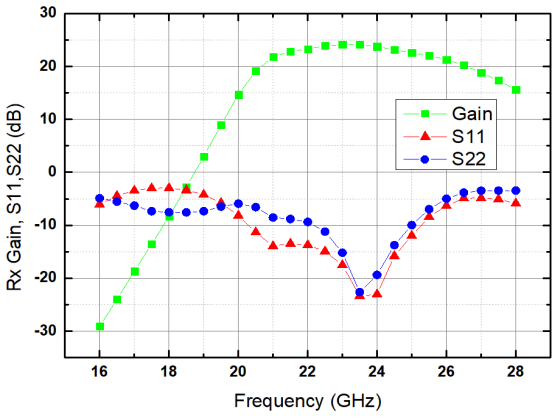

FIGURE 11. Measured S-parameter of dual-channel transceiver chip in Rx mode.

The insertion loss of switch and the loss caused by the microstrip line at the input port of Rx significantly deteriorates the LNA's performance by more than 1.5 dB.

The S-parameter in Tx mode and the measured output power from 21.5 GHz to 22 GHz are illustrated in Fig. 13 and Fig. 14 respectively. The chip's Tx gain is approximately 33 dB. The S11 and S22 of Tx are both below -15 dB. At the bandwidth of interest, the output power at 3 dB compression point is more than 19 dBm and the power-added efficiency (PAE) is higher than 25%, as shown in Fig. 14.

B. QUAD-CHANNEL BEAMFORMER

The quad-channel beamformer integrates four identical reflection-type vector modulators [23], which are connected by a 1:4 Wilkinson power divider as shown in Fig. 15. The vector modulator (VM) is not only compact in size, but also can adjust both phase and amplitude.

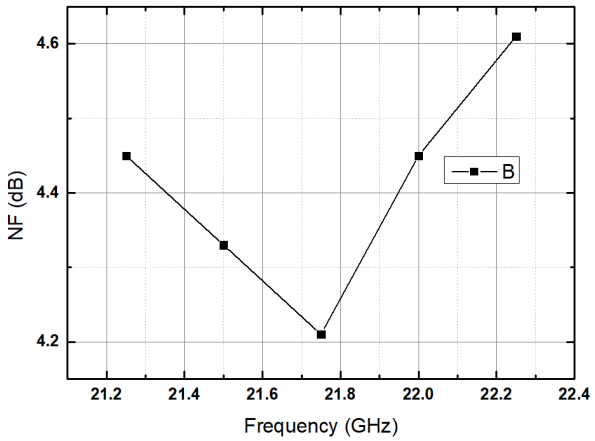

FIGURE 12. Measured NF in Rx mode.

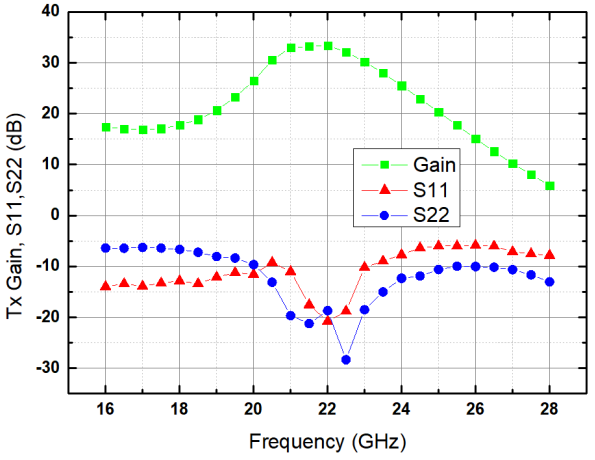

FIGURE 13. Measured S-parameter of dual-channel transceiver chip in Tx mode.

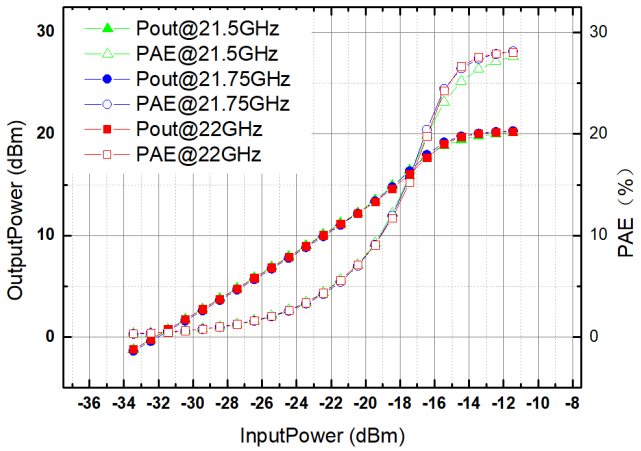

FIGURE 14. Measured output power and PAE in Tx mode.

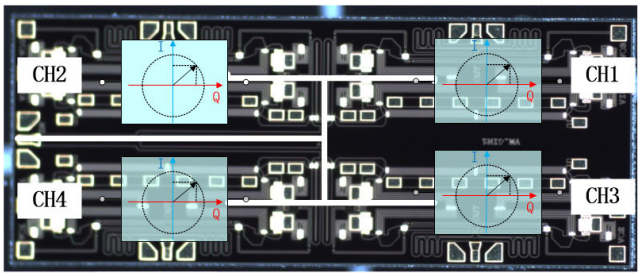

FIGURE 15. Quad-channel beamformer chip.

The measured constellation of the quad-channel beamformer at 21.75 GHz is shown in Fig. 16.

The constellation in Fig. 16 is a map that records the VM's phase and amplitude's responses to control voltages from -2 V to 0 V with a step of 50 mV. From the measured results, we find that phase variation of the test data with different amplitude levels achieves 360deg. However, not all the area covered by the test data is available. The amplitude of phase shifters is required to be constant when the phase changes. Consequently, only the data forming an entire concentric circle in constellation is available, as in the red and yellow circles shown in the CH1 constellation. The red circle demonstrates that the VM can be equivalent to a phase shifter with −20 insertion loss. Moreover, the phase variation of VM is continuous. Thus, the VM phase shifter is able to achieve any phase resolution. The red circle is the largest circle that can be achieved in the constellation of CH1. Therefore, only the data from the area inside the red circle is available. The yellow circle inside the red one demonstrates that the VM also has the ability to attenuate its amplitude. For example, if we applied the data in the yellow circle, the attenuation of the VM is 5 dB.

The constellation differences among CH1, CH3, CH2 and CH4 are shown in Fig. 17. This problem might be caused by an undesirable coupling between the 1:4 Wilkinson power divider and the VM of CH2 and CH4. Although the VM can be equivalent to a digital phase shifter with any resolution, it is practical to apply the VM as a 6-bit phase shifter. Obviously, as shown in Fig. 16, there isn't enough data to fulfill a 6-bit phase shifter when the control voltage step is 50mV. Therefore, it's necessary to change the step of control voltage from 50mV to 5mV and the related constellation is shown in Fig. 18.

V. SIMULATION OF ANTENNA ELEMENT AND TRANSITION BETWEEN MMIC AND ANTENNA

A. ANTENNA ELEMENT SIMULATION

The Array Antenna unit (AAU) consists of 36 U-slot microstrip patch antennas. The array applying square lattice with the spacing equal to 6.7 mm in both X and Y direction avoids the grating lobe within ±60° scanning range at the bandwidth from 21.5 GHz to 22 GHz. By considering the coupling between elements, which is not negligible, it is more exact to simulate the antenna element among array rather than an isolated antenna. The simulation model is shown

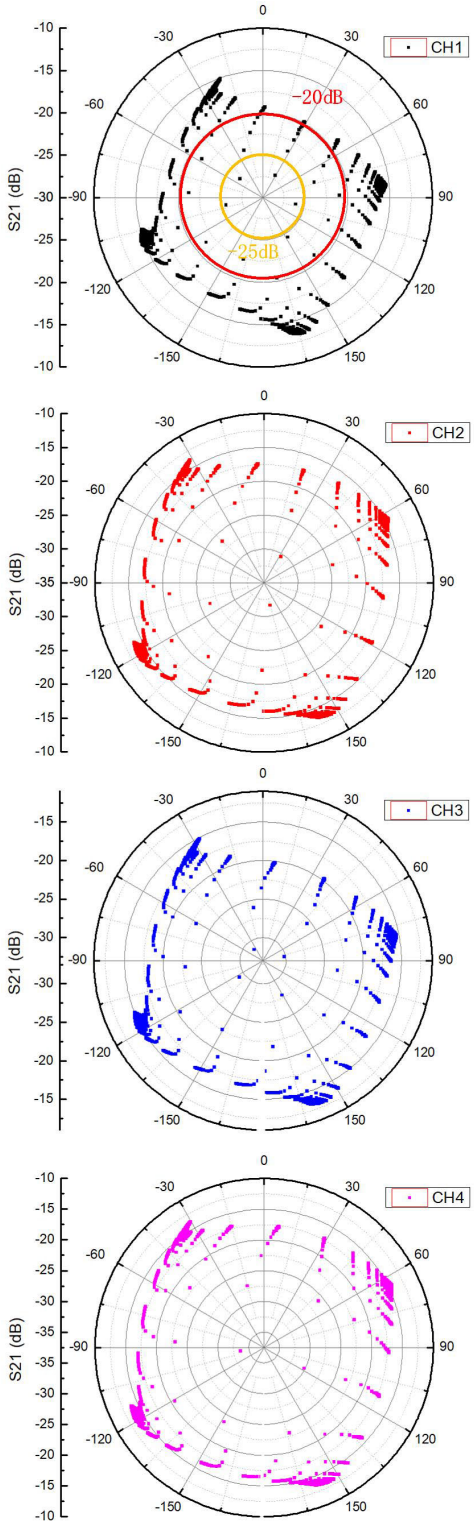

FIGURE 16. Measured constellation of the four channels of quad-channel beamformer.

in Fig. 19. The 15th U-slot micro-strip antenna element is simulated which is in the center of the array.

As shown in Fig. 20, the input return loss of the 15th element is below −15dB within 1 GHz bandwidth and the

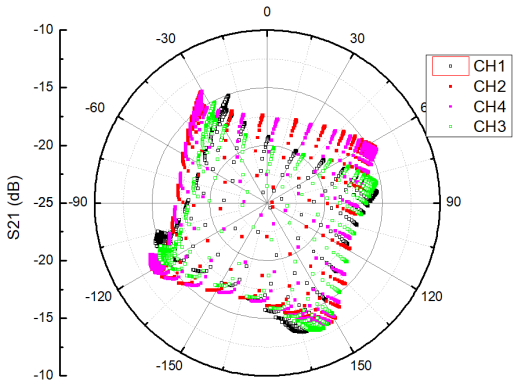

FIGURE 17. Constellation comparison among four channels.

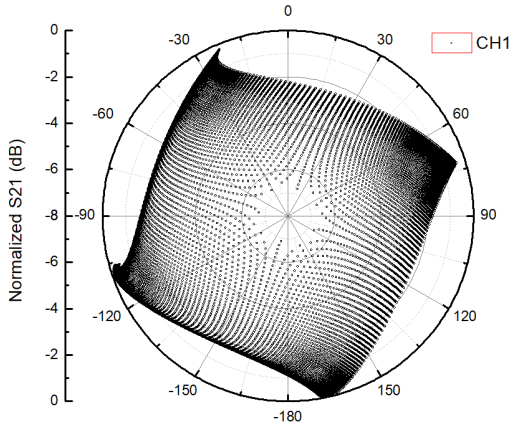

FIGURE 18. Measured constellation of CH1 with step of 5 mV.

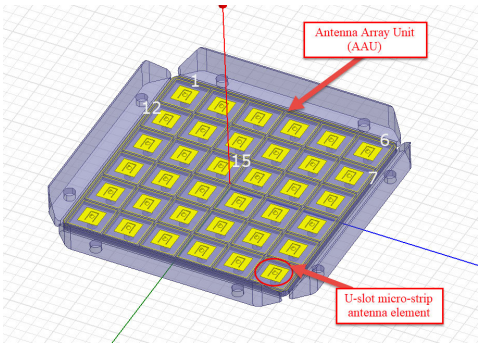

FIGURE 19. Simulation model of AAU.

pattern of the element at 21.75 GHz in E-plane and H-plane is shown in Fig. 21.

The 3dB beamwidth are 80° and 112° in E-plane and H-plane respectively. The simulated antenna gain at 21.75 GHz is approximately 4∼5 dBi.

B. TRANSITION CIRCUIT SIMULATION

The simulation model of the transition circuit is shown in Fig. 21(a). In this model, the glass bead serves as a coaxial line interconnecting the antenna element and the GaAs MMIC. A microstrip line is applied to compensate for the gap

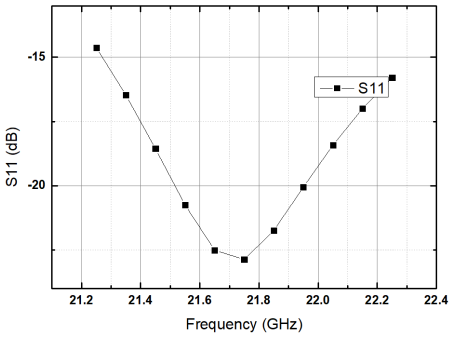

FIGURE 20. Simulated S11 of U-slot microstrip antenna element.

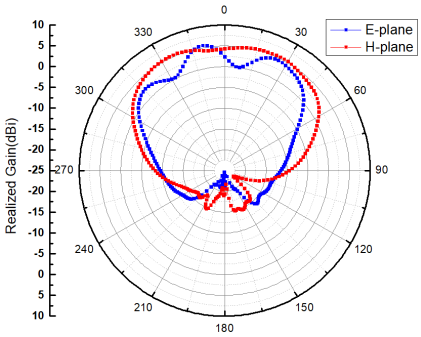

FIGURE 21. Simulated radiation pattern of element antenna in E-plane and H-plane.

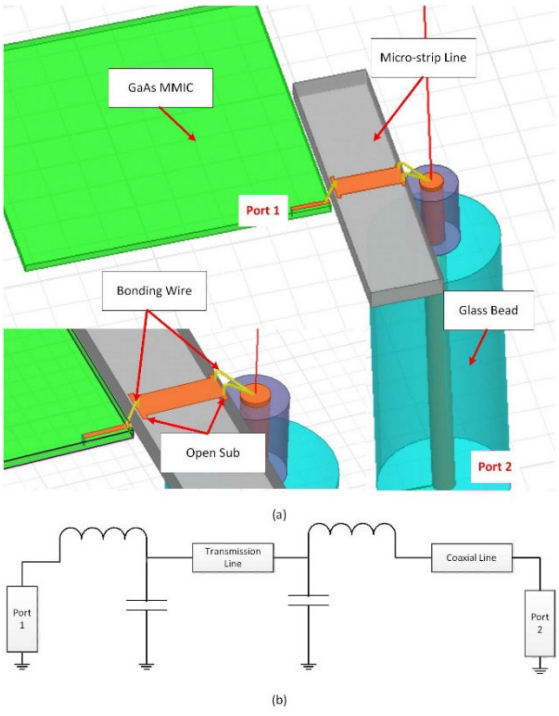

FIGURE 22. Simulation model of transition circuit (a) equivalent circuit (b).

between the inner conductor of glass bead and the MMIC. Meanwhile, in order to eliminate inductor effect introduced by bonding wire, two open stubs acting as capacitors in

TABLE 1. Performanc comparison with prior art.

	This work	Kibaroglu [15]	Nakagawa [22]	Dunworth [26]	Sadhu [13]
Process	0.15umGaAs	0.18um SiGe BiCMOS	0.15um GaAs and 65nm CMOS	28nm CMOS	0.13um SiGe BiCMOS
Frequency (GHz)	21.5~22	28-32	27.5-29.5	28	27.2-28.7
Elements in array	36TRX	64 TRX	256 TRX	24 TRX	64 TRX
E-/H-plane scan (°)	±50/±50	±25/±50	±12/±45	±12/±45	±50/±50
EIRP at Psat (dBm)	51.8	52	not mentioned	35	54
system NF (dB)	6.2	7.5	> 3.5	4.7	6

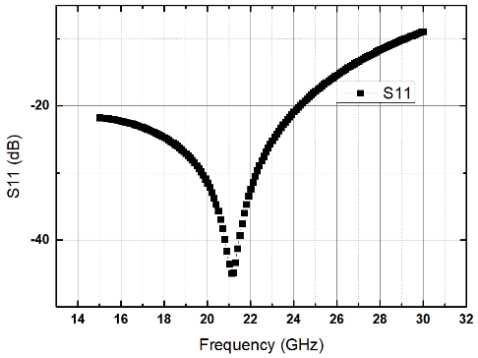

FIGURE 23. Simulated S11 of transition circuit.

parallel are added at both ends of the microstrip line. The equivalent circuit is shown in Fig. 22(b).

The simulation result of the transition circuit is shown in Fig. 23.

From the simulation, the S11 of the transition is much lower than −20 dB at the bandwidth of interest.

VI. PHASED ARRAY PERFORMANCE CALCULATION AND MEASUREMENT

A. LINK CALCULATION

With the measurement result of the RFU and the simulation result of the AAU, the performance of the phased array can be estimated by the link calculation as shown in Fig. 24.

As shown in Fig. 24(a), if the input power of the array reaches −8 dBm, each channel can be driven to output saturated power, and the output power of each channel is 18 dBm. From the antenna simulation result, the gain of antenna is at least 4 dB. Therefore, the EIRP of the 36 elements phased array can be calculated by using Formula (1). The result is 53 dBm at boresight when the array is of uniform distribution.

$$EIRP = P_{OUT} + 10\times log_{10}N + G_{ant} + 10\times log_{10}N \quad (1)$$

in which P_{out} represents the output power of each channel. N is the number of array elements; and G_{ant} is the gain of the element antenna.

Before calculating the G/T, the system noise figure is first needed. By the method introduced in [24], a complex array with several sets and levels of combiners can be divided into simple arrays which are then replaced by a single two-port equivalent receiver section. By repeating these steps, the array system can be finally converted into a two-port equivalent receiver. All the calculation steps and each section's noise figure and gain are shown in Fig. 23(b). The system noise figure is 6.2 dB from the calculation.

Therefore, the corresponding G/T can be calculated by using Formula (2). The result is −11.3 dB/K at boresight.

$$\frac{G}{T} = G_{ant} + 10\times log_{10}N - 10 \times log_{10}(T_b + 290 \times (NF - 1))) \quad (2)$$

The T_b is the brightness temperature, which is assumed to be 290K.

B. POWER CONSUMPTION CALCULATION

The power consumption of the array comes from the RFU and the Antenna Control Unit (ACU). The power consumption of ACU is 3W. In Rx mode, the power consumption for each channel is 0.042W. By taking into account the consumption of two TR chips applied as a driver chip, the total DC consumption of the RFU is 1.68W. The final DC consumption of Rx is: (1.68+3)/0.88=5.32W where 88% is the conversion efficiency of PSU. In Tx mode, when the chip outputs saturated power, the power consumption of each channel is 0.35W and the power consumption of each driver is 0.27W. Thus, the total power consumption of the array is: (0.35 × 36+0.27 × 4+3)/0.88=18.9W.

C. CALIBRATION

The array is calibrated in the far-field anechoic chamber as shown in Fig. 25.

The REV method [25] has been applied for calibration in this work. The procedure of calibration is presented as follow:

1. In the far-field anechoic chamber, set the array in Tx (or Rx) mode. Then obtain the initial phase (φ_n) and amplitude (E_n) of each channel by the REV method.

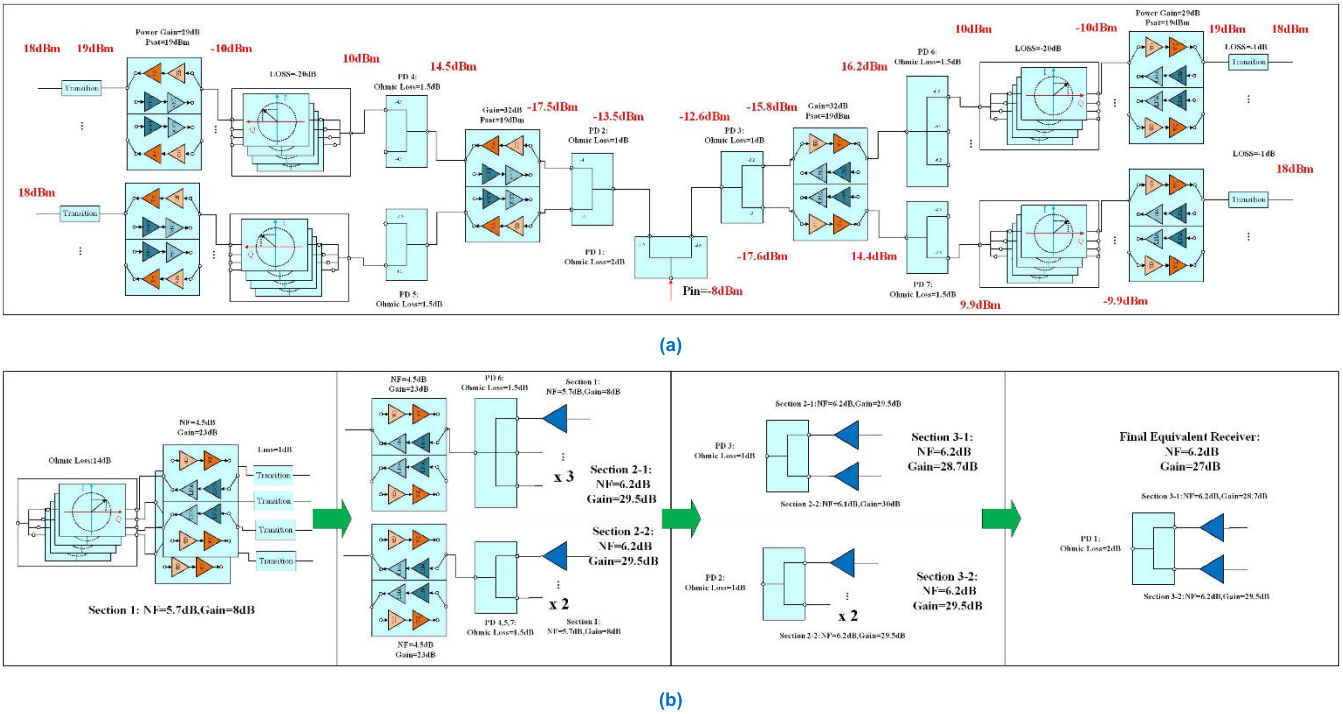

FIGURE 24. Link calculation in (a) Tx mode and (b) Rx mode.

2. For phase calibration, the first channel would be treated as a reference channel. Then, adjust the phase of the other 35 channels by the phase difference $\varphi_n - \varphi_0$.
3. For amplitude calibration, select the channel with the lowest amplitude as the reference channel. Then, attenuate the amplitude of other channels to the reference level.

The normalized results of initial phase and the amplitude of each channel at 21.75 GHz are shown in Fig. 26.

As shown in Fig. 26(a) and Fig. 26(b), the amplitude distribution of the array is quite unequal. The largest amplitude difference between different channel is more than 6 dB. There are two reasons for this problem: first, the MMIC chips used in this work have only undergone DC testing, so their rf performance is unknown before installation. Secondly, the handmade micro-assembly can cause undesirable difference, especially in mmWave frequency. Generally, both the phase and amplitude of an array should be calibrated to obtain an anticipated antenna pattern. Although amplitude calibration provides better performance on sidelobe, its influence on the array's EIRP and G/T of this work cannot be neglected. Particularly for UAV swarm communications, the communication distance is one of the most important factors and directly impacted by the antenna's EIRP and G/T. In Tx mode, the rule of amplitude calibration allows the VM of each channel to attenuate approximately 1∼8 dB. As a result, the dual-channel TR chips as driver amplifiers fail to drive most channel to output saturated power. In Rx mode, after amplitude calibration, the system noise figure decreases

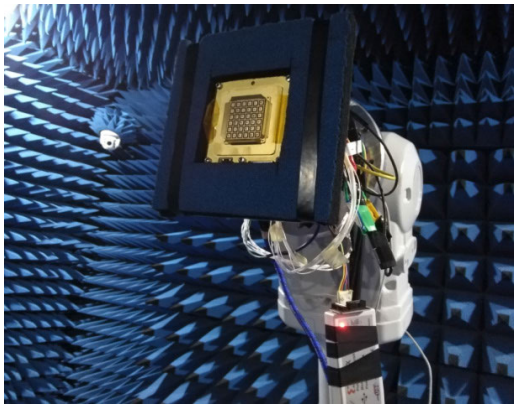

FIGURE 25. Phased array under test in far field.

approximately 0.5 dB by link calculation. The amplitude calibration has an apparent impact on the EIRP and G/T in this work. Hence, only the phase of the array is calibrated at last. The phase calibration result is shown in Fig. 27.

After calibration, the phase difference of Rx and Tx converges to 5°.

D. PATTERNS AND EIRP IN TX MODE

Fig. 28. and Fig 29. show the measured H-plane and E-plane pattern with the beam scanning from 0° to ±60° at 21.75 GHz.

The measured patterns basically agree with simulation result, especially in the H-plane. At bore sight, the measured

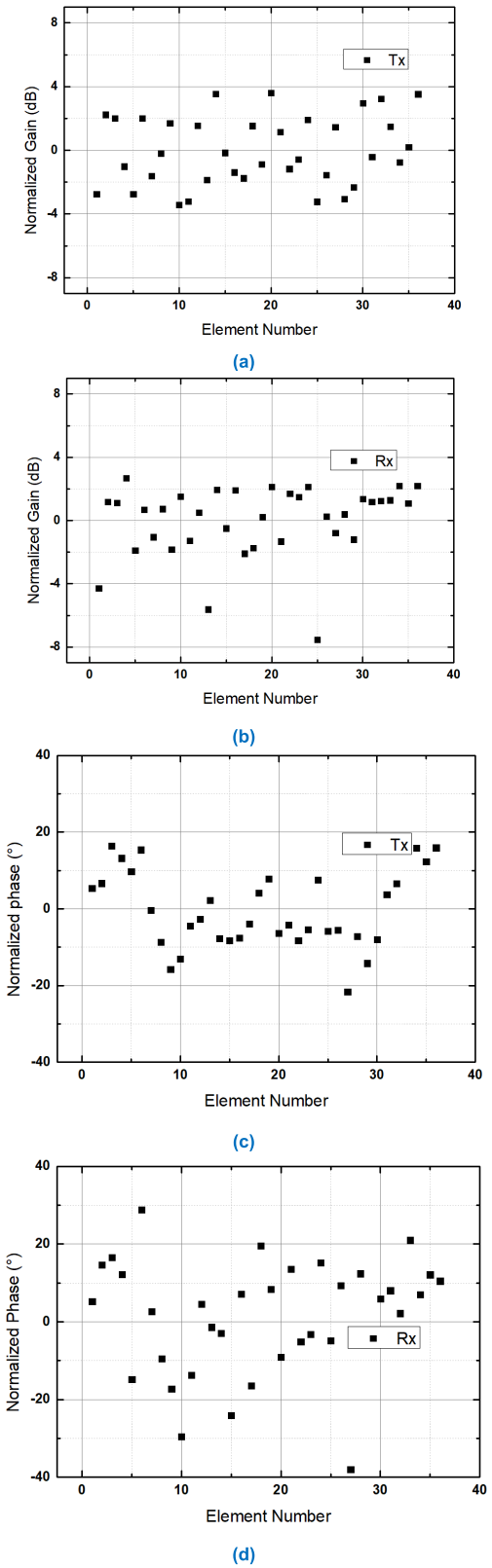

FIGURE 26. Normalized initial gain of (a) Tx and (b) Rx and normalized initial phase of (c) Tx and (d) Rx.

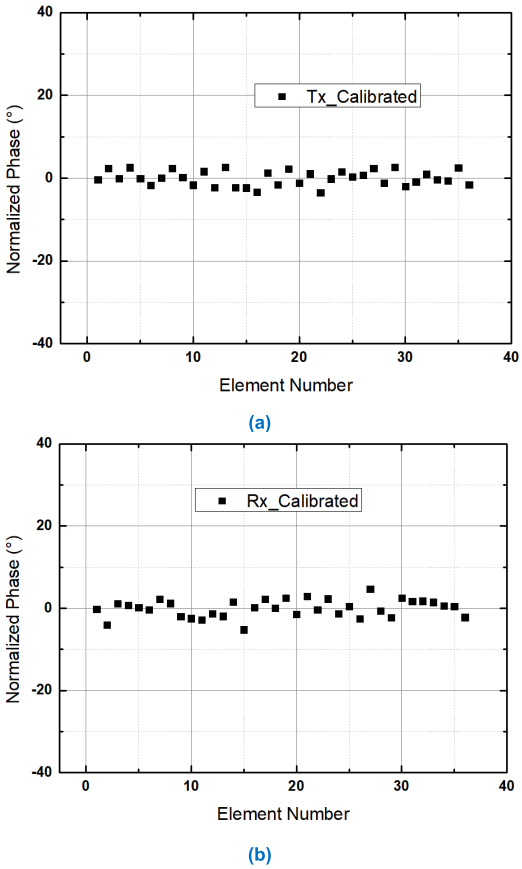

FIGURE 27. Normalized phase of (a) Tx and (b) Rx after calibration.

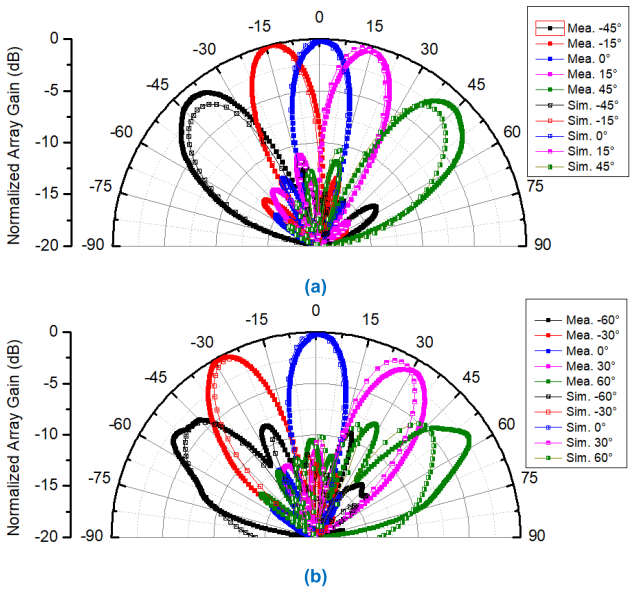

FIGURE 28. Measured patterns at (a) 0°, ±15°, ±45° and (b) 0°, ±30°, ±60° in E-plane.

3 dB beamwidth is 16° with the side lobe < -14 dB in the H-plane. In the E-plane, the measured 3 dB beamwidth is 16° with the side lobe < -12.5 dB. However, due to the limited element of phased array, the scan angle only reaches ±50° at last and the sidelobe is lower than -5 dB over all scan angles in both E-plane and H-plane.

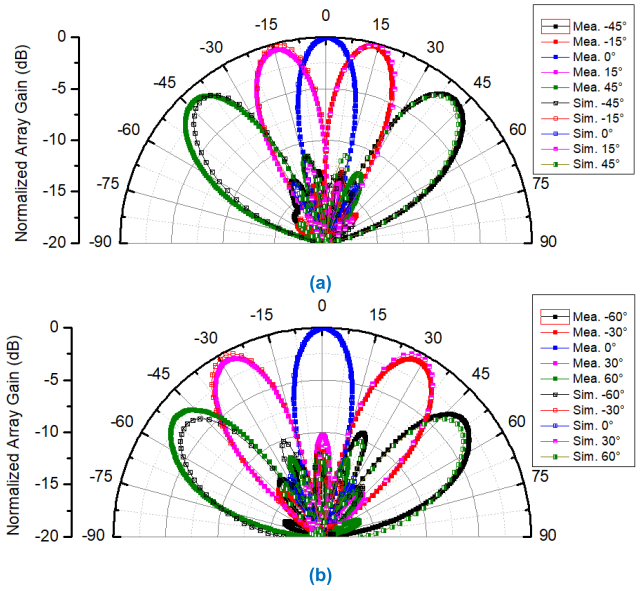

FIGURE 29. Measured patterns in Tx at (a) 0°, ±15°, ±45° and (b) 0°, ±30°, ±60° in H-plane.

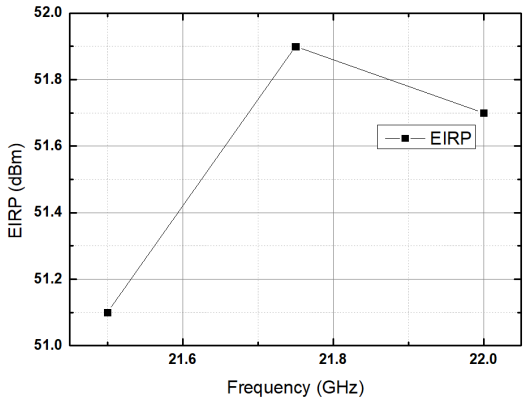

FIGURE 30. Measured EIRP from 21.5 GHz to 22 GHz.

Fig. 30 shows the measured EIRP at the bandwidth of interest. The measured EIRP is higher than 51 dBm, but lower than the link calculation result (53 dBm). The reason caused the difference is that the output power for each channel is assumed to be saturated when we calculated the EIRP in Section VI. However, the measured amplitude distribution is not uniform as anticipated. After taking into account the unequal amplitude distribution, there is about 1 dB loss due to some channels of the array are not driven into saturated operation at the same time.

E. PATTERN AND G/T IN RX MODE

As shown in Fig. 31 and Fig. 32, the scan angle at 21.57 GHz is up to ±50° in both the E-plane and H-plane. The measured 3 dB beamwidth in the E-plane is 16° with the sidelobe < -11 dB. And the measured 3 dB beamwidth in the H-plane is 16° with the sidelobe < -14.5 dB. The sidelobe is

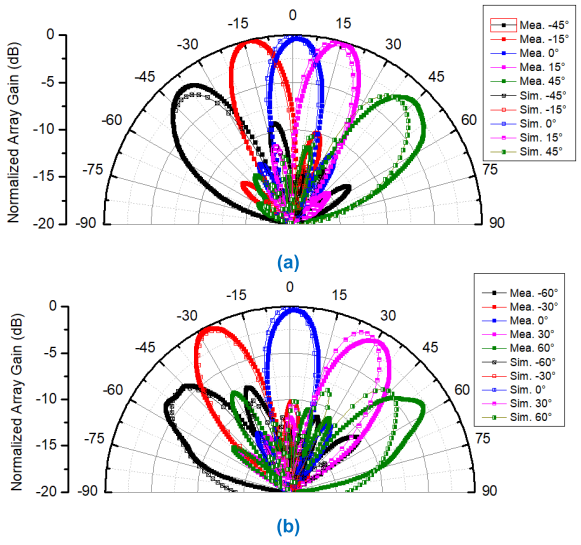

FIGURE 31. Measured patterns in Rx at (a) 0°, ±15°, ±45° and (b) 0°, ±30°, ±60° in E-plane.

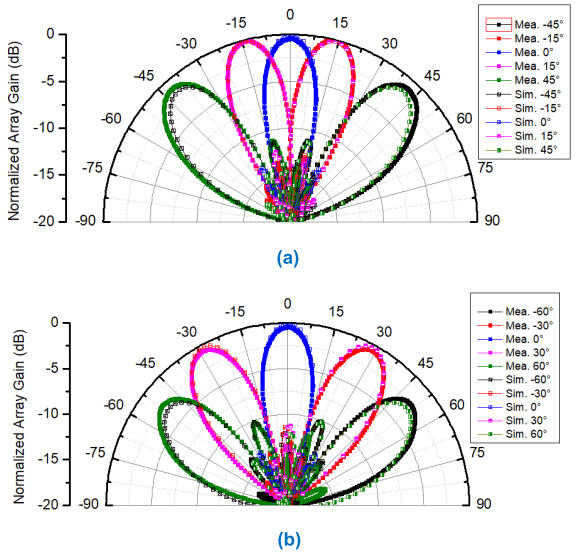

FIGURE 32. Measured patterns in Rx at (a) 0°, ±15°, ±45° and (b) 0°, ±30°, ±60° in H-plane.

lower than −4 dB over all scan angles in both the E-plane and H-plane.

As shown in Fig. 31(b), the measured result is not consistent with simulation when the beam scans to 60° in E-plane. The metal shields around the AAU (as Fig.1 shown) might be one reason for the problem. If one of the shields was not attached well with metal housing, the reflection of shield has an unpredictable impact on radiation pattern, especially when the beam scans to large angles.

The measured figure of merit (G/T) in the band width of interest is shown in Fig. 33. The measured G/T at 21.75 GHz is −11.4 dB/K which agrees well with link calculation result.

Table 1 shows the performance comparison of this work and other published phased array in K and Ka band.

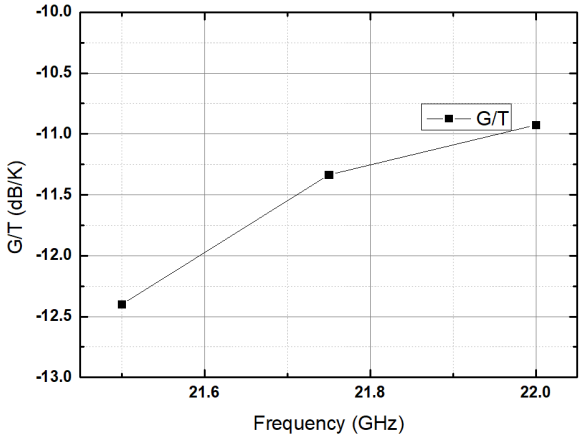

FIGURE 33. Measured G/T from 21.5 GHz to 22 GHz.

VII. CONCLUSION

This paper presents a K-band low-profile phased array in ultra-small aperture with high performance. The height of the 36-element array is only 12.3 mm. By using GaAs dual-channel TR chip and a quad-channel beamformer chip, the array achieves an EIRP of 51.8 dBm and G/T of -11.4 dB/K at boresight at 21.75 GHz. Future work is to design an 8 x 8 element scalable phased array for general application.

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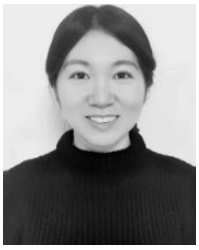

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