IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 7, 2020, accepted March 20, 2020, date of publication March 26, 2020, date of current version April 16, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2983419

A Carrier-Based Modulation With Planned Zero Sequence Voltage Injection to Control Neutral Point Voltage for Three-Level Inverter

JINPING WANG[1], (Member, IEEE), ZAIYI GUI[1], PEIXIA WANG[2], JUNCAN WANG[1], AND WEIDONG JIANG[1], (Member, IEEE)

[1]School of Electrical Engineering and Automation, Hefei University of Technology, Hefei 230009, China
[2]State Grid Feidong Power Supply Company, Feidong 231600, China

Corresponding author: Jinping Wang (waupter919@163.com)

This work was supported in part by the Fundamental Research Funds for the Central Universities of China under Grant JZ2019HGTB0074 and Grant PA2019GDPK0080, and in part by the Tianchang-Hefei University of Technology (HFUT) Industrial Innovation Lead Key Funds Project under Grant JZ2019AHDS0002.

ABSTRACT In this paper, a carrier-based modulation strategy with planned zero sequence voltage (ZSV) injection for T-type three-level inverter (TLI) is proposed to control neutral point (NP) voltage, which is simple to be implemented. This strategy is analyzed comprehensively based on the relationship between NP current and the injected ZSV in one switching cycle. The planned ZSV is calculated according to the voltage difference between upper and lower capacitors and the injectable ZSV range without over-modulation. Furthermore, in order to reduce switching losses, the closest clamping mode method is applied, in which specific ZSV is injected to form discontinuous pulse width modulation (DPWM), and the NP voltage control ability is sacrificed to some extent. In most applications of the two proposed methods, the NP voltage can be perfectly controlled almost like virtual space vector PWM (VSVPWM). However, the switching numbers of the strategy with planned ZSV injection are a third even half less than that of VSVPWM. And the switching numbers of the closest clamping mode method are even a third less than that of SVPWM. Comprehensive experiments are carried out to verify the feasibility of the proposed two methods.

INDEX TERMS Modulation strategy, neutral-point voltage oscillation, T-type three-level inverter, zero sequence voltage injection.

I. INTRODUCTION

Recently, multilevel inverters have gained more and more attentions since they are suitable for high-power and high- and/or medium-voltage industrial products [1], [2]. Multilevel inverter has superior advantages compared with the conventional two-level inverter on the better output voltage harmonic characteristic, lower voltage stress across switching devices, and improved power quality, which is widely used in new energy [3], motor drive [4] and so on. Among multilevel inverters, three-level inverter (TLI) has been widely employed, where the neutral-point-clamped and T-type are the two most commonly used TLI topologies.

In terms of three-level topology, neutral point (NP) voltage potential unbalance is an inherent drawback, which is an important factor restricted the development of TLI. The NP voltage unbalance has a serious effect on the reliability of the inverter system, which may trigger pre-designed over-voltage protection or cause serious failure of the switching devices if there is no perfect over-voltage protection. The AC ripple and DC offset are two cases of NP voltage unbalance. The AC ripple behaves with low frequency oscillation, typically with triple fundamental frequency in TLI, resulting in output voltage waveform and power quality distortion [5]. Generally, the AC ripple can be reduced by increasing DC-link capacitances, which cause the increasement of the system cost and volume. The DC offset has a greater impact on TLI. Not only the output waveform is deteriorated but also the predesigned over-voltage protection will be triggered eventually if there is a gradually increased DC offset [6]. Increasing DC-link capacitances can only prolong the time to trigger protection, but cannot overcome this problem fundamentally. Therefore,

The associate editor coordinating the review of this manuscript and approving it for publication was Meng Huang.

the control target for NP voltage of TLI can be expressed as: (1) the gradually increased DC offset must be avoided to ensure the stable and reliable work of the TLI; (2) the AC ripple should be reduced as much as possible. Thus, a well-established solution of NP voltage should provide to reduce capacitance of dc-link, reduce the system cost and improve the output voltage and current qualities.

At present, a number of NP voltage control have been proposed for TLI, which can be classified into two categories. One category is to add extra hardware equipment or controller. For instance, to maintain NP voltage constant, two isolated dc-voltage sources have been applied at the dc side [7]. In [8], the front-end circuit through back-to-back topology or three-level boost converters has been described. Nevertheless, these methods significantly increase the system complexities, costs and volumes.

Another category is to adopt the various pulse width modulation (PWM) strategies or their hybrid PWM strategies. It can be known that the most strategies aimed at NP voltage control are based on carrier-based PWM (CBPWM) [9], [10] and space vector PWM (SVPWM) [11]–[13]. The relationship between CBPWM and SVPWM can be de-scribed: an arbitrary carrier-based modulation signals can be transformed into an equivalent space vectors by injecting special zero-sequence voltage (ZSV) [14]. A method of injecting zero-sequence voltage to control the NP voltage for a neutral-point-clamped TLI is introduced [9], where the zero-sequence voltage obtained from the dual relationship between CBPWM and the nearest three-vector SVPWM can improve the sinusoidal modulation wave. However, the disadvantage of the above strategies is the NP voltage control capability greatly depending on the power factor and modulation index.

To solve the above problem, the virtual space vector de-fined by the basic space vector is used to eliminate NP voltage fluctuation in theory at any power factors and modulation indexes. An improved virtual space vector PWM (VSVPWM) based on the repartitioned space vector sectors is proposed in [15], in which only one small vector instead of redundant small vectors pairs is used to realize NP voltage precise control and balancing over the whole modulation index range. In this method, the small vector is selected according to the factor of NP voltage imbalance and direction of phase current. In addition, active NP voltage control approach is employed in VSVPWM to make TLI have the NP voltage recovery ability [6]. In order to apply the VSVPWM in a real system, the relationship between VSVPWM and CBPWM is studied in [16] to significantly simplify the calculation amount and time when VSVPWM is carried out with a carrier wave. However, the inherent drawback of VSVPWM is that the switching losses increase with the increased number of switching action.

Loss produced by switching devices is another major issue of TLI, which can be roughly divided into conduction loss and switching loss. In order to meet the high efficiency requirement, T-type TLI topology has been presented to reduce conduction loss. For the purpose of reducing switching loss, the inverter usually operates under the condition of low switching frequency and uses discontinuous pulse width modulation (DPWM) [17], [18]. Therefore, DPWM can be employed in T-type TLI to minimize losses. In [19], the proposed DPWM method for T-type TLI is carried out by adjusting medium voltage vectors, where P-type DPWM increase the NP voltage and N-type DPWM decrease the NP voltage. In this method, DPWMMAX and DPWMMIN is integrated into medium voltage vectors to generate P-type DPWM and N-type DPWM, since they possess maximum balancing capability among various DPWM methods. However, the researches on NP voltage control based on DPWM are relatively little.

It can be concluded from the above analysis that a PWM with good output performance should be satisfied the following points: i) Reduce or eliminate the NP voltage unbalance. ii) Reduce switching losses and achieve high efficiency. iii) Achieve NP voltage control over full power factor and modulation index. iv) Have simple algorithm, which is featured with short code length and execution time.

Based on the relationship between the NP current and the injected ZSV revealed in latter paper, two PWM methods to achieve NP voltage control methods have been proposed for T-type TLI. One is based on planned ZSV injection, which can achieve the maximum NP voltage balance capability. The other is based on the closest clamping mode, which can reduce the losses as much as possible. At last, the experimental results are provided to validate the feasibility of the proposed two methods.

II. ANALYSIS OF T-TYPE THREE-LEVEL INVERTERS

A. T-TYPE TLI AND ITS NP CURRENT

The topology of the three-phase T-type TLI is illustrated in Fig 1, which is composed of three AC-side inductors (L_S), three phase independent bridge leg (leg x, $x = a, b$ and c) and two DC-side capacitors (C_1, C_2). Each bridge leg consists of four controllable switching devices ($S_{x1} - S_{x4}$). It can be seen from Fig 1 that if the NP considered as reference point, three voltages, namely u_{dc}, 0, $-u_{dc}$, will be outputted depend on the switching device state, where $2u_{dc}$ is the DC-link voltage. These three voltages corresponds to the symbolized as level 1, level 0, level -1, respectively. In this paper, the current direction labeled in Fig 1 is defined as positive.

Supposed $u_{dc} = 1$, the three-phase symmetrical fundamental voltage signals u_x satisfy:

$$\begin{cases} u_a = m \sin \omega t \\ u_b = m \sin(\omega t - 2\pi/3) \\ u_c = m \sin(\omega t + 2\pi/3) \end{cases} \tag{1}$$

where ω is the angular frequency, m is the modulation index. With lagging u_x one power factor angle φ, the three-phase current i_x satisfy:

$$\begin{cases} i_a = I_m \sin(\omega t - \varphi) \\ i_b = I_m \sin(\omega t - 2\pi/3 - \varphi) \\ i_c = I_m \sin(\omega t + 2\pi/3 - \varphi) \end{cases} \tag{2}$$

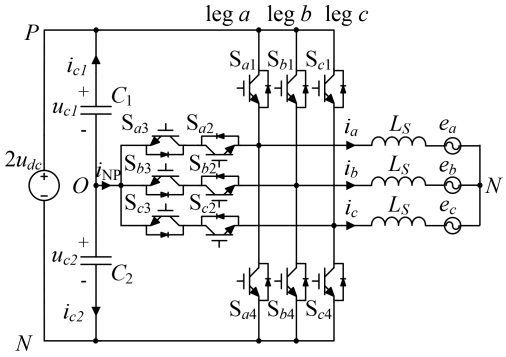


FIGURE 1. The three-phase T-type TLI.

where I_m is the amplitude of sinusoidal current signals. The rearranged u_x satisfy:

$$\begin{cases} u_{\max} = \max(u_a, u_b, u_c) \\ u_{\min} = \min(u_a, u_b, u_c) \\ u_{\text{mid}} = \text{mid}(u_a, u_b, u_c) \end{cases} \tag{3}$$

And $i_{\max}$, i_{mid} and $i_{\min}$ are defined as the phase currents corresponding to $u_{\max}$, u_{mid} and $u_{\min}$, respectively. In order to effectively control the NP voltage or achieve other control targets, the ZSV u_{ZSV} is injected into three-phase voltages usually. After u_{ZSV} being injected, the three-phase modulation voltages u'_{X}(X = max, mid, min) can be obtained as:

$$u'_{\text{X}} = u_{\text{X}} + u_{\text{ZSV}} \tag{4}$$

To avoid over-modulation, the range of u_{ZSV} can be expressed as:

$$-1 - u_{\min} \le u_{\text{ZSV}} \le 1 - u_{\max} \tag{5}$$

The following analysis takes one switching cycle as an example. When the output of one phase is level 1, the NP voltage is affected due to the phase current flowing into or from NP. The duty ratio of phase X level $1d_{\text{X1}}$ is:

$$d_{\text{X1}} = 1 - |u'_{\text{X}}| \tag{6}$$

Then, the average NP current of phase X is:

$$i_{\text{NP, X}}(m, I_m, \omega t, \varphi, u_{\text{ZSV}}) = i_{\text{X}}(1 - |u_{\text{X}} + u_{\text{ZSV}}|) \tag{7}$$

And then, the average NP current of all phases can be linearly added as:

$$i_{\text{NP}}(m, I_m, \omega t, \varphi, u_{\text{ZSV}}) = i_{\text{NP, max}} + i_{\text{NP, mid}} + i_{\text{NP, min}} \tag{8}$$

From (8), there are five variables in the function i_{NP}, including m, I_{m}, ωt, φ and u_{ZSV}, where m and ωt are determined by operating points, I_{m} and φ depend on load conditions. However, u_{ZSV} is injected according to the active NP control algorithm to realize effective NP voltage control.

In one switching cycle, the NP voltage variation Δu_{NP} caused by the NP current can be indicated as:

$$\Delta u_{\text{NP}} = -\frac{i_{\text{NP}}}{(C_1 + C_2)} T_S \tag{9}$$

TABLE 1. The redefined boundary points and demarcation points.

u_{ZSV}	u_{ZSV1}	u_{ZSV2}	u_{ZSV3}	u_{ZSV4}	u_{ZSV5}
Case 1	$-1-u_{\min}$	$1-u_{\max}$	—	—	—
Case 2	$-1-u_{\min}$	$-u_{\text{mid}}$	$1-u_{\max}$	—	—
Case 3	$-1-u_{\min}$	$-u_{\max}$	$-u_{\text{mid}}$	$-u_{\min}$	$1-u_{\max}$
i^*_{NP}	i^*_{NP1}	i^*_{NP2}	i^*_{NP3}	i^*_{NP4}	i^*_{NP5}

Equation (9) demonstrates that NP current is a key factor in NP voltage variation, where positive and negative NP current are used to decrease and increase the NP voltage, respectively.

When $I_{\text{m}} = 1$, assuming the normalized phase current, NP current and NP voltage variation are i^*_{X}, i^*_{NP} and Δu^*_{NP} in one switching cycle, respectively. To simplify the latter analysis, the normalized values are used.

B. THE VARIATION OF THE NP CURRENT WITH U_{ZSV}

The modulation voltages may change the polarity after injecting u_{ZSV}, and the relationship between i^*_{NP} and u_{ZSV} may be not linear. Assuming the maximum and minimum NP currents over the range of u_{ZSV} are i^*_{NPmax} and i^*_{NPmin}, respectively, there are three cases of i^*_{NPmax} and i^*_{NPmin} after injecting u_{ZSV}.

Case 1: $-u_{\max}, -u_{\text{mid}}, -u_{\min} \notin [-1 - u_{\min}, 1 - u_{\max}]$

In this case, the injected u_{ZSV} does not change the polarity of the modulation voltages, which indicates that i^*_{NP} has simple linear relation with u_{ZSV}. It means that i^*_{NPmax} and i^*_{NPmin} can be acquired at the boundary points.

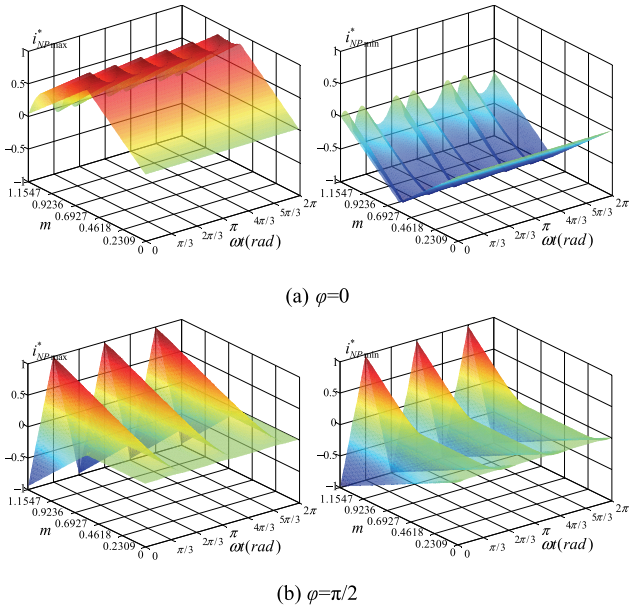
Case 2: $-u_{\text{mid}} \in [-1 - u_{\min}, 1 - u_{\max}]$

Under this case, the variation of i^*_{NP} with u_{ZSV} can be divided into two segments, which are $[-1 - u_{\min}, -u_{\text{mid}})$ and $[-u_{\text{mid}}, 1 - u_{\max}]$. In the former segment, while u_{ZSV} gradually increasing from $-1-u_{\min}$ to $-u_{\text{mid}}$, the duty ratios of level 1 of $u_{\min}$ and u_{mid} increase but that of $u_{\max}$ decreases. While $u_{\text{zsv}} = -u_{\text{mid}}$, it should be noted that the duty ratio of level 1 of u_{mid} is 100%. In the latter segment, while u_{ZSV} gradually increasing from $-u_{\text{mid}}$ to $1 - u_{\max}$, the duty ratio of level 1 of $u_{\min}$ continuously increase, but that of u_{mid} and $u_{\max}$ decrease. Therefore, $u_{\text{ZSV}} = -u_{\text{mid}}$ is the demarcation point, and on the both sides i^*_{NP} has simple linear relation with u_{ZSV}, respectively. So, i^*_{NPmax} and i^*_{NPmin} are located at the boundary points or the demarcation point.

Case 3: $-u_{\max}, -u_{\text{mid}}, -u_{\min} \in [-1 - u_{\min}, 1 - u_{\max}]$

The analysis is similar to case 2. There are three demarcation points, u_{ZSV} =-$u_{\max}$, -u_{mid}, $-u_{\min}$, respectively. As a result, the variation of i^*_{NP} with u_{ZSV} consists of four segments, which are $[-1 - u_{\min}, -u_{\max})$, $[-u_{\max}, -u_{\text{mid}})$, $[-u_{\text{mid}}, -u_{\min})$ and $[-u_{\min}, 1-u_{\max}]$. Similarly, i^*_{NP} has simple linear relation with u_{ZSV} in each segment, and i^*_{NPmax} and i^*_{NPmin} can be acquired at the boundary points or demarcation points.

For simplifying analysis, the boundary points and demarcation points are redefined according to the injected u_{ZSV}, as shown in Table 1.



(a) φ=0

(b) φ=π/2

FIGURE 2. The distribution of i^*_{NPmax} and i^*_{NPmin}.

C. NECESSARY CONDITIONS FOR KEEPING NP VOLTAGE UNCHANGED IN A SWITCHING CYCLE

Hypothesis 1: The NP voltage is balanced at the beginning of a switching cycle. If the NP voltage still keeps balance at the end of this switching cycle, there is $\Delta u^*_{NP} = 0$, which means the NP voltage is unchanged in this switching cycle. When several successive switching cycles also have this characteristic, the NP voltage can keep balancing during this interval. The necessary conditions for the establishment of this hypothesis are explained as below.

When u_{ZSV} satisfies within the range given by (5), under the condition of the same m, ωt, φ, the NP current change is only related to the injected u_{ZSV}. According to the analysis in the above section, i^*_{NPmax} and i^*_{NPmin} can be acquired at the boundary points or the demarcation points. Form (9), i^*_{NP}=0 must be established to meet the requirement Δu^*_{NP}=0.

In $[-1-u_{min}, 1-u_{max}]$, the relationship between i^*_{NP} and u_{ZSV} is linear or piecewise linear. So, if $i^*_{NPmin} \le 0 \le i^*_{NPmax}$, there must be at least one u_{ZSV}, which can satisfy i^*_{NP}=0 and Δu^*_{NP}=0. If $0 < i^*_{NPmin} < i^*_{NPmax}$ or $i^*_{NPmin} < i^*_{NPmax} < 0$, u_{ZSV}, which can satisfy i^*_{NP}=0 and Δu^*_{NP}=0, does not exist. Therefore, the possible change of NP voltage in a switching cycle can be described as the following three situations.

(1) $i^*_{NPmin} \le 0 \le i^*_{NPmax}$. If u_{ZSV} corresponding to i^*_{NPmin} is injected into modulation voltages, it makes NP voltage increase. If u_{ZSV} corresponding to i^*_{NPmax} is injected, it makes NP voltage decrease. It means that NP voltage can be adjusted bidirectionally in a switching cycle. To satisfy i^*_{NP}=0, u_{ZSV} can be found.

(2) $i^*_{NPmin} < i^*_{NPmax} < 0$. No matters how large u_{ZSV} is injected, the NP voltage always increases. However, the NP voltage rising rate under i^*_{NPmax} is smaller than that under i^*_{NPmin}.

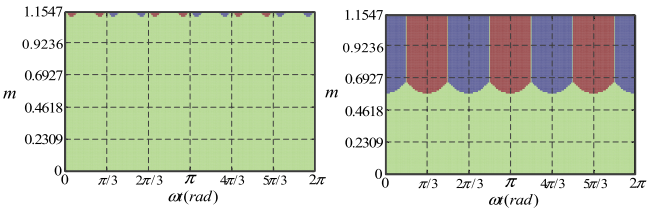
(3) $0 < i^*_{NPmin} < i^*_{NPmax}$. No matters how large u_{ZSV} is injected, the NP voltage always decreases. However, the NP voltage falling rate under i^*_{NPmin} is smaller than that under i^*_{NPmax}.

When $\varphi = 0$ and $\pi/2$, the distribution of i^*_{NPmax} and i^*_{NPmin} is given in Fig. 2, respectively. For $\varphi = 0$, i^*_{NPmax} and i^*_{NPmin} almost satisfy the first situation. For $\varphi = \pi/2$, i^*_{NPmax} and i^*_{NPmin} satisfy the first situation at lower modulation index ($m < 0.577$). When $m > 0.577$, the second and third situations are satisfied. In order to better reveal the distribution of i^*_{NPmax} and i^*_{NPmin}, Fig. 3 shows the distribution regions of different situations for $\varphi = 0$ and $\varphi = \pi/2$, where the green, blue and red regions means that the first, second and third situations are respectively satisfied.

When $\varphi \ne 0$ and $\pi/2$, the phase current can be decomposed into active and reactive components. Therefore, i^*_{NPmax} and i^*_{NPmin} at any power factor angle can be calculated by:

$$\begin{cases} i^*_{NPmax}(m, \omega t, \varphi) \\ = i^*_{NPmax}(m, \omega t)|_{\varphi=0} \cos\varphi + i^*_{NPmax}(m, \omega t)|_{\varphi=\frac{\pi}{2}} \sin\varphi \\ i^*_{NPmin}(m, \omega t, \varphi) \\ = i^*_{NPmin}(m, \omega t)|_{\varphi=0} \cos\varphi + i^*_{NPmin}(m, \omega t)|_{\varphi=\frac{\pi}{2}} \sin\varphi \end{cases} \tag{10}$$

The distribution of i^*_{NPmax} and i^*_{NPmin} can be calculated by the appendix procedure and then the distribution regions similar to that of Fig. 3 can be acquired.



(a) φ=0 (b) φ=π/2

FIGURE 3. The distribution regions of different situations.

D. NECESSARY CONDITIONS FOR KEEPING NP VOLTAGE UN-CHANGED IN A FUNDAMENTAL CYCLE

Hypothesis 2: It is supposed that the NP voltage is balanced at the beginning of a fundamental cycle. If the NP voltage still keeps equilibrium state at the end of this fundamental cycle, thus it means the NP voltage is unchanged in this fundamental cycle. Based on the hypothesis, the DC offset can be completely eliminated, which is a prerequisite to guarantee the reliable and safe operation of TLI.

The NP voltage variation Δu_{NPf} between the beginning and end of a fundamental cycle can be expressed as:

$$\Delta u_{NPf} = \frac{-\int_0^{2\pi} i^*_{NP} d\omega t}{2\pi f(C_1 + C_2)} = \frac{\Delta u^*_{NPf}}{2\pi f(C_1 + C_2)} \tag{11}$$

where $\Delta u^*_{\mathrm{NPf}} = -\int_0^{2\pi} i^*_{\mathrm{NP}} d\omega t$ is related to m, φ and u_{ZSV}, which depicts the NP voltage variation characteristics.

So as to effectively balance the NP voltage, particularly to prevent a gradually increased DC offset, the possible NP voltage variation should be paid attention over a fundamental cycle. When u_{ZSV} satisfies the eq. (5), there are countless values in each switching cycle. When the injected u_{ZSV} corresponding to i^*_{NPmin} is always selected for each switching cycle, the maximum NP voltage adjustable ability towards the increasing direction is achieved. Similarly, when the injected u_{ZSV} corresponding to i^*_{NPmax} is always selected for each switching cycle, the maximum NP voltage adjustable ability towards the decreasing direction is achieved. Define the following functions:

$$\begin{cases} u^*_{\mathrm{NPfmax}} = -\int_0^{2\pi} i^*_{\mathrm{NPmax}}(m, \omega t, \phi) d\omega t \\ u^*_{\mathrm{NPfmin}} = -\int_0^{2\pi} i^*_{\mathrm{NPmin}}(m, \omega t, \phi) d\omega t \end{cases} \tag{12}$$

According to the above function, $\Delta u^*_{\mathrm{NPfmax}}$ represents the maximum NP voltage decrease capability ($\Delta u^*_{\mathrm{NPfmax}} < 0$) or the minimum NP voltage increase capability ($\Delta u^*_{\mathrm{NPfmax}} > 0$) in a fundamental cycle, and $\Delta u^*_{\mathrm{NPfmin}}$ represents the maximum NP voltage increase capability ($\Delta u^*_{\mathrm{NPfmin}} > 0$) or the minimum NP voltage decrease capability ($\Delta u^*_{\mathrm{NPfmin}} < 0$) in a fundamental cycle. Therefore, three situations can be summarized:

(1) When $\Delta u^*_{\mathrm{NPfmax}} < 0 < \Delta u^*_{\mathrm{NPfmin}}$, the injected u_{ZSV} can remain NP voltage unchanged in a fundamental cycle ($\Delta u^*_{\mathrm{NPf}} = 0$).

(2) When $\Delta u^*_{\mathrm{NPfmax}} < \Delta u^*_{\mathrm{NPfmin}} < 0$, the NP voltage always decreases in a fundamental cycle ($\Delta u^*_{\mathrm{NPf}} < 0$).

(3) When $0 < \Delta u^*_{\mathrm{NPfmax}} < \Delta u^*_{\mathrm{NPfmin}}$, the NP voltage always increases in a fundamental cycle ($\Delta u^*_{\mathrm{NPf}} > 0$).

The first situation can avoid the gradually increased DC offset but the NP voltage will present periodic oscillation problem. The latter two situations will result in gradually increased DC offset on NP voltage, so the latter two cases should be avoided. Fig. 4 shows the distribution of $\Delta u^*_{\mathrm{NPfmin}}$ and $\Delta u^*_{\mathrm{NPfmax}}$. From Fig. 4, it can be seen that the first situation is always satisfied at any m and φ, which means that the NP voltage is unconditional balanced in a fundamental cycle.

III. THE NP VOLTAGE CONTROL METHOD BASED ON PLANNED ZVS INJECTION

Since the NP current is related to the injected u_{ZSV}, two NP voltage control methods are proposed. One is based on planned ZSV injection, and the other is based on the closest clamping mode method, which are respectively named as PZIPWM and CCMDPWM. The control of the NP voltage is not only to balance NP voltage in every switching cycle, but more importantly to eliminate the possible cumulative offset on NP voltage.

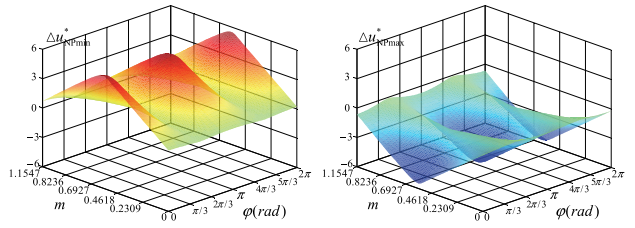


FIGURE 4. The distribution of $\Delta u^*_{\mathrm{NPfmin}}$ and $\Delta u^*_{\mathrm{NPfmax}}$.

If an offset on NP voltage u_{NPinit} is detected at the beginning of one switching cycle, to maintain NP voltage balance, it is expected that the NP voltage variation Δu_{NP} in this switching cycle satisfies the following conditions:

$$\Delta u_{\mathrm{NP}} = -u_{\mathrm{NPinit}} \tag{13}$$

Substituting (13) into (10), the NP current reference value i^*_{NPref} can be obtained:

$$i^*_{\mathrm{NPref}} = \frac{u_{\mathrm{NPinit}}(C_1 + C_2)}{I_{\mathrm{m}} T_{\mathrm{S}}} \tag{14}$$

A. THE PLANNED ZSV INJECTION METHOD

According to the i^*_{NPref} calculated by equation (14), the PZIPWM is proposed by solving the linear equation and then selecting the injected ZSV reference u_{ZSVref} to achieve the maximum NP voltage balance capability. The following three cases will be discussed.

Case1: $i^*_{\mathrm{NPmim}} < i^*_{\mathrm{NPref}} < i^*_{\mathrm{NPmax}}$. Since the relationship between i^*_{NP} and u_{ZSV} is piecewise linear, it yields $u_{\mathrm{ZSVref}} \in [u_{\mathrm{ZSVN}},\ u_{\mathrm{ZSV(N+1)}}]$ when $i^*_{\mathrm{NPref}} \in [i^*_{NPN},\ i^*_{NP(N+1)}]$. Then u_{ZSVref} can be determined by solving the linear equations, as shown in Fig. 5 (a). It should be noted that i^*_{NPref} may correspond to more than one u_{ZSVref}, which can recover the NP voltage to equilibrium state in a switching cycle. Generally, u_{ZSVref} with lower absolute value is selected.

Case2: $i^*_{\mathrm{NPref}} \geq i^*_{\mathrm{NPmax}}$. i^*_{NPref} is limited as i^*_{NPmax}, and the ZSV corresponding to i^*_{NPmax} is the expected u_{ZSVref}. This case is given in Fig. 5 (b), in which the injected u_{ZSVref} causes the NP voltage decreasing with maximum rate ($i^*_{\mathrm{NPmax}} > 0$) or increasing with minimum rate ($i^*_{\mathrm{NPmax}} < 0$). In this case, the boundary point or demarcation point is selected, which means one phase is clamped.

Case3: $i^*_{\mathrm{NPref}} \leq i^*_{\mathrm{NPmim}}$. i^*_{NPref} is limited as i^*_{NPmin}, and the ZSV corresponding to i^*_{NPmin} is the expected u_{ZSVref}. This case is given in Fig. 5 (c), in which the injected u_{ZSVref} causes the NP voltage decreasing with minimum rate ($i^*_{\mathrm{NPmin}} > 0$) or increasing with maximum rate ($i^*_{\mathrm{NPmin}} < 0$). In this case, similar to Case2, one phase is also clamped.

In conclusion, the rule of NP voltage control method based on PZIPWM can be summarized as:

$$\begin{cases} if\,(i^*_{\mathrm{NPref}} \geq i^*_{\mathrm{NPmax}}),\quad u_{\mathrm{ZSVref}} = u_{\mathrm{ZSV}} \Big|_{@i^*_{\mathrm{NPmax}}} \\ if\,(i^*_{\mathrm{NPref}} \leq i^*_{\mathrm{NPmin}}),\quad u_{\mathrm{ZSVref}} = u_{\mathrm{ZSV}} \Big|_{@i^*_{\mathrm{NPmin}}} \\ if\,(i^*_{\mathrm{NPmim}} < i^*_{\mathrm{NPref}} < i^*_{\mathrm{NPmax}}), \\ u_{\mathrm{ZSVref}} = \dfrac{i^*_{\mathrm{NPref}} - i^*_{\mathrm{NPN}}}{i^*_{\mathrm{NP(N+1)}} - i^*_{\mathrm{NPN}}}(u_{\mathrm{ZSV(N+1)}} - u_{\mathrm{ZSVN}}) \\ +u_{\mathrm{ZSVN}} \end{cases} \tag{15}$$

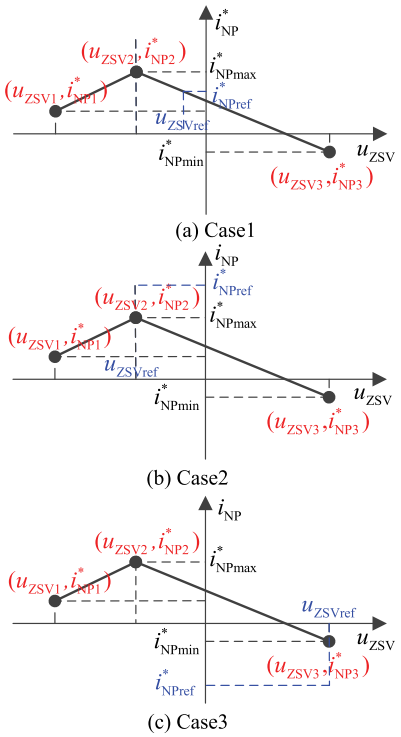


FIGURE 5. The planned ZSV injection method under different cases.

TABLE 2. T-type TLI hardware system parameters.

Parameter	Value
DC link voltage	200V
Upper and lower dc-link capacitor	1000μF
Resistive-inductive load 2 for high pf (Z_{H2})	$6e^{j\pi/12}\Omega$
Resistive-inductive load 1 for low pf (Z_{L1})	$2e^{j5\pi/12}\Omega$
Resistive-inductive load 2 for low pf (Z_{L2})	$6e^{j5\pi/12}\Omega$
Switching frequency	16kHz

The planned ZSV injection method with one demarcation point under different cases is illustrated in Fig. 5. In fact, according to Table 2, the number of demarcation point may be zero, one or three. Therefore, the other two situations can be similarly referred to Fig. 5, which are not discussed here.

B. THE CLOSEST CLAMPING MODE METHOD

When ZSV is injected at the boundary points or demarcation points, no switching behaviors can be realized for a certain phase. For example, when $u_{ZSV} = -1 - u_{min}$, the phase corresponding to u_{min} is clamped to the negative bus without switching behaviors, which outputs level 0; when $u_{ZSV} = -u_{min}$, the phase corresponding to u_{min} is clamped to the NP without switching behaviors, which outputs level 1. This method has advantages on reducing switching losses of the device.

When i^*_{NPref} calculated by equation (14) belongs to Case1 and Case2 of the previous section, the NP voltage control method based on CCMDPWM is consistent with the analysis of the above section.

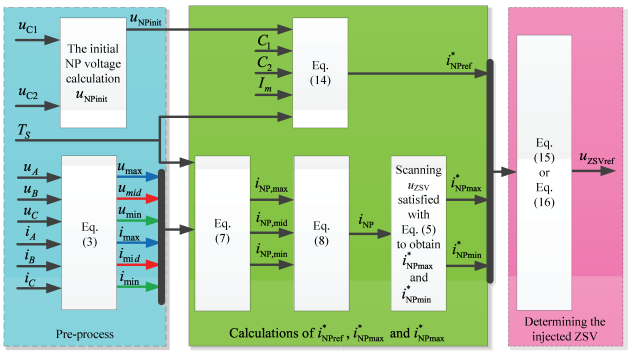


FIGURE 6. The flow diagram of the proposed two NP voltage control methods.

When i^*_{NPref} calculated by equation (14) belongs to Case1 of the previous section, u_{ZSVN} ($N = 1, 2, 3, 4$ or 5) closest to u_{ZSVref} is selected, and one phase is thus clamped. For example, as shown in Fig. 5(a), u_{ZSVref} is closest to u_{ZSV2}, so u_{ZSV2} is selected instead of u_{ZSVref} to make the inverter operate in clamping mode. However, the actual NP current corresponds to i^*_{NP2}. Thus, compared to PZIPWM, the NP voltage cannot be recovered to equilibrium state just in a switching cycle with CCMDPWM.

In conclusion, the rule of NP voltage control method based on CCMDPWM can be summarized as:

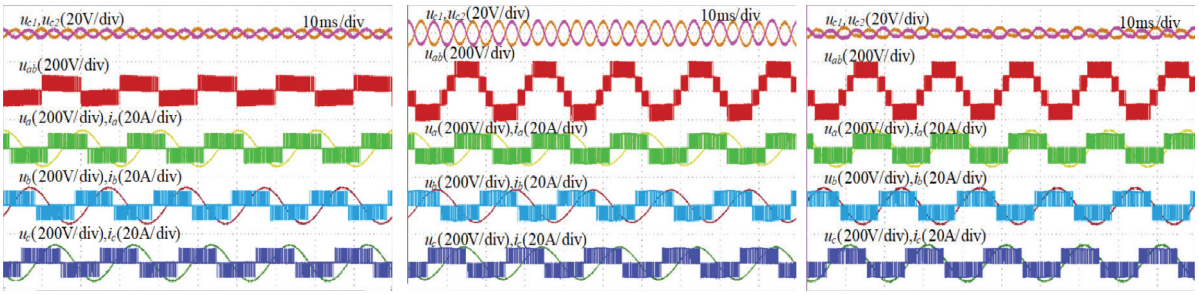
$$\begin{cases} if\,(i^*_{NPref} \geq i^*_{NPmax}),\quad u_{ZSVref} = u_{ZSV}\,\big|_{@i^*_{NPmax}} \\ if\,(i^*_{NPref} \leq i^*_{NPmin}),\quad u_{ZSVref} = u_{ZSV}\,\big|_{@i^*_{NPmin}} \\ if\,(i^*_{NPmim} < i^*_{NPref} < i^*_{NPmax}), \\ u_{ZSVref} = \begin{cases} u_{ZSVN},\ if\,(|i^*_{NPref} - i^*_{NPN}| \leq \\ |i^*_{NP(N+1)} - i^*_{NPref}|) \\ u_{ZSV(N+1)},\ if\,(|i^*_{NPref} - i^*_{NPN}| \\ > |i^*_{NP(N+1)} - i^*_{NPref}|) \end{cases} \end{cases} \tag{16}$$

IV. EXPERIMENTAL RESULTS

The experiments are implemented according to the flow diagram of the proposed two NP voltage control methods given in Fig. 6. In order to avoid the effect of the control method, open-loop control is adopted to evaluate the performances of the proposed modulation strategies. The system was assembled in the lab whose main parameters are listed in Table 2. In the experimental porotype, the switching device is SEMiX205TMLI12E4B and the commands are delivered to system from the DSP MC56F84789 master controller.

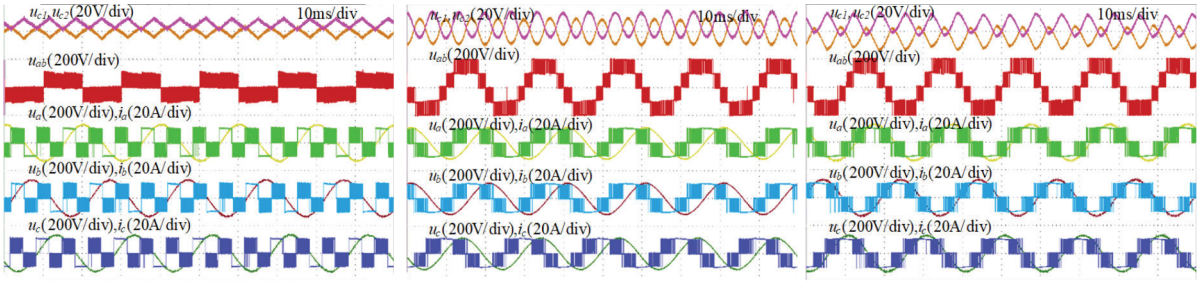
A. STEADY STATE EXPERIMENT

The experiment will be performed under three kinds of operating conditions. $m = 0.3$, $\varphi = 5\pi/12$ is recorded as operating condition 1; $m = 0.9$, $\varphi = 5\pi/12$ is recorded as operating condition 2; $m = 0.9$, $\varphi = \pi/12$ is recorded as operating condition 3. The experimental results for the SVPWM, DPWM I, VSVPWM, and the proposed two carrier-based modulation methods when the m and φ is changed, are shown in Figs. 7-11 respectively. These steady state results include



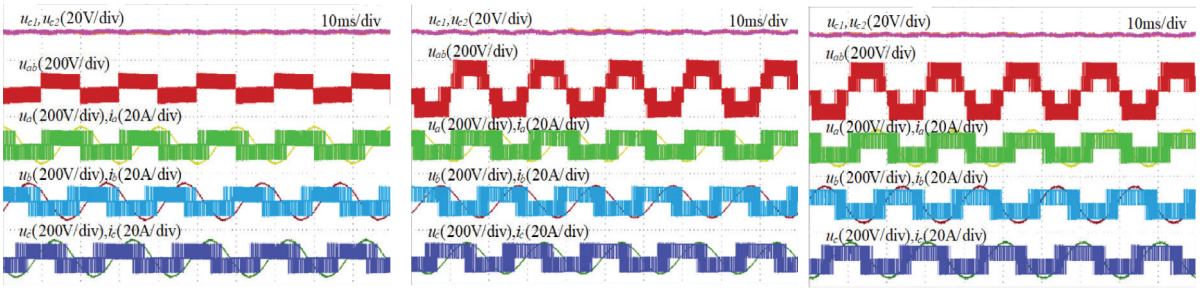
(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 7. Experimental results of SVPWM.



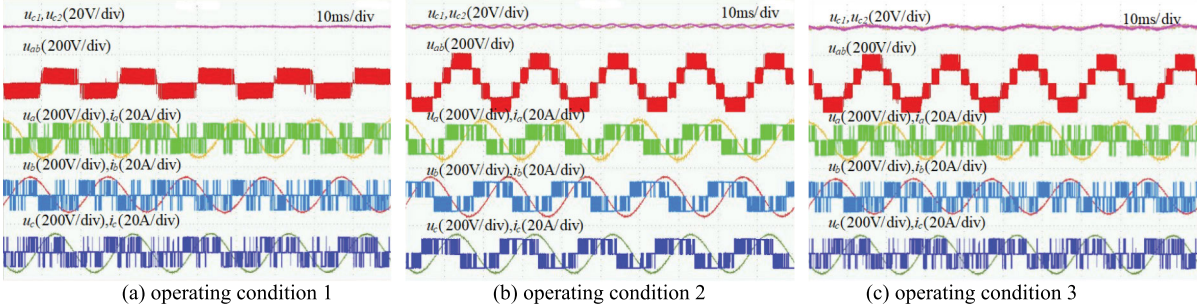
(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 8. Experimental results of DPWM I.



(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 9. Experimental results of VSVPWM.

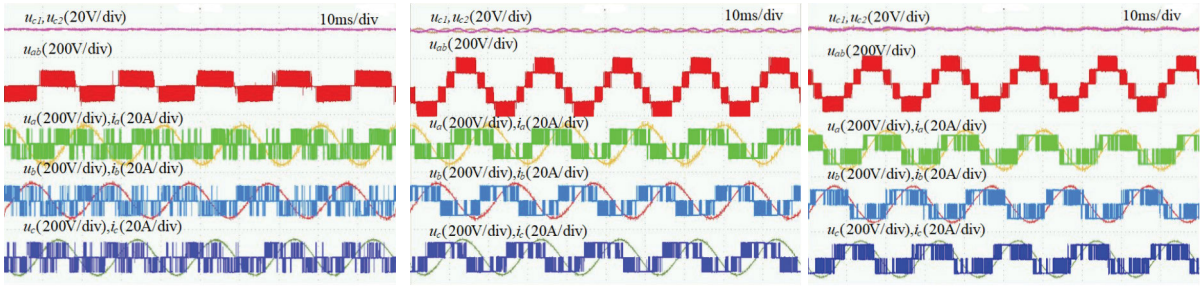


(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 10. Experimental results of the proposed PZIPWM.

the waveforms of NP voltage, line-to-line voltage and phase voltage. The condition of low m and high φ is not considered here, under which the NP voltage oscillation is very small [6].

Comparing the experimental results shown in Figs. 7-11, it can be found that the DC offset only exists in DPWM I and it can be eliminated in other modulation methods. Under the



(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 11. Experimental results of the proposed CCMDPWM.

TABLE 3. NP voltage oscillation under different operating conditions.

	SVPWM	DPWM	VSVPWM	PZIPWM	CCMDPWM
high m, high Pf	small	small	none	none	none
high m, low Pf	great	great	none	very small	very small
low m, low Pf	small	great	none	none	none
DC offset	none	have	none	none	none

TABLE 4. The low order harmonics distribution and THD.

		2-th	4-th	5-th	7-th	THD
SVPWM	Fig 7(a)	0.12	0.08	0.81	0.75	3.23
	Fig 7(b)	0.15	0.13	0.74	0.72	2.82
	Fig 7(c)	0.11	0.10	0.61	0.64	2.85
DPWM I	Fig 8(a)	0.73	0.71	0.87	0.81	4.11
	Fig 8(b)	0.52	0.48	1.13	1.07	4.43
	Fig 8(c)	0.62	0.55	0.73	0.65	4.23
VSVPWM	Fig 9(a)	0.09	0.08	0.07	0.05	3.09
	Fig 9(b)	0.11	0.13	0.11	0.12	4.03
	Fig 9(c)	0.12	0.10	0.09	0.11	4.11
PZIPWM	Fig 10(a)	0.12	0.13	0.06	0.08	3.08
	Fig 10(b)	0.15	0.14	0.21	0.24	2.56
	Fig 10(c)	0.11	0.15	0.10	0.07	2.43
CCMDPWM	Fig 11(a)	0.08	0.09	0.05	0.04	3.19
	Fig 11(b)	0.09	0.13	0.23	0.21	2.97
	Fig 11(c)	0.12	0.08	0.13	0.15	3.11

same conditions, these modulation methods are sorted from small to large according to the NP voltage control capabilities, which are DPWM I, SVPWM, CCMDPWM, PZIPWM and VSVPWM. The proposed two modulation methods almost have the same NP voltage control capability. Under operating condition 1 and 3, the NP voltage control capability of the proposed two modulation methods are the same as that of VSVPWM and the NP voltage can be controlled perfectly without fluctuation. Under operating condition 1, the NP voltage fluctuation is very small, which reduced significantly compared with that of SVPWM. In order to reveal the NP voltage control capability intuitively, the NP voltage oscillations under different operating conditions for five modulation methods are listed in Table 3, and the measured low order harmonics and THD are listed in Table 4.

It should be known that the switching losses are related to the switching numbers. The measured switching losses

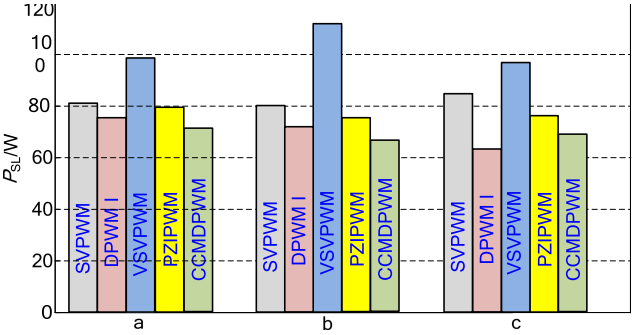


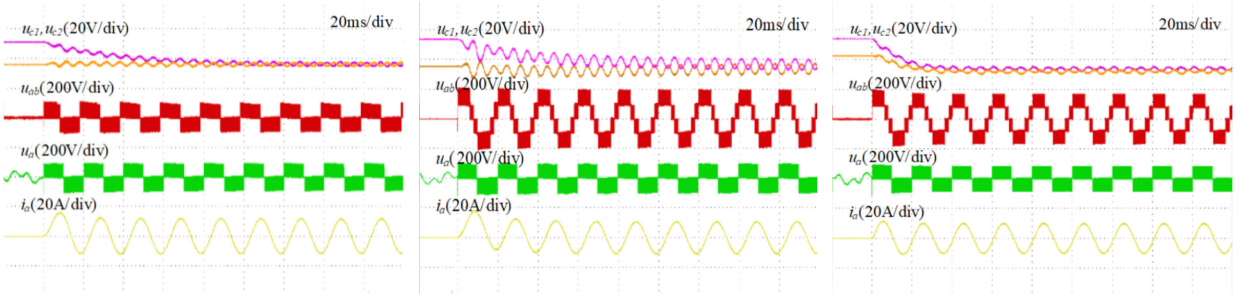
FIGURE 12. Measured losses under different modulation strategies.

corresponding to these five modulation strategies under the three conditions are shown in Fig. 12, which are denoted as a-c. In order to compare the switching losses, the amplitude of phase current keeps unchanged under different experimental conditions. In the experiments, the switching losses in one unit time are calculated by the power analysis module. According to the calculation results, VSVPWM has the highest switching loss among the five modulation strategies. The switching losses of SVPWM are lower than that of VSVPWM, which is about 80W. The switching losses of PZIPWM are slightly lower than that of SVPWM. That's because there are some regions in which one phase is clamped. The switching losses of DPWM I are lower than that under CCMDPWM when $\varphi = \pi/12$, but larger than that under CCMDPWM when $\varphi = 5\pi/12$.

B. DYNAMIC STATE OPERATION

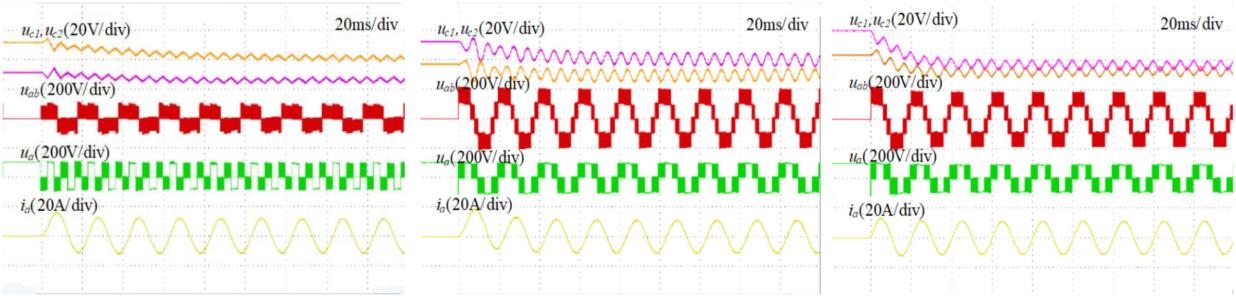
To observe NP voltage recovery process, the value of upper dc-link capacitor is increased from 1000uF to 1200uF to ensure that there is 18V offset approximately on the NP voltage during the establishment of the DC-side voltage. The NP voltage recovery process results of different PWM strategies, are shown in Figs. 13-17.

Under these five modulation strategies, it can be seen that the DC offset on NP voltage are reduced gradually, and finally the DC offset can be eliminated except DPWM I. The AC ripples on NP voltage are similar with that in steady state operation. In addition, the recovery rate of NP voltage is much



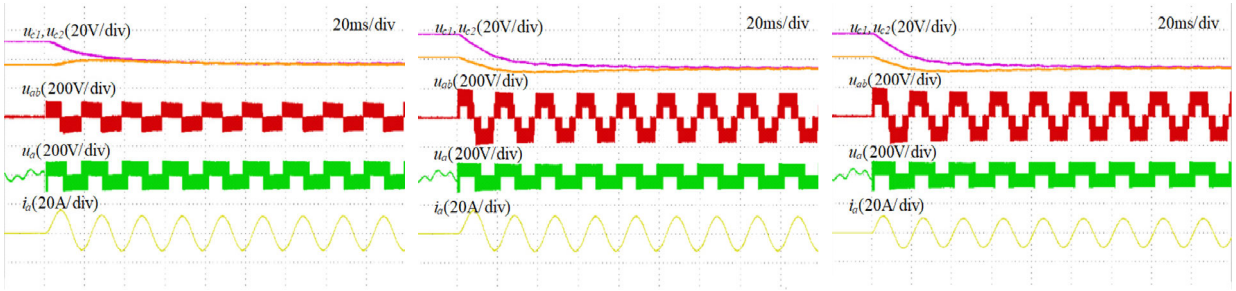
(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 13. The NP voltage recovery ability of SVPWM.



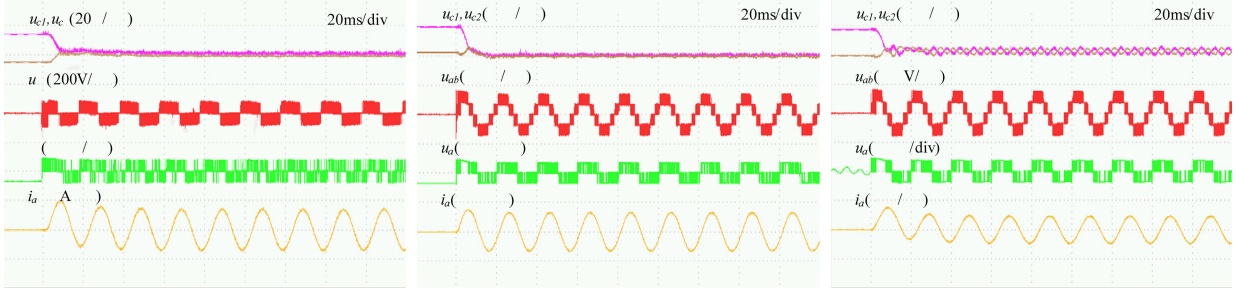
(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 14. The NP voltage recovery ability of DPWM I.



(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 15. The NP voltage recovery ability of VSVPWM.

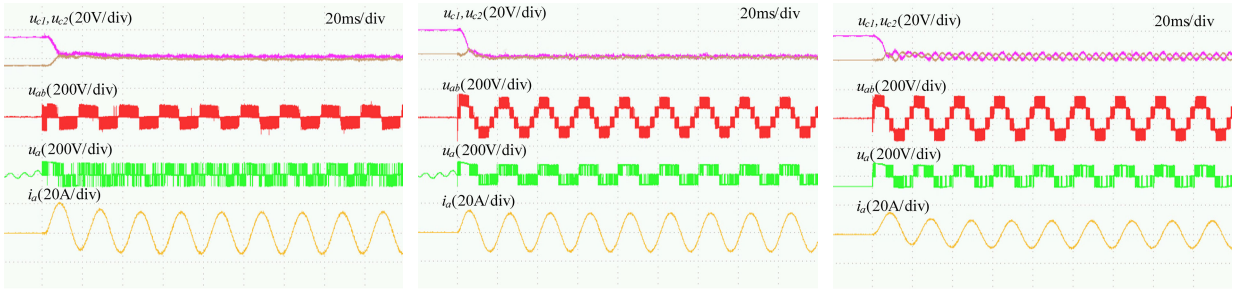


(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 16. The NP voltage recovery ability of the proposed PZIPWM.

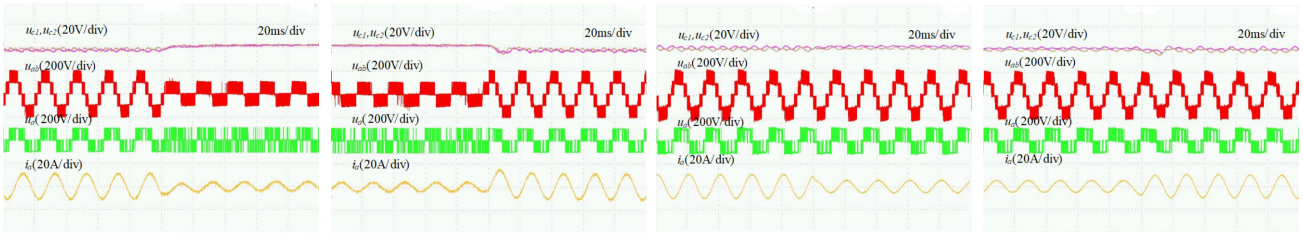
faster under the proposed two methods. It also indicates that the proposed two methods have superior NP voltage control ability.

The results of dynamic experimental, in which modulation index and load has a sudden step change, are shown in Figs. 18 and 19 respectively. Figs. 18 and 19 indicate that the



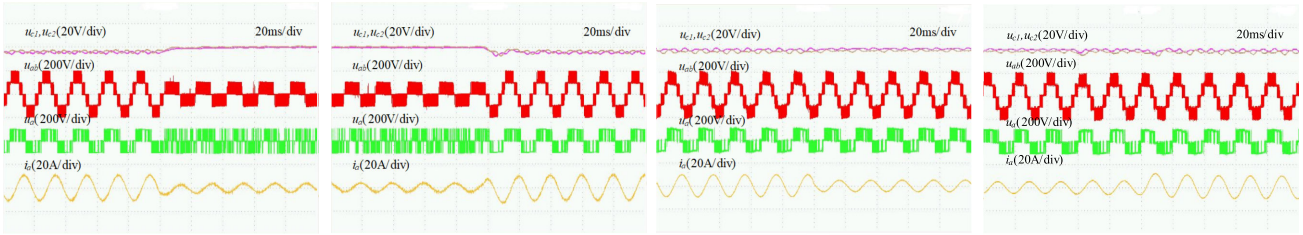
(a) operating condition 1 (b) operating condition 2 (c) operating condition 3

FIGURE 17. The NP voltage recovery ability of the proposed CCMDPWM.



(a) m is changed between 0.9 and 0.3 with Z_{L2} load (b) Inductive load is changed between 12mH and 22mH with m=0.9

FIGURE 18. The dynamic process under PZIPWM.



(a) m is changed between 0.9 and 0.3 with Z_{L2} load (b) Inductive load is changed between 12mH and 22mH with m=0.9

FIGURE 19. The dynamic process under CCMDPWM.

proposed two methods still have strong NP voltage control ability in the process of responding to step changes.

V. CONCLUSION

In this paper, the maximum and minimum NP current with respect to the injected ZSV in a switching cycle are revealed. Based on the analysis, a planned ZSV injection method is expected to balance NP voltage just in a switching cycle with appropriate ZSV injection. That's achievable if the NP current reference value is between the maximum and minimum NP current. Furthermore, a closest clamping mode method is proposed to reduce switching losses with a small sacrifice of controlling NP voltage. The proposed two methods are both based on ZSV injection, which makes their realization easy by carrier-based implementation. The effectiveness of the proposed methods is verified by lots of experimental results, which show good characteristics on NP voltage control.

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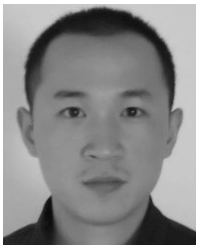


JINPING WANG (Member, IEEE) was born in Hunan, China, in 1984. He received the B.S. degree in electronic and information engineering and the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2007 and 2013, respectively.

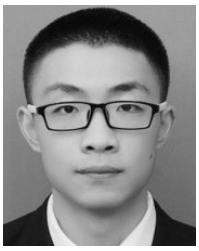
Since June 2013, he has been with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, where he is currently an Associate Professor. His main research interests include modeling, analysis, control, and applications of switching-mode power supplies.

ZAIYI GUI was born in Anqing, Anhui, China. He received the B.S. degree from the School of Electrical and Information Engineering, Anhui University of Technology, Maanshan, China, in 2016. He is currently pursuing the M.S. degree with the Department of Electrical Engineering, Hefei University of Technology, Hefei, China.

His main research interests include power electronics and power converters in renewable energy.

PEIXIA WANG was born in Anhui, China, in 1991. She received the B.S. degree from the Department of Electrical Engineering and Automation, Anhui Polytechnic University of Technology, Wuhu, China, in 2015, and the M.S. degree from the Department of Information Engineering, Hefei University of Technology, Hefei, China, in 2019.

She is currently with State Grid Feidong Power Supply Company. Her main research interest includes power converters in renewable energy.



JUNCAN WANG was born in Lu'an, Anhui, China. He received the B.S. degree from the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, in 2018. He is currently pursuing the M.S. degree with the Department of Electrical Engineering, Hefei University of Technology.

His main research interests include power electronics and power converters in renewable energy.

WEIDONG JIANG (Member, IEEE) was born in Sichuan, China, in 1976. He received the B.S. and Ph.D. degrees in electrical engineering from the Hefei University of Technology, Hefei, China, in 1999 and 2004, respectively.

Since June 2004, he has been with the School of Electrical Engineering and Automation, Hefei University of Technology, where he is currently a Professor. His research interests include electrical machines and their control systems, power electronics, and electric drives.