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SPECIAL SECTION ON EVOLVING TECHNOLOGIES IN ENERGY STORAGE SYSTEMS FOR ENERGY SYSTEMS APPLICATIONS

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Compact Three Phase Multilevel Inverter for Low and Medium Power Photovoltaic Systems

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ABSTRACT A new three phase multilevel inverter with reduced number of components count is proposed in this paper. This inverter is designed using a single DC source per phase to generate multiple level output voltage which makes it suitable for low and medium voltage applications, including ac-coupled renewables or energy storages. A generalized circuit configuration is shown in this paper following which the number of output voltage level can be increased as per expectation. Although, each element endures the voltage stress equivalent to the input DC voltage, the value of total standing voltage (TSV) is reduced by the utilization of minimized number of components with respect to the number of series connected capacitors. Further, staircase modulation scheme is used to generate the switching signals. Hence, the proposed inverter can be operated at low switching frequency with optimal output current harmonic distortion which decreases switching losses and suppresses power factor falling. In order to validate the theoretical explanations and practical performances of the proposed inverter, the hypothesis is simulated for 9, 13 and 39 output voltage level inverters for three phase with a line voltage total harmonic distortion (THD) of 6.06%, 4.16% and 2.10% respectively in MATLAB/Simulink and a 5-level single phase laboratory prototype is implemented in the laboratory.

INDEX TERMS Pulse width modulation inverters, multilevel inverters, total harmonic distortion, total standing voltage, photovoltaic systems, energy storage.

I. INTRODUCTION

The demand of electrical energy is still increasing gradually in various applications from an earlier age. In previous years, the generation of electrical energy was mainly dependent upon non-renewable sources such as fossil fuels, coal, natural gas, petroleum oil that imposes irreclaimable changes on the environment as well as the temperature of the earth. For this reason, nowadays, clean energy sources such as solar, ocean and wind energy are being encouraged to be used by the governments for producing electrical power to meet the desired demand level. In order to synchronize these type of new energy systems to the combined power grid, micro grid and local loads, especially to interconnect with energy storage systems to ensure resiliency, different families of power converter have already been introduced by the researchers [1], [2].

Usually, the generation, transmission, distribution and utilization of electric power take place through DC to AC power conversion process [3]. The DC to AC power converters are commonly called inverters that play a vital role in variable frequency drives, uninterruptible power supplies, induction heating, high voltage DC power transmission, electric vehicle drives, flexible AC transmission systems and energy storage systems [4], [5]. Depending on the shape of the output waveform, inverters may be classified as square wave inverters, quasi-square wave inverters, two-level PWM inverters and multilevel inverters (MLIs) [6]. Among these, the MLIs have drawn a special attention due to having the capability of operating at all the circumstances including low, medium and high voltage conditions. The elementary concept behind MLI is to achieve a staircase waveform, following a sinusoidal

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path, by adding up several lower voltage DC levels utilizing semiconductor switches [7]. Usually, the multiple input DC levels include capacitors, batteries or other conventional storages, and renewable energy voltage sources. Rearranging and controlling of the power switches fulfil the aggregation of these multiple input DC levels and provide a high voltage at the output. Thus, in MLIs, the operating voltage is much higher than the stress voltage on a power switch as the voltage source with which the switch is connected determines its rated voltage [8].

MLIs offer many advantages such as better harmonic profile, reduced dv/dt stress resulting in a substantial reduction of filter components, and operation in both medium and high voltage applications with low voltage rated switches. Furthermore, MLIs not only generate smaller common mode voltage that reduces stress on motors but also draw current with lower distortion, offering lower conduction and switching losses and enhanced efficiency [9], [10]. The most common and classic MLI topologies include neutral point clamped (NPC) [11], flying capacitor (FC) [12] and cascaded H-bridge (CHB) [13] which have been established extensively in numerous applications in energy storage and electrical conversion systems. NPC and FC inverters introduce balanced charging problem of DC link capacitors. The CHB topology requires a large number of isolated DC voltage sources for the generation of higher level output. Moreover, all of these classic topologies require large number of semiconductor components as the number of output levels increase. For these reasons, reduction of semiconductor components as well as passive elements have become an important concern which reduces both the size and weight of the whole system and decreases the conduction and switching losses by enhancing efficiency.

In recent years, several MLI topologies with reduced components have been proposed by the researchers. The three phase MLI topology proposed in [14] was represented with reduced number of semiconductor devices where modified H-bridge modules were cascaded to generate higher level output. But, the requirement of large number of isolated DC voltage sources remains as an unsolved problem. Furthermore, in the papers proposed in [15], [16], two cascaded MLI structures with moderate components had been exhibited by the authors with higher total standing voltage (TSV) and isolated DC sources. However, another most recent topology proposed in 2019 by M. D. Siddique *et al.* also suffered from large number of DC source requirement problem where the requirement of semiconductor components is significantly reduced in [17]. Furthermore, the authors of [18]–[20] also presented three more MLI topologies where the main circuital structure was formed by cascading the basic modules. Nevertheless, the MLI topologies with asymmetrical input DC voltage sources had been reported in [21]–[25] where each of the topology could generate multiple level output with minimized number of DC sources and semiconductor devices. But, the topologies proposed in [23], [25] suffered from large conduction losses and higher value of TSV problems respectively. The switched capacitor MLI topologies presented in [26], [27] had a similar need for semiconductor switches and provided a higher value of TSV with increased equipment costs, though they have balanced the capacitor charging capability.

In order to overcome the aforementioned problems, this paper proposes a new three phase MLI topology with significantly reduced circuital elements as well as active semiconductor switches for the applications associated with low and medium power in microgrids and energy storage systems which also makes the system more compact and lighter. Further, the offered topology uses only one main DC input voltage source per phase and several DC link capacitors as auxiliary small DC voltage sources that addresses the requirement for isolated DC voltage sources by storing charges and providing energy as needed. The proposed topology also offers enhanced efficiency with lower losses and lower value of TSV that decreases the total equipment costs as compared to the existing topologies. By the virtue of the proposed topology, any desired level of output can be obtained in a low voltage range, as it contains an H-bridge unit to produce the negative half cycle of the output voltage. However, in order to avoid the balanced capacitor charging problem, an additional charging circuit is connected to the input terminal during experiment. The proposed topology is compared in terms of the components used in single phase with the existing single phase MLI topologies to validate the performance for low and medium voltage applications.

The content of the paper is rearranged as follows: section II describes the generalized circuit configuration, modulation strategy, capacitor charging and discharging process and operating principle of the proposed three phase inverter. The calculation of losses are represented in section III. Section IV and V show the simulation based results analysis and experimental verification of the theoretical explanation respectively. The comparison of the proposed inverter with the existing topologies is exhibited in section VI. Finally, section VII summarizes the content to conclude the paper.

II. PROPOSED THREE PHASE MLI

A. GENERALIZED CIRCUIT CONFIGURATION

The generalized three phase circuit configuration of the proposed inverter topology is shown in Fig. 1. Each phase consists of a single DC source, battery or energy storage system, power diodes, DC bus capacitors and power switches. The DC bus capacitors are used to divide the input DC voltage into number of small voltage levels equivalent to 1/n times of the V_{dc} where n is the number of series connected capacitors and V_{dc} is the input DC voltage. The power diodes provide discharging path of the DC bus capacitors through the load and the power switches control the discharging current flow of each capacitor according to the switching signal applied in its gate which results in multiple levels in the output voltage waveform. The whole circuit structure of each phase except the H-bridge cell can generate positive voltage levels only.

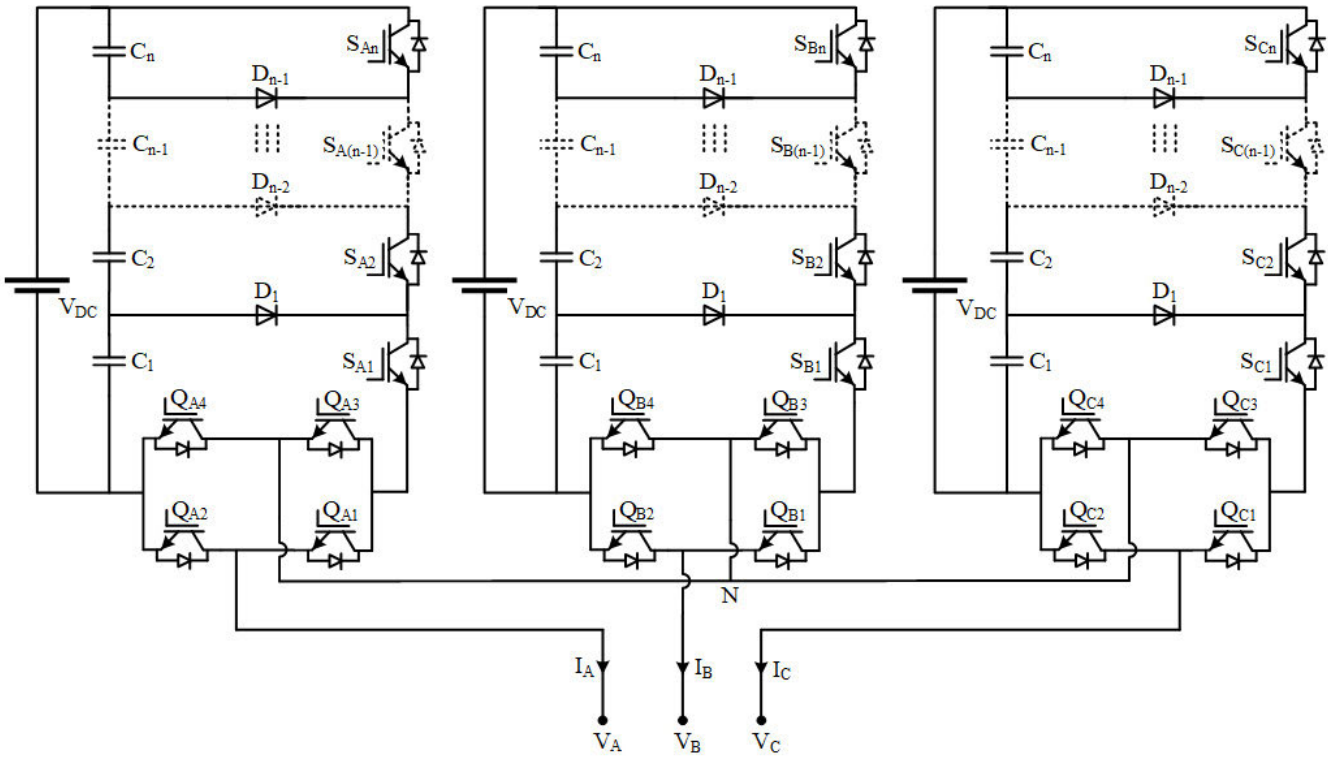

FIGURE 1. Generalized three phase circuit configuration of the proposed inverter topology.

Hence, an H-bridge cell is connected to the lower side of each phase leg for the generation of negative voltage levels which significantly reduces the utilization of power switches. The mathematical equations of the number of components required per phase for (2n+1) level proposed inverter can be expressed as follows:

$$N_{source} = 1 \tag{1}$$
$$N_{capacitor} = n \tag{2}$$
$$N_{diode} = n - 1 \tag{3}$$
$$N_{switch} = n + 4 \tag{4}$$
$$N_{driver\_circuit} = n + 4 \tag{5}$$

where n = 1, 2, 3 . . .

However, the sum of the voltage stress of all its power switches for a topology refers to the TSV [28]. Since all the switches are rated at V_{dc} in each phase, the TSV per phase of the proposed (2n+1) level inverter can be calculated by,

$$TSV = (n + 4)V_{dc} \tag{6}$$

B. MODULATION STRATEGY AND VOLTAGE THD CALCULATION

In order to generate the switching signals for driving the switches of the proposed inverter, level shifted multi-carrier based unipolar staircase modulation technique has been used in this paper. Thereby, the switching signal generation technique for the proposed inverter topology is very conventional and facile. However, the special benefit of unipolar staircase

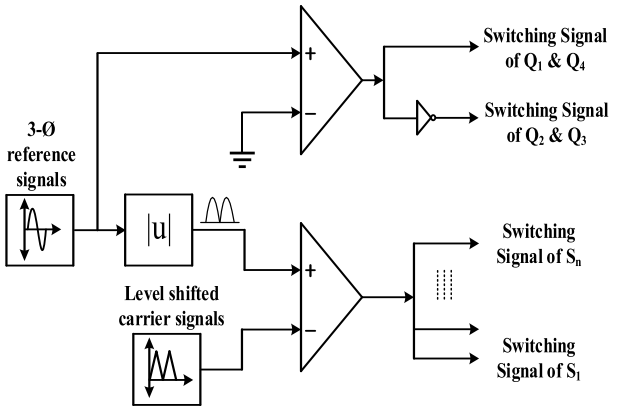

FIGURE 2. Generalized block diagram of the switching signal generation technique.

Pulse Width Modulation (PWM) technique is that it greatly reduces the lower order odd harmonic components and tends the output voltage waveform to the accurate 50 Hz sine wave resulting in reduction of THD.

Fig. 2 illustrates the block diagram of switching signal generation technique for the proposed three phase inverter. The level shifted carrier signals are compared with the three phase reference signals which provides the driving signals for the switches of each phase. The carrier frequency is used as, $f_s = 5\ kHz$. The comparison between reference signal and carrier signal which results in switching pulse is represented in Fig. 3.

For a (2n+1) level proposed three phase inverter, n number of carrier signals are required to generate the gate driving

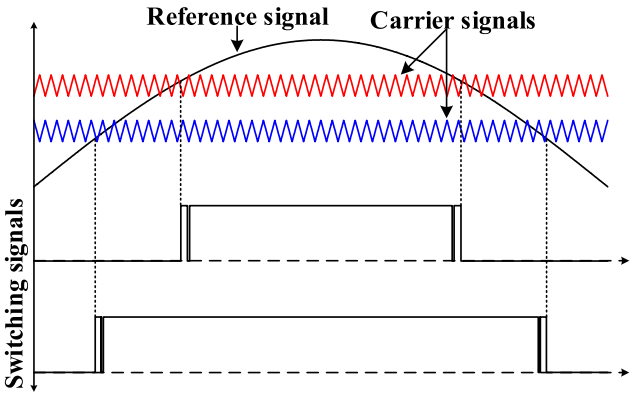

FIGURE 3. Switching pulse generation from the comparison between reference signal and carrier signal.

signals for 3n number of switches. If A_{ref} is assumed as the amplitude of the reference signal, then the individual peak amplitude of n number of carrier signals is expressed as,

$$A_c = \frac{A_{ref}}{2n} \tag{7}$$

However, for a three-phase multilevel inverter with staircase modulation, the line voltage THD is estimated as [29],

$$THD\,(m, n)\,\% = \frac{47}{(n-1)\,m}\% \tag{8}$$

where n and m denote the non-negative levels count and modulation index respectively.

C. OPERATING PRINCIPLES

The working principle of the proposed three phase inverter is explained with the help of a 5-level single phase unit. The mechanism of each phase being identical, the operating principle of a single phase unit is described in this paper to understand the working mechanism of other phases. A 5-level inverter unit contains 6 switches, 2 capacitors and a diode. The input DC voltage is divided equally by two DC link capacitors. The 5-level unit has 5 different operational modes which are described as follows:

Mode-0: When all the switches except Q_1 and Q_4 are OFF state, then it is called *Mode-0*. In this mode, both C_1 and C_2 get fully charged. Since, no discharging occurs from the capacitors in this mode, the output voltage level remains at V_0=0V. Fig. 4(a) shows Mode-0 operation of the proposed single phase 5-level inverter unit.

Mode-1: In this mode switch S_1, Q_1 and Q_4 are ON state and S_2, Q_2 and Q_3 are in OFF state. Capacitor C_1 discharges through the load using the path provide by switch S_1, Q_1, Q_4 and diode D_1. The current conduction loop for this mode is shown in Fig. 4(b). Thus, voltage across the capacitor C_1 is transferred to the load and the output voltage becomes, $V_1 = V_{dc}/2$.

Mode-2: In this mode, all the switches except Q_2 and Q_3 are ON state. Although S_1 switch is ON, capacitors C_1 and C_2 both discharge through the load using the path provided by S_2, Q_1 and Q_4 which is represented in Fig. 4(c). When S_2 goes to ON state, the anode terminal and cathode terminal voltages of D_1 become $V_{dc}/2$ and V_{dc} respectively which results in reverse bias condition. In this way, the entire DC input voltage appears across the load and the output voltage is, $V_2 = V_{dc}$.

TABLE 1. Switching states with their respective output voltage.

Output Voltage	Modes	Switching States (1=ON, 0=OFF)					
		S_1	S_2	Q_1	Q_2	Q_3	Q_4
V_{dc}	*Mode-2*	1	1	1	0	0	1
$V_{dc}/2$	*Mode-1*	1	0	1	0	0	1
0	*Mode-0*	0	0	1	0	0	1
$-V_{dc}/2$	*Mode-3*	1	0	0	1	1	0
$-V_{dc}$	*Mode-4*	1	1	0	1	1	0

Mode-3: Fig. 4(d) shows the *Mode-3* operation in which S_1, Q_2 and Q_3 are ON state and S_2, Q_1 and Q_4 are OFF state. This mode is almost same as *Mode-1* where switches S_1, Q_2 and Q_3 and diode D_1 provide a current conducting path for the discharge of the capacitor, C_1 through the opposite direction of the load. Hence, the output voltage is, $-V_1$=$-V_{dc}/2$.

Mode-4: In this mode all the switches except Q_1 and Q_4 are ON state. At this time, the discharging path for both capacitors C_1 and C_2 are provided by switch S_2, Q_2 and Q_3 through the opposite direction of the load and the diode is reverse biased for the same reason as mentioned in *Mode-2*. Fig. 4(e) depicts the *Mode-4* operation. Finally, the output voltage becomes, $-V_2$=$-V_{dc}$.

The switching states for the generation of 5-level output voltage according to the 5 modes described above is listed in Table 1. The duration of each operating mode with their corresponding output voltage is uphold in Fig. 5

D. CAPACITOR CHARGING-DISCHARGING PROCESS AND CAPACITANCE CALCULATION

The DC link capacitors are connected in series with the input DC voltage source, battery or energy storage system which is shown in Fig. 1. The capacitors works as miniature energy storages to provide energy to the circuit as per the requirement, omitting the need for redundant sources. The capacitors get fully charged when all the switches are in OFF state. The voltage across each capacitor can be expressed as,

$$V_C = \frac{V_{dc}}{n} \tag{9}$$

Here n is the number of capacitor for a given number of output voltage level of one phase. The capacitors are discharged across the load through the switches. Considering a 5-level single phase proposed inverter, the discharging period of the capacitors C_1 and C_2 are represented in Fig. 6. Initially, t_0 is the charging periods of C_1 and C_2. Then the discharging period of C_1 starts when S_1 is ON. Thereby, the discharging period of C_1 through S_1 is $tc1 = t1 - t0$. When S_2 switch starts conduction, C_1 and C_2 both capacitors discharge through it because the cathode terminal voltage of diode D_1 becomes higher than the anode terminal voltage which

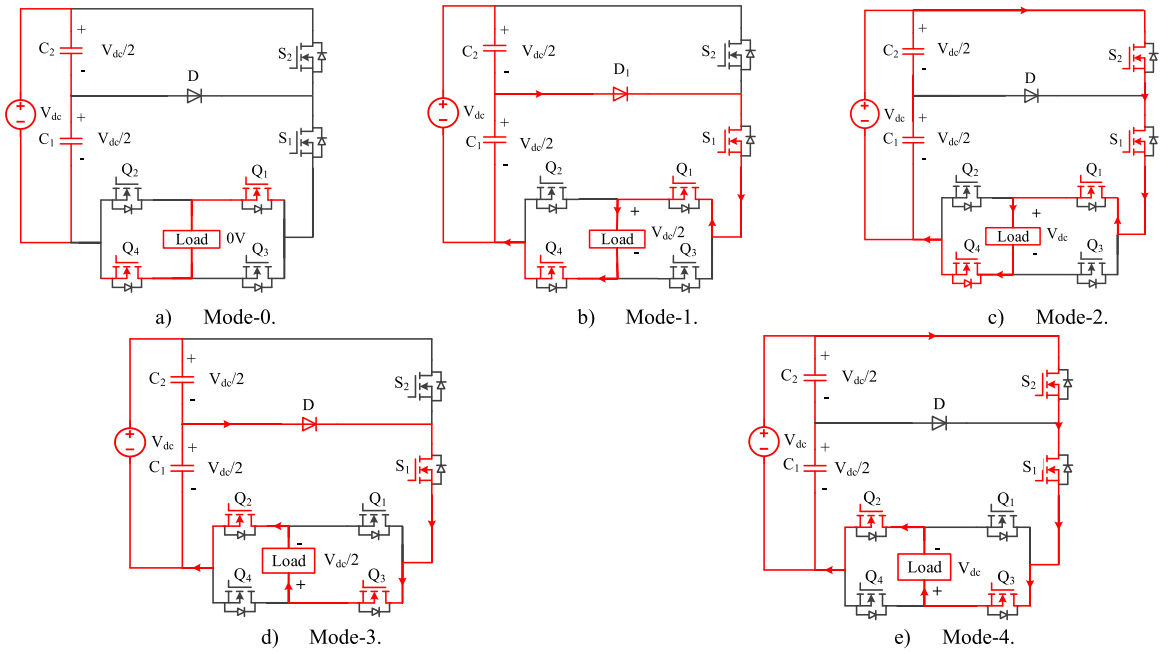

FIGURE 4. Five operating modes of the proposed 5-level inverter unit (single phase).

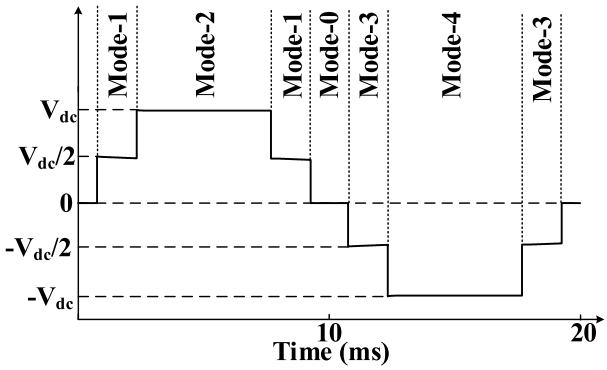

FIGURE 5. Duration of each operating mode with their corresponding output voltage.

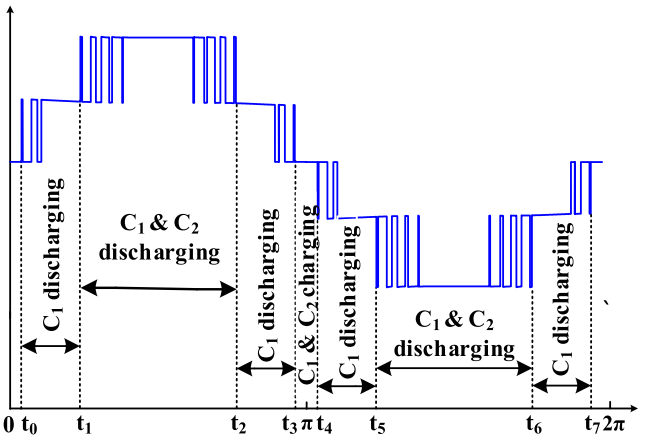

FIGURE 6. Charging and discharging process of capacitors for 5-level proposed inverter (for one phase).

results in reverse biased. Hence, the discharging period of both C_1 and C_2 capacitors becomes, $tc1 + tc2 = t2 - t1$. The discharging period of C_2 gets over when S_2 goes OFF state. Again, C_1 discharges for $t_3 - t_2$ during the on state of S_1. Further, the charging period of C_1 and C_2 is, $t_3 - t_4$. This process is also repeated for the negative half cycle. The entire charging and discharging process for a single cycle is shown in Fig. 6.

Therefore, the maximum discharging value of each capacitor is obtained by [30],

$$\Delta Q_C = \int_{t_a}^{t_b} I_{Load} Sin(2\pi f_{ref} t) dt \tag{10}$$

where I_{Load} is the maximum load current and (t_a, t_b) is the discharging interval of each capacitor. t_0 to t_3 and t_4 to t_7 are calculated as follows:

$$t_0 = \frac{\sin^{-1}\left(A_c/A_{ref}\right)}{2\pi f_{ref}} \tag{11}$$

$$t_1 = \frac{\sin^{-1}\left(2A_c/A_{ref}\right)}{2\pi f_{ref}} \tag{12}$$

$$t_2 = \frac{\pi - \sin^{-1}\left(2A_c/A_{ref}\right)}{2\pi f_{ref}} \tag{13}$$

$$t_3 = \frac{\pi - Sin^{-1}\left(A_c/A_{ref}\right)}{2\pi f_{ref}} \tag{14}$$

$$t_4 = \pi + t_0 \tag{15}$$

$$t_5 = \pi + t_1 \tag{16}$$

$$t_5 = \pi + t_2 \tag{17}$$
$$t_6 = \pi + t_3 \tag{18}$$

where f_{ref} and A_{ref} are the frequency and amplitude of reference waveform, respectively and A_c is the amplitude of carrier waveform. For the prevention of excessive voltage drop of the capacitors at discharging times, the value of capacitance need to be calculated properly to restrict the capacitor's voltage ripple in an acceptable range. Assuming k as the maximum capacitor voltage ripple ratio, the value of capacitance for each phase can be calculated as [31],

$$C_i \geq \frac{\Delta Q_{C_i}}{kV_{dc}} \tag{19}$$

III. CALCULATION OF LOSSES

In this section, the calculation processes of three types of losses of the proposed inverter are described in brief. Generally, two major losses are considered for NPC type inverters which are switching losses (P_{sw}) and conduction losses (P_{con}). Moreover, losses due to capacitors voltage ripple (P_{cap}) are also taken into count for more accuracy. All the losses are calculated connecting resistive load at the output terminal, as maximum losses occur at that time.

A. SWITCHING LOSSES (P_{sw})

The switching losses which are significant sources of power loss occur because of switching delays that involve to the semiconductor devices. When the off-state voltage and current of a switch overlap with each other at the time of changing its state, switching loss just occurs. There are two transition times denoted by t_{on} and t_{off}. Here, t_{on} and t_{off} define the time periods until the switch is completely turned-on and turn-off respectively. The amplitudes of voltage and current do not change instantly due to the rapid turn-on and turn-off processes of a switch. During these transition periods, both voltage and current simultaneously have significant values which cause noticeable power loss. Thus, the turn-on power loss (P_{sw_ON}) and the turn-off power loss (P_{sw_OFF}) are calculated as following equations [32]:

$$\begin{aligned} P_{sw\_ON,k} &= f_s \int_0^{t_{on}} v_{off\_state,k}(t).i(t)dt \\ &= f_s \int_0^{t_{on}} \left(-\frac{V_{off\_state,k}}{t_{on}}(t - t_{on})\right)\left(\frac{I_{on\_state1,k}}{t_{on}}t\right)dt \\ &= \frac{1}{6} f_s V_{off\_state,k} I_{on\_state1,k} t_{on} \end{aligned} \tag{20}$$

$$\begin{aligned} P_{sw\_OFF,k} &= f_s \int_0^{t_{off}} v_{off\_state,k}(t).i(t)dt \\ &= f_s \int_0^{t_{off}} \left(\frac{V_{off\_state,k}}{t_{off}}t\right)\left(-\frac{I_{on\_state2,k}}{t_{off}}(t - t_{off})\right)dt \\ &= \frac{1}{6} f_s V_{off\_state,k} I_{on\_state2,k} t_{off} \end{aligned} \tag{21}$$

where $V_{off\_state,k}$ represents the off state voltage of kth switch. $I_{on\_state1,k}$ and $I_{on\_state2,k}$ denote the currents of kth switch when it gets fully turned-on and before the turn-off state of it respectively. However, the switching frequency, f_s has two portions which can be obtained from the following equations [15]:

$$f_{s\_on} = N_{sw\_on}.f_{ref} \tag{22}$$
$$f_{s\_off} = N_{sw\_off}.f_{ref} \tag{23}$$

where the number of turn-on and turn-off of every single switch are represented by N_{sw_on} and N_{sw_off} respectively and they can be determined for an entire period as follows [26]:

$$N_{sw\_on} = \frac{t_{sw\_on}}{2\pi} \times N_t \times \frac{f_s}{f_{ref}} \tag{24}$$
$$N_{sw\_off} = \frac{t_{sw\_off}}{2\pi} \times N_t \times \frac{f_s}{f_{ref}} \tag{25}$$

In the above equations, t_{sw_on} and t_{sw_off} represent the time periods during which the switch is ON and OFF respectively. N_t is the total number of turn-on and turn-off during every switching cycle. Therefore, the total switching losses are determined by:

$$P_{sw\_total} = \sum_{k=1}^{N_{switch}} \left(\sum_{m=1}^{N_{sw\_on(k)}} P_{sw\_ON(km)} + \sum_{m=1}^{N_{sw\_off(k)}} P_{sw\_OFF(km)} \right) \tag{26}$$

where N_{switch} defines the total number of switches per phase. Hence, the total switching losses including all the three phase legs will the three times of P_{sw_total}.

B. CONDUCTION LOSSES

The parasitic impedances of the circuit elements cause conduction losses where the parasitic impedances include internal on-state resistance of switches (R_{sw_on}) and diodes (R_{D_on}). Therefore, the conduction losses caused by power switches and power diodes are calculated using the following equations [33]:

$$P_{con\_sw} = V_{sw\_on}.I_{sw\_avg} + R_{sw\_on}.I^2_{sw\_rms} \tag{27}$$
$$P_{con\_D} = V_{D\_on}.I_{D\_avg} + R_{D\_on}.I^2_{D\_rms} \tag{28}$$

where I_{sw_avg} and I_{sw_rms} represent the average and the RMS currents through the switches respectively and they are equivalent to average and RMS load currents. Further, I_{D_avg} and I_{D_rms} are the average and the RMS currents through the diodes respectively. However, the process of calculating the conduction losses of a 5-level single phase proposed inverter are as follows:

Step 1: When the value of output voltage is within 0 to $\pm V_{dc}/2$, then three switches and single diode conduct simultaneously. Hence, the conduction losses at this stage,

$$\begin{aligned} P_{con(\pm V_{dc}/2)} &= \left(3V_{sw\_on}.I_{load\_avg} + 3R_{sw\_on}.I^2_{load\_rms}\right) \\ &\quad + \left(V_{D\_on}.I_{load\_avg} + R_{D\_on}.I^2_{load\_rms}\right) \end{aligned} \tag{29}$$

Step 2: Further, four switches conduct together to make the amplitude of the output voltage from $\pm {}^{V_{dc}}/_{2}$ to $\pm V_{dc}$. So, the conduction losses are,

$$P_{con(\pm V_{dc})} = \left(4V_{sw\_on}.I_{load\_avg} + 4R_{sw\_on}.I^2_{load\_rms}\right) \quad (30)$$

Therefore, the total conduction losses are obtained by combining (29) and (30),

$$P_{con\_total} = 2 \times \left(P_{con(\pm {}^{Vdc}/_{2})} + P_{con(\pm Vdc)}\right) \quad (31)$$

C. CAPACITOR VOLTAGE RIPPLE LOSSES (P_{cap})

The voltage difference between the input supply or storage voltage and the voltage across capacitor during charging intervals causes power losses called capacitor voltage ripple losses (P_{cap}). The voltage ripple across individual capacitor can be determined using the following equation [34]:

$$\Delta V_{C\_ripple,i} = \frac{1}{C_i}\int_{ta,i}^{t_{b,i}} i_{C_i}(t)dt \quad (32)$$

where $[t_a, t_b]$ and i_{Ci} are the discharging interval and the current passing through i^{th} capacitor respectively. The discharging interval of each capacitor of a 5-level single phase inverter unit is shown is Fig. 6. Therefore, losses due to capacitors ripple voltage can be obtained from the following expression [33],

$$P_{cap} = \frac{f_{ref}}{2}\sum_{i=1}^{N_{capacitor}} C_i \Delta V^2_{C\_ripple,i} \quad (33)$$

Hence, the total losses of the inverter can be obtained by summing all the losses, that is,

$$P_{loss\_total} = P_{sw} + P_{con} + P_{cap} \quad (34)$$

Finally, the efficiency of the inverter can be determined as follows,

$$\eta(\%) = \frac{P_{out}}{P_{in}} \times 100 = \frac{P_{out}}{P_{out} + P_{loss\_total}} \times 100 \quad (35)$$

IV. SIMULATION BASED PERFORMANCE ANALYSIS

The performance of the proposed three phase inverter based on simulation results carried out by MATLAB/Simulink is analyzed in this section. The simulated waveforms of three phase line voltages, phase voltages and load currents with harmonic spectral analysis are represented for three different output voltage level which are 9-level, 13-level and 39-level. The necessary figures with proper descriptions for those given level are as follows:

A. 9-LEVEL PROPOSED MLI

Each phase of a 9-level proposed three phase MLI contains 8 power switches, 3 power diodes, 4 DC bus capacitors and a DC voltage source (battery) according to the equations (1) to (4). Hence, to design all the three phases of a 9-level inverter, total required components need to be three times of the single phase leg. Following Fig. 1, a 9-level three phase inverter was designed in MATLAB/Simulink. The simulated three phase line-to-line voltage waveforms, phase voltage waveforms and load current waveforms of the 9-level inverter are shown in from Fig. 7 to Fig. 9. The frequency spectrums of the output line voltage is illustrated in Fig. 10. The value of the line voltage THD is found 6.06% for the 9-level MLI which is optimal as compared to the existing.

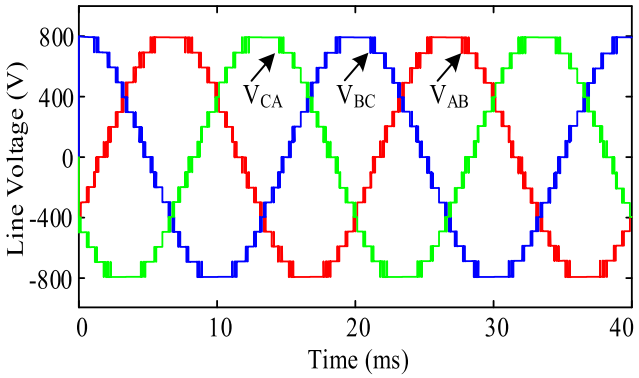

FIGURE 7. Output line voltage of the 9-level inverter (3-Ø).

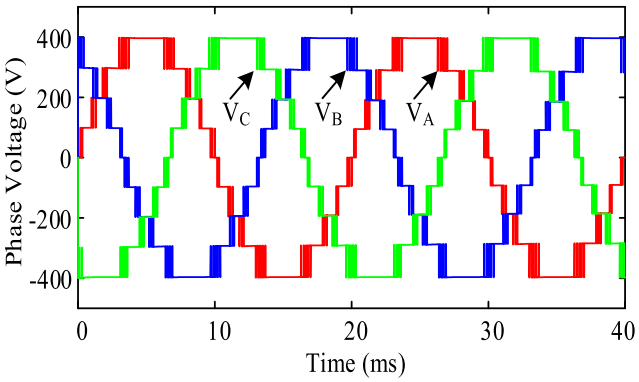

FIGURE 8. Output phase voltage of the 9-level inverter (3-Ø).

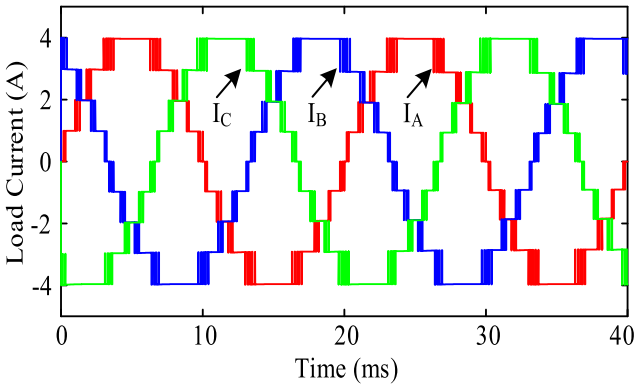

FIGURE 9. Output load current of the 9-level inverter (3-Ø).

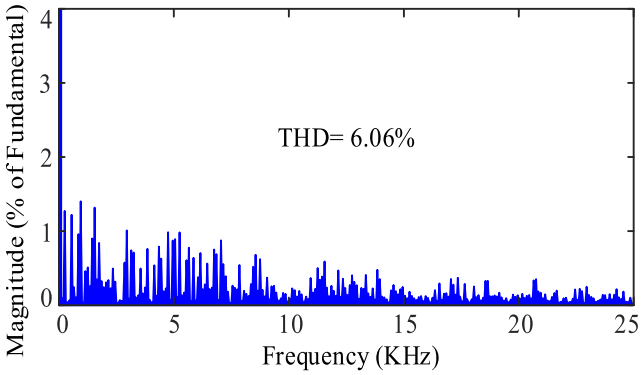

FIGURE 10. Frequency spectrums of the output line voltage.

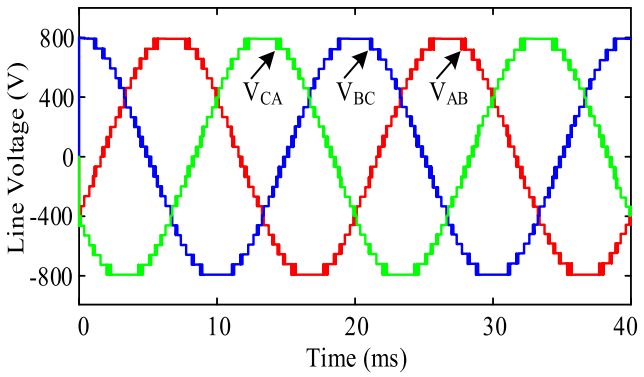

FIGURE 11. Output line voltage of the 13-level inverter (3-Ø).

B. 13-LEVEL PROPOSED MLI

In order to design a 13-level three phase proposed inverter, 3 DC voltage sources (batteries), 18 DC bus capacitors, 30 switches and 15 power diodes are needed. Using these equipment, a-13-level inverter is designed and simulated in MATLAB/Simulink. In Fig. 11, the 3-phase output line-to-line voltage is shown and Fig. 12 represents output phase voltage waveforms of the 13-level inverter. The three phase load current is illustrated in Fig. 13. Finally, the frequency spectrum of the output line voltage of the 13-level proposed MLI is exhibited in Fig. 14. The line voltage THD is measured as 4.16% without using any filter which satisfies the IEEE standard of voltage THD with filter (5%).

C. 39-LEVEL PROPOSED MLI

In this subsection, the simulated results of a 39-level proposed MLI are exhibited. The reason behind designing this higher level inverter is to analyze the line voltage THD performance. By rearranging 3 DC voltage source (batteries), 57 DC bus capacitors, 69 power switches and 54 power diodes according to Fig. 1, 39-level three phase proposed MLI can be designed. However, in Fig. 15, the three phase output line voltage waveforms is represented and Fig. 16 shows the output phase voltage of 39-level proposed MLI. The output load current is illustrated in Fig. 17 and the frequency spectrums of the line voltage of 39-level inverter is displayed in

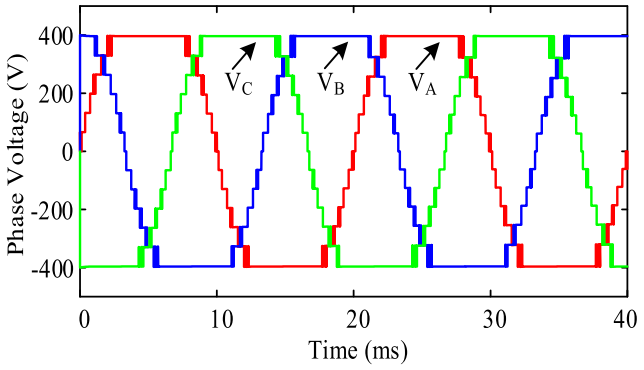

FIGURE 12. Output phase voltage of the 13-level inverter (3-Ø).

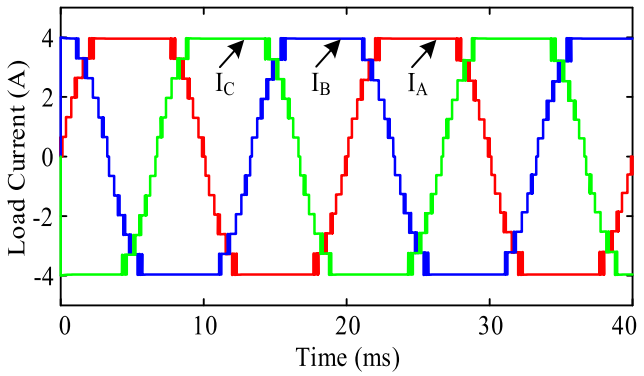

FIGURE 13. Output load current of the 13-level inverter (3-Ø).

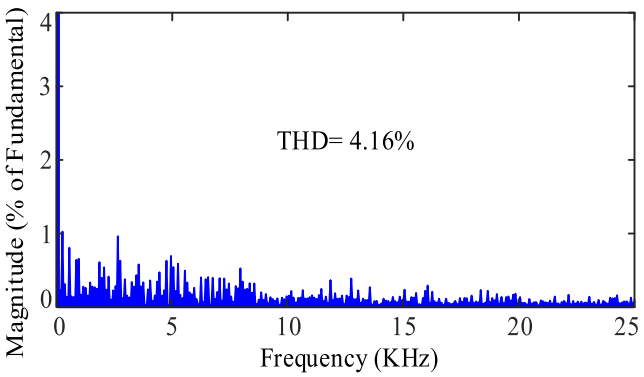

FIGURE 14. Frequency spectrums of the output line voltage.

Fig. 18. An outstanding THD performance of the line voltage is obtained from the 39-level inverter without using any filter which is 2.10% and it is obviously better than the existing topologies proposed in other papers. Further, in order to design a 39-level inverter, the proposed topology requires minimum number of components count as compared to the existing.

Therefore, from the above analysis, it can be concluded that the proposed three phase MLI topology requires reduced number of components count and provides better line voltage THD performance for a given output voltage level than other topologies.

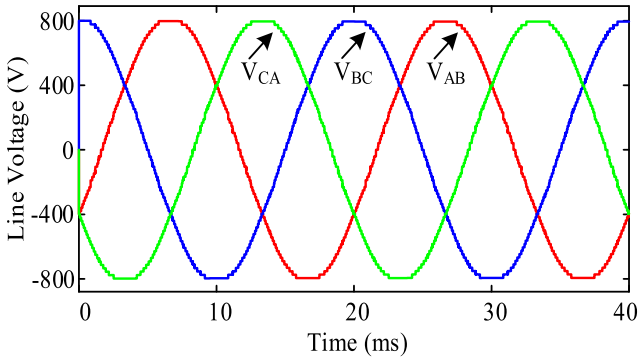

FIGURE 15. Output line voltage of the 39-level inverter (3-Ø).

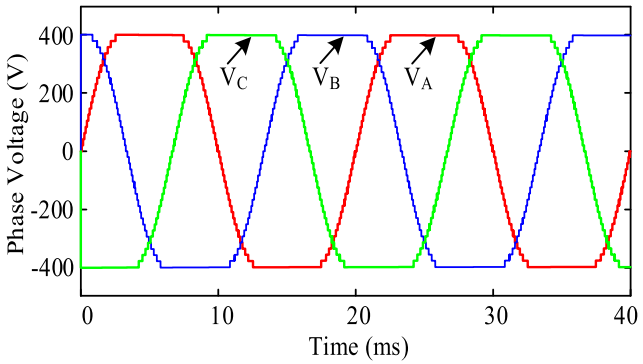

FIGURE 16. Output phase voltage of the 39-level inverter (3-Ø).

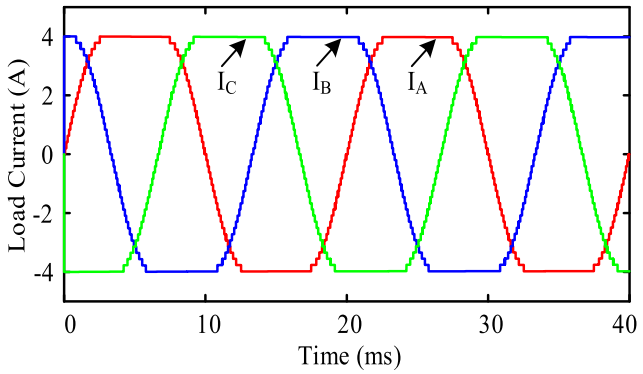

FIGURE 17. Output load current of the 39-level inverter (3-Ø).

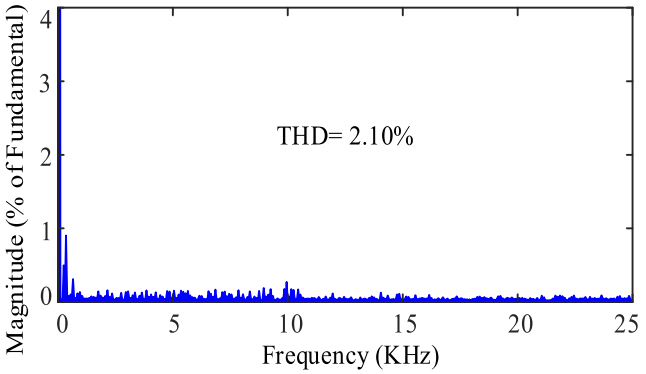

FIGURE 18. Frequency spectrums of the output line voltage.

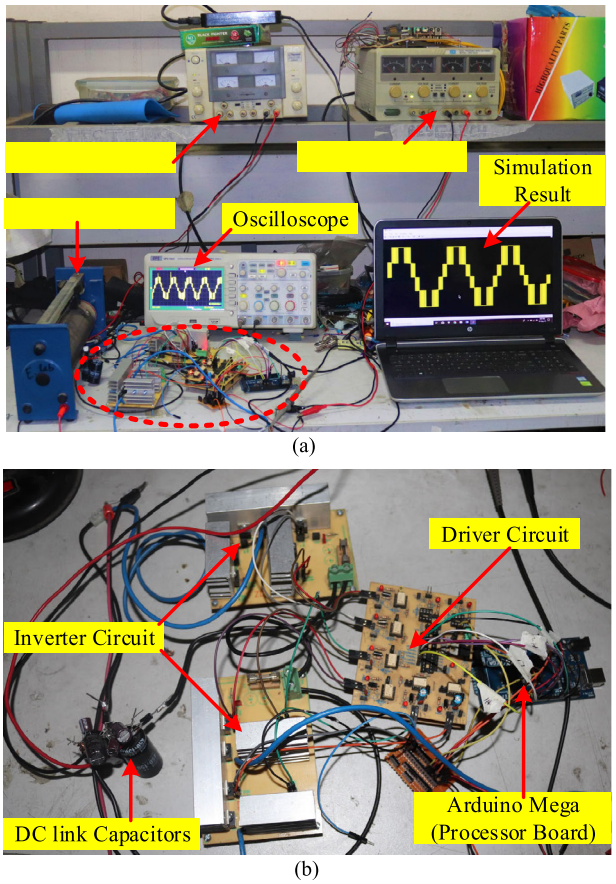

FIGURE 19. (a) Complete experimental set up for 5 level single phase proposed prototype, (b) Magnified view of the inverter and driver circuit consisting of DC link capacitors and Arduino Processor board.

V. EXPERIMENTAL RESULTS

In order to verify the theoretical explanation of the proposed inverter topology, a five level single phase laboratory prototype was implemented in the lab using a 24V DC input. Fig. 19 shows the experimental set up of the five level prototype where Arduino Mega (ATMEGA32) acts as the main pulse generating microcontroller board for the six switches. Fig. 19(b) represents the zoomed image of the marked portion within Fig. 19(a). The generated pulses were isolated and boosted up through the driver circuits made up with isolated DC-DC converters (B1212s) and optocouplers (TLP250). The boosted pulses were then applied to the gates of the power MOSFETs (STP60NF06) that act as the semiconductor switches in the proposed laboratory prototype. Two electrolyte capacitors of 4700μF were used as the DC link capacitors connected in series to divide the input DC voltage equally. A schottky diode (1N5822) was connected between the two capacitors to provide the conducting path during the generation of first level.

However, table 2 exhibits the components used to implement the prototype. The DC input voltage source (battery)

TABLE 2. Components used to implement the proposed 5 level prototype.

Parameters/Components Name	Values/Ratings
Input DC voltage (V_{dc})	24V
Number of output voltage levels	5
Output voltage frequency	50Hz
Electrolyte capacitors	4700μF
Resistive load	37Ω
Diode	1N5822 (40V, 3A)
MOSFETs	STP60NF06 (60V, 17A)
Driver/Optocouplers	TLP250
Isolated DC-DC converter	B1212S
Processor board	Arduino Mega 2560
Oscilloscope	Tektronix

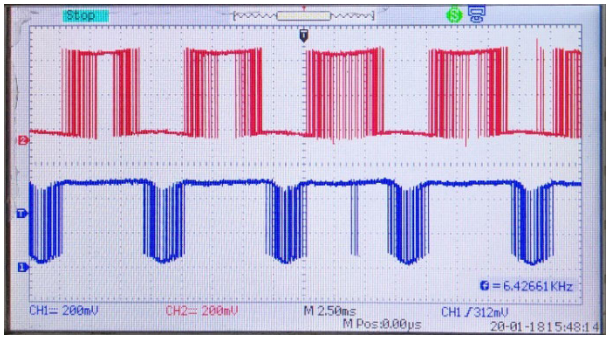

FIGURE 20. Switching pulses of S1 (lower) and S2 (upper) switches.

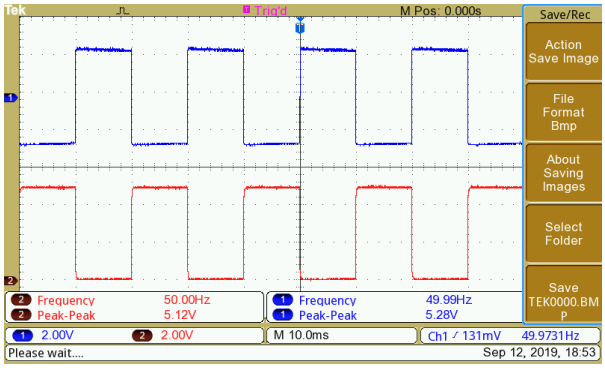

FIGURE 21. Switching pulses of Q1 & Q4 switches (lower) and Q2 & Q3 switches (upper).

can be replaced by the photovoltaic voltage generated from the solar panels connecting MPPT controller, or by the energy storage systems used for providing backup energy for low to medium voltage applications. In order to implement the three phase proposed inverter of a desired level, the equipment will be needed three times larger than that of the single phase leg and pulses must be generated using three reference signals that are out of phase by 120° each.

Nevertheless, the pulses for S_1 and S_2 switches are shown in Fig. 20. The pulses of Q_1 & Q_4 switches are identical.

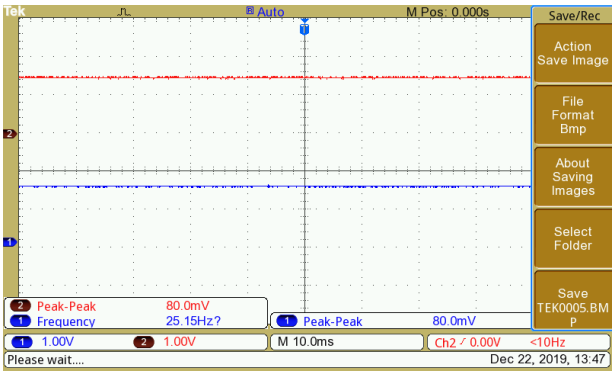

FIGURE 22. Voltage waveforms across C1 & C2 capacitors.

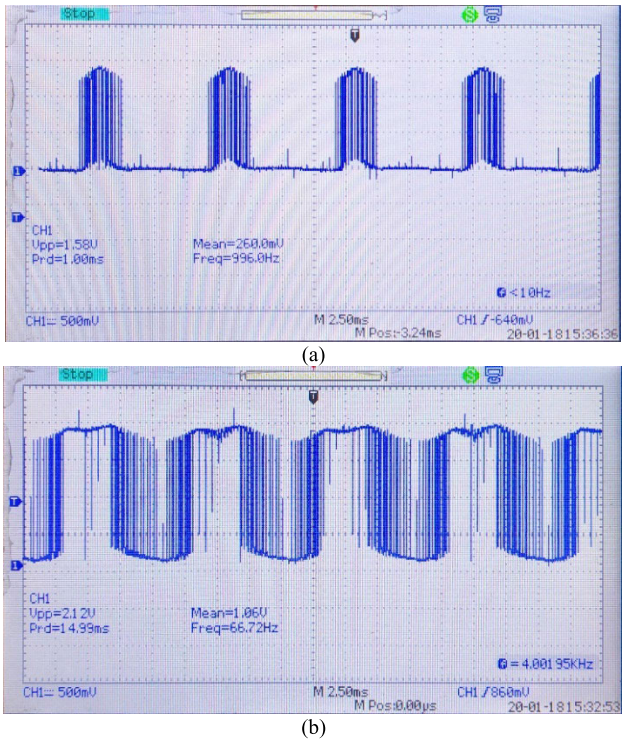

FIGURE 23. Blocking voltage across switches, (a) S2 and (b) S1.

Similarly, Q_2 & Q_3 switches use identical pulses. Thus pulses applied to the H-bridge unit are exhibited in Fig. 21.

The voltage waveforms obtained across the DC link capacitors are represented in Fig. 22. Fig. 23 exhibits the blocking voltage waveforms of *S1* and *S2* switches. Finally, the output voltage and current waveforms of the 5-level single phase prototype recorded connecting resistive load is illustrated in Fig. 24 which is quite similar to the simulated waveforms. Fig. 25 exhibits the unity power factor characteristics of the prototype. Hence, the performances of the proposed single phase 5-level unit are well validated experimentally.

VI. COMPARISON WITH THE EXISTING TOPOLOGIES

In order to demonstrate the importance of the proposed inverter, a comparative study is illustrated in this section

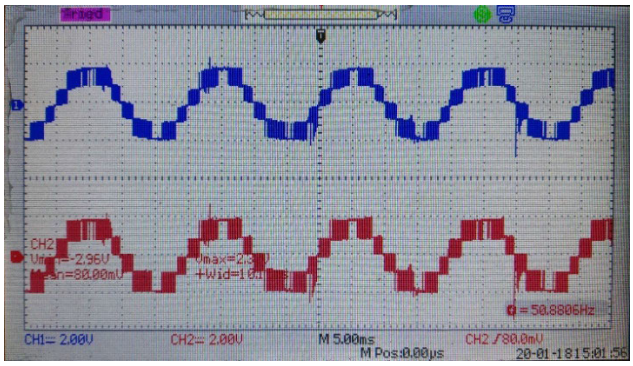

FIGURE 24. Output voltage (blue) and current (red) waveform of the 5-level proposed MLI with resistive load.

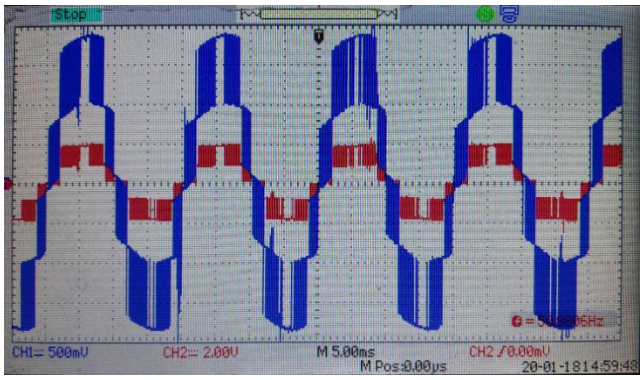

FIGURE 25. Unity power factor characteristics verification of the prototype.

TABLE 3. Comparison of the proposed topology with the existing topologies for single phase leg.

Topologies / Parameter	[35] 1981	[36] 2012	[37] 2016	[38] 2016	[26] 2017	[25] 2018	Proposed
Num. of Level	2n+1	2n+1	2n+1	12n+1	2n+1	12n+1	**2n+1**
Num. of active switch	4n	2n+4	3n+1	10n	5n-1	14n	**n+4**
Num. of capacitor	2n	n	n-1	4n	n-1	2n	**n**
Num. of diode	4n-2	2n+4	0	10n	0	14n	**n-1**
TSV ($\times V_{dc}$)	4n	2n+4	$0.5n^2+5n$	20n	5n-1	32n	**n+4**

where the proposed inverter is compared with some recently suggested inverter structures in terms of number of switch, number of diode, number of DC bus capacitor and total voltage stress of the system to generate odd level output voltage. Table 3 shows the comparison between the proposed inverter topology and the existing inverter topologies according to single phase leg to produce a definite number of levels. However, for design a three phase proposed inverter, the number of components need three times than that of the single phase leg.

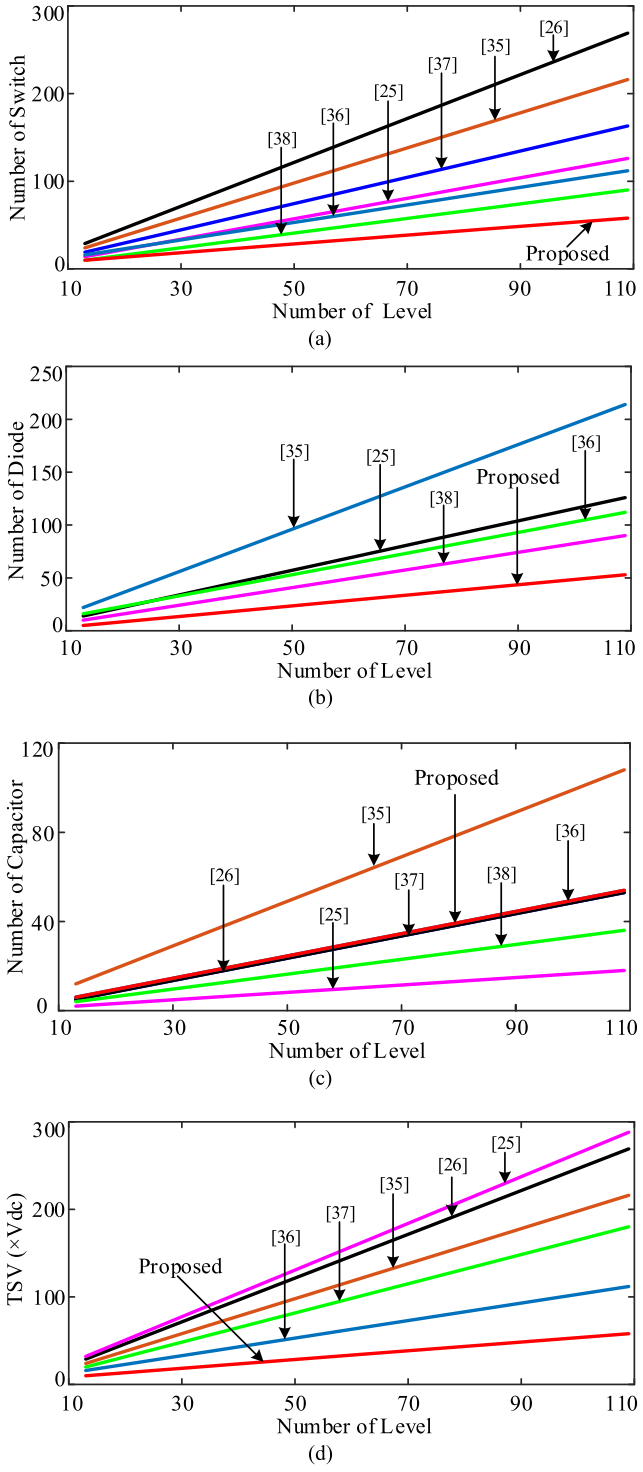

FIGURE 26. Comparison of the proposed topology (single phase) in terms of number of levels vs (a) number of active switches, (b) number of diodes, (c) number of capacitors and (d) TSV.

Using the equations listed in table III, four "number of components vs number of levels" plots are obtained which are shown in Fig. 25. Fig. 25(a) and Fig. 25(b) indicate that the proposed inverter topology requires the least number of switches and diodes respectively among all the topologies

for a definite level. The requirement of capacitors for the proposed topology is in the medium range as compared to other topologies which is illustrated in Fig. 25(c). Further, the value of TSV of the proposed inverter is lower than any other topology mentioned in Table-II for any specific level which is demonstrated in Fig. 25(d). The lower the TSV, the lower the ratings of equipment. Hence, equipment costs are reduced in the proposed structure.

Therefore, the proposed inverter topology requires least number of components which makes the size of the proposed inverter more compact. Hence, the weight becomes lighter and the power losses decrease. Further, it offers minimized equipment costs due to lower TSV and provides optimum voltage and current THDs performances. Thus, the proposed inverter has superior performance according to all the aspects.

VII. CONCLUSION

In this paper, a new three phase multilevel inverter has been introduced with proper explanations using a single energy storage or battery as the DC source per phase. In the theoretical descriptions, calculations of total number of component requirement, capacitances and losses along with the working principle and modulation scheme of the proposed inverter for a single phase leg have been illustrated with appropriate circuit diagrams and waveforms. Performances of the proposed multilevel inverter have been verified by both simulation and experimental analysis for different output voltage levels with respect to the number of capacitor count. Considering all the aspects, the proposed inverter offers the following advantages: (i) it requires a reduced number of components count than recently proposed topologies, (ii) it produces lower amount of losses resulting in an increased efficiency, (iii) it offers an optimum output voltage and current THDs performances at low switching frequency, (iv) its value of TSV for a definite level is smaller than others topologies which minimizes the voltage and current ratings of the devices resulting in reduced equipment costs. Therefore, the proposed inverter provides a compact and a light-weighted topology, fulfilling all the major demands in renewable domain or in energy storage systems for low or medium voltage and power applications.

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