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A Design of 6.8 mW All Digital Delay Locked Loop With Digitally Controlled Dither Cancellation for TDC in Ranging Sensor

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ABSTRACT This paper presents a design of 6.8 mW all digital delay locked loop (ADDLL) with digitally controlled dither cancellation (DCDC) for time to digital converter (TDC) in ranging sensors. ADDLL uses the accumulator (ACC) to control the delay of digitally controlled delay line (DCDL) during phase locking which utilizes less power and area as compared to analog delay locked loop (DLL). In the lock state, the ACC value dithers due to the closed loop operation. A digital controller is proposed to detect the lock state, performs dither cancelation and selects the optimum ACC value for controlling the delay of the replica DCDL for TDC operation. It helps the jitter reduction in the ADDLL. Additionally, it provides robustness against glitches, false locking and unlocking in a noisy environment. The ADDLL peak to peak jitter and RMS jitter at 625 MHz are 6.5 ps and 1.2 ps respectively. The ADDLL including DCDC is implemented on 0.18 μm CMOS technology with an operational range of 350∼900 MHz. It consumes only 6.8 mW at 625 MHz power with 1.8 V power supply. The area utilization is 0.06 mm^2.

INDEX TERMS All digital delay locked loop (ADDLL), digital controller, jitter, light detection and ranging (LIDAR), time to digital converter (TDC).

I. INTRODUCTION

The use of LIDAR based system is becoming significant in the design of autonomous automobiles and 3D virtual reconstruction of surrounding with very high precision [1]–[7]. To fulfill the high accuracy and resolution of distance measurement, multi-stage TDC structure is preferred for wide dynamic range. The architecture for the distance measurement for LIDAR based system is shown in Fig. 1. The digital signal processor sends the start of conversion (SOC) signal to the laser transmitter and TDC by activating SOC signal. The laser transmitter transmits the laser signal TX_L targeting the object. The transmitted laser signal is received at START receiver through internal reflection. Multiple copies of the transmitted laser signal arrives at the STOP receiver after reflection from the target and the surroundings. The digital signal processor performs the distance calculation based on received timing information from the TDC. Delay locked loops (DLLs) are typically used as multiphase clock generator and also to stabilize the timing information in TDC due to PVT variations [8]. The analog DLL consist of phase detector (PD), charge pump (CP), loop filter (LF) and voltage controlled delay line (VCDL) [9]. The architecture proposed in [10] offers better jitter performance and VCDL provides acceptable power supply rejection ratio (PSRR). However analog DLL suffers from high power consumption, long lock time and large area due to LF. To overcome the limitations of analog DLL, a semi digital DLL [11] is used which replaces

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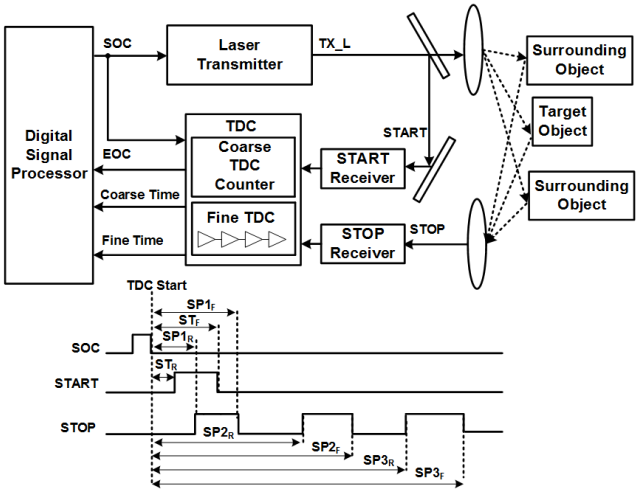

FIGURE 1. Architecture for TDC based LIDAR system.

CP and LF with an accumulator (ACC) and digital to analog converter (DAC). But it still uses VCDL and delay is controlled by an analog voltage. It shows improvement in lock time through controlling the loop gain based on phase difference and due to the DAC constant voltage it achieves a noticeable jitter improvement. However the use of 10-bit DAC increases the area and power consumption. In the lock state, the ACC is disabled and DAC provides constant value. Therefore this architecture cannot detect any phase error after the lock state. Here proposed ADDLL replaces VCDL with digitally controlled delay line (DCDL). It provides the compact size and low power performance. In ADDLL, the ACC digitally controls the DCDL to get into lock state. Due to finite fine delay resolution, when the ADDLL is in the lock state, its output phase moves back and forth of the reference clock edge. This causes dithering and increases the uncertainty at the TDC output. To overcome this issue different solutions have been proposed by adding additional control circuitry. A loop control unit (LCU) is proposed in [13] which disables the control logic when the DLL is in lock state as shown in Fig. 2 (a). This eliminates the dithering and reduces the power consumption. Drawback of this technique is lack of ability to compensate the phase errors which occur due to open loop operation thus cannot track the voltage and temperature variations or phase shift. To overcome this limitation, additional phase-error compensation block is proposed in [14] which keeps monitoring the phase error in the lock state as shown in Fig. 2 (b). When the error exceeds a threshold, the control logic is activated again and close loop operation starts which compensate the phase error due to PVT variation or phase shift. In [15], a tri-state digital phase detector (TSDPD) based DLL structure is proposed to suppress the dithering phenomenon and reduces the output peak to peak jitter for a counter-controlled digital DLL as shown in the Fig. 2 (c). The TSDPD supports three states UP, DOWN and HOLD. In HOLD the MSAR keeps its count value and then disregards the timing skew. In this way, dithering jitter is suppressed. The TSDPD prevents DDLL from

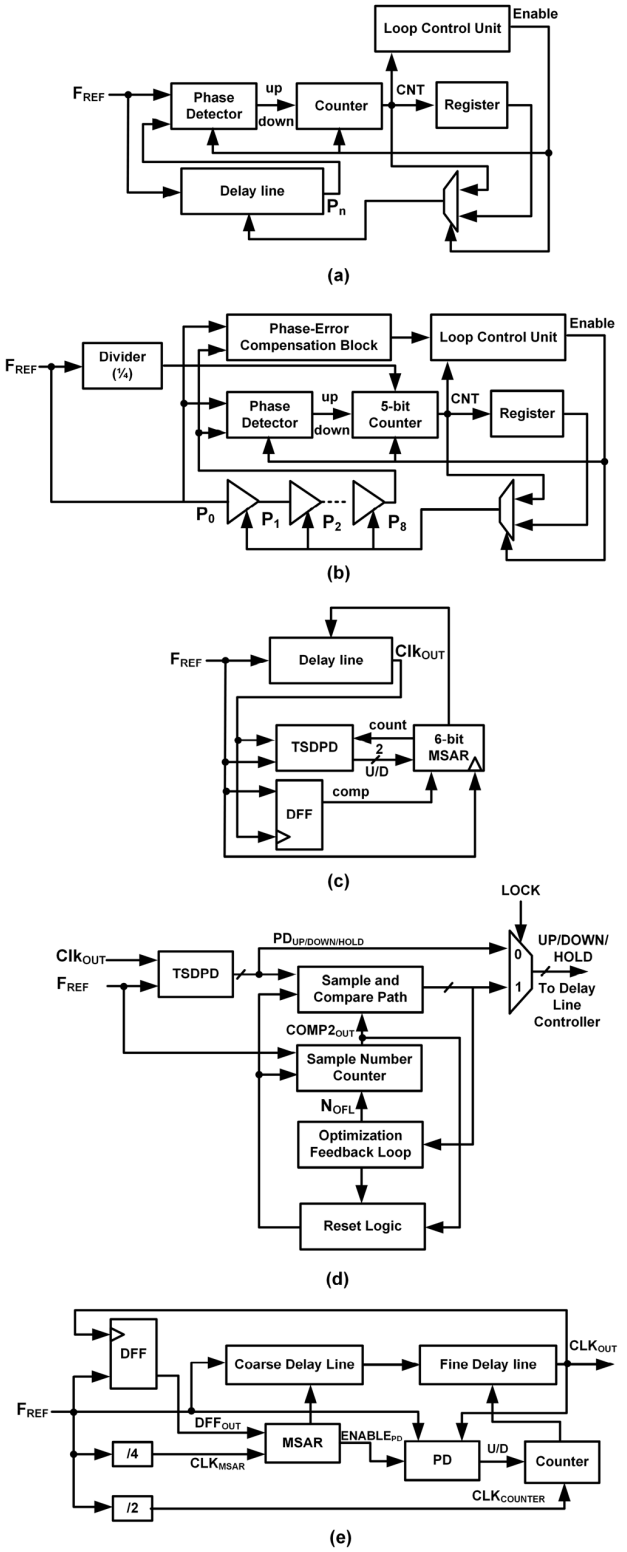

FIGURE 2. The conventional architectures to eliminate effect of dithering: (a) using LCU, (b) using phase-error compensation (c) using TSDPD (d) using DSLC (e) using dead-zone free PD with XOR-based controlled counter.

dithering larger than the input clock jitter range. However, the control code still dithers inside the input clock jitter range even though the TSDPD is used.

To overcome the limitation of TSDPD, dithering suppression loop controller (DSLC) is proposed in [16] as shown in the Fig. 2 (d). Before the lock state, the TSDPD signals are directly applied to the delay line controller. After getting into lock state, the DSLC controls the update rate of UP/DOWN/HOLD signals thus reducing the code dithering. But DSLC reduces the bandwidth of DLL in lock state and the efficiency of the DSLC depends on clock quality and PVT variations in the TSDPD. In [17] a dead-zone free PD with XOR-based controlled counter is used to reduce the jitter issue. PD is designed to detect 1ps delay difference and it only activates for fine delay line locking as shown in Fig. 2 (e). The XOR-based controlled counter keep the last value if the phase difference between the clocks is less than 1ps to reduce the dithering problem in lock state. The PVT variations in PD and fine delay line can degrade the jitter performance. Until now, in order to suppress the dithering in the lock state, controlling the PD output signals and its operation or disabling the counter is considered. In the case when the counter is disabled to avoid dithering then the counter holds value is not necessary to be optimum value for the minimum phase offset among F_{REF} and DLL_{OUT} in lock state. Also there is no method to select the optimum value of counter among two or three dithering values.

In this paper, the proposed design of DCDC can detect the lock condition by detecting the dithering and suppress it by dither cancelation algorithm. The proposed algorithm also selects the optimum values of ACC for the DCDL in the lock state. This minimizes the phase offset of the DLL in locked state. Also, it supports hysteresis limit to avoid unnecessary locking and unlocking under noise or glitches. In the case of phase error in the DLL output phase due to PVT variations, it updates the optimum value of ACC without deactivating the locking signal. Major contribution of this paper are:

- Detection of locking and unlocking state based on dithering of counter with hysteresis control for preventing false locking/unlocking due to glitches.
- Dithering cancelation by selecting a fixed optimum ACC value for the DCDL to minimize the phase offset and jitter in lock state.
- Continuous tracking of an optimum value of ACC to compensate the phase drift due to PVT or delay cell mismatches in the lock state.

Rest of the paper is structured as follows: In section II, the conventional architecture of ADDLL based TDC is discussed. Section III presents proposed architecture of ADDLL based TDC. Section IV elaborates digitally controlled dither cancellation. Post synthesis simulation and experimental results are discussed in section V. Lastly, paper is concluded in section VI.

II. CONVENTIONAL ARCHITECTURE OF ADDLL BASED TDC

The TDC comprises of delay line where the delay of each cell in the delay line can be controlled for an accurate measurement. The Fig. 3 (a) shows TDC based on VCDL [18]. This structure uses replica of VCDL for both DLL and TDC operation. DLL is tracking phase error due to any mismatch or PVT variations between the F_{REF} and the DLL output. The ADDLL based TDC structure is shown in the Fig. 3 (b). ADDLL includes DCDL, PD and ACC [19]. The UP/DN signals generated by the PD control the ACC value. The ACC value is then provided to the replica DCDL to adjust the delay for the TDC operation. When the DLL get into lock state, the ACC start toggling between two or three values which cause dithering. In case when the input clock has no jitter then this dithering cause the increase in the output clock jitter up to a maximum value of $2T_D$ where T_D is the step delay of DCDL. However, if the input clock source has jitter then the output clock jitter can be express by [17].

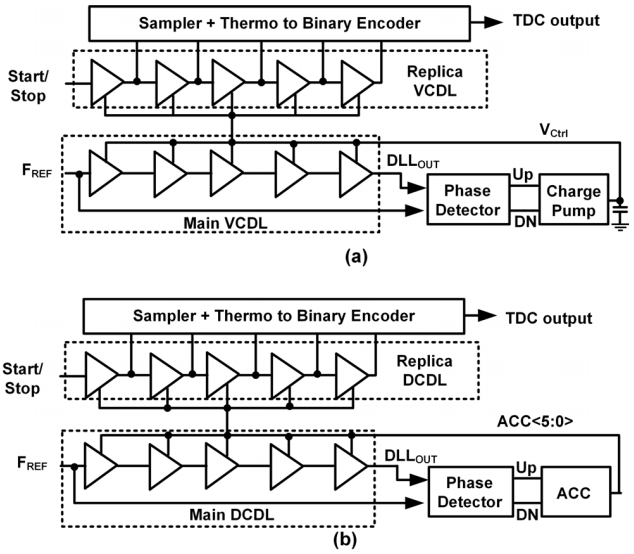

FIGURE 3. (a) Voltage control DLL based TDC. (b) ADDLL based TDC.

$$T_{J,pk-pk\_out} = T_{J,pk-pk\_in} + T_D\left(\left[\frac{T_{J,pk-pk\_in}}{T_D}\right]+1\right) \quad (1)$$

where $T_{J,pk-pk\_out,}$ is maximum peak to peak output clock jitter, $T_{J,pk-pk\_in}$ is the maximum peak to peak input clock jitter. This indicate the significant effect of input clock jitter on the output clock jitter. If $T_{J,pk-pk\_in}$ is 4.8 ps and T_D is 3 ps then $T_{J,pk-pk\_out}$ becomes 4.8+ 3(2+1)= 13.8 ps.

III. PROPOSED ARCHITECTURE OF ADDLL BASED TDC

The block diagram of proposed ADDLL based TDC is shown in the Fig. 4. A DCDC is inserted between main DCDL and the replica DCDL for the TDC operation. The main DCDL is operating in the close loop to keep tracking any PVT variation. The output of the ACC is provided to the DCDC as ACC_IN<5:0>. Based on the values of ACC_IN<5:0>, the DCDC controls the value of the ACC_OUT<5:0> and the LOCK.

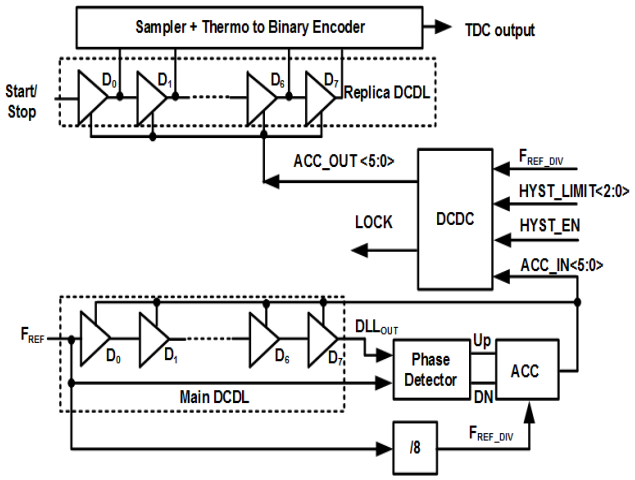

FIGURE 4. Proposed architecture of ADDLL based TDC with DCDC.

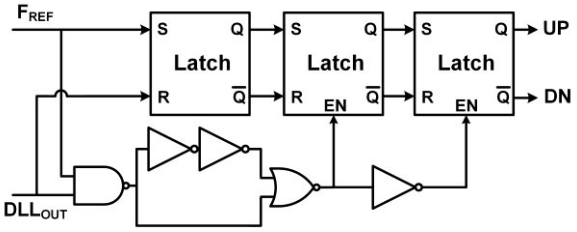

FIGURE 5. Proposed architecture of phase detector.

A. PHASE DETECTOR

A master-slave flip flop based phase detector is used as shown in the Fig. 5. The phase detector compares the rising edges of F_{REF} and DLL_{OUT} to control the ACC output values. The proposed phase detector can detect the phase errors less than 1ps at 625 MHz.

B. DIGITALLY CONTROLLED DELAY LINE

The structure of digitally controlled delay line is shown in the Fig. 6. It consist of eight delay elements and each delay element consists of two inverter stages with digitally controlled capacitive load. The capacitive load is formed by six binary-weighted capacitors. The ACC_IN<5:0> controls the switches connected to the capacitive load to adjust the delay of each delay element. The delay line provides delay from

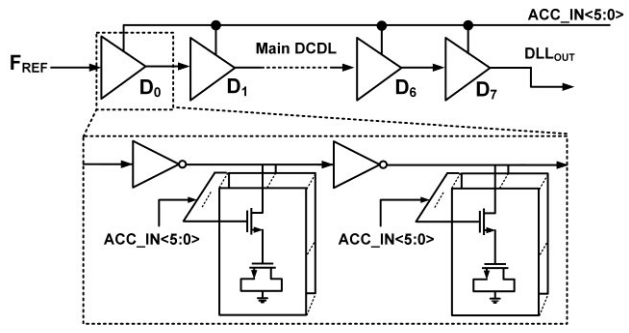

FIGURE 6. Proposed architecture of digitally controlled delay line.

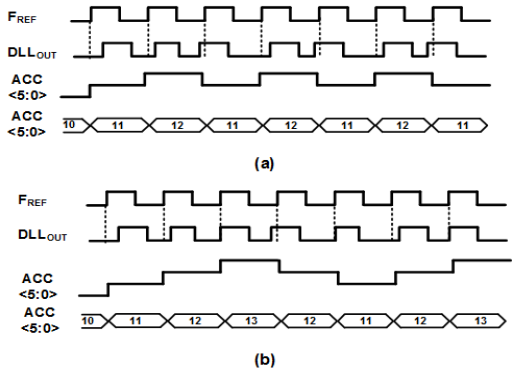

FIGURE 7. (a) ADDLL output phase dithering and ACC with lock pattern 1. (b) ADDLL output phase dithering and ACC with lock pattern 2.

105 ps to 285 ps which results in operating frequency range from 350 MHz to 900 MHz. The LSB resolution of DCDL is around 3.5 ps.

C. ACCUMULATOR (ACC)

The ACC structure is similar to proposed in [11]. The 6-bits ACC starts to count increasingly or decreasingly based on the state of the UP/DN signal from PD. The ACC for UP/DN operation, makes the second operand all zero or all one and just adjusts the input carry of the first stage. To improve the maximum operation frequency of the ACC, full-adders structure is based on carry select adder algorithm. The F_{REF} is divided by eight and then applied to ACC. This approach provides enough time to stabilize the delay in DCDL. It also reduce the power consumption and loop bandwidth during dithering effect.

D. LOCK PATTERNS IN LOCK STATE

In the lock state, the ACC values dithers in two patterns which are shown in the Fig. 7. As ACC is operating at F_{REF_DIV}, so only rising edges of F_{REF} and DLL_{OUT} are shown for the simplicity.To reduce the phase error between the F_{REF} and DLL_{OUT}, the ACC value is increased. At this point the DLL_{OUT} is lagging F_{REF} and the PD keep incrementing the ACC value. At a particular ACC value, the DLL_{OUT} leads the F_{REF}. Then the PD detects this condition and decrements the ACC value. Due to minimum LSB resolution of ACC, the DLL_{OUT} again lags the F_{REF}. This causes the dithering between two ACC values as shown in Fig. 7(a). In another case, the ACC values can dither between three values. In this case, the middle ACC value brings the F_{REF} and DLL_{OUT} phase aligned but due to the limited dead zone of PD in closed loop operation, it keeps incrementing or decrementing the ACC value until it detects lead or lag conditions. This causes the dithering among three ACC values in the lock state which is shown in the Fig. 7(b). By detecting these patterns, the lock condition can be identified in the DLL. In the Fig. 8, the generated control signals by the PD for the patterns 1 and 2 are shown. The ACC++ and ACC– indicates control signal to increment or decrement in the ACC value

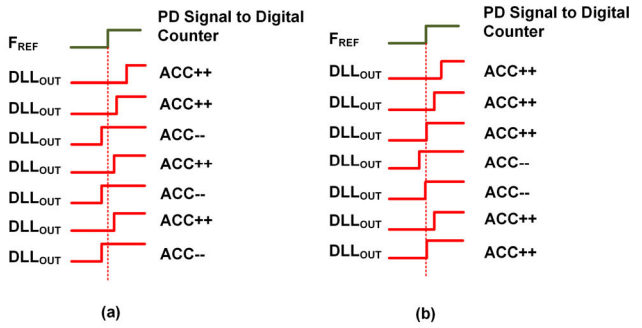

FIGURE 8. (a) Phase detector output signals with lock pattern 1. (b) Phase detector output signals with lock pattern 2.

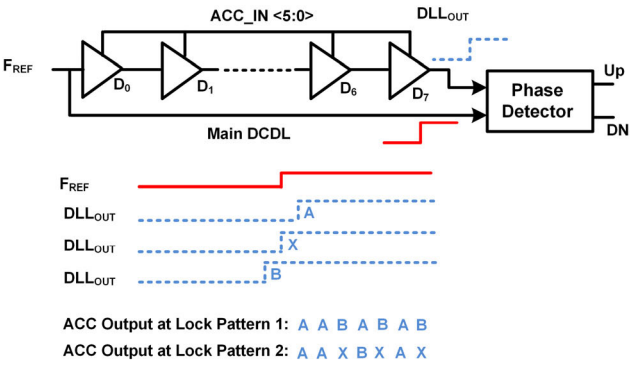

FIGURE 9. ADDLL output phase dithering patterns in the lock state.

depending on the lead or lag condition between F_{REF} and DLL_{OUT}. In the Fig. 8 (a), here we can observe that in the case of lock pattern 1, ACC++ and ACC– alternatingly applied. While for the lock pattern 2 in Fig. 8 (b), ACC++ ACC++ and ACC– ACC– are alternatingly applied. This observation is important to detect the lock condition in DLL. Now the important decision in the lock state is the selection of a particular ACC value among dithering ACC values. Consider the ACC values which causes the phase of the DLL_{OUT} lag, lead or exactly match to the phase of F_{REF} are A, B and X in the Fig. 9, respectively. During the lock pattern 1 the output of the ACC dithers between the two values A and B. In the lock pattern 2, the output of the ACC dithers between three ACC values which are A, X and B. The ACC value X aligns the phases of F_{REF} and DLL_{OUT} but cannot stay on this value due to limited detection range of PD in close loop operation. While setting the lock signal high, a fix value of ACC for the replica DCDL is needed to avoid dithering jitter in the TDC measurement results.

IV. DIGITALLY CONTROLLED DITHER CANCELLATION

The block diagram of the digital controller is shown in the Fig. 10. The ACC_IN<5:0> is sampled by the three sampling registers which gives the output D1, D2 and D3. These registers plays a critical role in the detection of the lock condition and selection of optimum value of ACC_OUT<5:0> for the replica DCDL. The dithering detection (DD) block detects the locking condition by comparing D1 and D3.

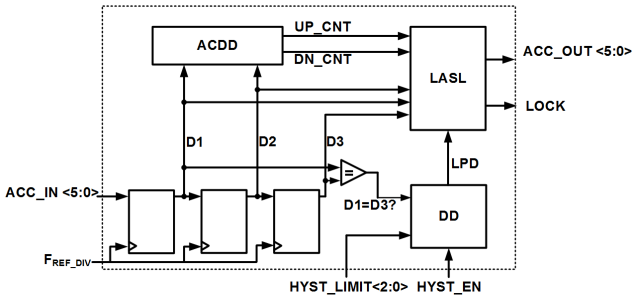

FIGURE 10. Block diagram of digital controller for DCDC.

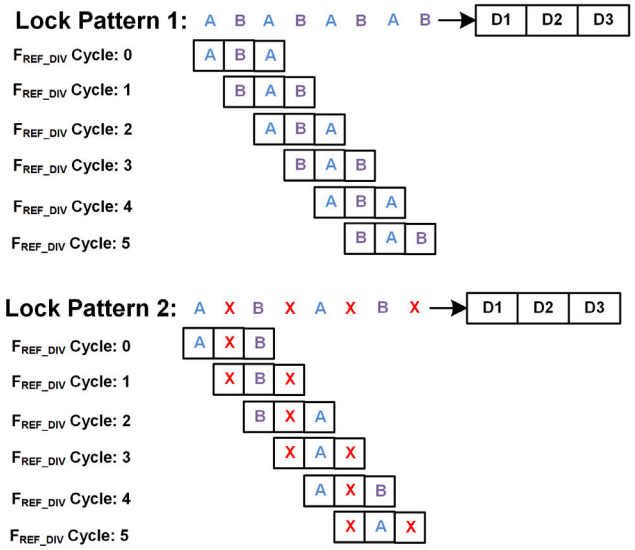

FIGURE 11. The role of values in the registers D1, D2 and D3 in lock detection and optimum ACC_OUT selection.

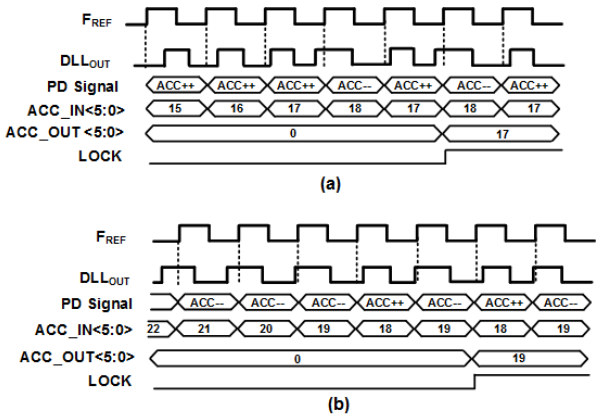

FIGURE 12. Selection of ACC_OUT<5:0> when lock pattern 1 (a) ACC<5:0> incrementing (b) ACC<5:0> decrementing.

When the lock condition is detected, a verification of the lock condition is performed if the HYST_EN is high. The HYST_EN signal enables the verification of lock condition which is performed by the hysteresis. In hysteresis, the DCDC verifies the lock condition multiple times to avoid false detection of lock and unlock condition especially in a noisy environment. The HYST_LIMT<2:0> specifies the

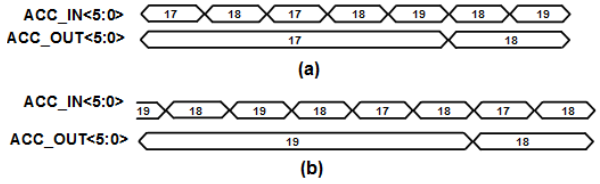

FIGURE 13. Update of ACC_OUT when lock pattern 1 (a) ACC incrementing (b) ACC decrementing.

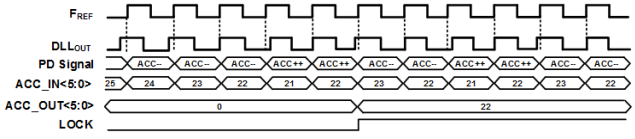

FIGURE 14. Selection of ACC_OUT when lock pattern 2.

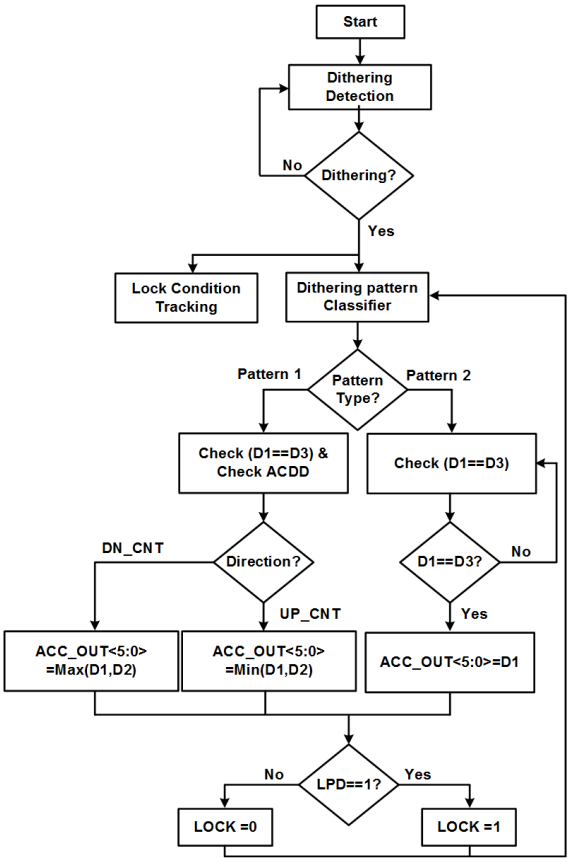

FIGURE 15. Flow diagram of the DCDC controller.

number of consecutive verifications of lock pattern. The lock condition is considered as a valid if it is verified consecutively as per HYST_LIMIT<2:0> value. Increase in the value of HYST_LIMIT<2:0> will increase the lock time but brings robustness in the detection of lock/unlocking conditions in a noisy environment. After the verification, the lock pattern detection (LPD) signal is set high. The lock and ACC selection logic (LASL) block selects the optimum ACC_OUT value for the replica DCDL. The ACC counting direction detection (ACDD) block detects the counting direction of ACC in tracking loop and activates the UP_CNT

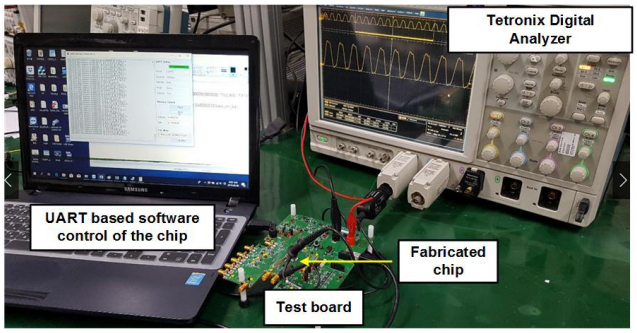

FIGURE 16. Chip measurement setup.

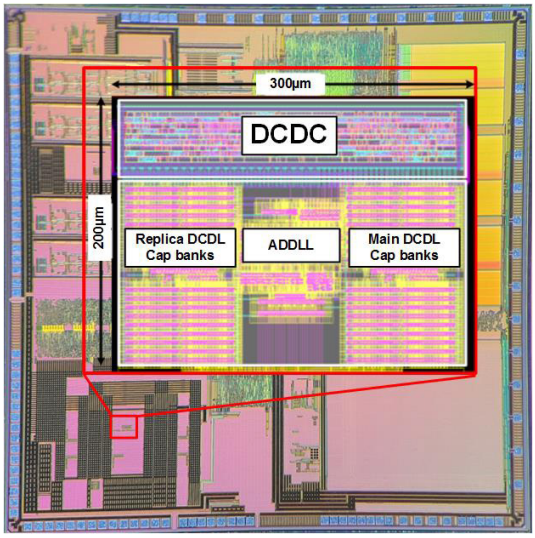

FIGURE 17. Chip Photo of the proposed DCDC based TDC.

and DN_CNT signals accordingly. The optimum value is provided at ACC_OUT and the LOCK signal is set high. The Fig. 11 explains the role of values in the registers D1, D2 and D3 for the process of lock detection and optimum ACC_OUT selection. The ACDD block detects the direction of the ACC_IN<5:0> by monitoring the values in D1 and D2. If the D1 value is greater than the D2 then ACC_IN<5:0> is considered as incrementing. Similarly, if the D1 is less than the D2 then ACC_IN<5:0> is considered as decrementing. The selection process of optimum value for ACC_OUT<5:0> in the case of lock pattern 1 is shown in the Fig. 12. In the Fig. 12 (a), first consider the ACC_IN<5:0> is incrementing initially. In the example as initially the ACC_IN<5:0> value is 15, the PD keeps generating ACC++ signal to increment the ACC_IN<5:0> value. When the ACC_IN<5:0> value reaches at 18 then the PD generates ACC– signal to decrement the ACC_IN<5:0> value. In the next cycle, the phase of DLL_{OUT} again lags the F_{REF} thus causes PD to generate the ACC++ signal. Here the ADDLL starts dithering between ACC_IN<5:0> values 17 and 18. As the ACC_IN<5:0> initially increments its value thus minimum value of 17 is selected as the ACC_OUT<5:0>. In Fig. 12 (b), the ACC_IN<5:0> is initially decrementing to track the phase of DLL_{OUT}, thus

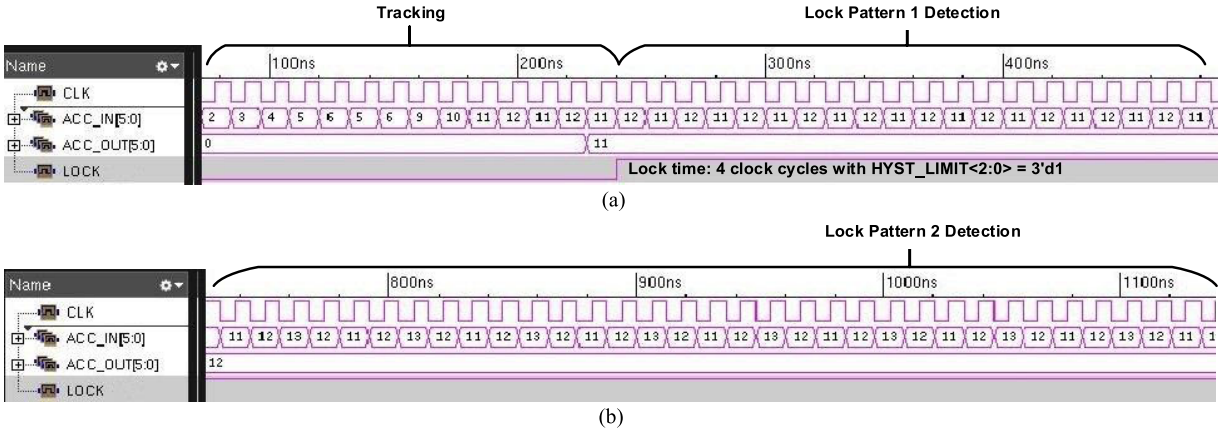

FIGURE 18. (a) Detection of lock pattern 1 and selection of ACC_OUT value. (b) Detection of lock pattern 2.

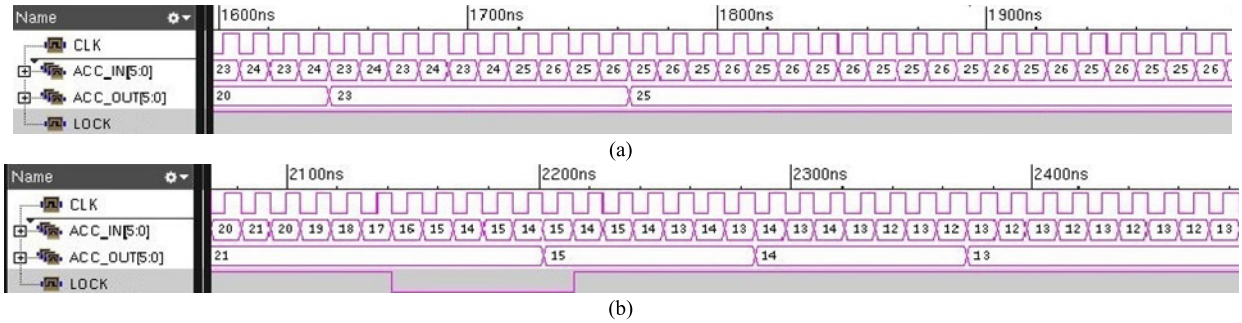

FIGURE 19. (a) Update of ACC_OUT by DCDC due to PVT variation when ACC_IN count up. (b) Update of ACC_OUT by DCDC due to PVT variation when ACC_IN count down.

maximum value of 19 is selected as the ACC_OUT<5:0> in the dithering condition. Due to PVT variation, any drift in the ACC_IN<5:0> values while in the lock state, the LSAL keeps updating the ACC_OUT<5:0> value for the minimum phase offset between DLL_{OUT} and F_{REF} as shown in the Fig. 13. In the case of lock pattern 2, the selection of the value for ACC_OUT<5:0> is shown in the Fig. 14. Here the initial ACC_IN<5:0> counting direction is not important. In this case, the LASL block selects the value of 22 for the ACC_OUT<5:0> to keep the minimum phase offset between DLL_{OUT} and F_{REF}. The operational flow of the DCDC is shown in the Fig. 15. At the start, it check for the dithering condition by comparing the values D1 and D3. In the case of successful detection of dithering, the controller starts two parallel tasks; Lock condition tracking and dithering pattern classifier. In the dither pattern classification, the controller detects the type of dithering pattern. In the case of dithering pattern 1, the values D1 and D3 are compared along with the output of ACDD. If ACC_IN<5:0> is counting up then maximum value among D1 and D2 is assigned to ACC_OUT<5:0> otherwise minimum value among D1 and D2 is assigned to ACC_OUT<5:0>. For the case of dithering pattern 2, only the values D1 and D3 are compared. If the values D1 and D3 are similar then the value D1 is assign to ACC_OUT<5:0>. After this LPD signal is checked for the activation of LOCK signal.

V. EXPERIMENTAL RESULTS

The DCDC based ADDLL is designed and fabricated in 0.18 μm CMOS technology. The DCDC operates at 1.8 V and consumes 463 uA. A test board for the measurement of the fabricated chip is designed and chip measurement setup is shown in the Fig. 16. The measurement setup consists of DCDC test board, Tetronix digital analyzer, and UART based software to configure internal registers of the fabricated chip. The chip photograph of the DCDC based ADDLL is shown in the Fig. 17. It occupies the area 200 $\times$ 300 μm^2. It consists of main DCDL with ADDLL, replica DCDL and the DCDC digital logic. The simulation results for the operation of DCDC are shown in the Fig. 18. In the Fig. 18 (a), while tracking the F_{REF}, the ACC_IN<5:0> is incrementing in the main DCDL. The ACC_OUT<5:0> for the replica DCDL is fixed and initialized to zero. When the main DCDL gets into lock state and DCDC detect the lock pattern 1, it selects the optimized ACC_OUT<5:0> value for the replica DCDL. It takes two clock cycles for HYST_LIMIT<2:0> = 3'd1 and two clock cycles for DCDC to detect the lock condition and setting LOCK signal high. In the Fig. 18 (b) the detection of lock pattern 2 is shown. The stable value at the ACC_OUT<5:0> significantly reduces the jitter in the replica DCDL. The Fig. 19 (a) shows the effect of PVT variation in the main DCDL. The dithering values in the ACC_IN<5:0> is keep increasing to track the PVT variation. The DCDC selects the optimum value for the replica DCDL and the LOCK

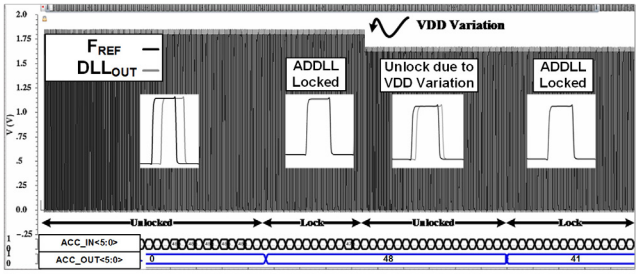

FIGURE 20. DCDC response with applying VDD variation after the lock.

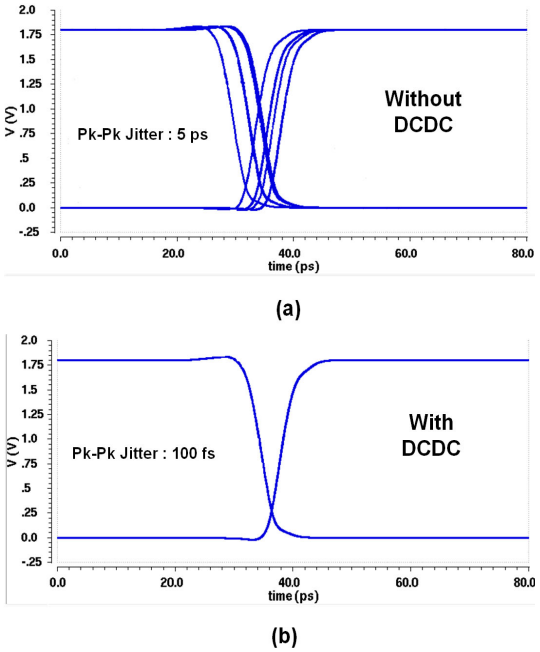

FIGURE 21. Effect of DCDC on the jitter in the ADDLL in simulation. (a) Without DCDC (b) with DCDC.

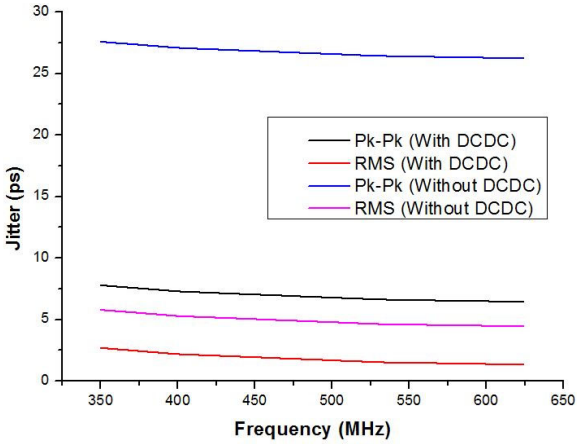

FIGURE 22. Jitter performance of ADDLL in measurement from 350 MHz to 625MHz.

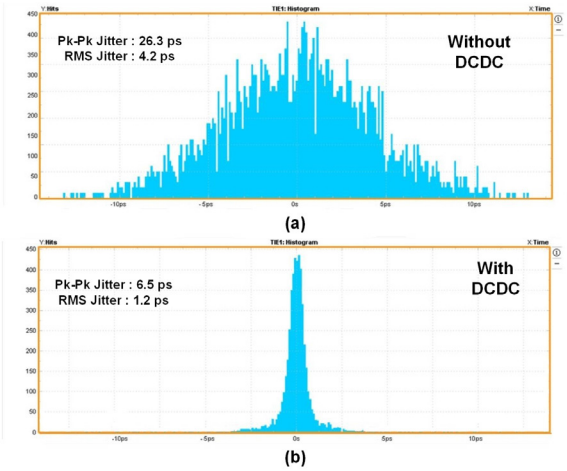

FIGURE 23. Measurement result for jitter performance of ADDLL (a) without DCDC (b) with DCDC.

signal stays high to avoid unnecessary locking and unlocking condition. The Fig. 19 (b) shows the condition where ACC_IN<5:0> is decreasing its value to track the PVT variation. When the DCDC detects the loss of dithering, it sets the LOCK signal low. The ACC_OUT<5:0> value for the replica DCDL remains stable to previous value. When the DCDC detects the new dithering and identifies the lock pattern 1 then it updates the ACC_OUT value with the new optimized value. The Fig. 20 shows the response of the DCDC under VDD variations. Due to the variation in the VDD, the DLL_{OUT} is no longer in lock state with the phase of F_{REF}. The DCDC avoids unnecessary variation in the ACC_OUT<5:0> for replica DCDL during the tracking phase of main DCDL. The simulation results exploring the effect of the DCDC on the jitter of replica DCDL are shown in the Fig. 21. The Fig. 21 (a) shows the jitter at the output of the replica DCDL when DCDC is not applied. This jitter is mainly due to the closed loop operation of the ADDLL. DCDC removes the dithering in the lock sate and effectively reduces the jitter at the replica DCDL as shown in the Fig. 21 (b). The performance comparison is shown in the Table 1. The operational range of the ADDLL is from 350 MHz to 900 MHz. The peak to peak jitter at 625 MHz is 6.5 ps. While the RMS jitter is 1.2 ps at 625 MHz operating frequency. The core area of proposed ADDLL is 0.06mm^2. The power consumption of ADDLL at 625 MHz is 6.8 mW. The figure of merits (FOMs) defined in [20] for area and power are given by

$$FOM_{AREA} = \frac{ActiveArea(mm^2)}{ChannelLength^2(\mu m^2)} \tag{2}$$

$$FOM_{POWER} = \frac{PowerConsumption(\mu W)}{OperatingFrequency(MHz) \times Voltage^2(V^2)} \tag{3}$$

In the comparison Table 1, FOM_{AREA} and FOM_{POWER} is calculated for each paper and compared with proposed ADDLL design. Lower values of FOM_{AREA} and FOM_{POWER} indicates the better design performance. Due to the use of DCDC in the ADDLL, it shows better jitter performance than previous works. Due to replica design of DCDL, the area and power consumption is increased but still the performance is comparable with previous designs and suitable for low

TABLE 1. Performance comparison.

	ISSCC 2003 [13]	JSSC 2009 [14]	JSSC 2007 [15]	JSSC 2007 [21]	VLSI 2015 [22]	TCAS-1 2018 [17]	This work
Technology (μm)	0.15	0.09	0.13	0.18	0.13	0.13	0.18
Architecture	ADDLL	ADDLL	ADDLL	SAR DLL	TDC based DLL	ADDLL	ADDLL
Supply(V)	1.6	1	1.5	1.8	1.5	1.2	1.8
Pk-Pk Jitter (ps)	40@3.5GHz	9.5@2GHz	14@2.5GHz	32.9@40MHz	10@180MHz	12@3.3GHz	6.5@625MHz
RMS Jitter (ps)	NA	1.6@2GHz	NA	3.96@40MHz	2.3@180MHz	1.63@3.3GHz	1.2@625MHz
Operating Frequency (MHz)	2100-3500	1400-2000	1500-2500	40-550	80-450	1500-3300	350-900
Power (mW)	70	7@2GHz	30@2.5GHz	12.6@550MHz	26@180 MHz	7	6.8@625MHz
Area (mm^2)	0.14	0.037	0.03	0.2	0.08	0.0077	0.06
FOM_{AREA}	6.22	4.57	1.78	6.17	4.73	0.46	1.85
FOM_{POWER}	7.81	3.5	5.33	7.07	64.2	1.47	3.35

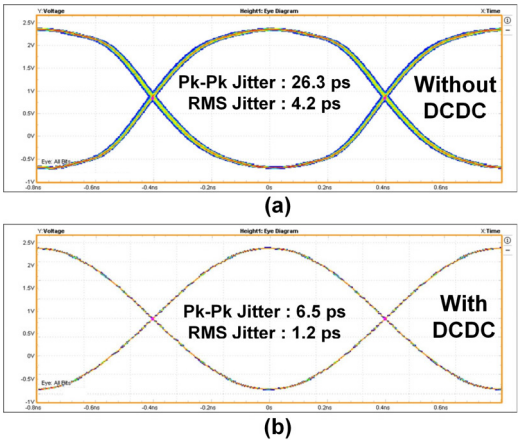

FIGURE 24. Eye diagram in measurement for jitter performance of ADDLL (a) without DCDC (b) with DCDC.

jitter application like TDC. The jitter performance of the proposed ADDLL over full operational frequency range is shown in the Fig. 22. The jitter reduces as the operating frequency of the ADDLL is increased. The jitter measurement results of the ADDLL is shown in the Fig. 23. The jitter in the replica DCDL when the DCDC is disabled is shown in the Fig. 23 (a).

When the DCDC is operating then the jitter in the replica DCDL is reduced which is shown in the Fig. 23 (b).The eye diagram for the jitter performance of replica DCDL is shown in Fig. 24. The Fig 24 (a) shows the performance without the DCDC activation while the Fig 24 (b) shows improvement in the jitter performance when DCDC is activated.

VI. CONCLUSION

This paper proposed a design of 6.8 mW all digital delay locked loop (ADDLL) with digitally controlled dither cancellation (DCDC) for time to digital converter (TDC). The proposed DCDC design reduces the jitter in replica DCDL while continuously compensates the PVT variations. The experimental results show that proposed design provides robustness and reduces the jitter for the TDC operation. The ADDLL including DCDC is implemented on 0.18 μm CMOS technology and operates in the range of 350-900 MHz. It consumes only 6.8 mW@625 MHz power at 1.8 V power supply. The area utilization is 0.06 mm^2.

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