IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received March 4, 2020, accepted March 11, 2020, date of publication March 23, 2020, date of current version April 7, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2982738

A Systematic Method to Design Efficient Ternary High Performance CNTFET-Based Logic Cells

AREZOO DABAGHI ZARANDI[1], MOHAMMAD REZA RESHADINEZHAD[1], AND ANTONIO RUBIO[2], (Senior Member, IEEE)

[1]Faculty of Computer Engineering, University of Isfahan, Isfahan 8174673441, Iran
[2]Department of Electronic Engineering, Polytechnic University of Catalonia (UPC), BarcelonaTech, 08034 Barcelona, Spain

Corresponding author: Mohammad Reza Reshadinezhad (m.reshadinezhad@eng.ui.ac.ir)

ABSTRACT The huge quantity of nodes and interconnections in modern binary circuits leads to extremely high levels of energy consumption. The interconnection complexity and other issues of binary circuits encourage researchers to consider multiple-valued logic (MVL) alternatives. Features of Carbon Nanotube Field-Effect Transistors (CNTFETs) make this technology a potential candidate to implement MVL circuits. In this article, a new systematic methodology is proposed to design ternary logic block circuits based on CNTFETs. The methodology is applied to the design of two basic logic circuits, a half adder and a 1-digit multiplier, which are evaluated through HSPICE simulations. Simulation results indicate improvements over current equivalents in transistor count and PDP mean with the half adder version of 19.2%, and 74.07% respectively, and with the 1-digit multiplier of 24.67% and 81.12% respectively.

INDEX TERMS CNTFET, MVL, ternary, half adder, multiplier.

I. INTRODUCTION

According to Moore's law, chip transistor counts have approximately doubled every two years over the last decades with technology scalability. Complementary Metal Oxide Semiconductor (CMOS) technology faces major problems such as short channel effects [1], high current leakage, decreasing gate control and high lithography costs, etc., when scaled down near to nanometers [1]. Scientists and researchers seek to find alternatives to the traditional CMOS process [2]–[4], to overcome the above mentioned problems.

To find replacements for the CMOS technology, many devices and techniques are being introduced and evaluated by researchers, such as Spin-wave architecture, Single-electron devices, Quantum Computing etc. [2], [3]. Among the existing new techniques, CNTFET is one of the demonstrated alternatives to CMOS transistors, which operates satisfactorily [5], [6]. It reduces transistor size and power consumption and increases the performance compared to current equivalents. These advantages are achievable due to its intrinsic attributes including the high mobility of P-CNTFET and N-CNTFET, and low off-current [7].

In a modern VLSI circuit, about 70 % of the area is occupied by interconnections [7]. This volume of interconnections leads to many restrictions in fabricating and implementing the binary circuits and can be a source of failures. According to [7], MVL is one of the most suitable techniques for improving the value and data transferability in binary systems, which reduces the complexity of interconnections and achieves high-energy efficiency in comparison with traditional binary circuits. One of the characteristics of CNTFETs is that they manifest different threshold voltages (V_{th}), a variable related to nanotube diameter, and this feature makes them an optimal candidate to implement MVL circuits [7].

In this article, based on the potential of CNTFET ternary circuits, we propose a systematic methodology to implement optimized circuits in terms of power consumption, transistor count and delay.

The rest of this article is organized as follows: CNTFET and MVL are briefly reviewed in Section II, the state of the art of basic ternary circuits proposals is explored in Section III, the new methodology is proposed in Section IV, detailed design of a half-adder is presented in Section V, results and comparisons with other research are discussed in Section VI and Section VII concludes on the methodology design and improvements.

II. CNTFET TECHNOLOGY AND MVL CIRCUITS REVIEW

A. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Carbon Nanotubes (CNT), discovered by Iijima [12], have been the focus of nanoelectronics scientists and engineers

The associate editor coordinating the review of this manuscript and approving it for publication was Chaitanya U. Kshirsagar.

for a long time. Due to their relatively small dimensions and unique morphologies, they constitute an attractive emerging alternative to modern binary circuits.

CNTs are made up of narrow strips of a tiny graphite sheets rolled into a tube shape. Depending on the number of sheets in the construction, CNTs can be multi-wall (MWCNT) or single-wall (SWCNT) types.

The arrangement of the carbon atoms in the tube sheet is specified with a chiral vector $ch = n_1a_1 + n_2a_2$, in which a_1 and a_2 are two vectors for the hexagonal lattice and the two indexes (n_1,n_2) are determined according to the rolling orientation of the sheet. Three different SWCNT behaviors are determined by the chiral vector: a) the zigzag nanotube, when $n_1 = 0$ or $n_2 = 0$; b) the armchair nanotube when $n_1 = n_2$ and c) the chiral nanotube when $n_1 \neq n_2 \neq 0$. The electricity conducting attribute of the SWCNT is based on the chiral vector, behaving as a semiconductor if the two indexes n_1 and n_2 fit the relation $n_1 - n_2 \neq 3i$ (where i is an integer) [9].

Electrical properties of a SWCNT semiconductor make it ideal for controlling the conductance channel in a CNT transistor. Consequently, transistor channels can be constructed of the SWCNT type instead of bulk silicon, which is used in traditional CMOS transistors. By positioning the CNT as a channel in the field-effect transistor, a new device is devised, generally known as CNTFET [10] or tube-FET [9].

Considering the chiral vector, the diameter of the CNTFET tube D_{CNT} is calculated through Equation (1):

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_1n_2 + n_2^2}}{\pi} \tag{1}$$

where a is the inter-carbon-atom distance of approximately 0.249 nm [4].

The V_{th} is determined by Equation (2):

$$V_{th} = \frac{aV_\pi}{\sqrt{3}\, eD_{CNT}} \tag{2}$$

where, V_π is a constant parameter which determines the carbon π-π bound energy in tight bonding with a value of 3.033 eV and e is the electron charge [10]; the V_{th} has an inverse relation with tube diameter and varies with the tube diameter derived from n_1 and n_2. This feature, together with other advantages of CNTFETs such as fine pitch and excellent device characteristics, makes them promising candidates for replacing silicon CMOS transistors. In this paper, devices with four different chiral vectors are used; the corresponding threshold voltages related to these chiral vectors are reported in Table 1.

B. MULTIPLE-VALUED LOGIC UNITS

Designing a sizable area of VLSI circuits with lots of interconnection requires consideration of challenges such as increasing the manufacturing complexity and power consumption. Over the last decades, the MVL ternary logic has been shown to have better characteristics than binary circuits, positioning it as a compelling alternative. These characteristics are: increased data processing capability per unit area and increased flexibility and speed of the circuit combined with lower power dissipation, lower interconnection complexity and lower active devices count inside a chip [7].

TABLE 1. The threshold voltage of the four chiral vectors used.

Chiral Vector (n_1 ,n_2)	Threshold Voltage (V)
(8,0)	0.7
(10,0)	0.56
(19,0)	0.3
(29,0)	0.2

TABLE 2. The truth table of the NTI, STI and PTI.

Input X	NTI (Y_0)	STI (Y_1)	PTI (Y_2)
0	2	2	2
1	0	1	2
2	0	0	0

One of the most applicable MVL systems is the Voltage mode ternary logic system, consisting of three logic states '0', '1' and '2', corresponding with GND, $\frac{Vdd}{2}$ and Vdd, respectively. The basic ternary gate is structured with one input (x) and three outputs Y_0, Y_1 and Y_2, which are the symbols of Negative, Standard and Positive ternary inverter operations (NTI, STI and PTI respectively). The equations for these inverters are expressed in Equation (3). The related truth-table is shown in Table 2 [11].

$$\begin{aligned} Y_0 &= \begin{cases} 2, & if\ x = 0 \\ 0, & if\ x \neq 0 \end{cases} \\ Y_1 &= \bar{x} = 2{-}x \\ Y_2 &= \begin{cases} 0, & if\ x = 2 \\ 2, & if\ x \neq 2 \end{cases} \end{aligned} \tag{3}$$

Equation (4) expresses the fundamental function for ternary logic gates AND, NAND, OR and NOR.

$$\begin{aligned} Y_{AND} &= X_i.X_j = min\{X_i, X_j\} \\ Y_{NAND} &= \overline{min\{X_i, X_j\}} \\ Y_{OR} &= X_i + X_j = max\{X_i, X_j\} \\ Y_{NOR} &= \overline{max\{X_i, X_j\}} \end{aligned} \tag{4}$$

where, both X_i and X_j are variables exhibiting one of the three values of '0', '1' and '2' [18].

The truth tables of two-input ternary NAND and NOR gates are tabulated in Table 3.

The most straightforward implementation of NTI, STI and PTI with low count transistors and low power consumption [13] is shown in Fig. 1, where A is the input variable.

III. PREVIOUS WORKS

Several studies have designed different ternary CNTFET-based circuits; the primary arithmetic circuits presented in these works are of the types half adder and 1-digit multiplier, focusing on the implementation of efficient circuits in terms of transistor count [7], [8], delay [12] and power, [14]–[18].

TABLE 3. The truth table of two-input ternary NAND and NOR gates.

Input X_i	Input X_j	Y_{NAND}	Y_{NOR}
0	0	2	2
0	1	2	1
0	2	2	0
1	0	2	1
1	1	1	1
1	2	1	0
2	0	2	0
2	1	1	0
2	2	0	0

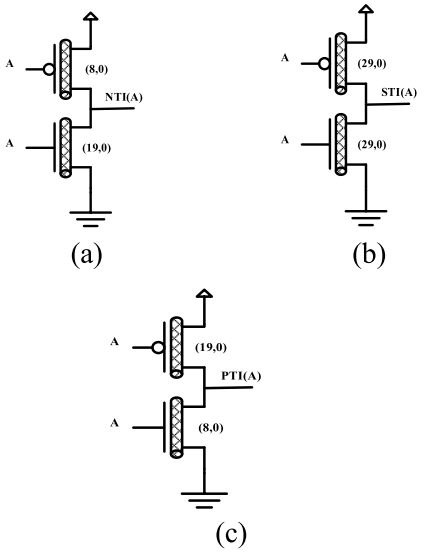

FIGURE 1. Transistor level of (a) NTI (b) STI (c) PTI [13].

A ternary half adder has been designed by applying a ternary decoder and basic ternary logic gates by Dhande and Ingole [8]. Other designs used binary common logic gates instead of ternary logic gates to implement a ternary half adder [7], [8]. Methods presented by Lin *et al.* [7] and Dhande and Ingole [8] use a high number of transistors. In digital designs, high transistor count increases power consumption and design complexity.

A ternary half adder and 1-digit multiplier have been developed by Tabrizchi *et al.* [12] using the pull up-down and pass transistor methods, applying the decoder of [7]. Power consumption and transistor count of these designs are low, due to the decoding of one of the inputs in ternary values while the delay is high, because in the output paths, pass transistors are applied.

Further designs of a ternary half adder and a 1-digit multiplier using pass transistors with a lower transistor count, but high power consumption and delay have also been proposed by Srinivasu and Sridharan [14].

The design proposed by [7] has been revised for two further ternary half adder designs: 1) by adding an optimized transistor level implementation for three AND and one OR gates, which reduced the transistor count and 2) with an optimized ternary decoder which uses 8 transistors, (the ternary decoder introduced by [7] and [8] used 16 transistors). The ternary half adder of Sahoo *et al.* [15] is superior in terms of transistor count and performance in comparison with [7] and [8], but its power consumption is high.

A whole methodology to design each ternary circuit has been proposed by Kim *et al.* [16], although how to determine the chiral vector of each transistor is unclear and the circuits consume high power, caused by paths that connect the power supply node to GND.

Half adder and 1-digit multiplier versions with STI, ternary NAND have low power consumption but use a large number of transistors, Jaber *et al.* [17].

Finally a ternary half adder has been designed with the multiplexer-based method, using pass transistor methods, NTI and PTI gates by Jaber *et al.* [18]. Transistor count and delay of this half adder are high, while it is optimum in terms of power consumption.

IV. PROPOSED DESIGN METHODOLOGY

The complete and systematic method proposed in this article to design a combinational ternary circuit based on CNTFET comprises six steps:

Step 1: Design a ternary to binary decoder (A (*ternary*) converted to A_0, A_1 and A_2 (*binary*)) for each input.

In this article, a new decoder is presented with a lower transistor count than proposed in previous research. This decoder generates only A_0 and A_1 values, while A_2 is applied through selecting a transistor with high V_{th}, which will be turned on just for value '2'. The method to generate A_0 and A_1 values is defined through Equation (5) and the transistor level of this Equation is shown in Fig. 2.

$$\begin{aligned} A_0 &= NTI(A) \\ A_1 &= \overline{NTI\ (A)}.PTI(A) \end{aligned} \tag{5}$$

Step 2: Draw the truth table of the complete ternary circuit for each output value (*Out*)

Step 3: Separate '1' and '2' output values (Out_1 and Out_2) in the previous table. Each output of ternary circuits (*Out*) has maximum three values '0', '1' and '2'. Here, the value of *Out* must convert to two new values Out_1 and Out_2. In fact, if the value of *Out* is '1', the value of Out_1 would be '2', else '0' and if the value of *Out* is '2', the value of Out_2 would be '2', else '0'.

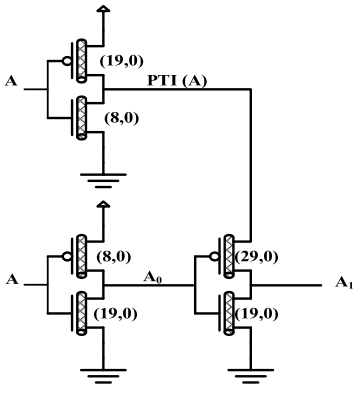

FIGURE 2. Transistor level of ternary to binary decoder (A_0 and A_1).

Step 4: Express the *Out1* and *Out2* variables as the sum of the products: draw the Karnaugh map (for circuits with less than 6 inputs) or Quine-McCluskey table (for circuits with more than 6 inputs) for each output value from step 3 (Out_1 and Out_2) to extract the simplified sum-of-products equation for each of them.

Step 5: Draw the pull-up and pull-down circuits for each equation of step 4, which leads to full swing outputs and low power consumption. The chiral vector of each pull-up and pull-down transistor has an essential effect on the functionality, power consumption and delay of the whole circuit. In Table 4, the chiral vector of each transistor for both pull-up and pull-down networks with various inputs A_0, A_1 and A are presented. For instance, if one transistor in the pull-down network with input '2' needs to be turned on, A is used instead of A_2 and the chiral vector of this transistor is (10,0), this transistor is turned on just for values higher than 0.56 V which is '2' value (VDD is assumed to be 0.9, here).

TABLE 4. The chiral vector of pull-up and pull-down transistors with various inputs, A_0, A_1 and A.

Input	Chiral vector of Pull-Up Transistor with Input	Chiral vector of Pull-Down Transistor with Input
A_0	(8,0)	(19,0)
A_1	(8,0)	(19,0)
$A_2 = A$	(19,0)	(10,0)

Step 6: Generate *Out*, designing a binary to ternary encoder circuit according to the results obtained from $\overline{Out1}$ and $\overline{Out2}$. The function and transistor level of this circuit according to the two inputs of $\overline{Out1}$ and $\overline{Out2}$ are tabulated in Table 5 and shown in Fig. 3.a.

TABLE 5. The truth table of encoder circuit.

$\overline{Out1}$	$\overline{Out2}$	*Out*
0	0	Forbidden
0	2	1
2	0	2
2	2	0

In Table 5 and Fig. 3.a, the first row's values ($\overline{Out1} = 0$ and $\overline{Out2} = 0$) never occur, since the *Out* cannot be '1' and '2', simultaneously. In the second row ($\overline{Out1} = 0$ and $\overline{Out2} = 2$), the path through T_2 turn ON, thus the value of *Out* is '1'. In the third row ($\overline{Out1} = 2$ and $\overline{Out2} = 0$), transistor T_1 turn ON, while other paths remain OFF, thus the value of *Out* is '2'. In the final row ($\overline{Out1} = 2$ and $\overline{Out2} = 2$), the path through transistors T_3 and T_4 turn ON and the value of *Out* is '0'. If the *Out* has only two values '0' and '1', the encoder circuit of Fig. 3.b, which is a PTI circuit with power supply $\frac{Vdd}{2}$, can be applied instead of the circuit shown in Fig. 3.a.

The circuits of steps 1 to 6 are similar for each input and output nodes of ternary CNTFET-based circuits.

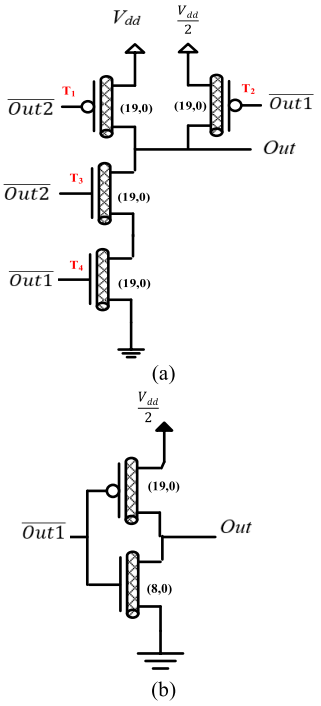

FIGURE 3. Transistor level of binary to ternary encoder circuit with (a) Two inputs (b) One input.

V. DETAILED IMPLEMENTATION OF TERNARY HALF ADDER

In this section, a ternary half adder is designed following the above proposed methodology. Based on steps 2 and 3, a typical truth table of a ternary half adder is presented in Table 6, where the two variables *Sum*1 and *Sum*2 indicate when *Sum* of two variables A and B will become '1' and '2', respectively [15]. Based on step 4, the Karnaugh map of *Sum*1, *Sum*2 and *Carry*1 are shown in Figs. 4 to 6, respectively.

*Sum*1, *Sum*2 and *Carry*1 are defined through Equation (6) according to the above mentioned Karnaugh maps. Based

A_i / B_i	0	1	2
0	0	2	0
1	2	0	0
2	0	0	2

FIGURE 4. Karnaugh map of *Sum*1.

A_i / B_i	0	1	2
0	0	0	2
1	0	2	0
2	2	0	0

FIGURE 5. Karnaugh Map of *Sum*2.

A_i/ B_i	0	1	2
0	0	0	0
1	0	0	2
2	0	2	2

FIGURE 6. Karnaugh map of *Carry*1.

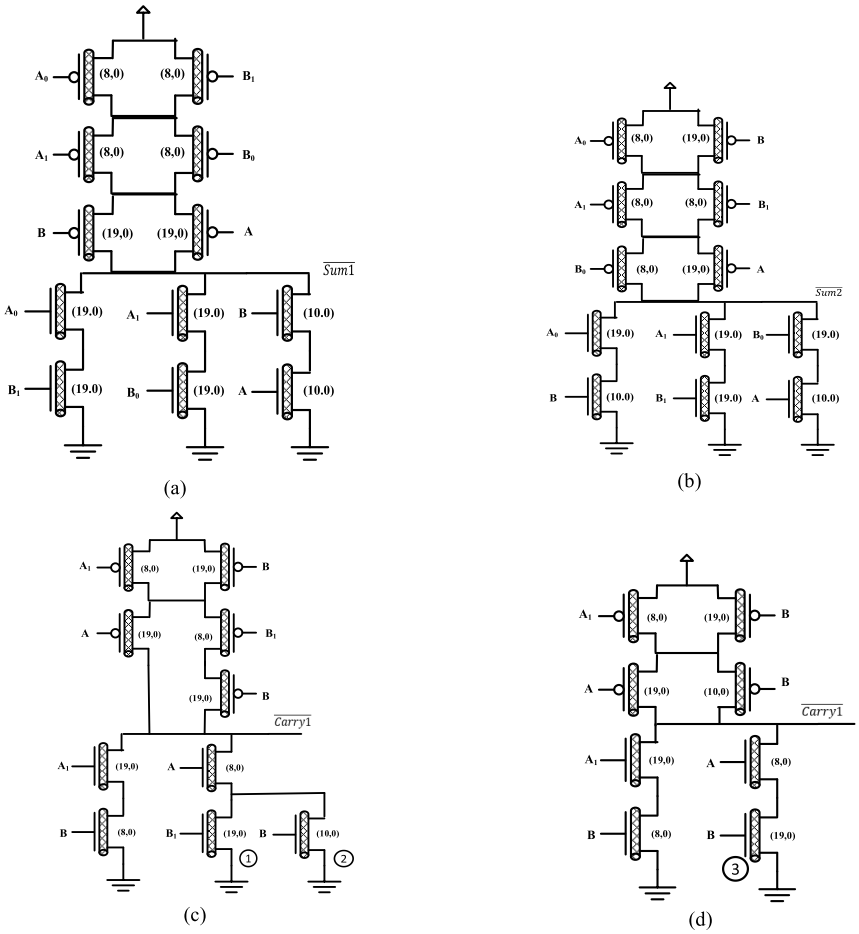

FIGURE 7. The transistor level of (a) $\overline{Sum1}$ (b) $\overline{Sum2}$ (c) $\overline{Carry1}$ (d) Revised $\overline{Carry1}$.

TABLE 6. The truth table of ternary half adder.

A	B	Sum	$Carry$	$Sum1$	$Sum2$	Carry1
0	0	0	0	0	0	0
0	1	1	0	2	0	0
0	2	2	0	0	2	0
1	0	1	0	2	0	0
1	1	2	0	0	2	0
1	2	0	1	0	0	2
2	0	2	0	0	2	0
2	1	0	1	0	0	2
2	2	1	1	2	0	2

on step 5 and Table 3, the transistor level of $\overline{Sum1}$, $\overline{Sum2}$ and $\overline{Carry1}$ are depicted through pull up and down networks which are shown in Fig. 7.

$$\begin{aligned} Sum1 &= A_0.B_1 + A_1.B_0 + A_2.B_2 \\ Sum2 &= A_0.B_2 + A_1.B_1 + A_2.B_0 \\ Carry1 &= A_1.B_2 + A_2.B_1 + A_2.B_2 = A_1.B_2 + A_2.(B_1 + B_2) \end{aligned} \tag{6}$$

The circuit of the output $\overline{Carry1}$ in Fig. 7.c, can be revised and improved by replacing transistors 1 and 2 with transistor 3, the V_{th} of which is 0.7 V and would be turned on when B takes the logics of '1' or '2'. The schematic of this revised $\overline{Carry1}$ is shown in Fig. 7.d.

Based on step 6, the circuit of Fig. 8.a is applied to generate Sum through two values $\overline{Sum1}$ and $\overline{Sum2}$. To generate the $Carry$, the circuit of Fig. 8.b is proposed, since $Carry$ has only two values '0' and '1'.

A similar procedure can be applied for the implementation of any other logic block. The results of the implementation for a 1-digit multiplier (a typical logic block reported in [14] and [17]), following the methodology from section IV is presented in the next section.

VI. SIMULATION RESULTS

The proposed decoder, a half adder and a 1-digit multiplier, as well as the latest published works [12] and [14]–[18] have been simulated through HSPICE [19] in 32nm technology by applying the Stanford compact model for CNTFET [20] and keeping the same voltages and parasitic capacitances.

The functionality of the proposed ternary to binary decoder is shown in Fig. 9. When A is equal to '2' (0.9 V), A_1 is weak '0' (0.15 V). But it does not affect the functionality of the proposed circuits since the threshold voltages of the

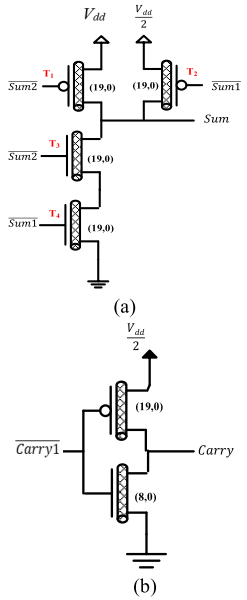

FIGURE 8. The transistor level of (a) *Sum* encoder circuit and (b) *Carry* encoder circuit.

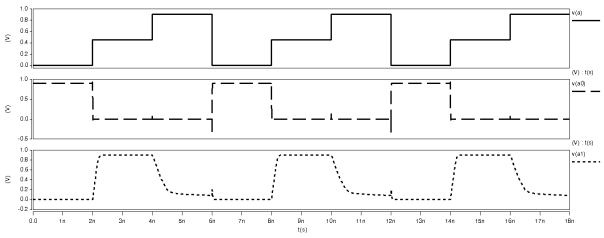

FIGURE 9. The simulation result of the proposed ternary to binary decoder.

pull-down and pull-up transistors, which are connected to input A_1, are 0.3 V and -0.7 V respectively, which will not turn on and off with the value of 0.15 V, respectively.

The input simulation pattern and responses of the half adder and multiplier circuits proposed in this article are illustrated in Fig. 10.a and b, respectively. As can be seen from Fig. 10, there are no hazards and the outputs are smooth and fast.

To evaluate the operation of the proposed ternary to binary decoder compared with other designs [15] and [17], all were simulated at 1 *GHz* frequency, 0.9 V supply voltage, 20 *ps* rise, 20 *ps* fall time, 25 °*C* temperature and various load capacitances from 3 *fF* to 31 *fF*. Power consumption, delay and PDP of the proposed decoder and previous designs ([15] and [17]) are reported in Table 7. Although the decoder of [15] is superior in terms of delay, the power consumption and PDP of the proposed decoder are lower compared with the other decoders ([15] and [17]) with various load capacitances (7 *fF* to 31 *fF*). Also, the transistor count of the proposed decoder is 6, while the transistor counts of designs [15] and [17] are 8 and 9 respectively.

The proposed half adder and 1-digit multiplier are compared with [12] and [14]–[18] designs at 1 *GHz* frequency,

TABLE 7. Simulation results of ternary to binary decoder.

	Load (fF)	Power ($\times 10^{-6}$ W)	Delay ($\times 10^{-10}$S)	PDP $\times$ 10^{-15}
Sahoo [15]	3	1.59	**1.62**	**0.257**
Jaber [17]	3	1.83	7.03	1.28
Proposed	3	**1.15**	3.58	0.411
Sahoo [15]	7	3.24	3.46	1.12
Jaber [17]	7	2.5	7.19	1.8
Proposed	7	**2.15**	**5.01**	**1.08**
Sahoo [15]	11	4.27	4.43	1.89
Jaber [17]	11	3.03	7.35	2.23
Proposed	11	**2.85**	**5.5**	**1.57**
Sahoo [15]	15	4.79	**4.84**	2.32
Jaber [17]	15	3.44	7.5	2.58
Proposed	15	**3.06**	6.1	**1.87**
Sahoo [15]	19	5.09	**4.98**	2.54
Jaber [17]	19	3.75	7.78	2.92
Proposed	19	**3.1**	6.43	**1.99**
Sahoo [15]	23	5.31	**5.02**	2.66
Jaber [17]	23	4	7.98	3.19
Proposed	23	**3.11**	6.73	**2.1**
Sahoo [15]	27	5.48	**5.02**	2.75
Jaber [17]	27	4.19	8.11	3.4
Proposed	27	**3.13**	6.87	**2.15**
Sahoo [15]	31	5.64	**5.73**	3.23
Jaber [17]	31	4.37	8.25	3.61
Proposed	31	**3.13**	7.73	**2.42**

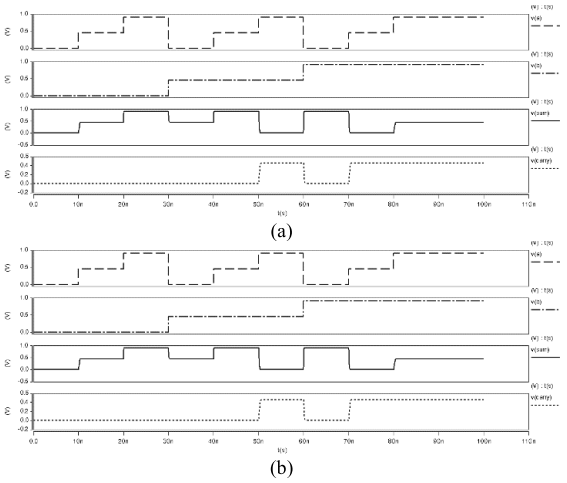

FIGURE 10. The simulation result of the proposed ternary (a) half adder and (b) 1-digit multiplier.

0.9 V supply voltage, 3.5 *fF* load capacitance, 20 *ps* rise, 20 *ps* fall time scenario and 25 °*C* temperature conditions in Table 8 and 9 respectively, showing transistor count, power consumption, delay, PDP and power supply count.

The proposed ternary half adder (figures section IV) is made of 50 transistors, revealing a 3.85%, 24.24%, 10.71% and 41.18% transistor count improvement over [12], [15], [16] and [17] designs, respectively. The power consumption of the proposed half adder is reduced by 32.35%, 73% and 10.85% compared with [15], [16] and [17] respectively. The delay of the proposed half adder is 65.25%, 16.33%, 78.38% and 80.16% lower than [12], [15], [16] and [17] designs respectively. The PDP of the proposed half adder is

TABLE 8. Simulation results of ternary half adder.

Circuit	Transistor count	Power ($\times 10^{-6}$ W)	Delay ($\times 10^{-10}$ S)	PDP $\times 10^{-15}$	Power supply count
Tabrizchi [12]	52	1.15	3.54	0.41	1
Srinivasu [14]	**35**	86.75	2.88	24.96	1
Sahoo [15]	66	1.7	1.47	0.25	1
Kim [16]	56	4.26	5.69	2.43	1
Jaber [17]	85	1.29	6.2	0.80	2
Jaber [18]	90	**0.686**	4.99	0.34	2
Proposed	50	1.15	**1.23**	**0.14**	2

TABLE 9. Simulation results of ternary 1-digit multiplier.

Circuit	Transistor count	Power ($\times 10^{-6}$ W)	Delay ($\times 10^{-10}$S)	PDP $\times 10^{-15}$	Power supply count
Tabrizchi [12]	43	0.74	4.35	0.32	1
Srinivasu [14]	**26**	32.6	2.98	9.73	1
Jaber [17]	61	0.86	6.11	0.52	2
Proposed	38	**0.66**	**1.69**	**0.11**	2

lower by 65.85%, 44%, 94.24% and 82.05% than with [12], [15], [16] and [17] designs, respectively. Although the power consumption of the proposed half adder is 40.35% higher than with design [18], its transistor count, delay and PDP are optimized by 44.44%, 75.35% and 58.82%, respectively. Although, the transistor count of the proposed half adder is 30% higher than design [14], power consumption, delay and PDP are improved by 98.67%, 57.29% and 99.44% respectively.

Table 9 presents data for the 1-digit multiplier circuit, showing a higher transistor count (31.58%) and lower PDP (98.87%) compared with design [14]. The transistor count of the proposed multiplier is 11.63% and 37.7% lower than designs [12] and [17] respectively. PDP of the proposed multiplier is improved by 65.63% and 78.85% compared with designs [12] and [17] respectively. The proposed multiplier has the least power consumption and latency compared with the other designs: [12], [14] and [17].

Although the proposed half adder and 1-digit multiplier are designed by applying two power supplies as in designs [17] and [18], their robustness is not compromised due to the fact that generating the power supply $V_{dd}/2$ through a DC/DC converter circuit is possible with no difficulty.

To run Monte Carlo simulations in order to evaluate variability (PVT) with the proposed half adder and previous designs [12] and [14]–[18], three cases were simulated:

Case I: frequency, supply voltage and load capacitance were set at 1 *GHz*, 0.9 *V* and 2 *fF*, respectively and temperature varied from 0 °*C* to 70 °*C*, (see Fig. 11.a). In the range from 20 °*C* to 70 °*C*, the PDP of the proposed half adder was optimized over [12] and [14]–[18] and varied less with varying temperature.

Case II: the frequency, load capacitance and temperature were set at 1 *GHz*, 2 *fF* and 25 °*C*, respectively and supply voltage varied from 0.8 *V* to 1 *V*, (see Fig. 11.b). With 0.9 and 1 *V* supply voltage range, the PDP of the proposed half adder was lower than other designs [12] and [14]–[18].

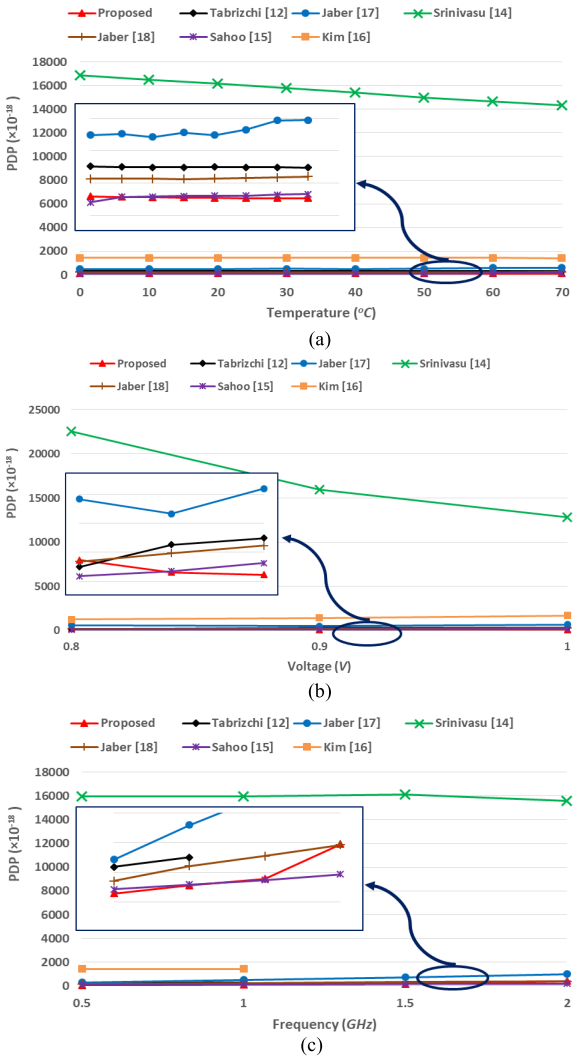

FIGURE 11. PDP of the proposed half adder and previous designs [12] and [14]–[18] at various (a) temperatures (b) voltage supplies, and (c) working frequencies.

Case III: the supply voltage, load capacitance and temperature were set at 0.9 *V*, 2 *fF* and 25 °*C*, respectively and frequency varied from 0.5 *GHz* to 2 *GHz*, (see Fig. 11.c). With 0.5, 1 and 1.5 *GHz* frequency, the PDP of the proposed half adder was lower than other designs [12] and [14]–[18].

The proposed 1-digit multiplier and corresponding designs [12], [14] and [17] were also simulated in the above three cases and the PDPs are shown in Fig. 12. PDP of the proposed 1-digit multiplier was lower than other designs ([12], [14] and [17]) in all simulations.

Process variations have a great impact on the performance and robustness of the design of nanoscale devices and circuits. CNT diameter and tube count are two important parameters; fluctuations in CNT diameter and tube count impact significantly on threshold voltage and output current of the circuits, respectively. Consequently, manufacturing process variations have a negative impact on the functionality and performance of CNTFET-based circuits.

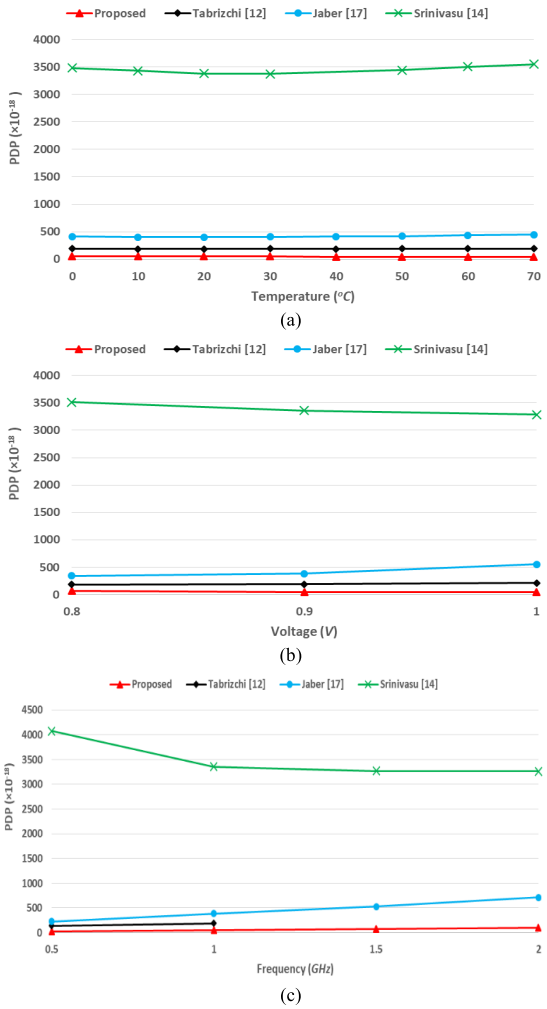

FIGURE 12. PDP of the proposed 1-digit multiplier and previous designs [12], [14] and [17] at various (a) temperatures (b) voltage supplies and (c) working frequencies.

TABLE 10. Simulation results of cascade of two and three proposed half adders.

Cascade of	Power ($\times 10^{-6}$ W)	Delay ($\times 10^{-10}$ S)	PDP ($\times 10^{-15}$)
Two proposed half adders	0.91	2.5	0.23
Three proposed half adders	1.014	3.03	0.3

Process variability impacts on the proposed design were therefore evaluated using the Monte Carlo analysis with 30 simulation runs, based on the statistical model of a Gaussian distribution with $\pm 3\sigma$ levels of 0.04% to 0.2% for the CNT diameter variation and 5% to 15% for the tube count variation. The PDP variations of the proposed half adder and previous designs ([12] and [14]–[18]) with the CNT diameter and tube count variations are shown in Fig. 13.a-b. The proposed design is more robust in terms of process variations compared with other designs [14]–[18]. The impact of variation of CNT diameter and tube count were also simulated for the proposed 1-digit multiplier and previous designs

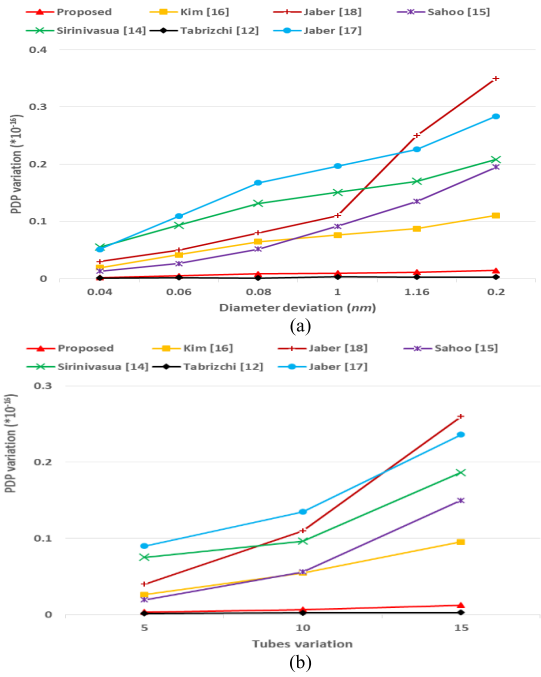

FIGURE 13. Process variations of proposed half adder and other designs [12] and [14]–[18] in terms of (a) diameter and (b) tube count variations.

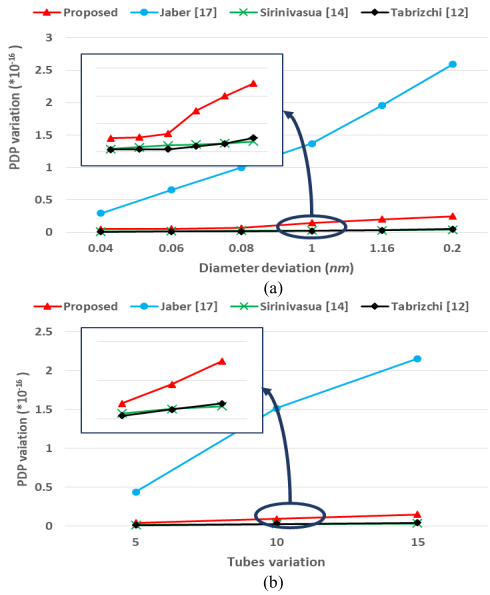

FIGURE 14. Process variations of proposed 1-digit multiplier and other designs [12], [14] and [17] in terms of (a) diameter (b) tube count variations.

[12], [14] and [17] and the results are depicted in Fig. 14. PDP variation of the proposed design is near to zero, suggesting a robust design.

To verify the applicability of the proposed half adder in large circuits, two and three proposed half adders were cascaded and simulated at 1 *GHz* frequency, 0.9 *V* supply voltage, 3.5 *fF* load capacitance, 20 *ps* rise, 20 *ps* fall time and 25 °*C* temperature. The power consumption, delay and PDP

of these cascade adders are reported in Table 10. When the number of cascade adders increases, the power consumption, delay and PDP increases moderately.

VII. CONCLUSION

MVL circuits offer crucial advantages in terms of area, the number of devices, interconnections and consequently low power consumption. CNTFET technology, due to its ability to implement multi-threshold voltage devices, is a traditional alternative to implement MVL circuits, as recent publications have shown. In this paper, a systematic procedure for implementing MVL combinational logic blocks, from the truth table of the logic to the complete circuit implementation, using a discrete number of CNTFET diameters is presented. The procedure is applied, in six detailed steps, to the design of a half adder. Simulation results, with the same electrical conditions in all cases, reveal a significant reduction in PDP compared with other designs (44.44 to 99.44%) and the lowest delay with an acceptable power consumption and number of devices. The enhanced results were also manifest when applying the systematic methodology to the design of a 1-digit multiplier (another benchmark circuit), which demonstrated the lowest PDP, delay and power consumption compared with other designs.

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AREZOO DABAGHI ZARANDI received the B.S. degree in hardware computer engineering from the Amirkabir University of Technology, Tehran, Iran, and the master's degree in computer architecture from the Sharif University of Technology, Tehran. She is currently pursuing the Ph.D. degree in computer architecture with the University of Isfahan, Isfahan, Iran. Her research interests include nanoelectronics with emphasis on CNTFET, QCA, VLSI implementation of MVL, FPGA, and ASIC implementation of arithmetic circuits.

MOHAMMAD REZA RESHADINEZHAD received the B.S. and M.S. degrees in electrical engineering from the University of Wisconsin, Milwaukee, USA, in 1982 and 1985, respectively, and the Ph.D. degree from Shahid Beheshti University, Tehran, Iran, in 2012. He is currently an Assistant Professor with the Faculty of Computer Engineering, University of Isfahan, Isfahan, Iran. He has served as the Program Chair, General Chair, and Program Committee Member of various conferences. His research interests include low-power design, digital circuit design and implementation of field programmable gate array (FPGA), nanotechnology concerning CNTFET, VLSI implementation, quantum computing, residue number system (RNS), and cryptography.

ANTONIO RUBIO (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees from the Industrial Engineering Faculty, Polytechnic University of Catalonia (UPC), Barcelona, Spain. He has been an Associate Professor with the Electronic Engineering Department, UPC, and a Professor with the Physics Department, Balearic Islands University, Palma, Spain. He is currently a Professor of electronic technology with the Telecommunication Engineering Faculty, UPC. His research interests include VLSI design and test, device and circuit modeling, high-speed circuit design, and new emerging nanodevices and nanoarchitectures. He is an Associate Editor of the TRANSACTIONS ON COMPUTERS, a Senior Editor of the TRANSACTIONS OF NANOTECHNOLOGY, the Chair Elect of Nano-Giga TC, and the IEEE Computer Sciences Integrity Chair.