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Synchronized Switching Modulation to Reduce the DC-Link Current in SRM Drives

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ABSTRACT Switched Reluctance Machines (SRM) are emerging as a possible alternative in terms of cost and supply stability to rare earth based electric vehicle traction systems. However, because of the huge amounts of energy stored and transferred back and forth between the DC source and the SRM, large DC-link capacitors must be used as buffers, which increases overall costs and size. This paper proposes a novel modulation technique which forces the exchange of energy between phases while decreasing the energy transfer between the DC bus and the SRM. This means lower DC bus currents (capacitor size and cost reduction) and lower Joule-effect conduction losses (better efficiency). The proposed modulation has been validated experimentally in a test bench and compared with the conventional torque-sharing function.

INDEX TERMS Switched reluctance motors, motor current control, inverter modulation, capacitor current reduction.

I. INTRODUCTION

Considering the growing concern and societal awareness over the global warming of our planet and the need to protect the environment, the Electric Vehicle (EV) and Hybrid Electric Vehicle (HEV) are attracting close attention of consumers, policymakers and the automotive sector.

Nowadays, Permanent Magnet (PM) Synchronous Machine technology is preferred for EV and, especially, HEV applications due to a number of features such as high power density, high efficiency and reliability [1]–[3]. However, PM-based technology depends on the supply of rare-earth raw materials to manufacture the permanent magnets, usually made of NdFeB alloys [2]. But costs and availability of rare-earth magnets have been experiencing high fluctuations [4], particularly during the rare-earth crisis of 2010-2012 [5], and EVs/HEVs represent a cost-sensitive market.

Switched reluctance machines (SRMs) can be highlighted as an alternative due to their flexibility of control, high efficiency, simple structure, low cost and robustness to run under failure conditions [6]–[8]. All this reasons make SRMs a serious contender for propulsion systems in EVs and HEVs [9]–[13]. Also, because SRM rotors have no windings, they are particularly suited for high-speed, high-temperature operation [14], [15].

Nonetheless, some factors are still conditioning a more widespread adoption of SRM-based traction systems. As to the SRM itself, it is well known that the pulsed nature of its excitation currents result in torque ripple, vibrations and noise [1], [3]; thus, ellaborated control strategies are required to cope with its nonlinear features [16]. But a system-wide look reveals another important pitfall to overcome: the large amount of magnetic energy stored in the windings, which is transferred back and forth between the DC source and the SRM through the power converter, causing considerable current peaks [17]. This fact calls for larger DC-link capacitors than would be needed should the current behave less violently, which increases the volume and cost of the converters.

Within this context, the U.S. Department of Energy (DoE) proposes stringent technological targets with regard to power density, efficiency and costs for both motors and power converters [18]. Indeed, nowadays most SRM-related

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research focuses on machine structural improvements, control improvements (which affect machine performance), or new converter topologies [19]–[21].

One key method to improve the performance of SRMs is to employ a more complex converter topology or/and a special machine design [22]. A multiport converter is used in [23] which introduces the DC-link capacitor as an extra port; also it reduces the required capacitance by allowing an increase of the voltage ripple. Ref. [24] validates a dc-dc boost converter to reduce the size of the capacitor by actively filtering the current. In [25] a bidirectional cascaded buck-boost converter is used in parallel to the SRM drive to filter the ripple current, thus allowing to reduce the capacitor size. And [26] presents a quasi-Z-source integrated multiport converter to reduce the DC-link capacitor. However, these topologies employ more devices, reduce the fault tolerance and increase the total volume.

A way to reduce the DC-link current with no changes in either the converter or the machine is by means of the control. Ref. [27] proposes an improved phase current waveform to reduce the DC-link current ripple and [28] uses a low-pass filter to eliminate low harmonics. Both of them use FEM non-linear magnetic models, so they do not consider the degradation and construction errors. In [29] a real-time calculated commutation shift angle is applied to minimize the DC-link current, but it adds an extra current sensor into the DC-link and needs a large computational capability.

Ref. [30] proposes a method to take advantage of a phenomenon which favors the magnetic energy exchange between phases, and [31] applies the method to develop a technique which aims to maintain a constant average DC-link current over a switching cycle. However, they do not make efficient use of this phenomenon and omit reliability and performance aspects (fault-tolerance, efficiency, torque ripple) of the SRM. Furthermore, these proposals are not applicable to any other control scheme without changes.

This paper presents an enhanced modulation scheme, named *Synchronized Switching Modulation* (SSM), which takes advantage of the phenomenon synchronizing the phases during the overlap which favors the magnetic energy exchange between phases during overlap, thus decreasing the DC bus – SRM energy transfer. This approach has two benefits: on one hand, the current peaks that DC-link capacitors must sink / source are significatly mitigated, which makes it possible to use lower capacitances, i.e. smaller capacitors, thus increasing power density and reducing costs; on the other, Joule-effect conduction losses drop, which relaxes cooling requirements and improves overall system efficiency. This scheme allows to easily apply the SSM to any kind of current control and is independent of the structural design.

This paper is organized as follows: Section II analyzes the particularities of an SRM, both mathematical modelling and relevant control aspects, as well as the main operational issues. Section III exposes the novel SSM scheme in detail. Sections IV-V describe the SRM drive testbench and the results obtained, respectively. Finally, Section VI draws the main conclusions of the work.

II. SRM PRELIMINARIES

A. DRIVING AN SRM

Fig. 1 shows a simplified view of an SRM drive, including the power converter stage, which is an asymmetrical H-bridge converter. Indeed, although many topologies exist meeting the basic requirements of SRM driving, such as phase independence and de/magnetization promptness, the asymmetric H-bridge converter exhibits a good controllability over most of the speed range, which makes it particularly suited for the purposes of this work [17], [32], [33]. Therefore, and also because the SSM, i.e. the novel modulation scheme being presented here, is compatible with any converter topology, an asymmetric H-bridge converter was chosen to carry out the simulations and experimental validation.

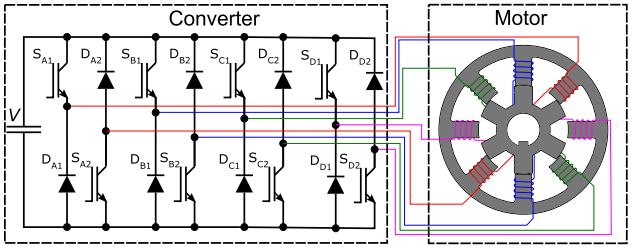


FIGURE 1. Simplified view of a 4-phase 8/6-pole SRM drive.

B. MATHEMATICAL MODEL

Fig. 2 shows the per-phase equivalent circuit of an SRM, where phase mutual inductances have been neglected for simplicity, and also because it is difficult to obtain reliable data from nonlinear models via FEM simulations [34].

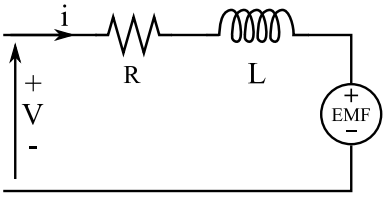


FIGURE 2. Phase equivalent circuit of an SRM.

From Ohm's and Faraday's laws

$$V = R\,i + \frac{d\psi\,(\theta, i)}{dt}, \tag{1}$$

where R and i are the phase resistance and phase current, and ψ, the magnetic flux, equals

$$\psi = L\,(\theta, i)\;i, \tag{2}$$

which emphasizes that L, the phase self-inductance, depends on both i and θ, the angular position of the rotor. Now, putting

together (1)-(2) yields

$$V = R\,i + L\,(\theta, i)\,\frac{di}{dt} + \underbrace{\frac{dL\,(\theta, i)}{d\theta}\omega i}_{\text{EMF}}, \tag{3}$$

where ω is the angular velocity of the rotor.

Finally, from coenergy considerations, the instantaneous per-phase electromagnetic torque can be expressed as

$$T_{em} = \frac{\partial}{\partial\theta}\int \psi\, di = \int \frac{\partial L}{\partial\theta} i\, di = \frac{1}{2} i^2 \frac{dL\,(\theta, i)}{d\theta}. \tag{4}$$

C. CONTROL PARTICULARITIES

Effective torque control is one of the key factors affecting EV performance, as e.g. prompt speed-up and braking responsiveness critically depend on it. Several well-known control strategies exist for SRM-based traction systems, such as Direct Instantaneous Torque Control (DITC), Average Torque Control (ATC), and Indirect Torque Control (ITC) [32]. Here, ITC stands out because of its ease of implementation and good cost-to-effectiveness ratio [35]. Therefore, and again also because the SSM can be used together with any torque control strategy, ITC was chosen to carry out the simulations and experimental validation.

The torque ripple inherent to SRMs is mainly due to the discrete excitation of the phase windings, especially during overlaps, as a result of two adjacent windings being energized together at the same time [32]. To address this, ITC usually employs a current control or some torque-sharing function (TSF) [35], derived from the destructive interference phenomenon. During overlap, the TSF splits the torque reference between the active phases, in such a way that the torque ripple is minimized.

Among all available TSFs, the following cubic patterns were chosen because of real-time computation efficiency and a low copper loss ratio (with respect to other alternatives),

$$f_{in}\,(x) = \begin{cases} 0, & 0 \leqslant \theta < \theta_{on} \\ 3x^2 - 2x^3 & , \quad \theta_{on} \leqslant \theta < \theta_{off} \\ 1, & \theta_{off} \leqslant \theta < \theta_T/2 \end{cases} \tag{5}$$

$$f_{out}\,(x) = \begin{cases} 0, & 0 \leqslant \theta < \theta_{on} \\ 1 - 3x^2 + 2x^3, & \theta_{on} \leqslant \theta < \theta_{off} \\ 1, & \theta_{off} \leqslant \theta < \theta_T/2, \end{cases} \tag{6}$$

where $f_{in}(\cdot)$ and $f_{out}(\cdot)$ stand for the incoming and outgoing patterns respectively, with

$$x \triangleq \frac{\theta - \theta_{on}}{\theta_{ov}}, \quad \theta_{ov} \triangleq \text{overlap angle}.$$

Fig. 3(a) shows the typical torque references T_j^*, current references i_j^*, and currents read i_j of each phase. Note that the phase torque reference T_j^* is built from the general torque reference T_{em}^*, depending on which zone each phase is operating; namely,

$$\text{Zone \#1 } T_j^* = T_{em}^* f_{in}(\cdot), \tag{7}$$

$$\text{Zone \#2 } T_j^* = T_{em}^*, \tag{8}$$

$$\text{Zone \#3 } T_j^* = T_{em}^* f_{out}(\cdot); \tag{9}$$

recall (5)-(6).

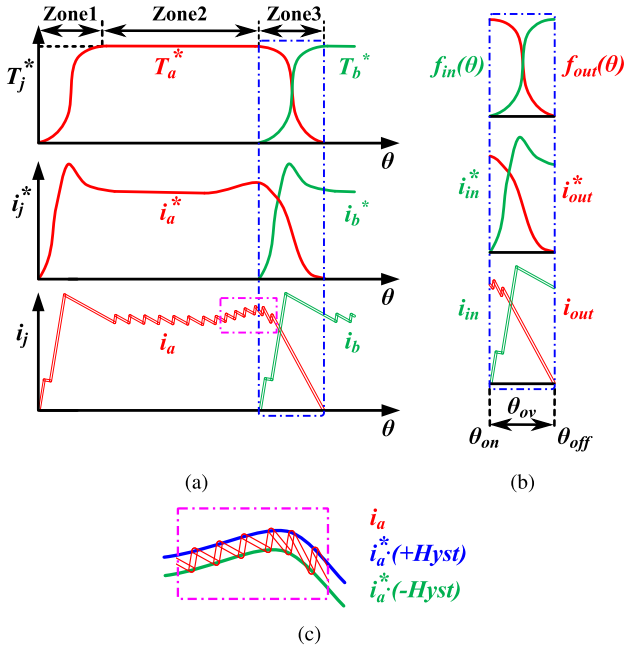


FIGURE 3. Typical profiles of reference torques T_j^*, reference currents i_j^*, and measured currents i_j produced by a TSF.

Fig. 3(b) zooms in on an overlap interval, which always coincides with zone #1 of one phase and zone #3 of its adjacent phase (depending on the sense of rotation). Because the work presented here focuses on the overlap interval, for the sake of clarity in what follows the zone #1 phase magnetizing current will be called i_{in}, and the zone #3 phase demagnetizing current, i_{out}; and their references will be called i_{in}^* and i_{out}^*, respectively.

Fig. 4 displays the control diagram selected for this application, whose SRM has four phases named $A \cdots D$. The encoder provides the rotor position θ, from which the actual angular velocity ω is easily derived. Now, for a given velocity reference ω^* the general torque reference T_{em}^* is obtained using a Proportional-Integral (PI) controller. Next, the TSF splits the torque reference in the four 'sub-references' $T_A^* \cdots T_D^*$, according to (7)-(9), which obviously need to know θ. These four values are then translated into the current

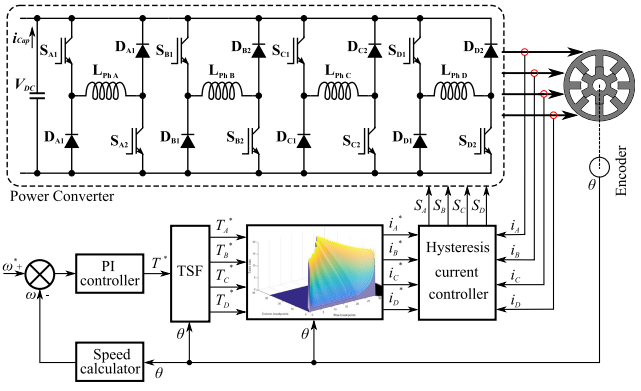


FIGURE 4. Control diagram of a TSF based ITC.

TABLE 1. Switch state in the asymmetric topology.

	Magnetization	Freewheeling	Demagnetization
S_{j1}	1	0	0
S_{j2}	1	1	0

references $i_A^* \cdots i_D^*$ using a look-up table, which also needs previous knowledge of θ. Finally, the hysteresis block compares these references with the actual $i_A \cdots i_D$ currents, thus generating the firing signals for the solid-state switches.

Last but not least, it should be pointed out that a strategy has been adopted in order to minimize the total number of commutations (see Table 1). Essentially it consists on favoring freewheeling over demagnetization in zones #1 and #2, and over magnetization in zone #3 (see Fig. 3(a)).

D. DO SRMs REALLY NEED SUCH BIG CAPS?

When a phase switches off, the magnetic energy stored in the windings is transferred to the DC bus; and when it switches on, such energy is claimed back from the DC bus. It is therefore a process that resembles the useless reactive energy transfer occurring in low-frequency linear AC systems; but in the SRM case significant current peaks are produced to / from the DC bus. The situation is further aggravated because any phase of an SRM must be able to deliver the full rated power to the load.

These big current peaks are usually mitigated by means of big capacitors, larger than would otherwise be required, in order to facilitate a smooth as possible energy flow in both directions [17]. Yet the DC bus is, by itself, rather a bulky part, and a major source of faults in modern power converters [36], as well as one of the elements with shortest service life [2]. And having to have exceedingly large capacitors makes things even worse.

III. SSM – SYNCHRONIZED SWITCHING MODULATION

A. A SMART WAY TO REDUCE CAPACITANCE REQUIREMENTS

By encouraging freewheeling over magnetization and demagnetization it is possible to reduce the total number of commutations, and also to isolate the phase, which decreases the number of current peaks that the DC bus must endure. But the stress is still too high, which calls for large charge reservoirs — capacitances.

All commutation logic, both incoming and outgoing, are mutually independent; each follows its own reference and they switch depending on the hysteresis window applied, whose width was set to 1%. In spite of that, sometimes commutations do coincide in time (see Fig. 5). As a result, energy gets transfered between phases, thus diminishing the current 'mirrored' onto the DC bus.

Then, i_{Cap}, the current that the DC bus must sink / source, equals

$$i_{Cap} = i_{Inv} - i_{Source} = i_{in} - i_{out} - i_{Source}, \qquad (10)$$

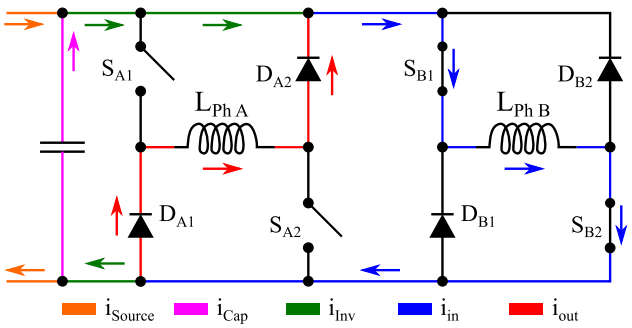
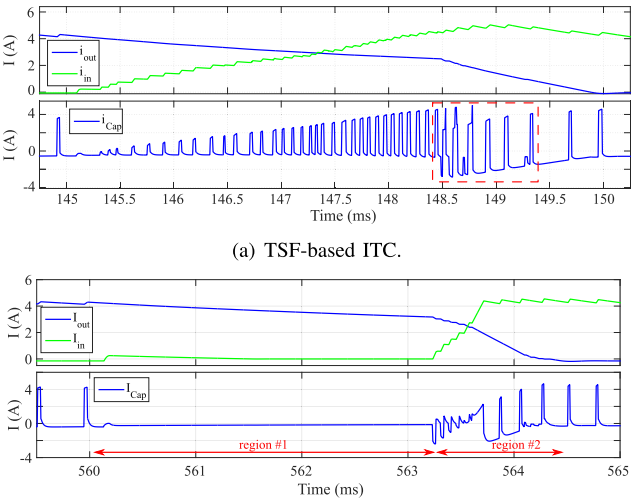


FIGURE 5. Current diagram in a synchronized switching.



(a) TSF-based ITC.

(b) SSM-enhanced ITC.

FIGURE 6. Simulation overlap current profiles at 200 rpm and 1.7 Nm.

where i_{Source} is the current supplied by the energy source, and i_{Inv} the current provided by the inverter to the phases. In fact, the red inset of Fig. 6(a) displays some instants when this happens by chance.

In view of all this, why not try to harness this phenomenon to our benefit? As a matter of fact, basically it just takes to design a new modulation paradigm, compatible with and independent of whatever control model, which forces the synchronization of phase commutation.

B. SSM DEVELOPMENT

As was justified in Sec. II-C, a cubic TSF-based ITC was chosen as a comparison model. Thus, the SSM, which implements the logic required to exploit the energy transfer phenomenon described above, was built 'on top of' the TSF.

In order to synchronize the overlapped phases, one must 'obey' the other, i.e. act on a master-slave scheme. When the overlap starts, the Nm/A ratio is larger in i_{out} than in i_{in}; recall the $\frac{d}{d\theta}L(\theta, i)$ factor in (4). Therefore it was decided that the first would be the master, following $f_{out}(\cdot)$, and the second, the slave, thus departing from the $f_{in}(\cdot)$ that minimizes the torque ripple. As a result of altering the TSF, an increase in torque ripple can be expected — and does occur.

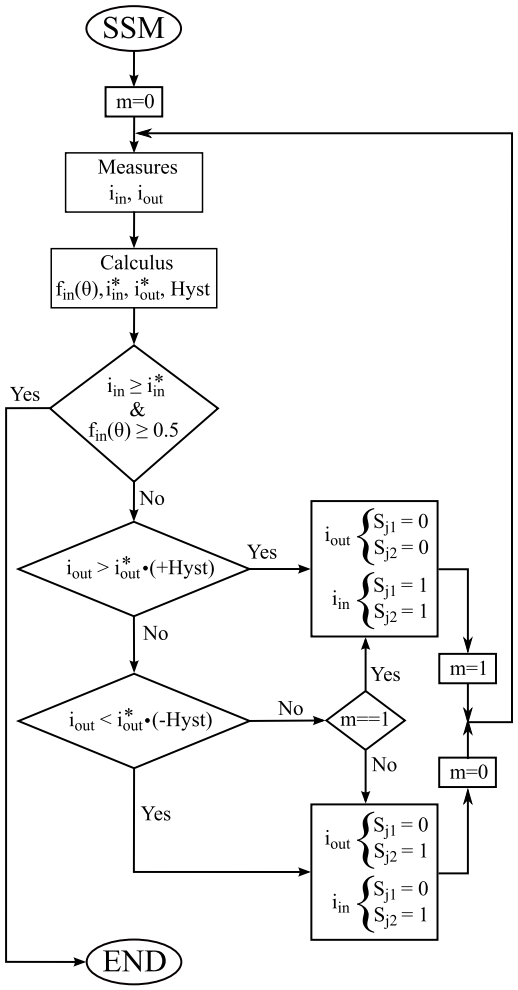


FIGURE 7. SSM flowchart.

Fig. 7 shows the flowchart explaining the SSM logic in detail. It follows a hysteresis-based current control pattern, where both phases are monitorized and controlled (see Fig. 3(c)), with *Hyst* the hysteresis window considered. However, SSM only controls the phase designated as master, i_{out}, to which the slave phase, i_{in}, is synchronized.

At the beginning of each iteration, the required data are read, so that it can be determined, through the first decision block, whether the execution of the SSM has to be started or finished. Because commutations are synchronized, i_{in} gets magnetized faster than i_{out} gets demagnetized; as a result, i_{in} always overshoots its reference before ending the overlap, thus causing a greater torque ripple and unnecessary i_{Cap} peaks. Therefore, SSM is applied once the overlap interval starts but only until $i_{in} \geqslant i^*_{in}$ is satisfied. Likewise, to avoid initial situations where both i_{in} and i^*_{in} are nearly zero, which could cause the SSM finish condition to trigger, a second condition of $f_{in}(\cdot) \geqslant 0.5$ is added as a safety measure.

If such conditions are not met, the following blocks execute the hysteresis logic, and determine the state of the i_{in} and i_{out} switches. After all that, the iteration finishes and the algorithm goes back to the data reading step.

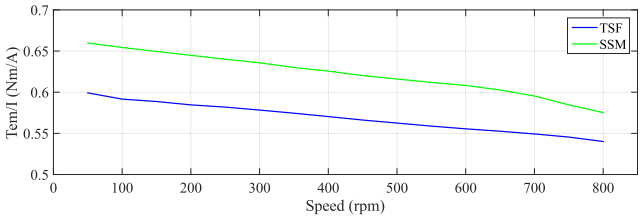


FIGURE 8. Speed/torque-per-amp ratio sweep at 4 Nm.

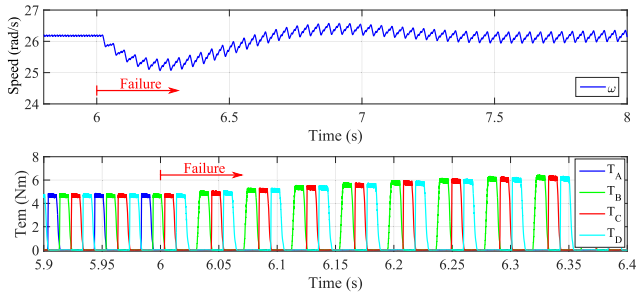


FIGURE 9. Failure simulation profiles of a SSM enhanced ITC.

It remains to be said that the *m* parameter introduced at the beginning is a tool to let the hysteresis know about the previous state of the master phase in each iteration — freewheeling or demagnetization. This is why it is reassigned in each iteration, together with the states of the switches.

This scheme allows to easily apply the SSM to any kind of current control.

C. VALIDATION BY SIMULATION

Fig. 6(b) shows the results of the SSM implementation on the operation conditions depicted by Fig. 6(a). It is noticeable the reduction of i_{Cap} during the overlap interval: zone #1 peaks vanish as a result of the slave phase obeying the master phase, and zone #2 peaks diminish due to the synchronization of the commutations.

Because i_{in} delays the magnetization of the phase, that phase acts over a shorter interval. To compensate this, i_j curves reach values that are slightly higher than with the classic TSF. To analyze the effect of this on the torque produced, a simulation sweep was realized by setting a 4-Nm load and then calculating the Tem/I ratio, i.e. average torque per RMS phases current. The results of Fig. 8 show a better performance of the SSM over all the interval studied, which is due to a more energy-efficient behaviour.

Indeed, the Tem/I ratio is a good figure-of-merit for the energy efficiency of the SRM. Although it leaves out iron losses, this should be of no concern, because hysteresis losses depend on frequency and maximum flux value, but not on the modulation technique. Eddy current losses, however, can be expected to be affected, because SSM results in steeper di/dt values [31].

Last but not least, the question of fault-tolerance has to be analized, because phases are no longer independently

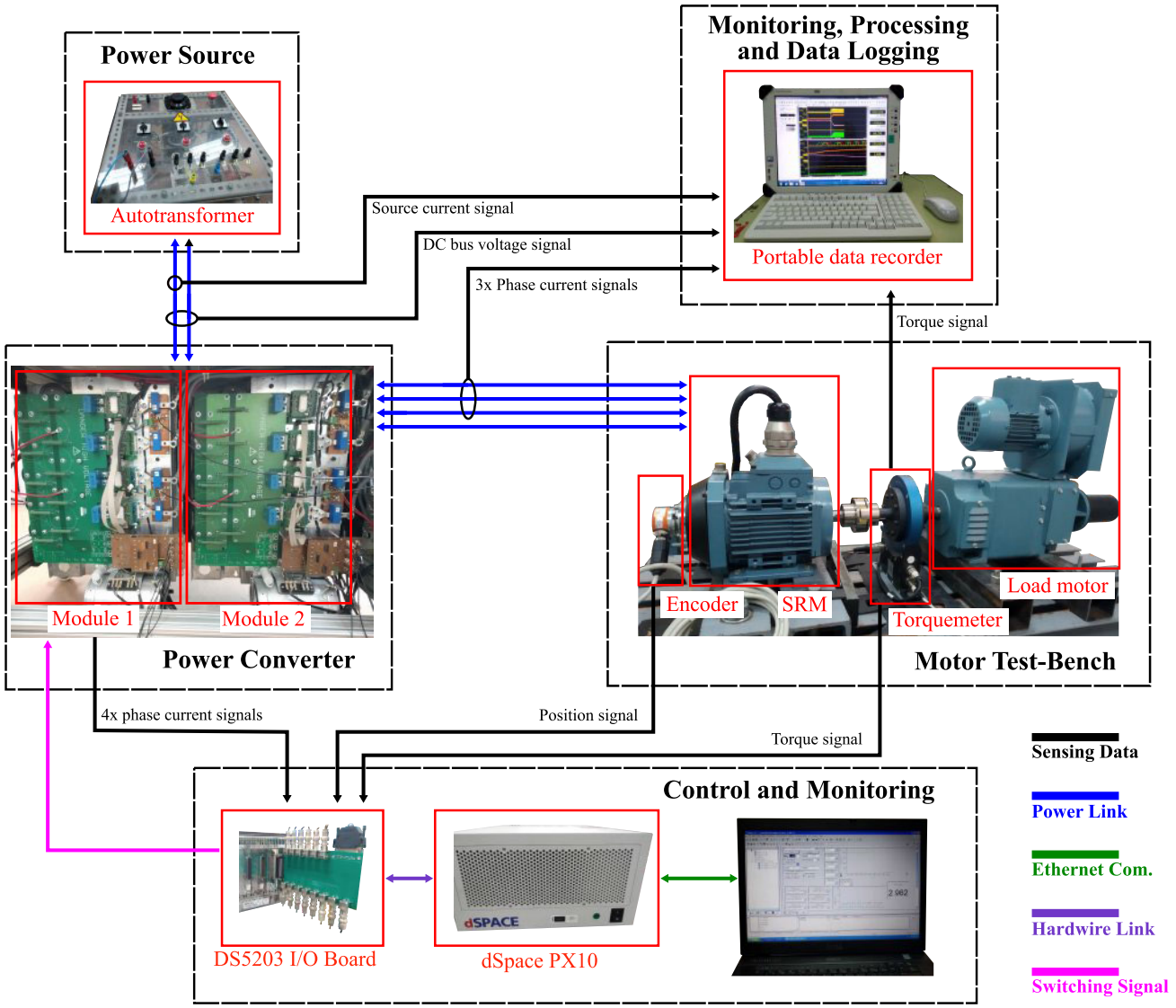
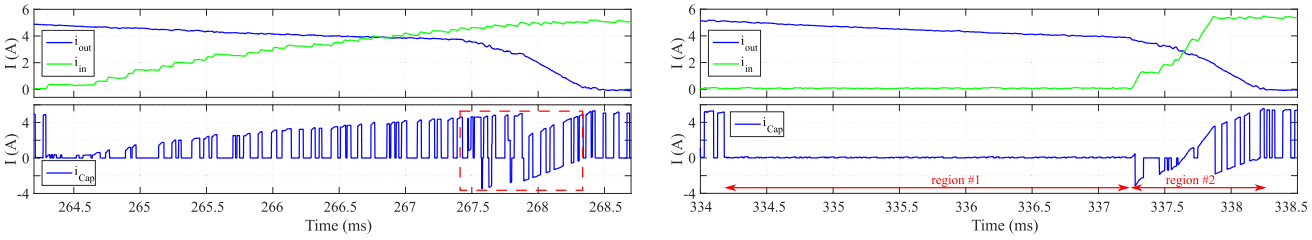


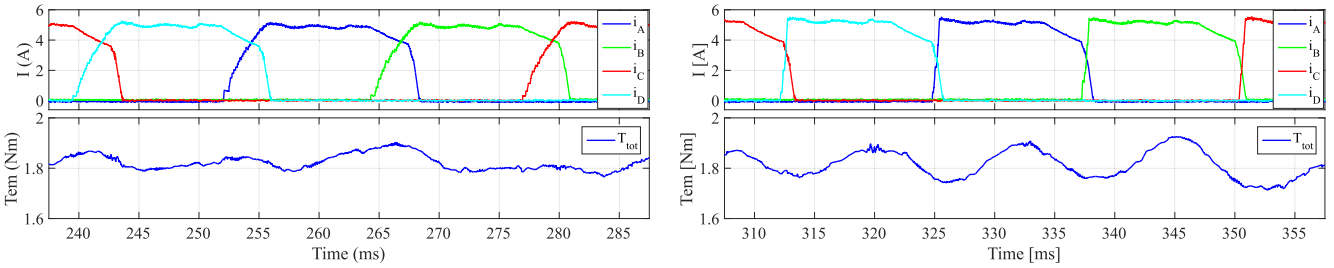
FIGURE 10. Electric drive test bench overview.



(a) TSF-based ITC. (b) SSM-enhanced ITC.

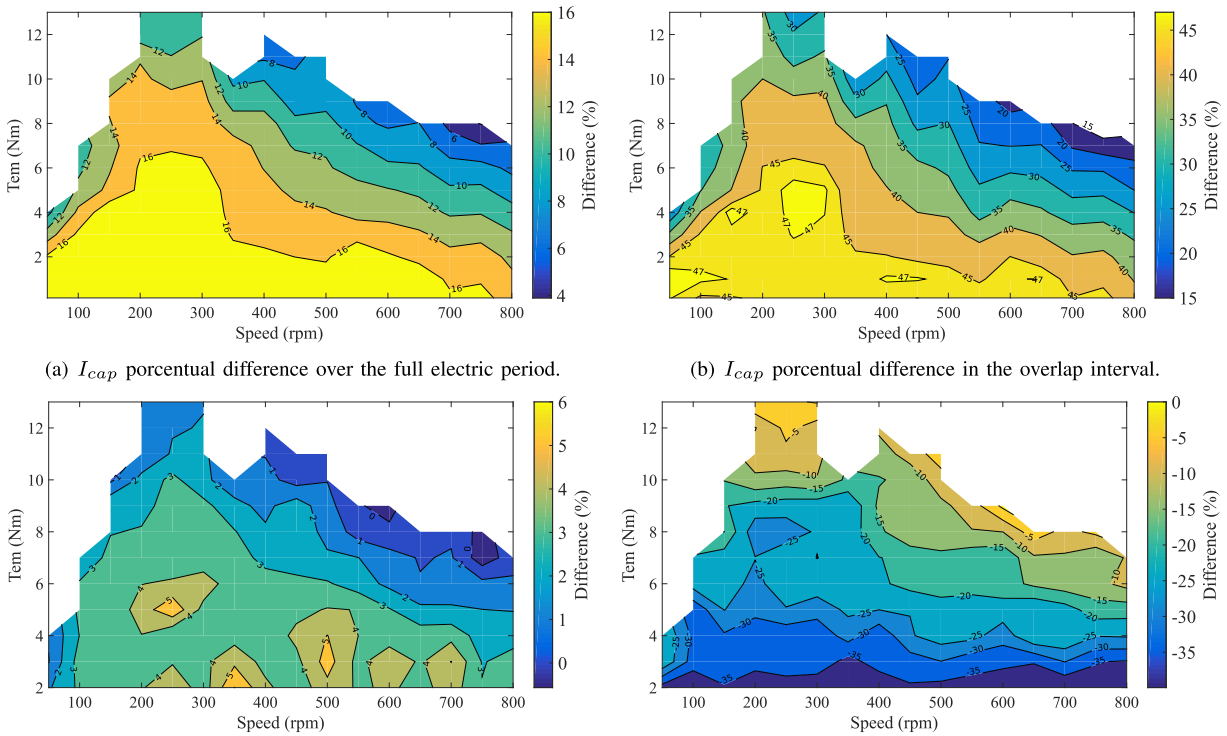
FIGURE 11. Experimental overlap current profiles at 200 rpm and 1.7 Nm.

controlled as a result of the slave phase being subjets to the master phase, which means that if a phase fails, its adjacent phases will be affected. This can be solved by implementing a fault control routine that modifies a portion of the modulation in such a situation. For example, Fig. 9 shows the simulation of a fault in phase A at $t = 6$ s; the system detected the incident and modified the TSF-produced commands of phase B, when its current acts as i_{in}, and of phase D, when it acts as i_{out}. Phases therefore recovered their independent behaviour, which made ω stabilize by incrementing



(a) TSF-based ITC. (b) SSM-enhanced ITC.

FIGURE 12. **Actual phase currents and total torque profiles at 200 rpm and 1.7 Nm.**



(a) I_{cap} porcentual difference over the full electric period. (b) I_{cap} porcentual difference in the overlap interval.

(c) Overall (motor+converter system) efficiency difference. (d) T_{rf} porcentual difference.

FIGURE 13. **Experimental map of results.**

the torque produced by the remaining phases to compensate the missing phase.

IV. ELECTRIC DRIVE TESTBENCH

Fig. 10 displays a general overview of the electric drive testbench employed to experimantally validate the SSM, comprising a power converter (on the left) and the motor testbench itself (on the right). There, a 4-phase, 1500-rpm SRM stands out (see Table 2). To measure the rotor position a Kuebler 8.5870 encoder was used, and to measure the exerted torque, a 100-Nm Kistler 4504B torquemeter. The load is a 3000-rpm, 4.4-kW standard DC machine.

The power converter comprises two units of Semikron's IGBT Stack "Semistack SKS 180F B8CI 118 V12", each providing two complete H-bridges and two Hall-effect current sensors. This makes a total of four measurement signals, which were input to the SRM control algorithm. In order to implement an asymetric H-bridge topology, the two corresponding IGBTs were left turned off permanently.

In addition, an HBM GEN3i recorder implemented both monitorization and signal logging and processing, by measuring the DC-link voltage as well as the variables T_{em}, i_{Source}, i_{Inv}, i_A, i_B, i_C, and i_D. The i_{Cap} current was not directly measured because there was no practical way to attach the required probe; instead, it was inferred from i_{Source} and i_{Inv} by using (10).

The control algorithm was carried out by a dSpace PX10 modular rapid control prototyping platform, equipped with an ACE1005 processor and a DS5203 FPGA board. The processor took charge of the velocity and torque control,

TABLE 2. Most relevant parameters of the used SRM.

Parameter	Symbol	Value	Units
Nominal power	P_n	1.5	kW
Nominal speed	ω_n	1500	rpm
Nominal voltage	V_n	300	V
Nominal current	I_n	20	A
Alineated inductance	L_a	0.086	H
Stator resistance (conection cabling included)	R_s	1.1	Ω
No of stator poles	-	8	-
No of rotor poles	-	6	-
No of phases	-	4	-

with a task execution time of 55 μs, whereas current regulation and input/outpu management was handed over to the FPGA, with a time step of 10 ns, so that much faster reaction times could be achieved.

V. EXPERIMENTAL RESULTS

Fig. 11 compares the results obtained with an SSM-enhanced TSF with respect to a classic TSF, for a typical operation point of 200 rpm and 1.7 Nm. First of all, note the close matching of 11(a), which shows the actual experimental results, with Fig. 6(a), which shows the simulation results. However, as the red inset of 11(a) reveals, the effect of energy exchange between phases, when their commutation coincides in time, actually happens out of the simulation.

By analyzing 11(a) with respect to Fig. 11(b), two observations can be made. On the one hand, current peaks vanished during overlap, because no commutation is ordered during this period, as a result of the master phase governing the slave phase (delimited as region #1); on the other, less and smoother current peaks occurred whenever phases commuted in a synchronized fashion (delimited as region #2). In this regard, Fig. 12 shows the waveforms of the phase currents.

As ω and/or load torque increase, so will the EMF; but the $|di/dt|$ affecting phase de/magnetization will decrease. As a result, controllability will also diminish, so results in terms of i_{Cap} can be expected to be less apparent. General results can be seen in Fig. 13. Due to a constraint in the load control, it was not possible to test all load points below 250 rpm.

Fig. 13(a) shows the relative RMS current difference of current i_{Cap} considering the cases studied, and bearing in mind the full electric period of the machine. Clearly, the SSM reduced the value of i_{Cap} over all the timespan tested, with a remarkable inprovement at low-to-medium loads.

Fig. 13(b) also shows the relative RMS current reduction of i_{Cap}, but considering just the overlap window, where the SSM acts, and therefore produced a much better improvement. In particular, improvements of up to 47 % were achieved, which nevertheless dropped progressively as load and velocity rise.

This drop in i_{Cap} makes it possible to also reduce the required capacitance value. This relationship can be quantified by the theoretical minimum capacitance value [23]

$$C_{min} = \frac{L_a i_{Cap}^2}{0.1 V_{dc}^2}, \tag{11}$$

where L_a is the inductance with alienated poles, and V_{dc} is the rated DC bus voltage. For example, considering the worst operating point at 250 rpm and 13 Nm, application of the TSF-based ITC resulted in $C_{min} = 782$ μF, whereas the SSM-based ITC yielded $C_{min} = 619$ μF, i.e. a reduction of 20.8 %.

The efficiency was calculated for the whole system, i.e. converter plus motor, considering the power supplied by the energy source, as well as the power generated by the motor. Thus, the variation of the efficiency exhibited the same trend as i_{Cap}; see Fig. 13(c): it improved considerably, with peaks of up to 5% at low-to-medium loads, but tending to the value of the efficiency yielded by the classic TSF-based scheme as load and velocity rise. Two factors lead to this efficiency improvement. On one hand, the SRM makes a better use of the energy, which is reflected in a higher Tem/I ratio (recall Sec. III-C); on the other, conduction losses are lowered due to the reduction of the ''reactive'' energy fluctuation between the SRM and the DC bus.

Finally, to assess how negatively all this affects the torque ripple, Fig. 13(d) shows the relative differences in torque ripple factor,

$$T_{rf} = \frac{T_{max} - T_{min}}{T_{av}}, \tag{12}$$

where T_{max}, T_{min}, and T_{av} are the maximum, minimum and average torque exerted. As anticipated, torque ripple worsened as a result of modifying the TSF; Fig. 12 displays the corresponding waveforms.

VI. CONCLUSION

This paper has presented a novel modulation logic, called 'Synchronized Switching Modulation' — SSM, aimed at switched reluctance machine (SRM) driving. This modulation scheme synchronizes phase commutations during overlap intervals, which results in great reductions of current peaks to/from the DC bus. This is confirmed not only by performance simulations but also by experimental testing in a real-world motor testbench equipped with its corresponding power converter, where SSM-enhanced torque sharing has been compared with the classic torque sharing scheme.

Such comparisons have shown that:

1) The reduction of i_{Cap} was significant over the full range tested, and mainly with low-to-medium load regimes, exhibiting an average improvement of 16% over a wide operating area.
2) This drop in i_{Cap} allows a reduction of 20.8 % in the required capacitance considering the worst operating point.

3) The overall system efficiency improved up to 6%, as a result of the reduction of energy exchange between the SRM and the power converter.
4) Because the torque sharing function gets distorted by the SSM, the torque ripple worsened slightly.

These experimental results are promising, and make the SSM particularly suitable for SRMs operating at low-to-medium loads. This suggests to use the SSM in heavy-duty applications or in-wheel without gearbox, where operating speeds are relatively low. But also, because EV motors usually run under low-to-medium load regimes, the SSM could also be used along with other modulation schemes in central motor-equipped EVs, by combining the SSM with other modulation schemes in an adaptive fashion — i.e. choosing the best scheme on the fly as a function of operating conditions.

With respect to the main drawback of slightly worsening the torque ripple, this can be regarded to be a small price to be paid in exchange of a much better benefit: to greatly reduce the capacitance requirements of the DC bus (lower system cost and higher power density and reliability), and to improve overall system efficiency, relax cooling requirements, etc.

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