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A Novel Grid Synchronization Method Based on Hybrid Filter Under Distorted Voltage Conditions

NANMU HUI[1], ZONGAN LUO[2], YINGYING FENG[2], AND XIAOWEI HAN[1]
[1]Institute of Scientific and Technological Innovation, Shenyang University, Shenyang 110044, China
[2]The State Key Laboratory of Rolling and Automation, Northeastern University, Shenyang 110819, China

Corresponding authors: Nanmu Hui (huinanmu@126.com) and Zongan Luo (luoza2020@163.com)

ABSTRACT The phase-locked accuracy of conventional phase-locked method is reduced when the grid voltage contains fundamental frequency negative sequence(FFNS) component, harmonic component, and DC offset component. Aiming at this problem, a novel adaptive notch filter (NANF) is proposed, and a dual NANF (DNANF) structure is designed to eliminate the FFNS component and extract the fundamental frequency positive sequence(FFPS) component based on NANF. Furthermore, *dc*DNANF with DC offset rejection capability is proposed by adopting DNANF. Then a novel hybrid filter in *dq*-frame is designed by combining *dc*DNANF and the cascaded delay signal cancellation operator filter whose delay parameters are 4 and 24 in *dq*-frame (*dq*CDSC$_{4,24}$). Meanwhile, a new SRF-PLL design method is proposed based on the novel hybrid filter. This proposed method employs *dq*CDSC$_{4,24}$ to separate the positive and negative sequences of the voltage and eliminate the high frequency harmonics in the grid voltage, and uses *dc*DNANF to reject the DC offset, so as to achieve the accurate acquisition of the fundamental voltage information under distortion and unbalanced grid. Simulation and experimental results show that compared with the conventional SRF-PLL methods, the proposed method can obtain faster phase tracking speed, better phase-locked effect, faster dynamic response, and better stability.

INDEX TERMS Novel adaptive notch filter (NANF), harmonic, phase-locked loop (PLL), dc offset, cascaded delay signal cancellation (CDSC).

I. INTRODUCTION

With the development of new renewable energy generation technologies such as photovoltaic, wind power, etc., distributed generation is increasingly becoming an effective way for meeting the requirement for load growth, reducing environmental pollution, improving the comprehensive utilization efficiency of energy, and improving the reliability of power supply, so it is widely used in the distribution networks[1]. In order to connect the renewable energy generated by distributed generation to the utility grid through grid-connected power converters, and realize continuous and stable operation of the system especially under medium and high voltage conditions, appropriate grid synchronization method is required to realize operation and control on grid-connected converter, and ensures that the output voltage is synchronized with the grid voltage[2]. Grid synchronization technology is usually aimed at the phase and frequency of the grid voltage signal. The ideal grid synchronization technology must meet the following conditions[3]:

- Fast phase angle tracking ability of power grid.
- Effective detection of grid frequency variation.
- Fast response to grid voltage variation.
- Effective elimination of interference and higher harmonic components.

Phase-locked loop (PLL) is one of the essential key grid synchronization technologies in three-phase system applications [4], [5]. It has extremely strict requirements on the dynamic performance and the phase quality. Therefore, it is necessary to track the voltage phase of power grid quickly and accurately, and eliminate the harmonic content in the phase information to meet various adverse grid voltage conditions [6], [7]. The synchronous reference frame phase-locked loop (SRF-PLL) has the advantages of simple structure and easy implementation, and has been widely used in power electronics and power systems. When the three-phase voltage is balanced and not distorted, the SRF-PLL can track the voltage phase quickly and accurately. When the

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three-phase voltage is unbalanced and distorted, the bandwidth of SRF-PLL needs to be reduced to improve the harmonic suppression capability, but the response speed is also reduced [8], [9]. In order to further improve the filtering performance and dynamic response speed of SRF-PLL, many advanced three-phase PLLs based on SRF-PLL have been proposed. Most of these methods improve the performance of SRF-PLL by improving the filtering stage [10]–[13].

To eliminate different harmonic components in the grid voltage, many DSC methods have been proposed by some scholars [14]–[16]. *dq*DSC-PLL proposed in [17] adopts a method of cascading multiple DSC operators with different time delays to achieve specific filtering effects in *dq*-frame. [18] proposed an improved frequency adaptive DSC-PLL structure to make the PLL adapting to grid voltage frequency changes. The adaptive process of this structure needs to calculate the difference, and the number of DSC modules will determine the computational burden of adaptive difference. But this method does not solve the problem of reducing the number of cascaded modules, so the system computational burden and implementation complexity is large. [19] adopted non-adaptive cascaded DSC module and additional phase and amplitude compensator to propose enhanced generalized DSC(EGDSC-PLL). The computational complexity of this method is much smaller than that of the adaptive DSC cascade method, but it can also accurately track the frequency change of power grid. However, the disadvantage of this approach is that when the power grid is distorted and the frequency is greatly changed, the filtering ability of the approach is deteriorated, and the large estimation error will occur.

Notch filter is another advanced method used in SRF-PLL [20]–[22]. [23] employed ANF-PLL to eliminate the specific harmonic interference components when the grid frequency changes. In addition, the narrow bandwidth of NF will not cause a large phase delay in the PLL, which will simplify the PLL parameter setting process, so it will not affect the dynamic characteristics and phase tracking accuracy of the PLL. However, these advantages of ANF come at the cost of increased computation. In order to eliminate multiple specific harmonic interference components, [24] adopted the method of connecting multiple NFs in series. Although the filtering performance can be improved by connecting multiple NFs in series, the computational burden will increase. [25] proposed a novel complex notch filter(CNF) based on complex filter. This approach is simple to implement and has fast dynamic response speed. At the same time, it solves the problem of large computational burden for conventional NF.

How to reject the DC offset in the grid voltage is also the main problem that the PLL needs to solve urgently [26]–[29]. In [30], a PLL based on cross-feedback network (CFN) and a PLL based on complex coefficient network (CNN) are proposed. These two approaches are mathematically equivalent, and both employ LPF to reject the DC offset of the input voltage. The estimated DC offset is then subtracted from the grid voltage to achieve the purpose of rejecting DC offset. However, CFN-PLL and CCN-PLL may cause slower dynamic response due to multiple LPFs, and the choice of LPF cutoff frequency may reduce harmonic filtering performance. Furthermore, [31] proposed a HIDHO-PLL composed of a novel DC offset compensation cell (DOCC) and a harmonics and / or interharmonics compensation network (HIH-CN) in the *dq*-frame. This approach can effectively eliminate harmonics, interharmonics and DC offsets in the power grid, but its structure is more complex and difficult to implement. [32] used a new structure with SOGI and TOGI to eliminate the DC offset and the FFNS component in the power grid. However, when the power grid is distorted, this approach has weak disturbance rejection ability.

To improve the filtering performance and dynamic response speed of SRF-PLL, this paper proposes a three-phase grid-connected phase-locked loop based on a hybrid filter composed of DNANF with DC offset rejection capability and $dq\text{CDSC}_{4,24}$. First, a novel adaptive ANF (NANF) is proposed, and a *dc*DNANF with DC offset rejection capability based on NANF is proposed to reject the DC offset component of the grid voltage. Simultaneously, the conventional *dq*DSC operator is studied, and the $dq\text{CDSC}_{4,24}$ cascaded with $dq\text{DSC}_4$ and $dq\text{DSC}_{24}$ are used to eliminate the FFNS component and other harmonic components of the power grid. Then, *dc*DNANF and $dq\text{CDSC}_{4,24}$ are combined to form a series hybrid filter, which is combined with the inner loop of the SRF-PLL to propose a hybrid filter-based PLL. Finally, the model accuracy of the proposed PLL is verified by simulation, and the validity of the proposed PLL is verified by simulation and experiments.

II. NOVEL ADAPTIVE NOTCH FILTER

In order to reduce the influence of the doubling power frequency fluctuation caused by the FFNS component of the SRF-PLL, and then effectively separate the fundamental frequency positive and negative sequence component, this paper proposes a novel adaptive notch filter (NANF) signal processing module, its structure is shown in Fig.1.

In Fig.1, the input signal is u, and the output signal is v' and its quadrature signal is qv'. It has frequency adaptive function, when the frequency of the grid voltage changes, this notch filter can adjust the frequency of the grid to achieve grid frequency tracking, and output an adaptive frequency estimation signal.

NANF can be described by the following differential equations:

$$\ddot{x} = \hat{\omega} e \tag{1}$$

$$e = 2\xi u - 2\xi \dot{x} - \hat{\omega} x \tag{2}$$

$$\dot{\hat{\omega}} = \eta x \hat{\omega} e \tag{3}$$

where, $\hat{\omega}$ is the voltage frequency estimated value of the power grid, its first derivative is $\dot{\hat{\omega}}$. The parameters η and ξ determine the accuracy and response speed of the voltage frequency estimation, respectively. x represents intermediate variables, $\dot{x}$ and $\ddot{x}$ are the first and second derivatives of x.

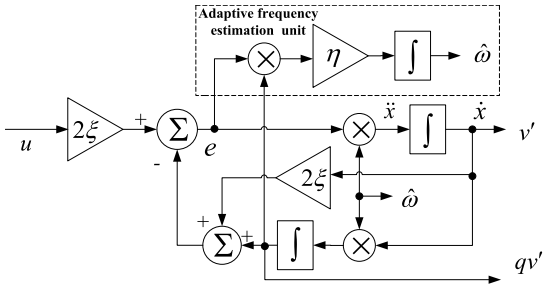

FIGURE 1. The implementation of NANF.

If the input of the adaptive notch filter is a sinusoidal input signal $u = A\sin(\omega t + \varphi)$, and the angular frequency of the input signal is the same as ω, then the mathematical equation of the adaptive notch filter has a unique solution as

$$\begin{bmatrix} x \\ \dot{x} \\ \hat{\omega} \end{bmatrix} = \begin{bmatrix} -\frac{A}{\omega}\cos(\omega t + \varphi) \\ A\sin(\omega t + \varphi) \\ \omega \end{bmatrix} \tag{4}$$

According to Fig.1, the output signals v' and qv' can be obtained as

$$v' = \dot{x} = A\sin(\omega t + \varphi) \tag{5}$$

$$qv' = \omega x = -A\cos(\omega t + \varphi) \tag{6}$$

It can be seen from the output characteristics of the NANF that the NANF unit can obtain a set of orthogonal output signals based on a single input signal.

In addition, according to Fig.1, the s-domain input-output relationship can be calculated as follow:

$$\begin{cases} 2\xi \cdot u(s) - 2\xi \cdot v'(s) - \dfrac{\hat{\omega}}{s} \cdot v'(s) = \dfrac{s}{\hat{\omega}} \cdot v'(s) \\ s \cdot qv'(s) = \hat{\omega} \cdot v'(s) \end{cases} \tag{7}$$

The transfer function of the NANF unit can be obtained from (7) as follows:

$$D(s) = \frac{v'(s)}{u(s)} = \frac{2\xi\hat{\omega}s}{s^2 + 2\xi\hat{\omega}s + \hat{\omega}^2} \tag{8}$$

$$Q(s) = \frac{qv'(s)}{u(s)} = \frac{2\xi\hat{\omega}^2}{s^2 + 2\xi\hat{\omega}s + \hat{\omega}^2} \tag{9}$$

According to equations (8) and (9), the steady-state components of the time response of v' and qv' can be calculated as

$$D(t) = |D(j\omega)|\angle D(j\omega) \tag{10}$$

$$Q(t) = \left|\frac{\hat{\omega}}{\omega}D(j\omega)\right| \angle\left[\angle D(j\omega) - \frac{\pi}{2}\right] \tag{11}$$

where

$$|D(j\omega)| = \frac{2\xi\omega\hat{\omega}}{\sqrt{(2\xi\omega\hat{\omega})^2 + (\omega^2 - \hat{\omega}^2)^2}} \tag{12}$$

$$\angle D(j\omega) = \arctan\left(\frac{\hat{\omega}^2 - \omega^2}{2\xi\omega\hat{\omega}}\right) \tag{13}$$

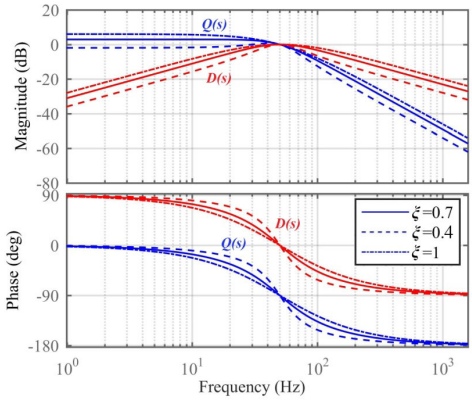

FIGURE 2. The Bode diagram of D(s) and Q(s).

Then equation (14) (15) can be obtained from equation (10)(11)

$$\lim_{\xi\to 0} \angle D(j\omega) = \begin{cases} \dfrac{\pi}{2}, & \hat{\omega} > \omega \\ -\dfrac{\pi}{2}, & \hat{\omega} < \omega \end{cases} \tag{14}$$

$$\lim_{\xi\to 0} |D(j\omega)| = \begin{cases} 1, & \hat{\omega} = \omega \\ 0, & \hat{\omega} \neq \omega \end{cases} \tag{15}$$

(14) and (15) show that reducing the parameter ξ, phase delay of the filter will increase, meanwhile, the bandwidth will narrow, and the frequency resolution of the filter will increase.

Fig.2 shows the D(s) and $Q(s)$ bode plots when $\hat{\omega} = 2\pi f = 100\pi$ and ξ is 1, 0.7 and 0.4, respectively. It can be seen from Fig.2 that the variation trend of the frequency response curves of v' and qv' with parameter ξ is consistent with the theoretical analysis results.

To achieve the frequency adaptive function, NANF introduced a frequency adaptive feedback unit. When the frequency of the input signal interferes, it can accurately track the frequency. It employs the difference signal e and the output signal qv' as feedback control to achieve adaptive adjustment. The transfer function of the difference signal e is

$$E(s) = \frac{e(s)}{u(s)} = \frac{s^2 + \hat{\omega}^2}{s^2 + 2\xi\hat{\omega}s + \hat{\omega}^2} \tag{16}$$

The bode plots for $Q(s)$ and $E(s)$ can be drawn from equations (9) and (16) as shown in Fig.3. From Fig.3, it can be observed that when the grid frequency is lower than the resonance frequency of the NF structure($\omega < \hat{\omega}$), the difference signal e and the output signal qv' have the same changing trends, and when the grid frequency is higher than the resonance frequency of the NF structure($\omega > \hat{\omega}$), the difference signal e and the output signal qv' have opposite changing trends. Therefore, the frequency error variable e_f can be defined as the product of qv' and e. So $e_f > 0$ when $\omega < \hat{\omega}$, $e_f = 0$ when $\omega = \hat{\omega}$, $e_f < 0$ when $\omega > \hat{\omega}$, and it can be controlled by adjusting the proportionality factor η which is

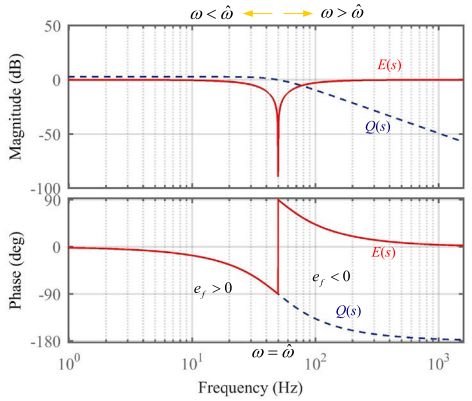

FIGURE 3. The Bode diagram of Q(s) and E(s).

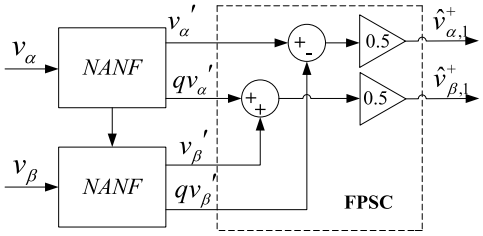

FIGURE 4. Block diagram of DNANF.

the negative feedback gain to make the difference between ω and $\hat{\omega}$ to zero for frequency tracking[11].

From the above analysis, it can be known that $\hat{\omega}$ determines the center frequency of NANF and can adaptively track the frequency change of the input signal. The convergence speed and error of frequency tracking are adjusted by the parameters ξ and η. Parameter ξ determines the filter's bandwidth and transient convergence speed. There is a contradiction between frequency selectivity and convergence speed, so the choice of parameter ξ should be considered in a compromise.

By analyzing the equation (16) which is the transfer function of NANF, it can be found that it is consistent with the transfer function of conventional ANF in [37], so the NANF is equivalent to the conventional adaptive notch filters proposed in [37]–[39], and its performance is consistent with the conventional adaptive notch filter.

III. DNANF WITH DC OFFSET REJECTION CAPABILITY

In phase-locked loop grid-connected synchronization applications, two NANFs are usually employed in parallel and combined with the fundamental frequency positive sequence calculator (FPSC) to extract the FFPS component.

The DNANF structure is shown in Fig.4. v_α and v_β are input signals in the $\alpha\beta$-frame, v_α and v_β are input into DNANF to generate orthogonal signals v_α', qv_α', v_β', and qv_β'. These signals are added as input signals to the FPSC to extract the FFPS components $\hat{v}^+_{\alpha,1}$ and $\hat{v}^+_{\beta,1}$,

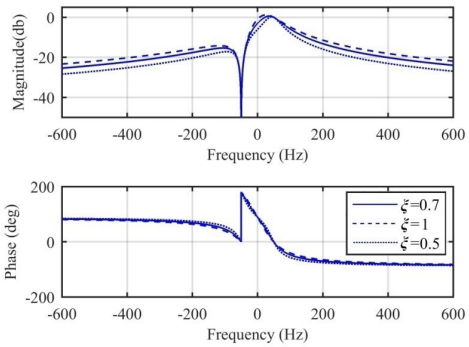

FIGURE 5. The Bode diagram of DNANF(s).

so equation (17) can be obtained from Fig.4.

$$\begin{bmatrix} \hat{v}^+_{\alpha,1} \\ \hat{v}^+_{\beta,1} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{17}$$

Here, the theory of complex filter is used to analyze DNANF. The complex filter is considered to be a transfer function with two inputs and two outputs[33]. The transfer function $H(s)$ is

$$H(s) = H^{Re}(s) + jH^{Im}(s) \tag{18}$$

where $H^{\mathrm{Re}}(s)$ is the real part of $H(\mathrm{s})$ and $H^{\mathrm{Im}}(s)$ is the imaginary part of $H(\mathrm{s})$.

Using the theory of complex filter, DNANF can be regarded as a complex filter. According to its structure diagram, it can be seen that the real and imaginary parts of the complex filter transfer functions are

$$R_{\mathrm{DNANF}}(s) = D(s) = \frac{2\xi\hat{\omega}s}{s^2 + 2\xi\hat{\omega}s + \hat{\omega}^2} \tag{19}$$

$$Q_{\mathrm{DNANF}}(s) = Q(s) = \frac{2\xi\hat{\omega}^2}{s^2 + 2\xi\hat{\omega}s + \hat{\omega}^2} \tag{20}$$

According to (17), DNANF can be written in the form of a complex transfer function, so the expression of DNANF's transfer function is as follow:

$$\begin{aligned} \mathrm{DNANF}(s) &= \frac{1}{2}(R_{\mathrm{DNANF}}(s) + jQ_{\mathrm{DNANF}}(s)) \\ &= \frac{1}{2}\frac{2\xi\hat{\omega}(s+j\hat{\omega})}{s^2+2\xi\hat{\omega}s+\hat{\omega}^2} = \frac{\xi\hat{\omega}(s+j\hat{\omega})}{s^2+2\xi\hat{\omega}s+\hat{\omega}^2} \end{aligned} \tag{21}$$

When ξ takes different values, the bode plot of DNANF(s) is shown in Fig.5

According to [25], the corresponding relationship between voltage components and frequencies in different frames under the adverse grid condition is shown in Table 1, and the grid frequency is 50 Hz.

As can be seen from Fig.5 and Table 1, for $\alpha\beta$-frame, the amplitude gain of DNANF (s) is 0 at +50Hz and the gain at −50Hz is $-\infty$. It shows that the method can detect the FFPS component without attenuation, and can completely attenuate the FFNS component. Furthermore, the phase at the

TABLE 1. Dominant components of grid voltage.

Harmonic order	⋯	-11	-5	-1	0	+1	+7	+13	⋯
$\alpha\beta$-frame (Hz)	⋯	-550	-250	-50	0	50	350	650	⋯
dq-frame (Hz)	⋯	-600	-300	-100	-50	0	300	600	⋯

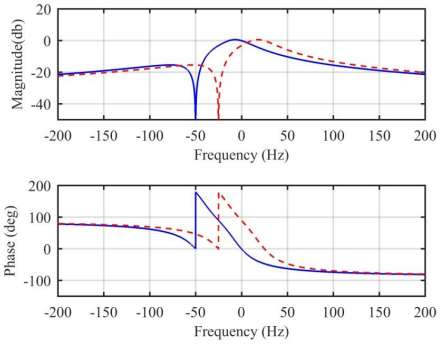

FIGURE 6. Bode diagram of dcDNANF(s).

fundamental frequency is 0, indicating that there is no phase difference in the detection of the FFPS component.

The DNANF with DC offset rejection capability (*dc*DNANF) proposed in this paper is obtained by taking the notch frequency $\hat{\omega}$ as $\hat{\omega}_{dc} = 0.5\hat{\omega}$ and then replacing s in DNANF(s) with $s+j\hat{\omega}_{dc}$. The transfer function of *dc*DNANF is

$$\begin{aligned} dc\text{DNANF}(s) &= \text{DNANF}(s+j\hat{\omega}_{dc}) \\ &= \frac{\xi\hat{\omega}_{dc}(s+j2\hat{\omega}_{dc})}{s^2+2(\xi\hat{\omega}_{dc}+j\hat{\omega}_{dc})s+j2\xi\hat{\omega}_{dc}^2} \end{aligned} \tag{22}$$

When the notch frequency $\hat{\omega}_{dc}$ is $0.5\hat{\omega}$, the corresponding frequency characteristics of DNANF(s) and the proposed *dc*DNANF(s) are shown in Fig.6, ξ temporarily takes 0.7. In the figure, the red dotted line is the frequency characteristic curve corresponding to DNANF(s). After changing the value of $\hat{\omega}$ from $2\pi 50$ rad/s to $2\pi 25$ rad/s, the notch frequency is -25Hz. Then replacing s with $s+j\hat{\omega}_{dc}$, that is, shifting the red dotted line to the left by 25Hz to obtain the frequency characteristic curve of *dc*DNANF(s) corresponding to the solid blue line.

As can be seen from Fig.6 and Table 1, for dq-frame, the amplitude gain of *dc*DNANF(s) is 0 at 0Hz and the gain at -50Hz is $-\infty$. It means that the method can detect the fundamental frequency positive sequence component without attenuation, and can completely reject the DC offset. Furthermore, the phase at the fundamental frequency is 0, indicating that there is no phase difference in the detection of the FFPS component.

The step response study of *dc*DNANF transfer function is helpful to further determine the value of ξ. For the complex transfer function *dc*DNANF(s), its unit step response of the

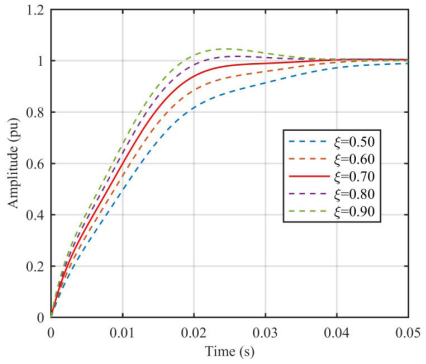

FIGURE 7. Step response of dcDNANF(s).

input signal is

$$U_{step}(s) = \frac{1}{s} + j0 \tag{23}$$

So the step response expression of *dc*DNANF(s) is

$$\begin{aligned} Y(s) &= dc\text{DNANF}(s)U_{step}(s) \\ &= \frac{\xi\hat{\omega}_{dc}(s+j2\hat{\omega}_{dc})}{s^2+2(\xi\hat{\omega}_{dc}+j\hat{\omega}_{dc})s+j2\xi\hat{\omega}_{dc}^2}\frac{1}{s} \end{aligned} \tag{24}$$

The time-domain expression of step response can be obtained by inverse Laplace transform of (24). The time domain expression curve is drawn with different damping coefficients, as shown in Fig.7. As shown in Fig. 7, when ξ increases, the step response is faster, but the overshoot is greater. When ξ is smaller, the settling time is longer, but the overshoot is smaller. To make the step response with faster response speed and smaller overshoot, select ξ to be 0.7.

Furthermore, the expressions of the real part $R_{dc\text{DNANF}}(s)$ of *dc*DNANF(s) can be obtained by conjugate operation of the numerator and denominator in (22).

$$\begin{aligned} &R_{dc\text{DNANF}}(s) \\ &= \frac{\xi\hat{\omega}_{dc}s^3+2\xi^2\hat{\omega}_{dc}^2s^2+4\xi\hat{\omega}_{dc}^3s+4\xi^2\hat{\omega}_{dc}^4}{s^4+4\xi\hat{\omega}_{dc}s^3+4\hat{\omega}_{dc}^2(1+\xi^2)s^2+8\xi\hat{\omega}_{dc}^3s+4\xi^2\hat{\omega}_{dc}^4} \end{aligned} \tag{25}$$

The transfer function of *dc*DNANF can be approximated equivalent using the real part $R_{dc\text{DNANF}}(s)$. Fig.8 shows the approximate equivalent bode plots of *dc*DNANF(s) and $R_{dc\text{DNANF}}(s)$, which are represented by solid blue and red dashed lines, respectively. As can be seen from the figure, $R_{dc\text{DNANF}}(s)$. can better describe the curve of *dc*DNANF(s) in amplitude and phase.

IV. CASCADED dqDSC$_{4,24}$ FILTER

The filtering method based on DSC is a widely studied method. The conventional DSC filter is usually set in the $\alpha\beta$- frame, and can be used in the dq-frame.

The transfer function of dqDSC is

$$dqDSC_n(s) = \frac{1}{2}(1+e^{-\frac{T}{n}s}) \tag{26}$$

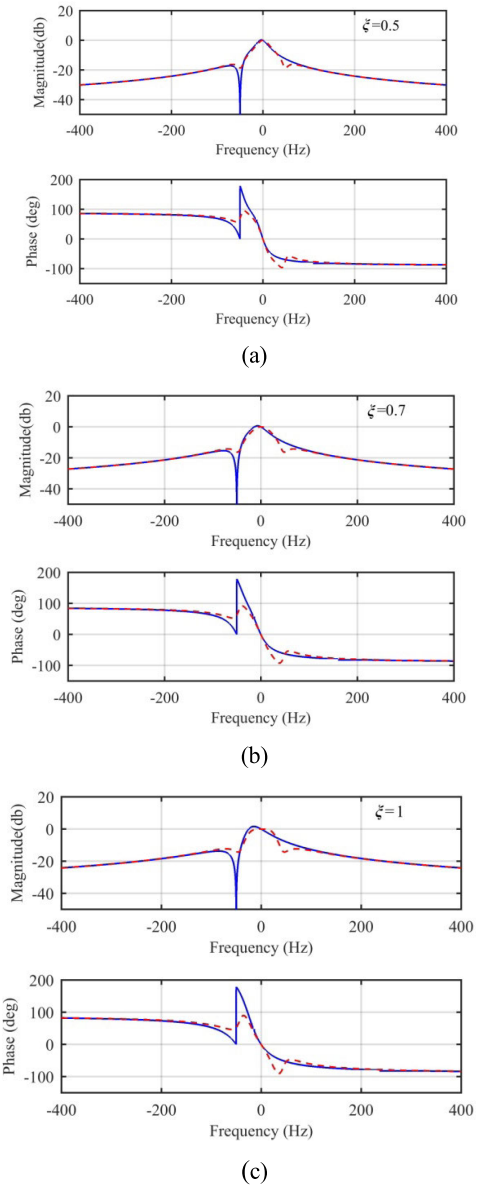

FIGURE 8. Approximate equivalent bode diagrams of dcDNANF(s) and $R_{dcDNANF}(s)$ (a) $\xi = 0.5$, (b) $\xi = 0.7$, (c) $\xi = 1$.

where, T is the fundamental frequency period of the grid voltage. n is a delay coefficient.

$$dqDSC_n(j\omega) = \left|\cos\left(\frac{\omega T}{2n} - \frac{\pi}{n}\right)\right| \angle -\left(\frac{\omega T}{2n} - \frac{\pi}{n}\right) \quad (27)$$

Obviously, the amplitude and time delay of the $dq\text{DSC}_n$ operator depend on the delay coefficient n.

By setting different n values of $dq\text{DSC}_\text{n}$, harmonics of different orders under dq-frame can be eliminated and the FFPS remains unchanged. In most cases, a single dqDSC operator cannot eliminate all harmonic components. Therefore, according to the type of power grid harmonics and the application environment, any specified harmonics can be eliminated by cascading multiple dqDSC operators with different values of n. (28) is the expression of the cascaded

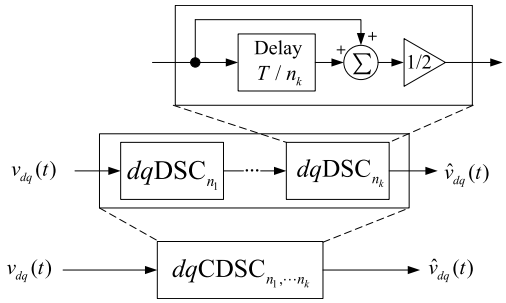

FIGURE 9. The implementation of dqCDSC.

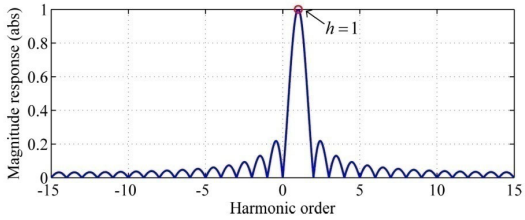

FIGURE 10. Magnitude frequency response of the $\text{dqCDSC}_{2,4,8,16,32}(s)$.

dqDSC operator (dqCDSC) in the s domain, where k is the number of dqDSC operators[16].

$$dqCDSC_{n_1,\cdots n_k}(s) = dqDSC_{n_1}(s) \times \cdots \times dqDSC_{n_k}(s) \quad (28)$$

Fig.9 shows the implementation structure of dqCDSC. In order to eliminate all harmonic interference in the dq-frame, $dq\text{DSC}_2$, $dq\text{DSC}_4$, $dq\text{DSC}_8$, $dq\text{DSC}_{16}$, and $dq\text{DSC}_{32}$ can be selected to cascade to form $dq\text{CDSC}_{2,4,8,16,32}$. The amplitude-frequency characteristics of $dq\text{CDSC}_{2,4,8,16,32}$ in abc-frame are shown in Fig.10.

However, $dq\text{CDSC}_{2,4,8,16,32}$ eliminates all harmonics at the cost of increasing the system delay time and the computational burden. The system delay time introduced by the $dq\text{CDSC}_{2,4,8,16,32}$ operator $T_d = T/2 + T/4 + \ldots + T/32 \approx 0.97T$. This delay of $0.97T$ will reduce the dynamic performance of the PLL.

In order to eliminate the non triple odd harmonics, namely -5th, $+7$th, -11th, $+13$th, -17th, $+19$th…,the $dq\text{CDSC}_{4,24}$ filter cascaded $dq\text{DSC}_4$ and $dq\text{DSC}_{24}$ is used in this paper. The filter can eliminate the FFNS component and other harmonic components in Table 1.

From the (26) and (28), the expression of $dq\text{CDSC}_{4,24}$ filter can be concluded as follow

$$\begin{aligned} dqCDSC_{4,24}(s) &= dqDSC_4(s) \times dqDSC_{24}(s) \\ &= \frac{1}{2}(1 + e^{-\frac{T}{4}s}) \times \frac{1}{2}(1 + e^{-\frac{T}{24}s}) \end{aligned} \quad (29)$$

then

$$dqCDSC_{4,24}(s) = \frac{1}{4}(1 + e^{-\frac{T}{4}s})(1 + e^{-\frac{T}{24}s}) \quad (30)$$

Fig.11 is the bode plot of $dq\text{CDSC}_{4,24}$ filter. It can be seen from the figure that $dq\text{CDSC}_{4,24}$ can eliminate the FFNS

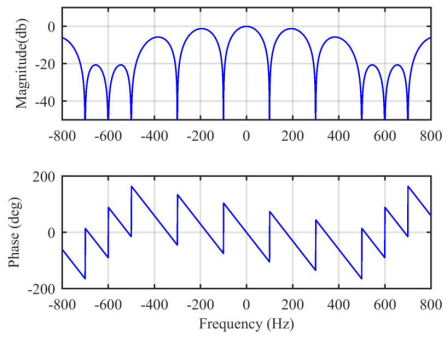

FIGURE 11. Bode diagram of $\mathrm{dqCDSC}_{4,24}(s)$.

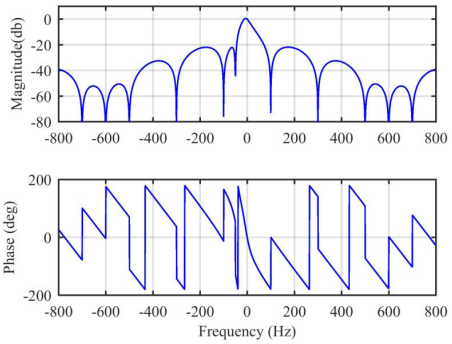

FIGURE 13. Frequency response of the proposed hybrid filter.

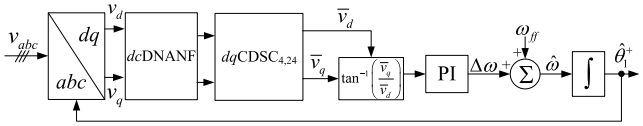

FIGURE 12. Block diagram of the proposed PLL.

FIGURE 14. Small-signal model of the proposed PLL.

component of the grid voltage and the corresponding harmonics component of ± 300Hz, ± 600Hz... At the same time, the FFPS component of the grid voltage corresponding to 0Hz is multiplied by 1, and the phase is 0, which means that FFPS component is not affected. In addition, the introduced system delay time $T_{\mathrm{d}} = T/4 + T/24 \approx 0.29T$, which is much shorter than the system delay time 0.97T introduced by $dq\mathrm{CDSC}_{2,4,8,16,32}$, it indicates that the dynamic performance of $dq\mathrm{CDSC}_{4,24}$ filter is much better than $dq\mathrm{CDSC}_{2,4,8,16,32}$.

V. HYBRID FILTER -BASED PLL

A. DESIGN OF HYBRID FILTER BASED ON dcDNAF AND $dq\mathrm{DSC}_{4,24}$

In this paper, dcDNANF and $dq\mathrm{CDSC}_{4,24}$ are combined in series to form a new hybrid filter, and this filter is integrated into the inner loop of the SRF-PLL to form the proposed PLL. Its structure is shown in Fig.12.

According to Table 1, dcDNANF is used to reject the DC offset component of −50Hz in the dq-frame, and $dq\mathrm{CDSC}_{4,24}$ is used to eliminate the fundamental frequency negative sequence component and the −5th, +7th, −11th, +13th... harmonic components.

The transfer function of a hybrid filter composed of dcDNANF and $dq\mathrm{CDSC}_{4,24}$ is.

$$\begin{aligned} H(s) &= dcDNANF(s)dqCDSC_{4,24}(s) \\ &= \frac{1}{4}\frac{\xi\hat{\omega}_{dc}(s+j2\hat{\omega}_{dc})}{s^2+2(\xi\hat{\omega}_{dc}+j\hat{\omega}_{dc})s+j2\xi\hat{\omega}_{dc}^2}(1+e^{-\frac{T}{4}s}) \\ &\quad\times(1+e^{-\frac{T}{24}s}) \end{aligned} \tag{31}$$

According to (31), the frequency response curve of the proposed hybrid filter is plotted, as shown in Fig.13. It can be seen from Fig.13 that in the dq-rame, the amplitude gain at 0Hz is 0, the amplitude gains at −100Hz, −50Hz and −5th, +7th, −11th, +13th... harmonics are $-\infty$, indicating that the hybrid filter can detect the FFPS component without attenuation, while the FFNS component, DC offset component and other harmonic components can achieve full attenuation. Simultaneously, the phase at the fundamental frequency is 0, it shows that there is no phase difference in the detection of FFPS component.

B. PARAMETER DESIGN GUIDELINES

As the structure of the proposed PLL has been shown in Fig.12, the small-signal model of the proposed PLL can be simply obtained in Fig.14. According to the modeling method in [25], the dcDNANF(s). is modeled by $R_{dc\mathrm{DNANF}}(s)$ for mathematical modeling. The accuracy will be examined later by simulation.

The open-loop transfer function for the small-signal model is

$$\begin{aligned} Gol(s) &= \frac{\hat{\theta}_1^+}{\Delta\theta_1^+} = R_{dc\mathrm{DNANF}}(s)dqCDSC_{4,24}(s)\frac{k_ps+k_i}{s^2} \\ &= \frac{\xi\hat{\omega}_{dc}s^3+2\xi^2\hat{\omega}_{dc}^2s^2+4\xi\hat{\omega}_{dc}^3s+4\xi^2\hat{\omega}_{dc}^4}{s^4+4\xi\hat{\omega}_{dc}s^3+4\hat{\omega}_{dc}^2(1+\xi^2)s^2+8\xi\hat{\omega}_{dc}^3s+4\xi^2\hat{\omega}_{dc}^4} \\ &\quad\times\frac{1}{4}(1+e^{-\frac{T}{4}s})(1+e^{-\frac{T}{24}s})\frac{k_ps+k_i}{s^2} \end{aligned} \tag{32}$$

Because the existence of delay link in $e^{-(T/4)s}$ and $e^{-(T/24)s}$ in (32), the first-order Pade approximation approach[30] is employed to replace the delay link as follows:

$$e^{-(T/4)s} \approx \frac{1-sT/8}{1+sT/8} \tag{33}$$

$$e^{-(T/24)s} \approx \frac{1-sT/48}{1+sT/48} \tag{34}$$

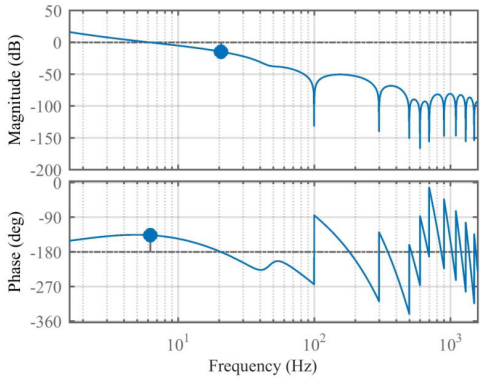

FIGURE 15. Open-loop bode diagram of proposed PLL.

So

$$dqCDSC_{4,24}(s) = \frac{1}{4}(1+e^{-\frac{T}{4}s})(1+e^{-\frac{T}{24}s}) \approx \frac{1}{1+sT/8}\cdot\frac{1}{1+sT/48} \tag{35}$$

The presence of the high-order components in (32) complicates the analysis and design PLL. According to the reduced order equivalent method of higher-order PLL system in [34], the Pade approximation reduction approach in [35] is adopted to equivalent $R_{dc\mathrm{DNANF}}(s)\cdot dq\mathrm{CDSC}_{4,24}(s)$ as the first order transfer function.

$$R_{dc\mathrm{DNANF}}(s)dqCDSC_{4,24}(s) = \frac{\xi\hat{\omega}_{dc}s^3+2\xi^2\hat{\omega}_{dc}^2s^2+4\xi\hat{\omega}_{dc}^3s+4\xi^2\hat{\omega}_{dc}^4}{s^4+4\xi\hat{\omega}_{dc}s^3+4\hat{\omega}_{dc}^2(1+\xi^2)s^2+8\xi\hat{\omega}_{dc}^3s+4\xi^2\hat{\omega}_{dc}^4}\cdot\frac{1}{1+sT/8}\cdot\frac{1}{1+sT/48}\approx\frac{86.36}{s+86.36} \tag{36}$$

So

$$Gol(s)\approx\frac{86.36}{s+86.36}\frac{k_ps+k_i}{s^2}=\frac{1}{1+s\underbrace{(1/86.36)}_{t_d}}\frac{k_ps+k_i}{s^2} \tag{37}$$

where, t_d is the delay factor of the system, in order to obtain the PI controller parameters for (37), this paper uses the symmetric optimal design method in [30] to give the two parameters of the PI controller as:

$$k_p = 1/(bt_d) \quad k_i = 1/(b^3t_d^2) \tag{38}$$

where $t_\mathrm{d} = 1/86.36$, b is the parameter of phase margin (PM) and is set to $1+\sqrt{2}$, then $k_p = 35.8$ and $k_i = 530.4$. The frequency response curve of the system open-loop transfer function is shown in Fig.15. The PM is 43.6° and the corresponding frequency is 6.24 Hz. The gain margin(GM) the PLL is 14.5dB, the corresponding frequency is 20.7Hz, so the system stability can be ensured.

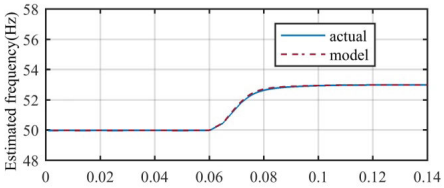

FIGURE 16. Performance comparison between proposed-PLL and its small-signal model.

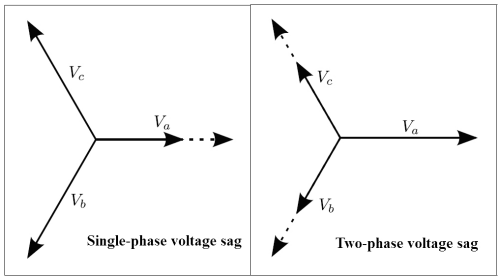

FIGURE 17. Schematic diagram of two types voltage sag faults.

TABLE 2. PLLs' design parameters.

	Proposed-PLL	EGDSC-PLL	NF-PLL
Damping coefficient, ξ	0.7	1	—
Proportional coefficient, k_p	35.8	440	92
Integral coefficient, k_i	530.4	48361	3507.1

C. ACCURACY OF MATHEMATICL MODEL

To verify the accuracy of the small-signal model, this section compares the proposed PLL and its mathematical model results under MATLAB/Simulink. In the simulation, the estimated frequency under frequency jump of +3Hz are compared, as shown in Fig.16. It can be observed that high accuracy of the small-signal model can be verified.

VI. SIMULATION RESULTS

To verify the performance of the proposed PLL, in this paper, MATLAB/Simulink software is employed to perform phase and frequency estimation simulation comparison experiments under two kinds of voltage sag faults. In the simulation, the grid frequency is 50 Hz, the three-phase voltage amplitude is normalized to 1 p.u, and the sampling frequency is 10 kHz.

The two common voltage sag faults in the power system are shown in Fig.17, including single-phase voltage sag and two-phase voltage sag. Because the proposed PLL method in this paper is based on the structure of NANF and uses the $dq\mathrm{DSC}_{4,24}$ method, the NF-PLL [30] with DC offset rejection capability and the EDGSC-PLL [19], which is one of newer DSC method and has the best dynamic performance in recent years, are employed for comparison experiments. The design parameters of the three PLLs are shown in Table 2.

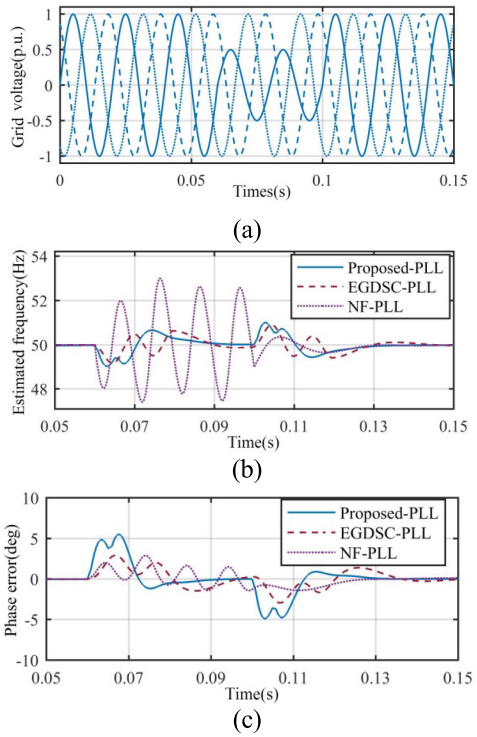

FIGURE 18. Simulation results of case1. (a) grid voltages, (b) estimated frequency, (c) phase error.

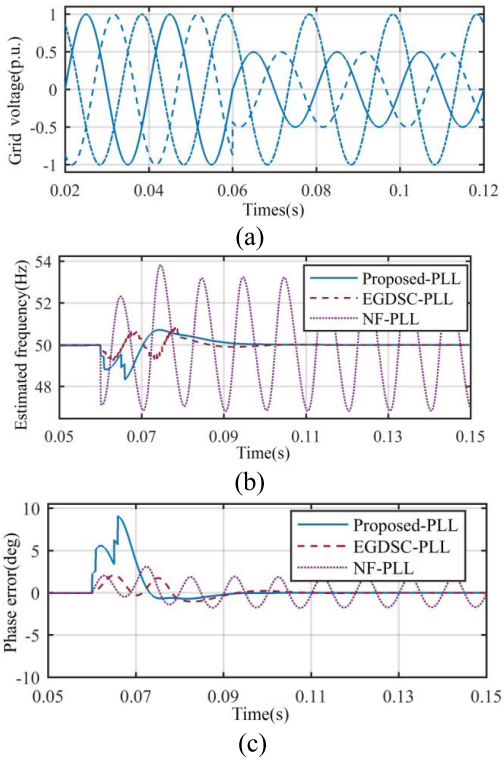

FIGURE 19. Simulation waveforms of case2 (a) grid voltages, (b) estimated frequency, (c) phase error.

A. CASE1:SINGLE-PHASE VOLTAGE SAG

When the single-phase voltage amplitude of the three-phase grid voltage drops by 50%, the simulation experiment waveform is shown in Fig.18. From Fig.18, it can be seen that the grid fault occurs at $t = 0.06$s, and the grid returns to normal at $t = 0.1$s.

It can be observed that between t $=$ 0.06s$\sim$0.1s, there are abnormal fluctuations in the phase error and estimated frequency waveforms of the three PLLs, while the NF-PLL fluctuations recover after 0.1s. The adjustment time of the proposed PLL is significantly shorter than the EDGSC-PLL, indicating that the dynamic response speed of the proposed PLL is better than the other two PLLs..

B. CASE2:TWO-PHASE VOLTAGE SAG

When the two-phase voltage amplitude of the three-phase grid voltage drops by 50%, the simulation experiment waveform is shown in Fig.19. By observing the simulation waveforms, it can be found that when the grid voltage has a two-phase sag, although the proposed PLL has large fluctuations in phase error and estimated frequency, but the dynamic adjustment time is the shortest. The dynamic adjustment time of EDGSC-PLL is longer, while the fluctuation of NF-PLL continues to be unrecoverable, which cannot meet the adjustment time requirements of the power equipment during grid connection. It can be seen that the dynamic characteristic of the proposed PLL is optimal.

VII. EXPERIMENTAL RESULTS

To confirm the effectiveness of the proposed PLL, the experiments are implemented in this section and the experimental results are analyzed, the comparison objects of the experiment are still NF-PLL and EDGSC-PLL. The DSP TMS320F28335 is employed in the experiments. The experiments are based on the arbitrary waveform generator to generate three-phase voltage signals. The sampling frequency is set to 10kHz. The nominal frequency is set to $2\pi 50$ rad/s, and the amplitude is normalized to 1p.u.. The third-order Adams-Bashforth method in[36] is used to ensure the accuracy of the discrete system model and avoid algebraic loop. The corresponding relation between the integral link of the continuous domain and the discrete domain is as follows

$$\frac{1}{s} \Leftrightarrow \frac{T_s}{12} \frac{23z^{-1} - 16z^{-2} + 5z^{-3}}{1 - z^{-1}} \tag{39}$$

A. CASE1:FREQUENCY RAMP CHANGE

Fig.20 shows the experimental waveforms when the grid voltage frequency changes from 50Hz to 55Hz. The grid voltage frequency ramp time is 50ms, and the growth rate is 100Hz / s.

By observing Fig.20, when the frequency of the grid gradually increases, the phase error of the proposed PLL in this paper is 1.5°, the phase error of EGDSC-PLL is 5.3°, and the phase error of NF-PLL is 9.1°. Therefore, when the grid frequency changes continuously, the proposed PLL in this

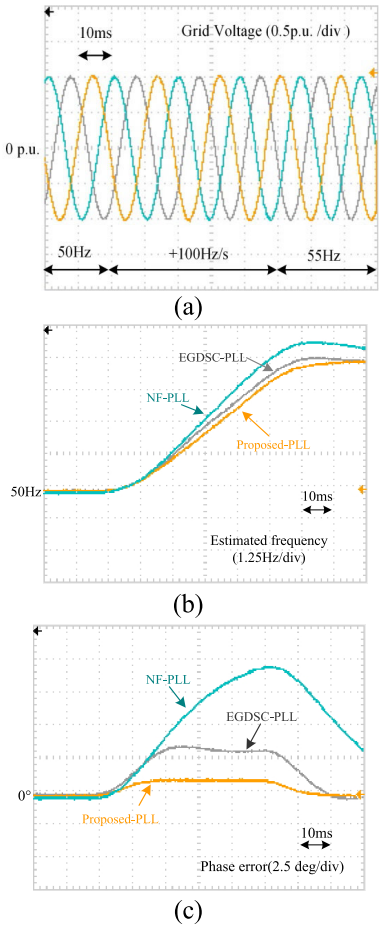

FIGURE 20. Experimental waveforms of case1. (a) grid voltages, (b) estimated frequency, (c) phase error.

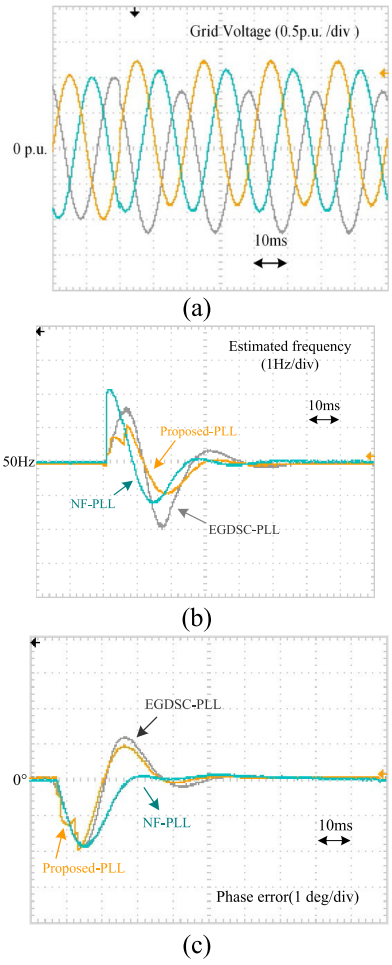

FIGURE 21. Experimental waveforms of Case2. (a) grid voltages, (b) estimated frequency, (c) phase error.

paper can achieve phase capture more accurately than the other two PLLs.

B. CASE2:DC OFFSET INJECT

In this section, the DC offset injection experiment is carried out, the DC offset injection values of the three-phase voltage are $V_a = 0.2$p.u., $V_b = 0.1$p.u., and $V_c = -0.2$p.u., respectively. The experimental waveforms are shown in Fig.21.

Fig.21 shows that after the DC offset is injected into the three-phase voltage, the DC offset has no effect on the phase error and estimated frequency of the three PLLs,because the EDGSC-PLL, NF-PLL and the proposed PLL all have DC offset rejection capability. Taking the frequency offset less than 0.2Hz as the standard, the proposed PLL and NF-PLL recover the acquisition of phase and frequency in about 30 ms, and the speed of EGDSC-PLL is slightly slower.

C. CASE3:UNBALANCED AND DISTORTED GRID VOLTAGES

The distorted voltage phase and frequency estimation experiment is carried out in this section. During the experiment, the frequency of the power grid is suddenly changed by +5Hz. The injected harmonic voltage is $V_1^+ = 1$p.u., $V_1^- = 0.1$p.u., $V_5^- = 0.1$p.u., $V_7^+ = 0.05$p.u., $V_{11}^- = 0.05$p.u., $V_{13}^+ = 0.05$p.u..

Fig.22 shows the experimental waveforms of distorted grid voltage. It can be observed from the figure that because the proposed PLL has the capability of frequency adaptive adjustment, when the grid frequency is 50Hz and 55Hz, only the waveform of the proposed PLL does not appear ripple, indicating that it is not interfered by harmonic components. The filtering stage of NF-PLL can only suppress but not completely eliminate harmonic interference. Therefore, there is a large oscillation error on the waveform of NF-PLL. In addition, because the EDGSC-PLL consists of five DSC cascades and does not have a frequency adaptive capability, there is also a certain ripple on the EDGSC-PLL waveform.

D. COMPARISON OF COMPUTATIONAL BURDEN

The mathematical operations required for the implementation of the proposed PLL and the other two PLLs used in the experiment are also compared, the comparison results are shown in the TABLE 3.

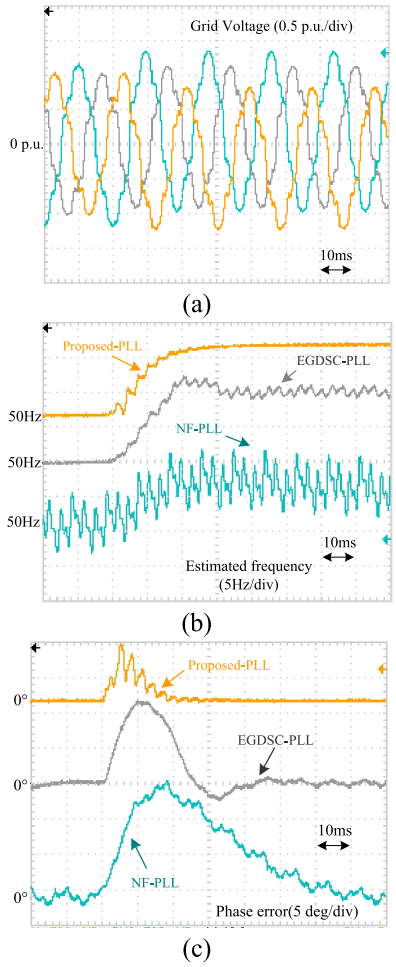

FIGURE 22. Experimental waveforms of Case3. (a) grid voltages., (b) estimated frequency, (c) phase error.

TABLE 3. Number of operations required for digital implementation of the THERR PLLS.

	M	A	T
Proposed PLL	12	8	0
EGDSC-PLL	12	16	0
NF-PLL	4	6	0

Where M=MULTIPLICATION, A=ADDITION, and T=TRIGONOMETRIC FUNCTION CALCULATION. And only the mathematical operations in the filtering stage is considered here.

Observing TABLE 3, the computational burden of the proposed PLL is lower than EDGSC-PLL and higher than NF-PLL, which will cause the operation execution time to be slightly slower than NF-PLL. However, compared with NF-PLL, the dynamic performance and filtering performance of the proposed PLL have been greatly improved, and most of the existing DSP processors can support such a computational burden, so the proposed PLL in this paper is feasible and effective.

TABLE 4. Summary of the results.

	Proposed-PLL	EGDSC-PLL	NF-PLL
+5 Hz frequency jump			
2% settling time	**28ms**	**≈40ms**	>60ms
Unbalanced and distortion			
Peak-to-peak phase-error	**0°**	1°	**2.3°**
Peak-to-peak frequency -error	**0Hz**	2Hz	**8Hz**
+100Hz/s frequency ramp change			
Phase-error	1.5°	5.3°	9.1°
DC offset			
2% settling time	**30ms**	40ms	≈30ms

TABLE 5. Summary of the compared results.

	Proposed-PLL	αβCDSC-PLL (Semi-adaptive)	CDSC-PLL$_{PI}$(With DC removal)	dqCDSC 3-PLL (with CPLC3)
+5 Hz frequency jump 2% settling time	28ms	32ms	67ms	61.3ms

E. SIMULATION AND EXPERIMENTAL RESULTS ANALYSIS

All of the experimental results are summarized in Table 4, according to Table 4 and the experimental results, the following analysis results can be obtained:

- The transient response speed and filtering capability of the proposed PLL in this paper are superior to the other two methods, and its dynamic adjustment time is the shortest under three non-ideal experimental conditions. In addition, the proposed PLL can completely remove the FFNS component, the DC offset component, and each harmonic components, and it is not affected in the phase and frequency estimation.

In order to further verify the transient response performance of the proposed PLL, the state-of-the-art PLL methods based on DSC technology in the recent 3 years are also compared. They are $\alpha\beta$ CDSC-PLL(Semi-adaptive) in [14], CDSC-PLL$_{PI}$ (With DC removal) in [29] and dqCDSC3-PLL(with CPLC3) in [17]. Based on the experiments in this paper, the dynamic adjustment time of these four methods when a +5Hz frequency jump occurs are compared. The comparison results are shown in Table 5. By the comparison, it can be found that the proposed PLL in this paper has the best transient performance.

- NF-PLL's transient response speed is inferior to the other two PLLs. Although it has DC offset rejection capability, it cannot completely eliminate all harmonics under non-ideal grid voltage conditions. In addition, when the power grid voltage drops, the NF-PLL will oscillate continuously and fail to work normally.

• The settling time of EGDSC-PLL is longer than the proposed PLL in this paper, but shorter than NF-PLL. Since the EDGSC-PLL is composed of multiple DSCs and has not frequency adaptive capability, the EDGSC-PLL has certain frequency and phase estimation oscillation errors.

VIII. CONCLUSION

This paper presents a three-phase grid-connected phase-locked loop based on *dc*DNANF with DC offset rejection capability and *dq*CDSC$_{4,24}$. First, a novel of adaptive ANF (NANF) is proposed, and a *dc*DNANF with DC offset rejection capability is designed based on NANF. Secondly, the cascaded *dq*DSC$_{4,24}$ filter is studied to eliminate the FFNS component and each harmonic component. Then, *dc*DNANF and *dq*CDS$_{C4,24}$ are connected in series to form a hybrid filter, and the designed hybrid filter is incorporated into the inner loop of the SRF-PLL. Simultaneously, the small-signal model of the proposed PLL is established and the parameter is designed. Finally, the effectiveness of the proposed new method is verified by simulation and the experiment, the results verify that the proposed method is more adaptable to the needs of actual grid-connected applications than the other two PLLs.

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NANMU HUI received the B.S. degree in electronic information engineering from the Minzu University of China, Beijing, China, in 2005, the M.S. degree in communication and information system from Capital Normal University, Beijing, in 2008, and the Ph.D. degree in power electronics and drives form Northeastern University, Shenyang, China, in 2018.

He is currently a Senior Engineer with the Institute of Scientific and Technological Innovation, Shenyang University. His research interests include phase-locked loop and nonlinear filtering techniques for distributed systems and power quality.

ZONGAN LUO received the B.S. degree in plastic processing from the Northeastern University of Technology, Shenyang, China, in 1990, and the M.S. degree in plastic processing and the Ph.D. degree in control material processing engineering from Northeastern University, Shenyang, in 1993 and 2006, respectively.

He is currently a Professor with the State Key Laboratory of Rolling and Automation, Northeastern University. His current research interests include metallurgical automation, metallurgical electrical control and R&D of experimental equipment, and intelligent control in processing field.

YINGYING FENG received the B.S. degree in material processing and control engineering and the Ph.D. degree in control material processing engineering from Northeastern University, Shenyang, China, in 2005 and 2010, respectively.

She is currently an Associate Researcher with the State Key Laboratory of Rolling and Automation, Northeastern University. Her current research interests include metallurgical automation, metallurgical electrical control, and material forming technology.

XIAOWEI HAN received the M.S. degree in control theory and application and the Ph.D. degree in control theory and control engineering from Northeastern University, in 1997 and 2005, respectively.

He engaged in postdoctoral research work at Beijing University, from 2005 to 2007. He is currently a Professor and the Dean of the Institute of Scientific and Technological Innovation, Shenyang University. His current research interests include computer vision processing, intelligent transportation, and wireless sensor networks.