IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 18, 2020, accepted March 11, 2020, date of publication March 17, 2020, date of current version March 27, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2981426

A Frequency-Adaptive Improved Moving-Average-Filter-Based Quasi-Type-1 PLL for Adverse Grid Conditions

WEI LUO, (Member, IEEE), AND DAFANG WEI
Department of Electrical Engineering, University of Shanghai for Science and Technology, Shanghai 200093, China
Corresponding author: Wei Luo (luowei@usst.edu.cn)

ABSTRACT The moving-average-filter-based quasi-type-1 phase-locked loop (MAF-QT1 PLL) can provide zero steady-state phase error in the presence of frequency drifts, achieving a high filtering capability. However, in the presence of an MAF and frequency drift, MAF-QT1 PLL cannot achieve a fast transient response and frequency-dependent characteristic under adverse grid conditions. To overcome this drawback of the MAF-QT1 PLL, this paper proposes a frequency-adaptive improved moving-average-filter-based quasi-type-1 PLL (FAIMAF-QT1 PLL). Aiming at the shortcoming of the slow dynamic response of the MAF-QT-1 PLL, a correction link is introduced, and an improved moving-average-filter-based quasi-type-1 PLL (IMAF-QT1 PLL) is obtained. To improve the anti-interference ability of the IMAF-QT1 PLL in response to grid frequency changes, a FAIMAF-QT1 PLL and a corresponding digital implementation scheme are proposed. The regulator parameter setting method is proposed based on the small-signal model of the FAIMAF-QT1 PLL. Simulation and experimental results show that the FAIMAF-QT1 PLL can accurately track the grid voltage phase in the presence of power grid frequency fluctuations, phase angle jumps, distorted harmonic injections and unbalanced voltage drops and has good steady-state and dynamic performance.

INDEX TERMS Phase-locked loop, moving average filter, frequency adaptive, synchronization, quasi-type-1 PLL.

I. INTRODUCTION

A phase-locked loop (PLL) is a closed-loop feedback control system whose output phase is related to the input phase and can be used in a variety of applications, especially for most grid-connected power electronic equipment and power generation based on renewable energy sources [1]–[4]. To improve the dynamic response and filtering capabilities of standard PLLs under adverse grid conditions, various PLLs have been proposed in the literature [5]–[9] and consist of three different parts: a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO) [10]. Type-2 PLLs are the most widely used three-phase PLLs due to their steady-state phase error during phase angle jumps and frequency drifts. Under ideal grid conditions, three-phase type-2 PLLs can achieve fast and accurate detection of the phase angle and frequency of the grid voltage [11], [12]. However, when the grid voltage is distorted and unbalanced, the performance of a three-phase type-2 PLL becomes unacceptable, because the traditional loop filter cannot effectively block the grid disturbances [13]. Additional filters are usually added in the PLL control loop to solve this problem. For instance, the notch filter [14]–[16], moving average filter (MAF) [17]–[19], multiple-complex-coefficient filter [20], [21], linear Kalman filter [22], delayed signal cancellation operator [23]–[25], and conventional low-pass filter (LPF) are typical choices that are used to obtain a high filtering capability. Among these filters, an MAF is a linear-phase finite-impulse-response (FIR) filter that can realize an ideal low-pass filter characteristic under certain conditions and is a widely used technique in PLL due to its simple digital realization and low computational burden. Reference [19] presented the control design guidelines of a typical MAF-based PLL. The frequency-dependent attenuation characteristic is a practical challenge of an MAF, and some theoretical solutions have been provided to overcome this challenge. However, a frequency-adaptive digital realization and hardware implementation were not considered in this paper. In [26], a phase-lead compensator was introduced

The associate editor coordinating the review of this manuscript and approving it for publication was Xin Zhang.

to improve the dynamic response of the standard MAF PLL However, this scheme would result in a high digital implementation cost and does not address the presence of frequency drifts.

A type-1 PLL is characterized by only one integrator in its control loop and has a high stability margin. However, a type-1 PLL cannot realize zero steady-state phase error when the grid voltage frequency deviates from its nominal value [27], [28]. Reference [28] provided an MAF-based quasi-type-1 PLL (MAF-QT1 PLL) by using an MAF as the LPF in the structure, which can provide a zero steady-state phase error in the presence of frequency drifts, achieving a high filtering capability. However, the MAF would produce a considerable phase delay and slow down the transient response of the PLL. Additionally, a frequency-adaptive digital realization and hardware implementation were not considered in the MAF-QT1 PLL. The MAF-QT1 PLL cannot accurately track the grid voltage phase when the power grid frequency fluctuates, especially under adverse grid conditions.

In this paper, a frequency-adaptive improved moving-average-filter-based quasi-type-1 PLL (FAIMAF-QT1 PLL) is proposed. The principles and operational characteristics of the typical type-1 PLL are presented in section II. The expression of the improved MAF-QT1 PLL is derived by introducing a correction link in section III, solving the slow dynamic response of the MAF-QT1 PLL. Additionally, a frequency-adaptive digital realization is presented in order to improve the anti-disturbance capability when the frequency of the power grid changes. Section IV presents the parameter tuning method based on the small-signal model of the proposed PLL. Then, the feasibility and effectiveness of the proposed scheme are verified by simulation and experiment results in section V and section VI, respectively. Conclusions are drawn in the final section.

II. TYPICAL TYPE-1 PLL

Fig. 1 shows the schematic diagram of a typical three-phase type-1 PLL. The phase discriminator consists of a Clarke transformation and a Park transformation, converting the three-phase grid voltage into a DC component in the synchronous rotating reference frame. In addition, a lead/lag controller with a continuous transfer function is considered as the loop filter in a typical type-1 PLL. Then, the estimated phase angle signal is obtained by integrating the estimate angular frequency signal by means of the voltage-controlled oscillator. Finally, the estimated phase angle signal is sent to the Park transformation as a rotation transform angle. Then, the small-single model of the typical type-1 PLL is shown in Fig. 2.

The phase tracking error of a typical type-1 PLL under phase and frequency step changes can be obtained, respectively, as

$$\begin{cases} \theta_e = 0 \\ \theta_e = \sin^{-1}\left(\Delta\omega_i / k_p U_i\right) \end{cases} \tag{1}$$

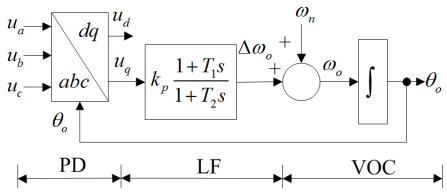


FIGURE 1. The schematic diagram of a typical type-1 PLL.

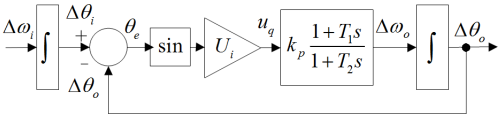


FIGURE 2. The small-single model of a typical type-1 PLL.

Equation (1) shows that the typical type-1 PLL can track a step change in the phase angle. However, the typical type-1 PLL cannot track a step change in the grid frequency. The tracking error can be reduced by increasing the proportional gain k_p. Nevertheless, increasing k_p reduces the filtering capability of a typical type-1 PLL. Thus, the phase-locked performance of a typical type-1 PLL is reduced, especially under adverse grid conditions.

III. PROPOSED QUASI-TYPE-1 PLL

A. MAF-BASED QUASI-TYPE-1 PLL

The moving average filter is a linear phase filter that can be considered to be an ideal LPF. The MAF transfer function in the s-domain can be described as [22]

$$G_{\mathrm{MAF}}(s) = \frac{1 - e^{-T_w s}}{T_w s} \tag{2}$$

where T_w is the window length of the MAF.

The transfer function (2) indicates that the transient response time of the MAF is equal to its window length. Assume that the window length of the MAF contains N samples of its input signal and $N = T_w/T_s$, where T_s is the sampling time of the control system. The transfer function and pole-zero expression of the MAF in the z-domain can be obtained as

$$G_{\mathrm{MAF}}(z) = \frac{1}{N}\frac{1 - z^{-N}}{1 - z^{-1}} = \frac{1}{N}\prod_{k=1}^{N}\frac{z - z_k}{z - p_1} \tag{3}$$

It can be seen that the MAF has N zeros and one pole. Meanwhile, the MAF has unity gain at zero frequency and zero gain at notch frequencies m/T_w ($m = 1, 2, 3\ldots$).

A schematic diagram of the MAF QT1 PLL is shown in Fig. 3. The amplitude normalization scheme is included in the MAF-QT1 PLL structure to remove the dependence of the phase tracking error under an off-nominal grid frequency on the input voltage amplitude. Additionally, the arctangent function is used to remove the nonlinearity of the control loop. As a result, the phase tracking error of the MAF-QT1 PLL under frequency step changes can be described as

$$\theta_e = \Delta\omega_i / k_p = \Delta\omega_o / k_p \tag{4}$$

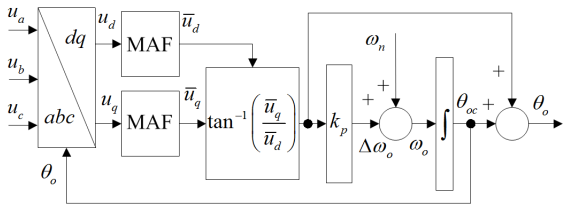


FIGURE 3. Schematic diagram of the MAF-QT1 PLL.

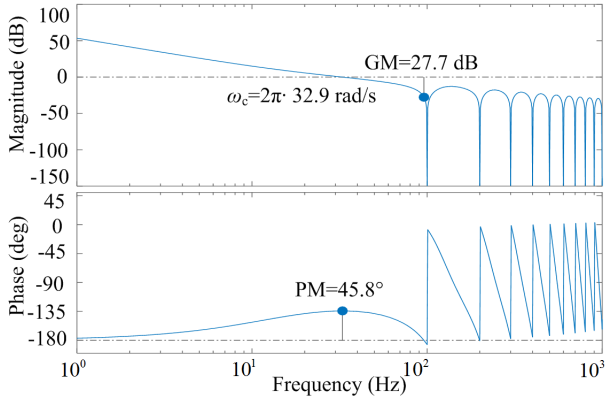


FIGURE 4. The Bode plot of the open-loop transfer function of the MAF-QT1 PLL.

Notice that $\Delta\omega_o$ is equal to $\Delta\omega_i$ under the phase-locked condition. The phase tracking error of the MAF-QT1 PLL becomes linearly proportional to $\Delta\omega_o$, which can be compensated based on equation (4), as shown in Fig. 3.

Generally, the disturbance frequency of an MAF is equal to the twice the fundamental grid frequency, $T_w = 10$ ms. In addition, the sampling frequency of the control system is 10 kHz, with $T_s = 0.1$ ms. Then, selecting the parameter of the proportional regulator according to the method proposed in reference [28], $k_p = 92.34$. The Bode plot of the open-loop transfer function of the MAF-QT1 PLL is shown in Fig. 4. It can be seen that the MAF-QT1 PLL can pass the DC component and block the notch frequency components completely. Additionally, Fig. 4 shows that the MAF-QT1 PLL has a phase margin (PM) of 45.8° and a gain margin (GM) of 27.7 dB, ensuring the stability of the MAF-QT1 PLL. Note that the cut-off frequency of the MAF-QT1 PLL is $2\pi \cdot 32.9$ rad/s, indicating that the dynamic response is slow, which is the drawback of MAF.

B. IMPROVED MAF-BASED QUASI-TYPE-1 PLL

The correction link in the s-domain is introduced based on the MAF transfer function

$$G_c(s) = \frac{1 + T_w s/2}{1 + \beta T_w s} \tag{5}$$

where β is the attenuation factor and $0 < \beta < 1$.

The improved MAF (IMAF) transfer function in the s-domain can be described as

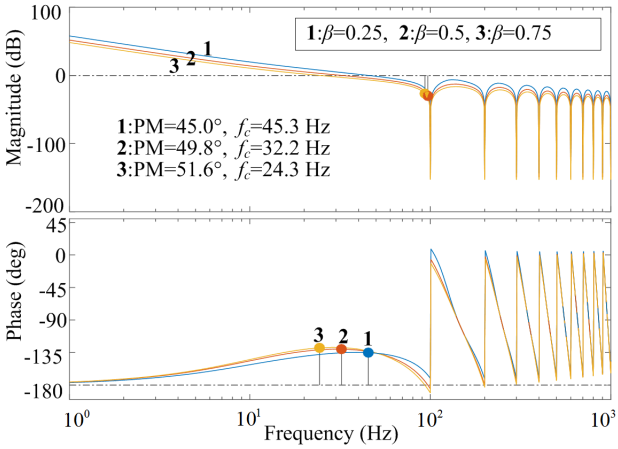


FIGURE 5. The Bode plot of the open-loop transfer function of the IMAF-QT1 PLL.

$$G_{\mathrm{IMAF}}(s) = \frac{\left(1 - e^{-T_w s}\right)\left(1 + T_w s/2\right)}{T_w s\left(1 + \beta T_w s\right)} \tag{6}$$

The transfer function of the improved MAF in the z-domain can be obtained as

$$G_{\mathrm{IMAF}}(z) = \frac{\left(1 - z^{-N}\right)\left(2 + N\left(1 - z^{-1}\right)\right)}{2N\left(1 - z^{-1}\right)\left(1 + \beta N\left(1 - z^{-1}\right)\right)} \tag{7}$$

This paper selects the parameter of the proportional regulator according to the section IV.B: $k_p = 76$. Then, the Bode plot of the open-loop transfer function of the IMAF-QT1 PLL is shown in Fig. 5. It can be seen that the phase margin of the IMAF-QT1 PLL increase as the attenuation factor increases. However, the amplitude margin and the cut-off frequency decrease as the attenuation factor increases. To ensure the stability of the system, the phase margin within the range of $30° \sim 60°$ is suggested; the cut-off frequency is higher than $0.3/T_w$ Hz to ensure the dynamic response of the system. This paper selects the parameter of the attenuation factor according to the stability and dynamic response of the PLL: $\beta = 0.25$; the IMAF-QT1 PLL has a phase margin of 45° and a cut-off frequency of 45.3 Hz. The IMAF-QT1 PLL cannot only maintain the stability but also improve the dynamic response compared with an MAF-QT1 PLL.

C. FREQUENCY-ADAPTIVE REALIZATION

The moving average filter cannot block the disturbance components completely if the grid frequency drifts. In such cases, the IMAF-QT1 PLL needs to adjust the IMAF sampling order, according to the variations in the grid voltage frequency. Then, the IMAF sampling order N is given by means of the "WMV" (weighted mean value) approach

$$\begin{cases} N_f = \mathrm{floor}\left(\pi / T_s\omega_o\right) \\ N_c = \mathrm{ceil}\left(\pi / T_s\omega_o\right) \\ \alpha = \left(T_w - N_f T_s\right)/T_s \end{cases} \tag{8}$$

where α is the weighting factor.

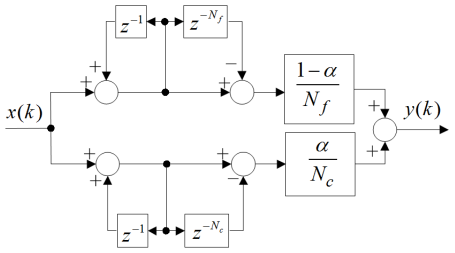


FIGURE 6. Digital implementation schematic diagram of the FAIMAF-QT1 PLL.

Fig. 6 presents a digital implementation schematic diagram of the FAIMAF-QT1 PLL. The diagram shows that the FAIMAF-QT1 PLL is easily implemented and computationally efficient. The digital implementation method of the FAIMAF-QT1 PLL can be described as

$$y(k) = \frac{1-\alpha}{N_f}\left[\sum_{i=0}^{k-1} x(k-i) - \sum_{i=N_f}^{k-1} x(k-i)\right] + \frac{\alpha}{N_c}\left[\sum_{i=0}^{k-1} x(k-i) - \sum_{i=N_c}^{k-1} x(k-i)\right] \quad (9)$$

where $x(k)$ is the input variable at sample time k and $y(k)$ is the output variable at sample time k.

IV. CONTROL DESIGN GUIDELINES

A. SMALL-SINGLE MODELING OF THE PROPOSED PLL

Let the three-phase input voltage of the FAIMAF-QT1 PLL be represented by

$$\begin{cases} u_a = \sum\limits_{k=1,5,7,\ldots} U_k \cos(\theta_k) \\ u_b = \sum\limits_{k=1,5,7,\ldots} U_k \cos(\theta_k - 2\pi/3) \\ u_c = \sum\limits_{k=1,5,7,\ldots} U_k \cos(\theta_k + 2\pi/3) \end{cases} \quad (10)$$

where U_k and θ_k ($k = 1, 5, 7, 11, 13\ldots$) represent the amplitude and phase angle of the kth harmonic component of the input voltage, respectively. Note that the even harmonic components and DC offset are neglected as they have negligible magnitudes compared to the magnitudes of the odd harmonic components in most practical cases.

Equation (10) can be rewritten in the dq reference frame by applying the Clarke transformation and Park transformation

$$\begin{cases} u_d = \sum\limits_{k=1,5,7,\ldots} U_k \cos(\theta_k - \theta_o) \\ u_q = \sum\limits_{k=1,5,7,\ldots} U_k \sin(\theta_k - \theta_o) \end{cases} \quad (11)$$

Under the phase-locked condition, equation (11) can be approximated by

$$\begin{cases} u_d \approx U_1 \cos\theta_e + f(2\omega_n, 4\omega_n, 6\omega_n, \ldots) \\ u_q \approx U_1 \sin\theta_e + f(2\omega_n, 4\omega_n, 6\omega_n, \ldots) \end{cases} \quad (12)$$

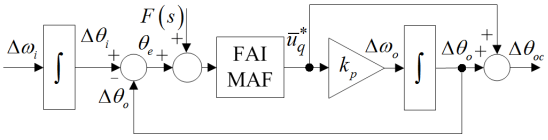


FIGURE 7. Small-signal model of the FAIMAF-QT1 PLL.

The disturbance frequency of the FAIMAF is equal to twice the fundamental input voltage frequency. Equation (12) can be simplified as

$$\begin{cases} \bar{u}_d \approx U_1 \cos\theta_e \\ \bar{u}_q \approx U_1 \sin\theta_e \end{cases} \quad (13)$$

Then, convert the input voltages' q axis component into a per-unit value expression

$$\bar{u}_q^* = \frac{\bar{u}_q}{\bar{u}_d} \approx \theta_e = \Delta\theta_i - \Delta\theta_o \quad (14)$$

The phase tracking error of the FAIMAF-QT1 PLL in the presence of frequency drifts can be compensated by an online calculation of equation (4), and adding the result to the output of the PLL. Then, the small-signal model of the FAIMAF-QT1 PLL can be obtained as shown in Fig. 7, where $F(s) = L[f(2\omega_n, 4\omega_n, 6\omega_n \ldots)]$ (L denotes the Laplace operator).

B. PARAMETER DESIGN GUIDELINES

The MAF window length can be simply selected according to the anticipated harmonic components in the PLL's input voltage. In this paper, the even harmonic components and DC offset are neglected because they have much smaller magnitudes than the odd harmonic components in most practical cases. The MAF can pass the DC component and block the notch frequency components completely. Therefore, the MAF window length should be set equal to half the fundamental period of the grid voltage, or $T_w = 0.01$ s in a 50 Hz system. As a consequence, the MAF can block even harmonic components of the grid voltage in the synchronous rotating frame.

The open-loop transfer function of the FAIMAF-QT1 PLL can be described as

$$G_{ol}(s) = \left[\frac{\text{FAIMAF}(s)}{1 - \text{FAIMAF}(s)}\right]\left(\frac{s + k_p}{s}\right) \quad (15)$$

Fig. 8 shows the proportional coefficient k_p and cut-off frequency f_c variations in the FAIMAF-QT1 PLL as a function of the phase margin (PM) based on equation (15). As shown in the figure, the PM of the FAIMAF-QT1 PLL decreases with the growth of k_p. The phase margin with a range of $30° \sim 60°$ is recommended to ensure the stability of the system. In this paper, PM $= 45°$ is considered to obtain a sufficient stability margin, which corresponds to $k_p = 76$.

V. SIMULATION ANALYSIS

Based on the MATLAB/Simulink platform, this paper simulates the FAIMAF-QT1 PLL, which is compared with the MAF PLL and MAF-QT1 PLL. Among these PLLs,

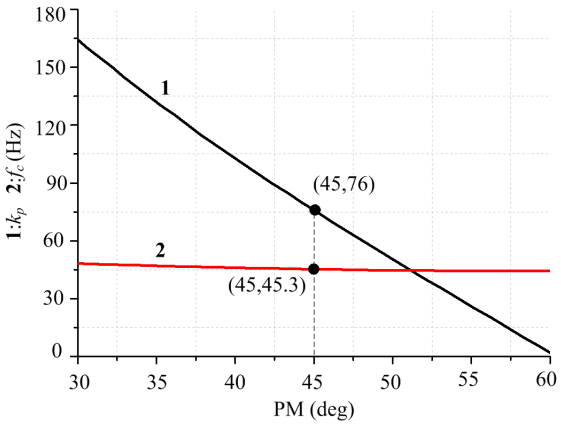


FIGURE 8. kp and fc variations in the FAIMAF-QT1 PLL as a function of the PM.

TABLE 1. Control parameters of the PLLs.

	MAF	MAF-QT1	FAIMAF-QT1
T_w/s	0.01	0.01	-
k_p	83.33	92.34	76
k_i	2893.5	-	-
β	-	-	0.25

the regulator parameter of the MAF PLL is based on the symmetric optimal method, and the regulator parameter of the MAF-QT1 PLL is based on the method proposed in reference [28]. The FAIMAF-QT1 PLL uses the regulator parameter adjustment method proposed in this paper. Table 1 presents the control parameters of the three phase-locked loops.

Four test conditions are designed to investigate the steady-state performance and dynamic performance of the FAIMAF-QT1 PLL.

Test condition 1: At 40 ms, the three-phase grid voltage undergoes a frequency step change of +5 Hz; At 160 ms, the phase angle of the three-phase grid voltage exhibits a jump of + 20 °.

Test condition 2: At 40 ms, the three-phase grid voltage undergoes a frequency step change of +5 Hz; At 160 ms, the three-phase grid voltage is injected with 20% of the 5th harmonic and 10% of the 7th harmonic.

Test condition 3: At 40 ms, the three-phase grid voltage undergoes a frequency step change of +5 Hz; At 160 ms, the voltage amplitude of phase B sags by 50%, and the voltage amplitude of phase C sags by 30%.

Test condition 4: At 40 ms, the three-phase grid voltage undergoes a frequency step change of +5 Hz; At 160 ms, the phase angle of the three-phase grid voltage exhibits a jump of + 20 °, and the three-phase grid voltage is injected with 20% of the 5th harmonic and 10% of the 7th harmonic. The voltage amplitude of phase B sags by 50%, and the voltage amplitude of phase C sags by 30%.

To verify the effectiveness of the frequency adaptation of the FAIMAF-QT1 PLL, the frequency steps by +5 Hz at 40 ms during each test condition. After the frequency step, the phase angle error and frequency error of the MAF PLL reach zero within 120 ms and 130 ms, respectively; the phase angle error and frequency error of the MAF-QT1 PLL reach zero within 80 ms and 90 ms, respectively; and the phase angle error and frequency error of the FAIMAF-QT1 PLL reach zero within 70 ms and 80 ms, respectively. The FAIMAF-QT1 PLL has the fastest dynamic response and the smallest overshoot among the three phase-locking methods, which indicates that the FAIMAF-QT1 PLL has improved the steady-state and dynamic characteristic.

The simulation results of the three phase-locked loops under test condition 1 are shown in Figure 9 (a). The phase angle jumps by +20° at 160 ms. The phase angle error and frequency error of the MAF PLL reach zero within 130 ms and 140 ms, respectively; the phase angle error and frequency error of the MAF-QT1 PLL reach zero within 80 ms and 100 ms, respectively; and the phase angle error and frequency error of the FAIMAF-QT1 PLL reach zero within 70 ms and 80 ms, respectively. The FAIMAF-QT1 PLL has the smallest phase angle error and frequency error. When the phase angle jumps, the FAIMAF-QT1 PLL proposed in this paper improves the dynamic response of the phase lock while ensuring that the phase angle error remains stable.

The simulation results of the three phase-locked loops under test condition 2 are shown in Figure 9 (b). The harmonics are injected at 160 ms. The phase angle error and frequency error of the MAF PLL fluctuate slightly around zero. The phase angle error of the MAF-QT1 PLL fluctuates sharply near zero, the frequency error fluctuates slightly near zero, and the phase locked cannot be achieved. The phase error and frequency error of the FAIMAF-QT1 PLL reach zero within 70 ms and 80 ms, respectively. When harmonics are injected, the FAIMAF-QT1 PLL improves the dynamic response while ensuring that the phase is locked accurately.

The simulation results of the three phase-locked loops under test condition 3 are shown in Figure 9 (c). The unbalanced grid voltage drops at 160 ms. The phase angle error and frequency error fluctuate slightly around zero. The phase angle error of the MAF-QT1 PLL fluctuates sharply near zero, the frequency error fluctuates slightly near zero, and the phase lock cannot be achieved. The phase angle error and frequency error of the FAIMAF-QT1 PLL reach zero within 50 ms and 60 ms, respectively. When the unbalanced grid voltage drops, the FAIMAF-QT1 PLL improves the dynamic response speed while ensuring that the phase is locked accurately.

The simulation results of the three phase-locked loops under operating condition 4 are shown in Figure 9 (d). A comprehensive fault occurs at 160 ms. The phase angle and frequency error fluctuate around zero. The phase angle error of the MAF-QT1 PLL fluctuates sharply near zero, the frequency error fluctuates slightly near zero, and the phase lock cannot be achieved. The phase error and frequency error of the FAIMAF-QT1 PLL reach zero within 80 ms and 90 ms, respectively. When the comprehensive fault

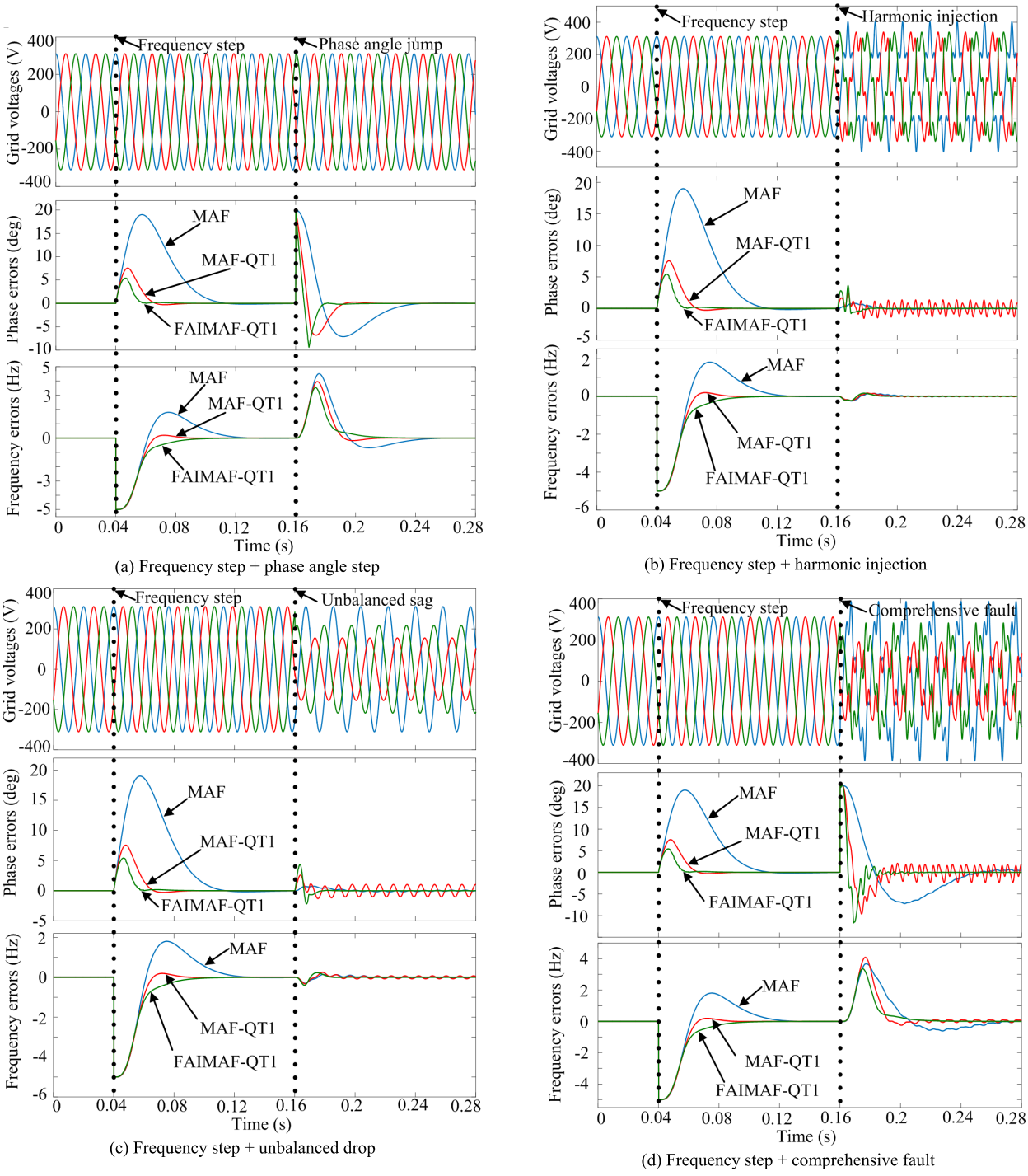


FIGURE 9. Simulation waveforms of the PLLs.

occurs, the FAIMAF-QT1 PLL technology improves the dynamic response speed while ensuring that the phase is locked accurately. Among the three phase-locking methods, the FAIMAF-QT1 PLL has the fastest phase and frequency dynamic response, and the phase and frequency peak-to-peak steady state errors are minimal.

VI. EXPERIMENTAL RESULTS

The dSPACE platform is used in the experiments to verify the effectiveness and hardware implementation of the FAIMAF-QT1 PLL proposed in this paper. The processor platform is RTI1202. The control algorithm is divided into two parts: the nonideal voltage generation and phase-locked

TABLE 2. Experimental results of the PLLs.

Test conditions	Index	MAF	MAF-QT1	FAIMAF-QT1
Frequency step change	2% frequency settling time / ms	77.67	40.12	46.68
	Maximum phase angle error / deg	19.03	7.79	5.39
	Frequency overshoot / %	36.4	4.2	0
1: Frequency step change and phase angle jump	2% phase angle settling time / ms	73.38	29.96	17.66
	Phase angle overshoot / %	36.07	34.65	47.25
	Maximum frequency error / Hz	4.52	3.96	3.53
2: Frequency step change and harmonic injection	Phase angle steady-state error peak-to-peak/deg	0.23	2.79	0
	Frequency steady-state error peak-to-peak/Hz	0.04	0.05	0
3: Frequency step change and unbalanced sag	Phase angle steady-state error peak-to-peak/deg	0.22	2.07	0
	Frequency steady-state error peak-to-peak/Hz	0.11	0.16	0
4: Frequency step change and comprehensive fault	Phase angle steady-state error peak-to-peak/deg	0.29	4.23	0
	Frequency steady-state error peak-to-peak/Hz	0.11	0.17	0

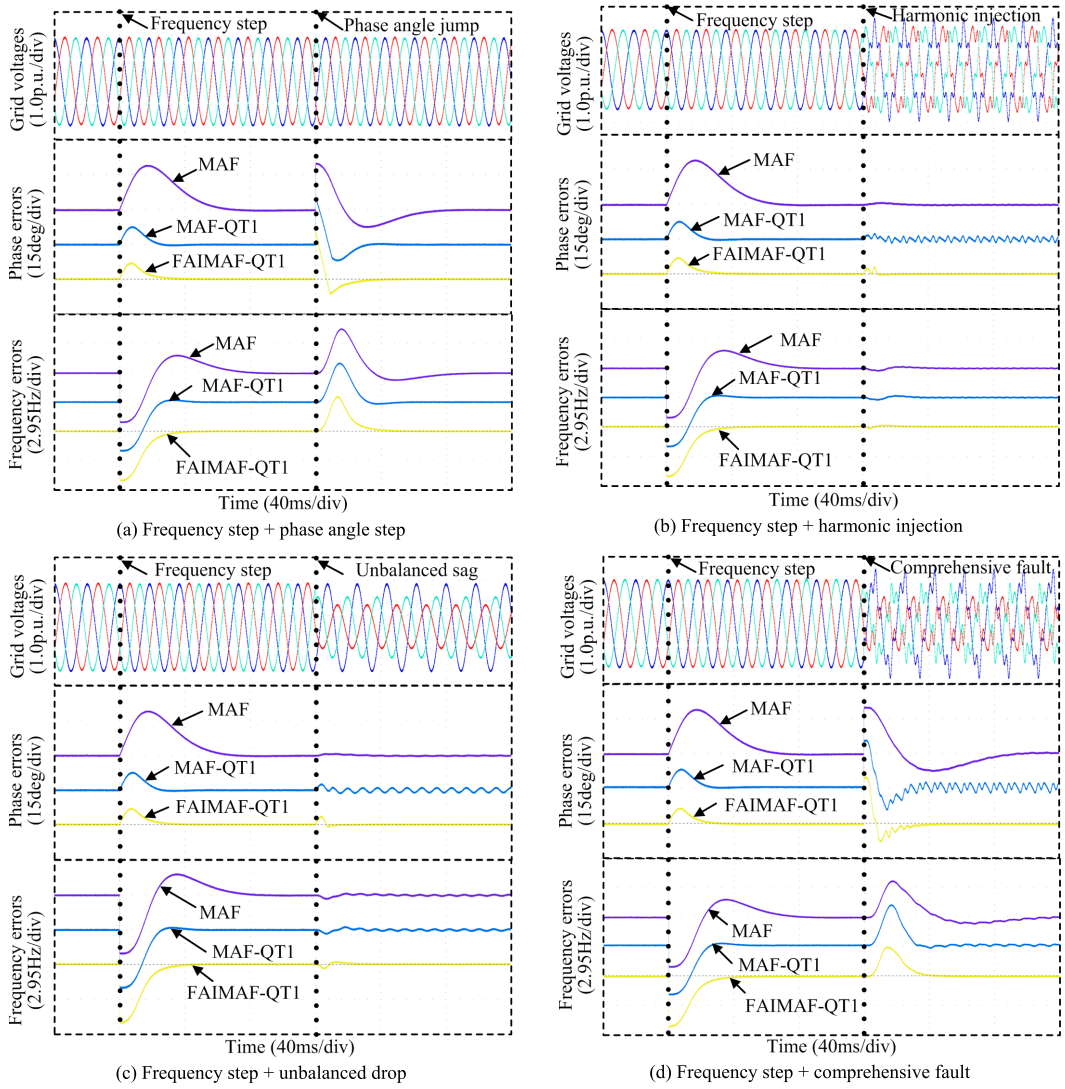


FIGURE 10. Experimental waveforms of the PLLs.

loops implementation. The sampling frequency of the CPU is 10 kHz. The internal variables are output to the oscilloscope (MSO58, Tektronix) through the analog output board. The control parameters of the phase-locked loops are consistent with the simulation, as shown in Table 1.

It can be seen from Fig. 10 that the experimental waveforms of the phase angle and frequency errors of the three phase locked loops under four different operating conditions are consistent with the simulation results. Under the test condition of the phase angle jumps, harmonic injections,

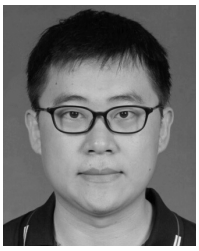
unbalanced sags and comprehensive fault after frequency steps, the frequency dynamic response of the MAF-QT1 PLL is fast, but the steady-state error of the phase angle and frequency are too large to meet the requirements of the phase-locked loop. The phase angle and frequency steady-state error of the MAF PLL are small, which can meet the requirements of the phase-locked loop, but the frequency dynamic response is too slow to obtain the phase and frequency information of the grid immediately. The FAIMAF-QT1 PLL proposed in this paper has a frequency adaptation ability, which can ensure that the phase angle and frequency steady-state error reach zero, and has the fastest phase angle and frequency dynamic response. The experimental results verify the feasibility and effectiveness of the parameter tuning and frequency-adaptive implementation of the FAIMAF-QT1 PLL proposed in this paper. See Table 2 for detailed technical indicators of the experimental results for the three phase-locked loops.

VII. CONCLUSION

The MAF-QT1 PLL cannot accurately track the grid voltage phase when the power grid frequency fluctuates, especially under adverse grid conditions. This paper proposes a FAIMAF-QT1 PLL by introducing a correction link and presents a corresponding regulator parameter setting method and frequency-adaptive digital implementation scheme. Simulation and experimental results show that compared with the MAF PLL and MAF-QT1 PLL, the FAIMAF-QT1 PLL has a good phase-locking capability and dynamic response when the frequency of the power grid changes, which can meet the grid-locking requirements under adverse grid conditions.

REFERENCES

[1] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017.
[2] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9013–9030, Dec. 2017.
[3] F. Hans, W. Schumacher, and L. Harnefors, "Small-signal modeling of three-phase synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5556–5560, Jul. 2018.
[4] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue, "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 310–321, Jan. 2015.
[5] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2167–2177, Jun. 2013.
[6] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194–1204, Apr. 2011.
[7] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Advantages and challenges of a type-3 PLL," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4985–4997, Nov. 2013.
[8] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639–3650, Aug. 2012.
[9] M. Karimi-Ghartemani, "A unifying approach to single-phase synchronous reference frame PLLs," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4550–4556, Oct. 2013.
[10] M. Karimi Ghartemani, *Enhanced Phase-Locked Loop Structures for Power and Energy Applications*. Piscataway, NJ, USA: Wiley, 2014.
[11] G. G. Pozzebon, A. F. Q. Goncalves, G. G. Pena, N. E. M. Mocambique, and R. Q. Machado, "Operation of a three-phase power converter connected to a distribution system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1810–1818, May 2013.
[12] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of phase-locked loops for power converters under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039–2047, Nov./Dec. 2009.
[13] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Trans. Ind. Electron.*, vol. 59, no. 6, pp. 2718–2731, Jun. 2012.
[14] M. Karimi-Ghartemani, S. A. Khajehoddin, P. K. Jain, A. Bakhshai, and M. Mojiri, "Addressing DC component in PLL and notch filter algorithms," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 78–86, Jan. 2012.
[15] K.-J. Lee, J.-P. Lee, D. Shin, D.-W. Yoo, and H.-J. Kim, "A novel grid synchronization PLL method based on adaptive low-pass notch filter for grid-connected PCS," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 292–301, Jan. 2014.
[16] Y. Li, D. Wang, W. Han, S. Tan, and X. Guo, "Performance improvement of quasi-type-1 PLL by using a complex notch filter," *IEEE Access*, vol. 4, pp. 6272–6282, 2016.
[17] J. Wang, J. Liang, F. Gao, L. Zhang, and Z. Wang, "A method to improve the dynamic performance of moving average filter-based PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5978–5990, Oct. 2015.
[18] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, and J. Doval-Gandoy, "PLL with MAF-based prefiltering stage: Small-signal modeling and performance enhancement," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4013–4019, Jun. 2016.
[19] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014.
[20] C. Blanco, D. Reigosa, F. Briz, J. M. Guerrero, and P. Garcia, "Grid synchronization of three-phase converters using cascaded complex vector filter PLL," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Raleigh, NC, USA, Sep. 2012, pp. 196–203.
[21] M. Ramezani, S. Golestan, S. Li, and J. M. Guerrero, "A simple approach to enhance the performance of complex-coefficient filter-based PLL in grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5081–5085, Jun. 2018.
[22] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Steady-state linear Kalman filter-based PLLs for power applications: A second look," *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9795–9800, Dec. 2018.
[23] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1067–1080, Apr. 2011.
[24] S. Golestan, M. Ramezani, J. M. Guerrero, and M. Monfared, "*dq*-frame cascaded delayed signal Cancellation- based PLL: Analysis, design, and comparison with moving average filter-based PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1618–1632, Mar. 2015.
[25] S. Gude and C.-C. Chu, "Three-phase PLLs by using frequency adaptive multiple delayed signal cancellation prefilters under adverse grid conditions," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3832–3844, Jul./Aug. 2018.
[26] S. Golestan, J. M. Guerrero, and A. Abusorrah, "MAF-PLL with phase-lead compensator," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3691–3695, Jun. 2015.
[27] P. Kanjiya, V. Khadkikar, and M. S. E. Moursi, "A novel type-1 frequency-locked loop for fast detection of frequency and phase with improved stability margins," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2550–2561, Mar. 2016.
[28] S. Golestan, F. D. Freijedo, A. Vidal, J. M. Guerrero, and J. Doval-Gandoy, "A quasi-type-1 phase-locked loop structure," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6264–6270, Dec. 2014.



WEI LUO (Member, IEEE) was born in Shanxi, China, in 1986. He received the B.S. degree in electrical engineering and automation from the China University of Mining and Technology, Xuzhou, China, in 2009, and the M.S. and Ph.D. degrees in electric engineering from Shanghai Jiao Tong University, Shanghai, China, in 2012 and 2018, respectively.

He is currently a Lecturer of electrical engineering with the University of Shanghai for Science and Technology, China. His research interests include multilevel converters, high-power motor drives, and the internet of things.

DAFANG WEI was born in Gansu, China, in 1995. He received the B.S. degree in electrical engineering and automation from the University of Shanghai for Science and Technology, Shanghai, China, in 2018, where he is currently pursuing the master's degree in power electronics and power drives with the Department of Electrical Engineering.

His current research interests include multilevel converters and PLLs.