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A Novel Decision Feedback Equalization Structure for Nonlinear High-Speed Links

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ABSTRACT As the degree of nonlinearity in high-speed links becomes more and more serious, traditional decision feedback equalization (DFE) which is based on linear time-invariant assumption can no longer eliminate the inter-symbol interference effectively. In this paper, the shortcomings of traditional DFE structure for nonlinear high-speed links are first analyzed. Then, the multi-bit response (MBR) method is proposed to accurately construct the bit stream responses of the nonlinear high-speed links. Lastly, a novel DFE structure based on the MBR method is presented to improve the signal quality of the nonlinear high-speed links. The accuracy of the proposed method is verified by the simulation based on a nonlinear high-speed link model. Compared with traditional DFE, the proposed DFE structure can significantly improve the signal quality of the nonlinear high-speed links. As the degree of nonlinearity increases, the advantage of the proposed DFE becomes more prominent.

INDEX TERMS Decision feedback equalization (DFE), inter-symbol interference (ISI), multi-bit response, nonlinearity, signal integrity.

I. INTRODUCTION

As the data rate in high-speed links continuously increases, signal integrity (SI) becomes a challenging problem in real-world applications. Without good SI design, the high-speed links may not function properly [1], [2].

The eye diagrams at the receiver side of an actual high-speed link under different data rates are shown in Fig. 1, which are obtained by transient simulations. It can be seen from Fig. 1(a) that the link has a very good performance when the data rate is 1 Gb/s. However, the eye diagram is closed when the data rate is increased to 32 Gb/s for the same channel, as shown in Fig. 1(b). Various equalization techniques are widely used to compensate the signal distortion induced by the channel [3], [4], which can significantly improve the performance of the high-speed links. Equalization can significantly improve signal quality. Fig. 1(c) shows the eye diagram of the received signal after continuous-time linear equalization (CTLE), which is much better than Fig. 1(b). When the received signal goes through CTLE and decision feedback equalization (DFE), the eye diagram is completely opened, as shown in Fig. 1(d).

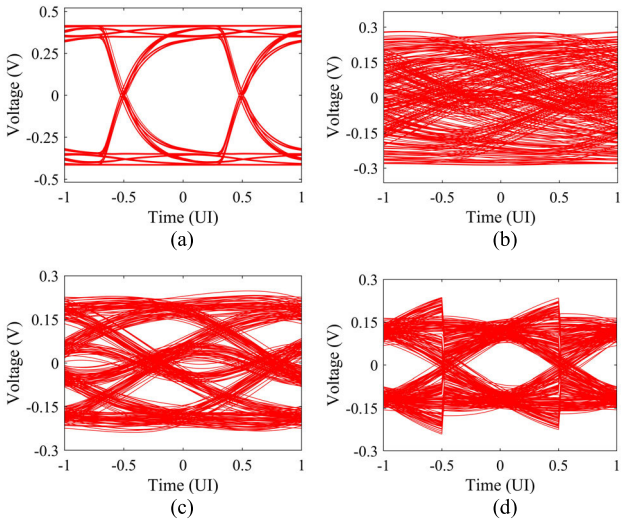

FIGURE 1. Eye diagram of an actual high-speed link at the receiver in different conditions. (a) 1 Gbps without EQ; (b) 32 Gbps without EQ; (c) 32 Gbps with CTLE; (d) 32 Gbps with CTLE+DFE.

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Typically, equalization is performed on the transmitter side and receiver side to flatten the frequency response of the channel and remove inter-symbol interference (ISI). A finite impulse response (FIR) filter is usually used for transmitter equalization because it is easy to implement at high speed [5]. A feed forward equalizer (FFE), which is basically similar to FIR, is widely used at the transmitter. FFE uses the waveform itself to correct the received signal without involving the logic decision. On the receiver side, CTLE is often used to flatten the channel response by amplifying the high frequency response according to its transfer function. However, it can also amplify the noise and crosstalk.

Compared to these linear equalization techniques, DFE is a nonlinear equalizer which has been widely used at the receiver to eliminate ISI due to loss and reflection [6]–[14]. The basic idea of DFE is to eliminate the ISI components by subtracting the interference on the currently received symbol from the previous symbols. The DFE's tap weight coefficients demonstrate the ISI contribution from previous bits. The currently received signal is summed with the previous bits multiplied by the tap weight coefficients to get the equalized output. Since the equalization process relies on logic decisions of previous bits, the DFE may have error propagation if the previous bits are wrongly determined. Therefore, DFE is generally used together with CTLE in the link when the loss of the channel is very large. The signal passes through CTLE firstly to avoid the occurrence of error propagation.

When the system meets the linear time-invariant (LTI) assumption, the response of input bit patterns can be constructed by the shifted SBR of the system. As a result, the ISI can be removed by DFE whose tap coefficients are determined by SBR [15], [16]. However, when the system is not LTI or cannot be approximated as LTI, SBR can no longer be used to accurately construct the system response. Then the equalizer in which the tap coefficients are determined by SBR cannot produce an ideal equalization effect.

With the increase of the data rates, the nonlinear behavior of the high-speed links gets more and more serious [17]. For example, there are saturation characteristics of active components, such as driver, re-driver and CTLE, in which the linear relationship between input and output is no longer satisfied [18], [19]. In addition, due to the application of active termination, the output impedance of the transmitter is a variable value. For the purpose of reducing power consumption, the output impedance of the transmitter is often designed as a variable value during the output level transit from '0' to '1' or from '1' to '0' [20], [21]. All these nonlinear factors are inconsistent with LTI hypothesis. Traditional DFE equalization technology does not consider the nonlinear factors and has a limited capability for the systems with serious nonlinear behaviors. In this paper, a novel DFE equalization structure is proposed, in which the non-LTI characteristics are taken into account.

The rest of this paper is organized as follows. In Section II, the algorithm of how to construct the response to an arbitrary bit pattern based on SBR is introduced. The traditional DFE structure based on SBR is given and the equalization effects for linear and nonlinear links are compared. In Section III, the concept of multi-bit responses (MBR) and a novel DFE structure based on the MBR are proposed. In Section IV, simulation results for a nonlinear high-speed link built in Simulink are presented to validate the performance of the proposed method. Section V gives the conclusion.

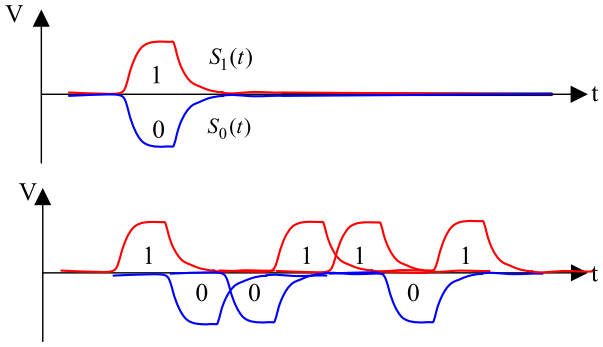

FIGURE 2. Construct the response for input bit pattern through SBR.

II. TRADITIONAL DFE EQUALIZATION TECHNOLOGY BASED ON SBR

For systems that can be well approximated as an LTI system, the system response to an arbitrary input data pattern can be constructed by a linear sum of the shifted SBR. Let $S(1, t)$ and $S(0, t)$ be the response of the bit '1' and bit '0', respectively. $S(1, t)$ and $S(0, t)$ can be considered symmetric and satisfy the following relationship:

$$S(1, t) = -S(0, t) = S(t) \tag{1}$$

The length of the SBR is determined by the memory of the passive channel, denote it as N^*T, where T is the unit interval for one bit and N is the number of UI of the response time. The logical state of the n^{th} bit transmitted in the link is denoted as $b(n)$, and its polarity is denoted as $d(n)$.

$$d(n) = \begin{cases} -1 & \text{when } b(n) = \text{'0'} \\ 1 & \text{when } b(n) = \text{'1'} \end{cases} \tag{2}$$

On the premise of LTI hypothesis, the response of the input bit pattern at the receiver is the linear superposition of the shifted SBR, as shown in Fig. 2. Then the voltage of the n^{th} bit at sampling time t_0 can be calculated by (3).

$$x(n)\,|_{t=t_0} = d(n) * S(t_0) + \sum_{i=1}^{N} d(n-i) * S(t_0 + i * T) \tag{3}$$

Fig. 3 shows the eye diagrams of transient simulation and SBR-based simulation for an LTI link. It can be observed that the eye diagram obtained by SBR-based method matches very well with that obtained by transient simulation.

The basic idea of the DFE is to eliminate the influence of the previous bits on current bit to improve the signal quality at the sampling time. Fig. 4 shows the structure of the full rate DFE, which consists of k delay elements, multipliers, adders, and slicers. It works by subtracting the ISI from the

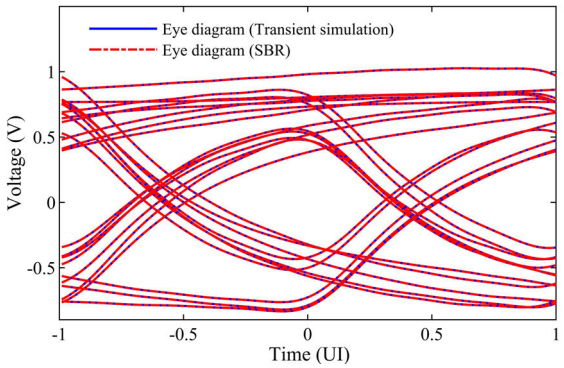

FIGURE 3. Comparison of the eye diagram obtained from transient simulation and SBR based method for a linear system.

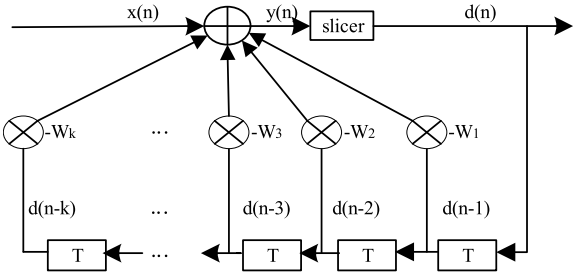

FIGURE 4. The structure of the traditional DFE.

current received signal through feedback. The tap coefficients w_i determine the effect of the equalization. According to (3)a, the coefficients can be determined by the single bit response:

$$w_i = S(t_0 + i * T) \tag{4}$$

At the sampling time t_0, the equalized signal $y(n)$ can be written as:

$$y(n)\,|_{t=t_0} = x(n)\,|_{t=t_0} - \sum_{i=1}^{k} d(n-i) * w_i \tag{5}$$

Under the condition that the link meets the LTI hypothesis, the DFE can theoretically eliminate all the effects of the previous bits on the current bit when the number of taps is large enough. But for the non-LTI system, there is a significant error between the real response and the linear superposition response. Therefore, the DFE in which the coefficients are determined by SBR cannot eliminate the ISI effectively for a non-LTI system.

Fig. 5 compares the equalization effect of the traditional 5-tap DFE based on SBR for an LTI system and a non-LTI system. Table 1 shows the parameters of the eye diagrams before and after DFE equalization for both systems. It can be seen that the traditional DFE based on SBR can improve the signal quality effectively for LTI system, but it is obviously limited to non-LTI system.

III. A NOVEL EQUALIZATION TECHNIQUE BASED ON MBR

For links with high non-LTI behaviors, (3) is violated. The response of arbitrary input bit patterns cannot be constructed accurately by SBR. In [22], a technique of modeling and

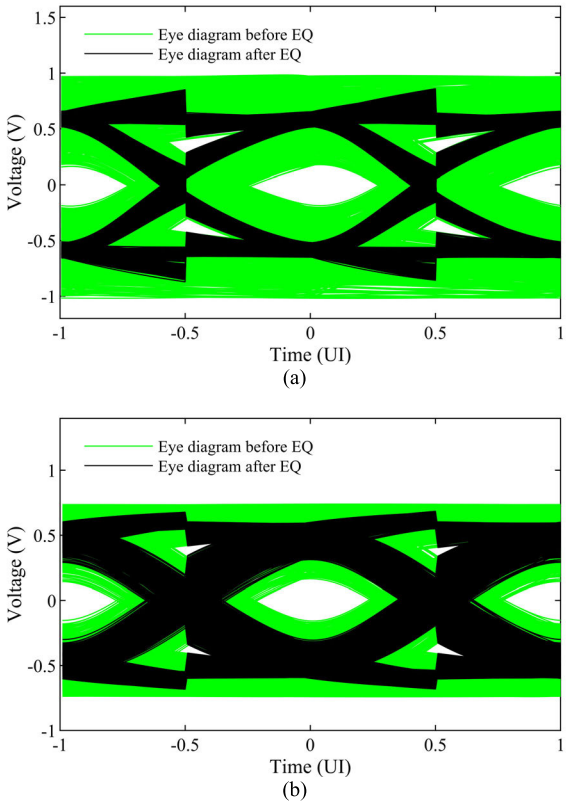

FIGURE 5. Comparison of the eye diagram before and after DFE equalization for (a) a LTI system and (b) a non-LTI system.

TABLE 1. Comparison of values of the eye diagrams for DFE.

	Eye-Diagram Parameters	Before EQ	After EQ	Improvement
LTI system	Max-height (mV)	340.7	1027.6	201.6%
	Eye-width (ps)	50.5	89.5	78.2%
Non-LTI system	Max-height (mV)	293.5	587.5	100.2%
	Eye-width (ps)	43	68	60%

analysis for nonlinear high-speed links is proposed based on Simulink. Fig. 6 shows the discrepancy between the transient simulation results and SBR-constructed results for a non-LTI system. There is an obvious error between SBR-based response and the actual response. DFE technique in which

For non-LTI system, the single bit response is related not only to the current bit, but also to the previous bit patterns. Based on this property, multi-bit responses method is proposed to construct the system response. A novel DFE equalization structure based on MBR is proposed to eliminate ISI for non-LTI high-speed links.

A. CONSTRUCT SYSTEM RESPONSE BY MBR

For a non-LTI link, the single bit response cannot accurately characterize the system response. Assume that it is needed to consider m previous bits to capture the nonlinear behavior and construct the system response correctly. m is considered as the order of the MBR. For m previous bits, each bit can be logic '1' or logic '0', and there are 2^m different previous bit patterns. Denote the i^{th} bit pattern as

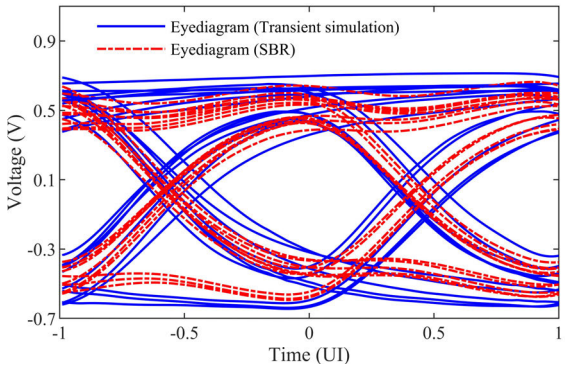

FIGURE 6. Discrepancy between the transient simulation results and SBR constructed results for a non-LTI system.

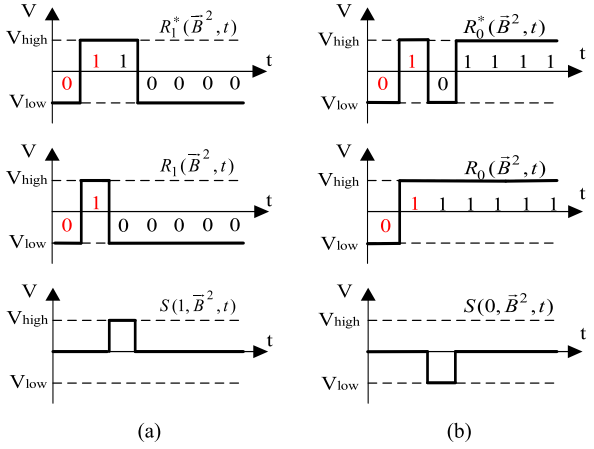

FIGURE 7. Responses of current logic '0' and '1' with different previous bit patterns. (a) current bit is '1'. (b) current bit is '0'.

$\overrightarrow{B^i}(i = 1, 2, \cdots, 2^m)$. Due to the nonlinear feature of the link, the response of the logic '1' or '0' will be different when it has a different previous bit patterns. The more serious the nonlinear behavior is, the more previous bits need to be considered.

The expressions of the response of logic '1' and '0' with the previous bit pattern can be written as (6) and (7), respectively.

$$S(1, \vec{B}^i, t) = \frac{R_1^*(\vec{B}^i, t) - R_1(\vec{B}^i, t)}{2} \quad i = 1, 2, \cdots, 2^m \tag{6}$$

$$S(0, \vec{B}^i, t) = \frac{R_0^*(\vec{B}^i, t) - R_0(\vec{B}^i, t)}{2} \quad i = 1, 2, \cdots, 2^m \tag{7}$$

where $R_1^*(\vec{B}^i, t)$ is the total response of the bit sequence, including the previous bit pattern $\vec{B}^i$ and the current logic '1'. $R_0^*(\vec{B}^i, t)$ is the total response of the bit sequence, including the previous bit pattern $\vec{B}^i$ and the current logic '0'. $R_1(\vec{B}^i, t)$ and $R_0(\vec{B}^i, t)$ are the responses of the previous bit pattern $\vec{B}^i$ when the current bit is logic '1' and '0', respectively.

Take $m = 2$ as an example, the previous bit pattern could be "00", "01", "10", and "11". Then the response of current logic "1" and "0" with the previous bit pattern $\vec{B}^2 = "01"$ is shown as in Fig. 7.

The length of ISI for multi-bit responses is finite, denote it as N^*T. The expression for the response voltage of the n^{th} bit at the sampling time t_0 is shown as follows:

$$x(n)\big|_{t=t_0} = S\left(b(n), \vec{B}^x, t_0\right) + \sum_{i=1}^{N} S\left(b(n-1), \vec{B}^y, t_0 + i * T\right) \tag{8}$$

where

$$\vec{B}^x = [b(n-m), b(n-m+1), \cdots, b(n-1)]$$
$$\vec{B}^y = [b(n-i-m), b(n-i-m+1), \cdots, b(n-i-1)]$$

The response of the nonlinear system can be accurately constructed through (8), which means that the inter-symbol interference caused by the previous bit pattern to the current bit can be determined and eliminated through MBR.

B. STRCUTURE OF THE NOVEL DFE BASED ON MBR

For nonlinear links, it can be seen from (8) that the impact of $b(n-i)$ to $b(n)$ is $S(b(n-i), \vec{B}^y, t_0 + i * T)$, which is related not only to the logic state of $b(n-i)$, but also to the state of the bits before $b(n-i)$. Based on this property, a new DFE equalization technique is proposed, which uses the multi-bit responses to determine the tap coefficients and eliminate the influence of the previous bits. The more serious the nonlinearity is, the more previous bits the MBR needs to consider. The number of previous bits to be considered is the order of MBR.

Assume the order of MBR is m and the number of the taps of DFE is k, $k \geq m$. When $n-(i+m) \geq n-k$, that means $i \leq k-m$, the m previous bits before the bit $b(n-i)$ can be obtained and marked as $\vec{\beta}_i$. The tap coefficients can be calculated by the following equations:

$$w_i = S\left(b(n-i), \vec{\beta}_i, t_0 + i * T\right) \tag{9}$$

$$\vec{\beta}_i = [b(n-(i+m)), b(n-(i+m-1)), \cdots, b(n-(k+1))] \tag{10}$$

In the above equation, w_i is related to the logic state of $b(n-i)$ and the logic state of m previous bits in $\vec{\beta}_i$. So there are $m+1$ previous bits that determine the value of w_i, and each bit has two possible logic levels, so there are 2^m different bit patterns. Each pattern corresponds to a value of w_i. The structure diagram of the DFE when $i > k-m$ is shown in Fig. 8(a).

When $n-(i+m) < n-k$, that means $i > k-m$, only $k-i$ bits of the previous bit pattern can be obtained. At this point, assuming that the remaining previous bits are '0', there are $k-i$ previous bits that determine the value of w_i, as shown in (11) and (12). The structure diagram of the DFE when $i > k-m$ is shown in Fig. 8(b).

$$w_i = S\left(b(n-i), \vec{\beta}_i, t_0 + i * T\right) \tag{11}$$

$$\vec{\beta}_i = [\underbrace{0, \cdots, 0}_{m-(k-i)}, \underbrace{b(n-k), b(n-(k-1)), \cdots, b(n-(i+1))}_{k-i}] \tag{12}$$

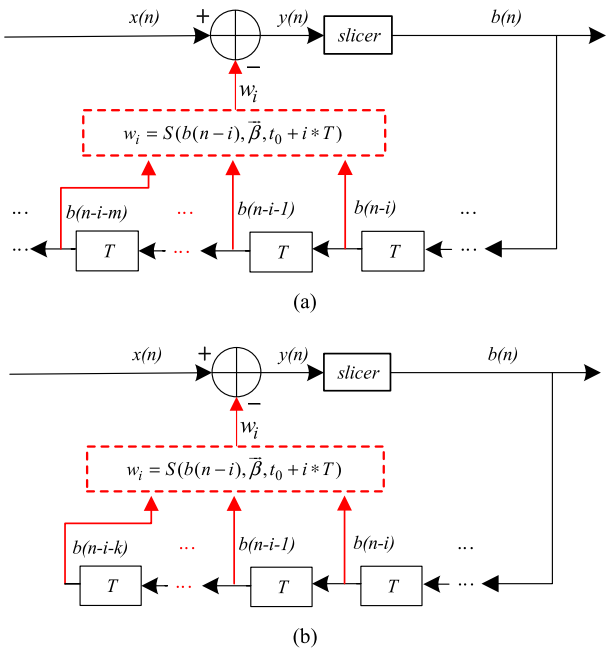

FIGURE 8. Structure of DFE based on MBR when (a) $i \le k - m$ and (b) $i > k - m$.

The equalized response can be written as:

$$y(n)\big|_{t=t_0} = x(n)\big|_{t=t_0} - \sum_{i=1}^{k} w_i \tag{13}$$

The DFE with k taps based on m-order MBR method is denoted as DFE_m^k.

When $m = 0$, no previous bits are considered. Therefore, (9) and (11) can be simplified as (14).

$$w_i = S\left(b(n-i), \vec{\beta_i}, t_0 + i*T\right) = S\left(b(n-i), t_0 + i*T\right) \tag{14}$$

With the logical state of $b(n-i)$ be '0' or '1', the responses are symmetric. Then,

$$S(1, t_0 + i*T) = -S(0, t_0 + i*T) = S(t_0 + i*T) \tag{15}$$

$$w_i|_{b(n-i)=1} = -w_i|_{b(n-i)=0} = S(t_0 + i*T) \tag{16}$$

$$w_i = d(n-i) * S(t_0 + i*T) \tag{17}$$

Substituting (17) into (13), the equalized response can be written as below:

$$y(n)\big|_{t=t_0} = x(n)\big|_{t=t_0} - \sum_{i=1}^{k} d(n-i) * S(t_0 + i*T) \tag{18}$$

Then the form of (13) is the same as (5) when $m = 0$. In that case it is essentially the traditional SBR-based DFE. In the followings, the symbol DFE_0^k refers to the DFE with k taps based on SBR.

C. DETERMINATION OF THE ORDER AND THE TAP NUMBER

The equalization effect of DFE_m^k depends on the order m and the number of taps k. The larger the m and k, the better the equalization effect will be. However, the cost of its hardware and power consumption will also increase with the increase of m and k in the implementation. The tap coefficients w_i can be determined based on multi-bit response and stored in advance. When the circuit works, the corresponding tap coefficients can be obtained from the storage module according to the states of the previous bit patterns. The relationship between the required size of the storage module and the order m is exponential. When $i \le k - m$, the storage module needs to store 2^{m+1} values for each tap; when $i > k - m$, it needs to store 2^{k-i+1} values. Compared with traditional DFE, only the storage module and multiplexers are additional.

Suppose the comprehensive cost of the delay unit and the storage module to store a value is u and v, respectively. Then the cost of DFE_m^k can be approximately denoted as C_m^k.

$$C_m^k = u * k + v * \left((k-m) * 2^{m+1} + \sum_{i=k-m+1}^{k} 2^{k-i+1} \right) \tag{19}$$

For a nonlinear system, the single-bit response is affected by the previous bits, and these previous bits are denoted as $b(-1), \ldots, b(-i), \ldots$. The previous bit sequence in which all logic states are '0' is denoted as a vector $\vec{x}_0$; the sequence, in which only $b(-i)$ is '0', is denoted as $\vec{x}_i$. Define δ_i to measure the impact of previous bit $b(-i)$ on current response:

$$\delta_i = \frac{1}{T} \int |(S(1, \vec{x}_i, t) - S(1, \vec{x}_0, t))\,(S(0, \vec{x}_i, t) - S(0, \vec{x}_0, t))|\, dt \tag{20}$$

It can be considered that the number of previous bits is enough until the following convergence criterion is met, to determine the order m.

$$\frac{\delta_i}{\frac{1}{i}\sum_{j=1}^{i} \delta_j} \le \varepsilon \tag{21}$$

When (21) is met, it means that the nonlinear effect induced by $b(-i)$ is weak enough. Therefore, the value of m can be determined as i. After m is determined, the responses of logic '1' and '0' with different previous bit patterns can be simulated. k is the number of the taps of DFE. The more taps the DFE is with, the more ISI will be eliminated. So, the value of k can be determined by compromising the hardware cost and equalization effect.

IV. SIMULATION VERIFICATION

In order to verify the effectiveness of the proposed DFE method, a nonlinear high-speed link model was built in Simulink, as shown in Fig. 9. Simulink has become a standard for system modeling, simulation and control [23].

The Data Source module is used to send different bit patterns to the link and a Bessel low-pass filter is used to simulate the frequency characteristic of the PHY. Thevenin equivalent circuit is given for the TX output port, which is equivalent to a series of voltage source Vs and output impedance Zs. The S-parameters of a backplane with a certain degree of

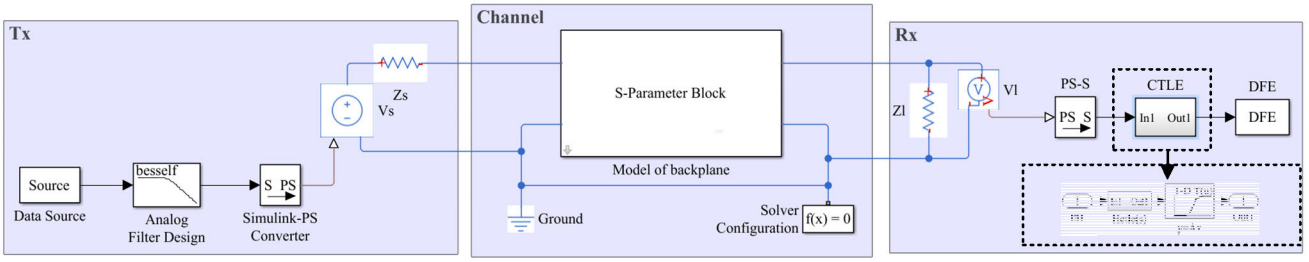

FIGURE 9. A nonlinear high-speed link model built in simulink.

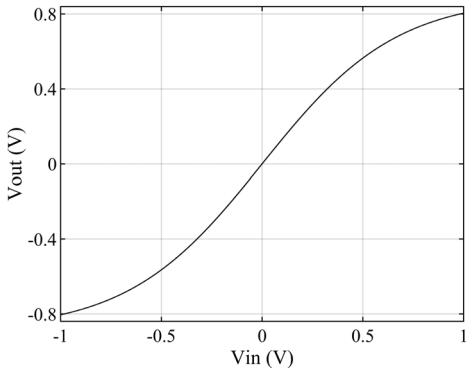

FIGURE 10. The saturation characteristics of active component.

impedance discontinuity are used to represent the channel. The input impedance of the Rx is denoted as Zl. CTLE and DFE are used for equalization at the receiver side. Hctle(s) module represents the transfer function of CTLE with one zero and two poles. The advantage of this model is that it can flexibly adjust the nonlinear degree. The validation of the nonlinear high-speed model can be referred in [22].

The data rate is set to 10 Gbps and two kinds of nonlinear behaviors are included. One is the asymmetry of signal rise and fall time. The rise and fall time of the input signal is set as 10 ps and 20 ps, respectively. Another nonlinear behavior is the saturation characteristics of active component after CTLE, which is represented by a hyperbolic tangent function, shown in (22).

$$V_{out} = \frac{1}{\lambda}\tanh(\lambda * V_{in}) \tag{22}$$

where λ indicates the degree of nonlinearity, the larger the value of λ, the more saturated the curve is. The relationship between V_{out} and V_{in} is shown in Fig. 10 when λ is set to 0.8. It is obvious that it does not satisfy linear map.

In order to construct the arbitrary system responses based on the proposed MBR, a total of 2^m multi-bit responses for logic '0' and '1' are required. It is prepared by transient simulation for 2^m data patterns and each pattern is usually no more than 10 bits. So, the impact on actual simulation time is negligible. 10000 bits of PRBS are used as the input stream for transient simulation and MBR-based method. Fig. 11 compares the eye diagrams of transient simulation with that of the MBR-based method under different orders.

Fig. 11(a) is the comparison for one-order MBR, which is essentially SBR. It can be observed that there is an obvious difference between the two eye diagrams. But in Fig. 11(d), the two eye diagrams are almost overlapped. With the increase of the order m, the eye diagram obtained by MBR-based method is getting closer to the transient simulation result. This validates that the higher-order MBR can capture more nonlinear characteristics. This is the basic idea of the proposed equalization scheme.

The errors of eye-height and eye-width between transient simulation and different order of MBR results are shown in Fig. 12. With the increase of the order of MBR, the errors of both eye-height and eye-width decrease monotonically. The decreased speed is faster from the first-order to the fifth-order than that from the fifth-order to the eighth-order. This reveals that the fifth-order MBR can capture dominate nonlinear behaviors.

A 5-tap DFE is simulated to equalize the response of the nonlinear high-speed link. The tap coefficients of the DFE are determined by the MBR method. For different order MBR, the tap coefficients will be different. The input of the DFE is the response of the nonlinear link after CTLE, which is obtained by transient simulation for 10000 PRBS.

Fig. 13 compares the eye diagrams before and after equalization of DFE_0^5 and DFE_3^5. DFE_0^5 is essentially the traditional 5-tap DFE, in which the tap coefficients are determined by SBR-based method. DFE_3^5 is the proposed 5-tap DFE, in which the tap coefficients are determined by the third-order MBR method. The green eye diagrams in Figs.13(a) and (b) are the received signals that before equalization; the black eye diagram in Fig. 13(a) is constructed by the received signal after equalization with DFE_0^5; the red eye diagram in Fig.13(b) is constructed by the received signal after equalization with DFE_3^5. Fig. 13(c) shows the inner contours of eye diagrams for three cases. The improvement in eye-height and eye-width brought by traditional DFE and the proposed method is shown in Table 2. Both equalization methods can improve the eye diagram quality. Compared to the traditional DFE, the proposed DFE_3^5 shows an increase of about 71% in eye-height and 35% in eye-width. Fig. 14 shows the trend of the improvement of the eye diagram with the order m for a 10-tap DFE. It can be seen that the larger the order m is, the better the effect of equalization will be.

In order to study the relationship between the orders of MBR-based DFE and the nonlinearity degree of the high-speed links, we set up 5 different degrees of nonlinear saturation characteristic for the link in Fig. 9. Different

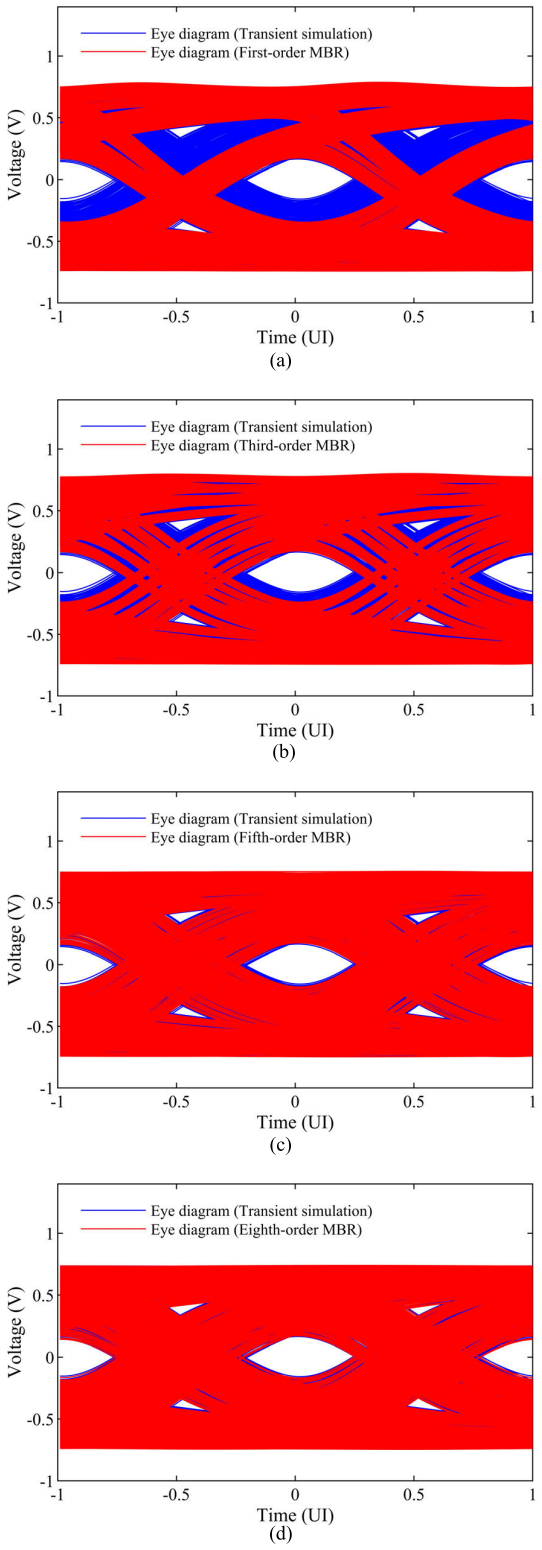

FIGURE 11. Comparison of the eye diagrams between transient simulation and MBR-based method for (a) first-order MBR, (b) third-order MBR, (c) fifth-order MBR, and (d) eighth-order MBR.

orders of MBR-based DFE are performed for these cases. Fig. 15 shows the $V_{out} - V_{in}$ curves with different saturation characteristics, and λ indicates the degree of nonlinearity.

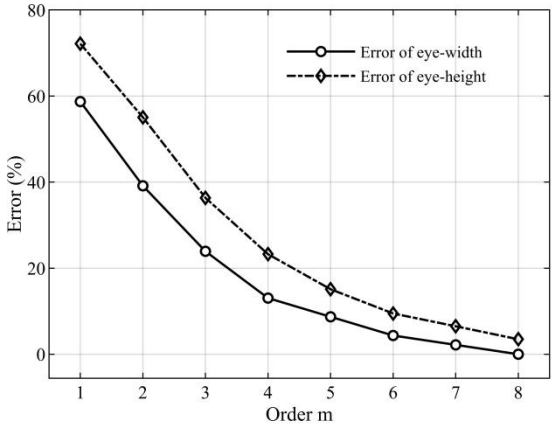

FIGURE 12. Errors of eye-width and eye-height between the transient simulation and MBR-based method.

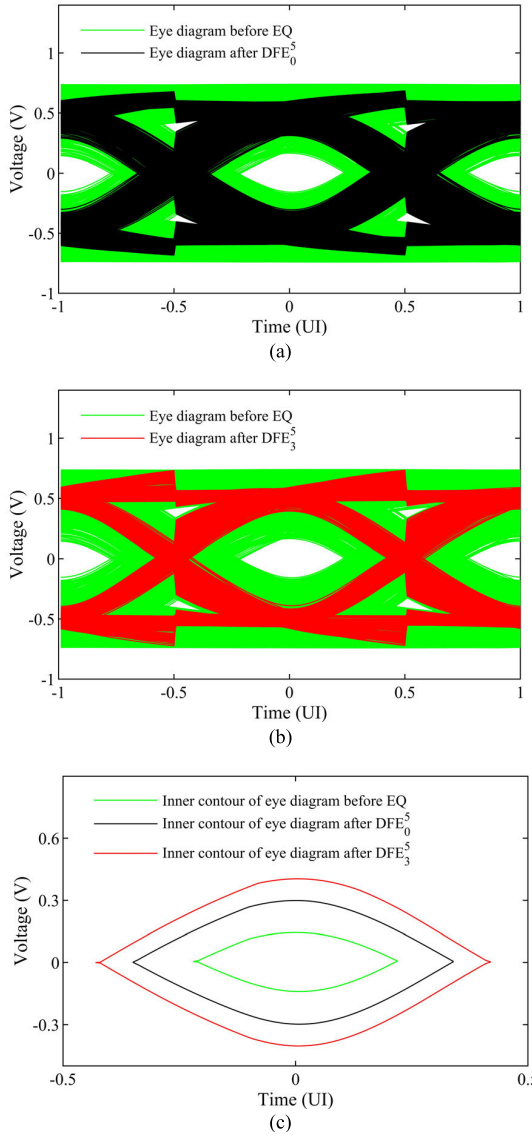

FIGURE 13. Comparison of the eye diagram before and after equalization of DFE_0^5 and DFE_3^5.

In order to show the efficiency of the proposed MBR-based DFE, the advantages of the proposed method DFE_m^k over

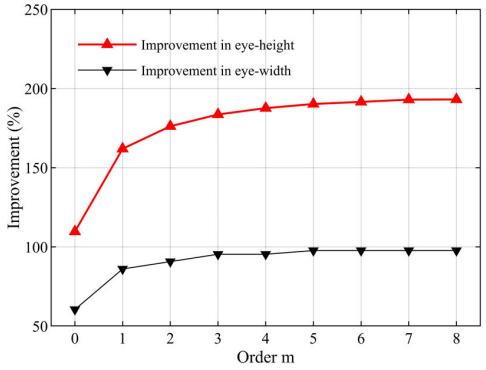

FIGURE 14. Relationship between the improvement in eye diagram and the order for a 10-tap DFE.

TABLE 2. Comparison of values of the eye diagrams before and after DFE.

Eye-Diagram Parameters	Before EQ	After EQ	
		Traditional DFE /Improvement	DFE_3^5 /Improvement
Max Eye-height (mV)	269.7	570.5/111.5%	763.4/183.1%
Eye-width (ps)	42	67/60.0%	82/95.2%

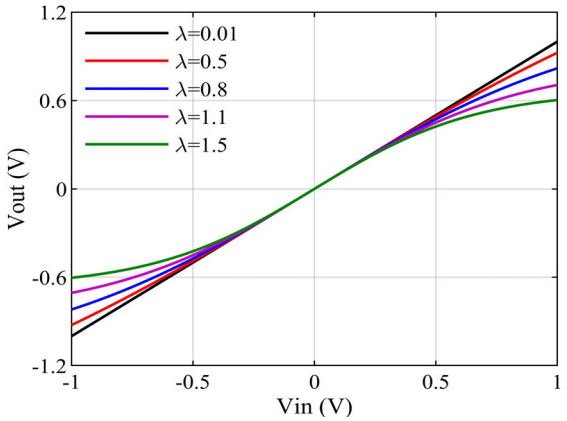

FIGURE 15. Five cases of the saturation characteristics.

the traditional method DFE_0^k is computed by the following equation.

$$\gamma_m^k = \frac{H_m^k - H_0^k}{H} * 100\% \tag{23}$$

where H is the eye-height before equalization, H_m^k is the eye-height after the proposed DFE_m^k equalization, and H_0^k is the eye-height after traditional DFE_0^k equalization.

Fig. 16(a) shows the improvement of eye diagram in different nonlinear cases by traditional equalization DFE_0^{10}. It can be observed that with the increasing nonlinearity, the effect of the traditional DFE based on SBR method becomes increasingly limited. For the linear case, there is an improvement of about 214% in eye-height and 78% in eye-width. But for the most serious nonlinear case, the improvement is only about 62% in eye-height and 35% in eye-width.

In Fig. 16(b), the trend of γ_m^{10} with the degree of nonlinearity is given when the order $m = 1, 2, 3$, and 8. In the linear case, the equalization effect of the proposed method is the same as that of the traditional method. But for nonlinear cases, the proposed method has obvious superiority over the traditional method. The larger the order of the MBR, the greater the advantage of the proposed method is. For the most serious nonlinear case, the proposed method has the great advantage compared with the traditional method. Therefore, the novel proposed DFE method can improve the signal quality more effectively than traditional DFE as the degree of nonlinearity increases.

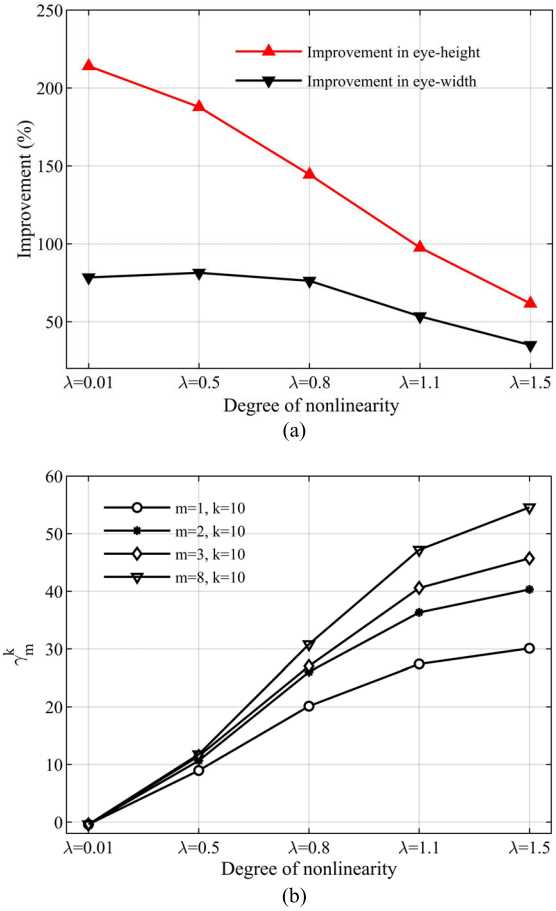

FIGURE 16. The effect of equalization for different nonlinear cases with (a) traditional DFE and (b) the proposed DFE.

V. CONCLUSION

The limitations of traditional DFE based on SBR for the non-LTI system are analyzed first. Results show that the eye diagram cannot be improved efficiently by the traditional DFE with the increase of the nonlinearity degree. In order to construct the responses of arbitrary bit patterns for a non-LTI system, the multi-bit responses method is proposed in this paper. Based on MBR method, a novel DFE structure is presented to equalize the response at the receiver side for high-speed links.

The performance of the proposed equalization method is validated with a nonlinear high-speed link built in Simulink. Simulation results show that the proposed method improves

the quality of the eye diagram significantly than traditional DFE for nonlinear systems. The higher the degree of nonlinearity, the greater the superiority of this method.

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