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Low On-Resistance H-Diamond MOSFETs With 300 °C ALD-Al_2O_3 Gate Dielectric

ZEYANG REN[1,2,*], QI HE[1,*], JIAMIN XU[1], GUANSHENG YUAN[1], JINFENG ZHANG[1,2], JINCHENG ZHANG[1], (Member, IEEE), KAI SU[1], AND YUE HAO[1], (Senior Member, IEEE)

[1]State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, China
[2]Xidian-Wuhu Research Institute, Wuhu 241002, China

Corresponding authors: Jinfeng Zhang (jfzhang@xidian.edu.cn) and Jincheng Zhang (jchzhang@xidian.edu.cn)

*(*Zeyang Ren and Qi He contributed equally to this work.)*

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ABSTRACT C-H diamond metal-oxide-semiconductor field effect transistors with different structures were fabricated on the same polycrystalline diamond plate. Devices A and B with 25-nm-thick high temperature (300°C) atomic layer deposition grown Al_2O_3 dielectric have the same source-to-drain distance of 6 μm and different gate length of 2 μm and 6 μm, respectively. Both devices show ultra-high on/off ratio of over 10^{10} and ultra-low gate leakage of below 10^{-10} A and continuous measurement stability. Device B with the source/drain-channel interspaces eliminated has achieved an on resistance of 46.20 Ω·mm, which is record low in the reported 6-μm H-diamond MOSFETs with the gate dielectric prepared at high temperature ($\geq$ 300 °C). Meanwhile, device B shows larger drain current in a large portion of the linear region at $V_{GS} = -6$ V, and a just slightly smaller I_{Dmax} compared with device A though its L_G is three times of that of device A. A simple model of I_D was used to explain the physics behind this phenomenon. In addition, the breakdown voltage is 145 V for device A and 27 V for device B, corresponding to the average breakdown field of about 0.72 MV/cm and 10.8 MV/cm, respectively.

INDEX TERMS Diamond, MOSFET, low on resistance, eliminating source/drain-gate interspaces.

I. INTRODUCTION

Diamond has tremendous potential to be used in power electronics devices, due to its outstanding properties, such as wide bandgap, high thermal conductivity, high carrier mobility, and high breakdown voltage [1]–[3]. Since p- and n-type doping of diamond is relatively difficult, the two-dimensional hole gas (2DHG) formed at the hydrogen terminated diamond (H-diamond) surface has been widely used to fabricate diamond field effect transistors (FETs) [4]–[7]. Presently, H-diamond FETs have achieved a maximum drain current, cutoff frequency (f_T), and maximum oscillation frequency (f_{max}) of 1.3 A/mm [8], 70 GHz [9], and 120 GHz [7], respectively. A high breakdown voltage of over 2 kV [10] has also been demonstrated. However, the low mobility and stability of the 2DHG on the H-diamond surface have significantly limited the development of H-diamond FETs. In order to improve the performance of the H-diamond FETs, various dielectrics have been used for the fabrication of H-diamond metal-oxide-semiconductor FETs (MOSFETs) [11]–[13]. Proper dielectrics are useful to improve the device performance [28], [29]. Among them, the Al_2O_3 dielectric grown at high temperature using atomic layer deposition (ALD) has shown the highest potential for use in H-diamond FETs due to the high breakdown voltage and high stability [14]–[16]. However, the output current is not sufficiently high. In addition, different device structures, such as [17] gate or the device eliminating source/drain-gate interspaces [12] have been investigated to improve the device performance. As reported by J. Liu *et al.* [12], after eliminating the source/drain-gate interspaces, the device achieved lower on-resistance (R_{on}), higher output current, and higher transconductance (g_m) than other devices with the same gate length (L_G). However, for the devices with the same source to drain distance (L_{SD}), whether those with source/drain-gate interspaces eliminated are still competitive in R_{on}, output current and g_m or not need be further investigated.

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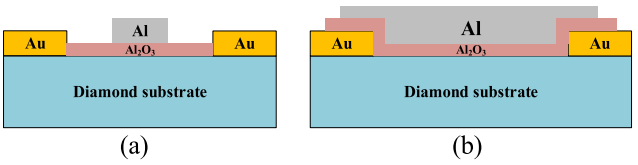

FIGURE 1. Schematic diagram of the device structures. (a) $L_G = 2\mu m$, $L_{DS} = 6\mu m$, (b) $L_G = L_{DS} = 6\mu m$.

In this report, we fabricated two kinds of H-diamond MOSFETs on the same diamond substrate and compared the properties of these devices. Device A has $L_G = 2\mu m$ and $L_{SD} = 6\mu m$. Device B with the source/drain-channel interspaces eliminated has $L_G = L_{SD} = 6\mu m$. The only distance of source- and drain-gate access region is the thickness of the dielectric. The properties of the devices were compared and analyzed.

II. DEVICE FABRICATION

The devices were fabricated on a 250-μm-thick microwave plasma chemical vapor deposition (MPCVD) grown polycrystalline diamond plate from Element Six Ltd. Before any device processes, the diamond sample was cleaned carefully to eliminate any contaminants on the surface. Then, the sample was placed into the MPCVD chamber and treated with hydrogen plasma for ten minutes to form the H-diamond surface. During the treatment, the hydrogen gas flow rate, sample temperature, and microwave power were 600 sccm, 850°C, and 2 kW, respectively. A 100-nm-thick gold layer was deposited on the H-diamond surface by electron beam evaporation to protect the H-diamond surface and form ohmic contact on it. Then, the first lithography was conducted to define the active region and low power oxygen plasma was used to achieve the device isolation. After the second lithography process, wet etching of gold with KI/I_2 was used to create the gate window. Subsequently, a 25-nm-thick Al_2O_3 layer was grown on the sample using an ALD system at 300°C. During the growth process, water was used as the oxidant. Finally, a 100-nm-thick aluminum layer was deposited on the sample and lifted off to form the gate and complete the device fabrication. The gate width (W_G) of the device was 50 μm.

The schematic diagrams of the device structures are shown in Figure 1. The properties of the devices were measured with a Keysight 1505 semiconductor parameter analyzer at room temperature in the air.

III. RESULTS AND DISCUSSIONS

The capacitances of the gate-source diode of the different devices are shown in Figure 2. Conventional FETs (such as device A) with gate length of 2 μm, 4 μm, and 6 μm exhibit a nearly linearly increasing capacitance with increasing gate length, indicating the uniformity of the electrical properties of the devices. However, Device B has significantly higher capacitance than the conventional device with an L_G of 6 μm. This capacitance increment of device B should be ascribed to the metal-insulator-metal (MIM) capacitance resulting from the overlap between the gate and the source/drain metal,

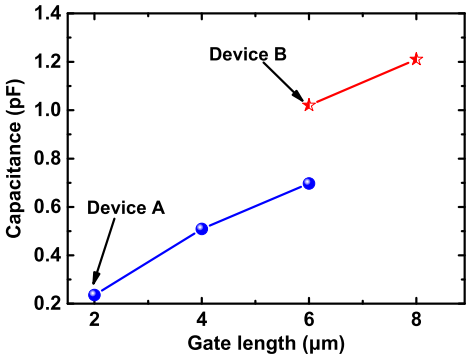

FIGURE 2. Relationship between the maximum gate capacitance and gate length at $V_{GS} = -6$ V.

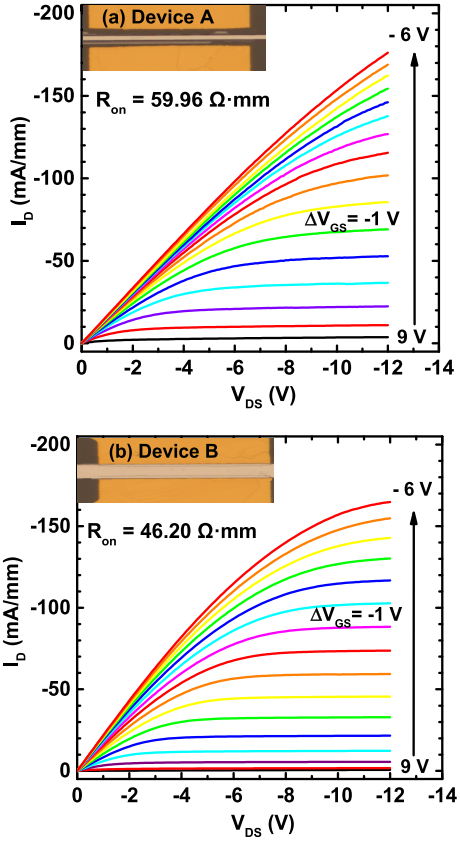

FIGURE 3. Output characteristics of the H-diamond MOSFETs.

with the 25-nm-thick ALD-grown Al_2O_3 used as the insulator. This parasitic capacitance infers that the length of the overlapping part of the gate on each side is about 2 μm. The characteristics of the device structures having the same gate length of 4 μm and with or without source/drain-gate interspaces have been compared by J. Liu *et al.* [12], and our results are very similar to them. Therefore, we only make the comparison of the devices with same source to drain distance and different gate lengths in this study.

The output characteristics of the devices are shown in Figure 3, and the top views of their gates observed by optical microscope are shown in the insets. The maximum saturation

TABLE 1. Summarization of the R_{ON} results of the reported H-diamond MOSFETs with high temperature dielectrics as gate insulator or passivation layer. The symbol ~ indicates that the references didn't report the exact Ron value, and the data are evaluated from the output characterizations of the devices.

Dielectrics	L_G (μm)	L_{SD} (μm)	Ron (Ω·mm)	Ref.
Al_2O_3 (200 °C)	2	6	~50	[18]
YSZ/Al_2O_3 (250 °C)	12	20	442.76	[23]
Al_2O_3 (300 °C)	5	17	~200	[24]
Al_2O_3 (300℃)	2	6.6	63.15	[25]
Al_2O_3 (300℃)	2	6	~120	[18]
Al_2O_3 (450 °C)	2	6	~130	[26]
Al_2O_3 (450 °C)	2	17	~2000	[22]
Al_2O_3 (450 °C)	2	6	~100	[27]
Al_2O_3 (300 °C)	6	6	46.2	This work
Al_2O_3 (300 °C)	2	6	59.96	This work

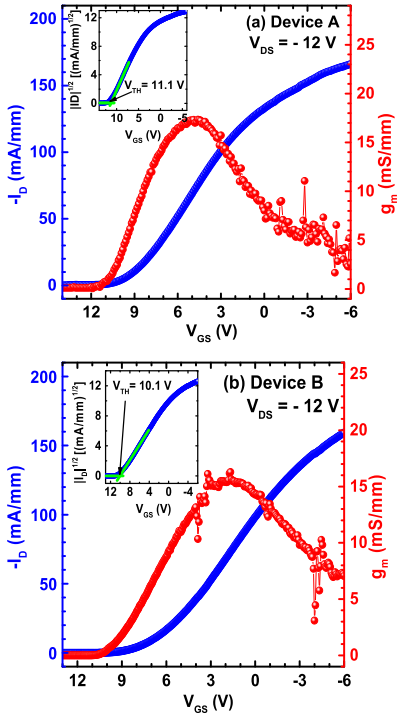

FIGURE 4. Transfer characteristics of the H-diamond MOSFETs. The insets show the threshold voltage of the device.

drain current (I_{Dmax}) and the R_{on} at the gate voltage (V_{GS}) of −6 V for devices A and B are 176 mA/mm and 163 mA/mm, and 59.96 Ω·mm and 46.20 Ω·mm, respectively. We summarized the reported values of R_{on} of the H-diamond MOSFETs with high temperature grown Al_2O_3 dielectrics as gate or passivation dielectric in Table 1. It can be observed that our devices show a record low R_{on} in the reported H-diamond MOSFETs with the gate dielectric prepared at high temperature (≥ 300 °C).

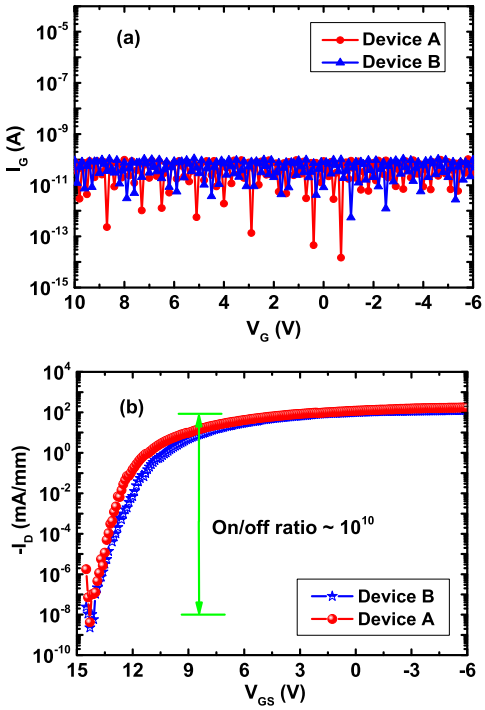

FIGURE 5. (a) Gate current and (b) logarithmic coordinate curves of I_D vs. V_{GS} of the devices.

The transfer characteristics of the devices at $V_{DS} = -12$ V are shown in Figure 4 and Figure 5. The threshold voltage (V_{TH}) extracted from the square root of the drain current vs. V_{GS} relations (insets of Figure 4) are 11.1 V and 10.1 V for Devices A and B, respectively. The maximum transconductance (g_{mmax}) are 17.34 mS/mm and 15.41 mS/mm, respectively. All devices show an ultra-low gate current of below 10^{-10} A (Figure 5(a)) and record-high on/off ratio of over 10^{10} (Figure 5(b)); the on/off ratio is limited by the gate leakage current. The ultra-high on/off ratio indicates perfect device isolation and good insulation of the substrate.

The output and transfer characteristics indicate that device B with $L_{SD} = L_G = 6\mu$m shows almost the same level of I_{Dmax} and g_{mmax} and even smaller R_{on} than device A with the same $L_{SD} = 6\mu$m and a much smaller $L_G = 2\mu$m. The R_{on} value of device B is not only smaller in this study but is also lowest among the reported H-diamond MOSFETs with a gate dielectric prepared at high temperature (≥ 300 °C). The smaller R_{on} value of device B is unexpected because the L_G of device B is much larger than that of device A. However, the sheet resistance of the gate with a V_{GS} of −6 V is 7.7 kΩ/sq if the ohmic contact resistance can be omitted, or even smaller if the ohmic contact resistance cannot be omitted. This gated sheet resistance is smaller than that of the ungated Al_2O_3/H-diamond structure (11.15 kΩ/sq), as deduced from the difference in the R_{on} data of devices A and B. Therefore, a relatively larger portion of the channel from the source to drain has lower resistance in device B than in device A with the same L_{SD}, and it is reasonable that device B has a smaller R_{on}. Moreover, if the sheet resistance of the considered V_{GS} is smaller for the device with the gate

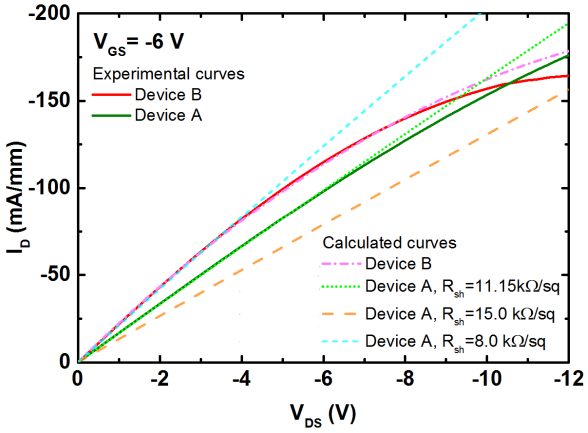

FIGURE 6. Experimental and calculated curves of I_D vs. V_{DS} relations of devices A and B at $V_{GS} = -6V$.

than without the gate, the smallest R_{on} of the devices with the same source-to-drain interspace will occur in the device without source/drain-gate interspaces.

It is also noteworthy that device B, whose L_G is three times that of device A, delivers almost the same output current as device A. Device B has a larger drain current in a large portion of the linear region at $V_{GS} = -6$ V and a slightly smaller I_{Dmax} than device A. We establish a simple model of I_D to determine the reasons for this phenomenon. For device B with the series resistance from the ohmic contacts and the source-to-gate and gate-to-drain interspaces taken as zero, the drain current in the linear region can be expressed as,

$$I_D = \beta(V_{GT} - \frac{V_{DS}}{2})V_{DS} \tag{1}$$

where $\beta = W_G \mu C_G / L_G$ is used, and C_G and μ are the gate capacitance and carrier mobility of the device, respectively. If the saturation drain voltage satisfies $V_{Dsat} = V_{GT}$ as in typical long-channel MOSFETs, in the considered V_{DS} range I_D will not saturate at $V_{GS} = -6$ V in both devices.

As for device A with non-ignorable source and drain series resistances (R_S and $R_D = R_S$), assume the voltage drop across the gated channel is $V_{ch} = xV_{DS}$, $0 < x < 1$, and there will be

$$I_D = \beta(V_{GT} - \frac{V_{ch}}{2})V_{ch}, \tag{2}$$

$$V_{DS} - V_{ch} = 2R_S I_D. \tag{3}$$

In Eqs. (2) and (3) I_D and V_{ch} will be solved simultaneously. Then I_D at a given V_{DS} can be calculated for devices A and B with different gate lengths, and the calculation results are shown in Figure 6. It is seen that the model described by Eqs. (2)-(3) reproduces the I_D vs. V_{DS} curves of both devices at $V_{GS} = -6$ V in their relative positions and the expected intersection. The error between the calculation curve and the experimental curve at large V_{DS} are ascribed to the adoption of the constant mobility rather than the more practical parallel-field-dependent mobility, but the error in principle doesn't influence our analysis.

It is found that device B outputs a large current because the V_{DS} can be completely applied on the gated channel, and creates a strong lateral electrical field to promote carrier drift. In contrast, in device A, the voltage drop on the whole gated channel occupies only 25.7% - 27.7% of the drain voltage in the range of 0 V < V_{DS} < 12 V; therefore, the source and drain series resistances shared almost three quarters of V_{DS} and significantly reducing the lateral electrical field under the gate of device A. This results in the smaller I_D of device A than device B at small or modest values of V_{DS}. However, this also means the almost linear I_D increasing due to the lateral electrical field enhancement under the gate will occur in a much larger V_{DS} range because $x = V_{ch}/V_{DS}$ is almost a constant. Therefore, the I_D of device A could possibly go beyond that of device B if the latter tends to saturate, as is observed in this study. Of course, the appearance and position of the intersection point will depend on the source and drain series resistances, which are determined by the sheet resistance of the ungated channel (Figure 6), L_{SG}, and L_{GD}, as well as the L_G and the property of the gated channel. As for the measured extrinsic g_m (Figure 4), it fundamentally shows the intrinsic g_m in device B due to $R_S \approx 0$ but is largely reduced from the intrinsic g_m in device A, so the magnitudes of the extrinsic g_m could be at almost the same level.

As a result, device B with $L_{SG} = L_{GD} = 0$ has a definitely lower R_{on} at strong forward gate bias compared with device A with the same L_{SD}, and its output current and g_m are almost the same as those of device A due to the negative effect of the series resistance on the latter.

Operation stability is very important to promote the wide application of H-diamond devices. The 2DHG on the H-diamond surface is induced by the transfer doping effect between the diamond surface and the adsorbed species. The performance of H-diamond FETs depends on the measurement conditions and the environment [19], [20], which is ascribed to the instability of the adsorbed species. In addition, the instability causes degradation of the device performance during continuous testing. We obtained 30 continuous measurements to characterize the stability of the proposed devices. The results of I_{Dmax} and R_{on} at V_{GS} of -6 V are summarized in Figure 7. The I_{Dmax} and R_{on} of both devices only exhibit a slight difference during 30 continuous measurements. In Device B, the current has even a slightly increase after 30 continuous measurements. In this work, the 25-nm-thick ALD-grown Al_2O_3 layer was used as both a gate insulator and a passivation layer. As reported by Daicho *et al.* [16] and Kawarada *et al.* [21], during grown Al_2O_3 using ALD with water as oxidants, a fresh 2DHG layer produces on the C-H diamond and Al_2O_3 interface. This conductive layer is protected by the Al_2O_3 dielectric layer, which lead to the improvement of the stability of the 2DHG. In addition, we suggest that the charges or traps existing in the Al_2O_3 layer has slightly changing during continuous measurement, which induces a slight changing of the 2DHG. This changing is corresponding with the slight changing of the device characterizations during continuous measurement.

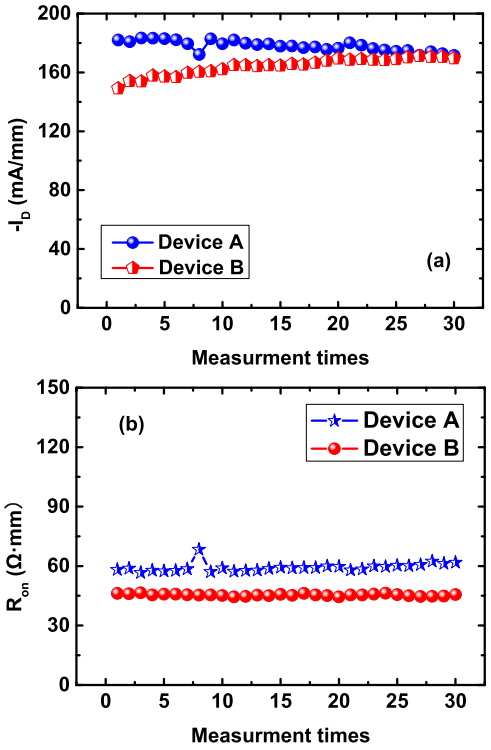

FIGURE 7. Summarization of (a) I_D and (b) Ron at $V_{GS} = -6$ V of different devices for 30 times continuous measurements.

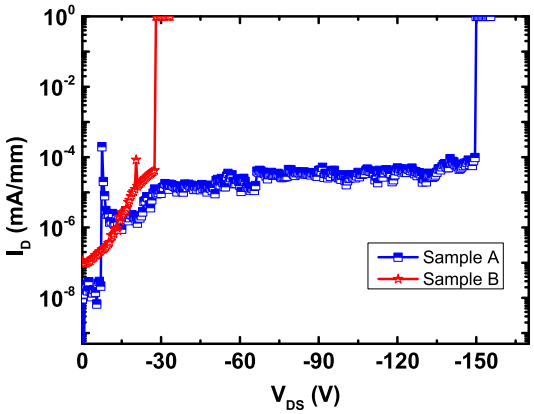

FIGURE 8. Breakdown voltage of different devices.

The breakdown performance is an important aspect of the use of H-diamond FETs in power electronics devices. We compared the breakdown voltage of different devices, as shown in Figure 8. The breakdown of both devices are due to gate-drain breakdown because the gate current shows the same increase as I_D. Device A has a breakdown voltage that is higher than 145 V. For the drain-gate distance of 2 μm, the average electric field strength is over 0.72 MV/cm. Compared with the results of a C-H diamond MOSFET fabricated on a polycrystalline diamond sample with a thick Al_2O_3 passivation layer by Syamsul *et al.* [22], our devices show higher breakdown field strength, and the values are comparable to a device on a single crystalline diamond sample (0.8∼0.9 MV/cm) [10], indicating the good device fabrication processes and high quality of the Al_2O_3 dielectrics in our devices. Meanwhile, the breakdown voltage of device B is 27 V. This breakdown could occur in the 25-nm-thick Al_2O_3 film between the drain and the gate, and thus the evaluated average electric field strength reaches 10.8 MV/cm.

IV. CONCLUSION

Two types of H-diamond MOSFET with a 25-nm-thick high-temperature (300°C) ALD-grown Al_2O_3 dielectric and the same L_{SD} of 6 μm were fabricated on a CVD-grown polycrystalline diamond substrate. The characteristics of the devices were compared. All devices demonstrated ultra-high on/off ratio of higher than 10^{10}, ultra-low gate leakage current of below 10^{-10}A, and continuous measurement stability. Device A with $L_G = 2\mu$m showed slightly larger output current and maximum g_m than device B with $L_G = 6\mu$m due to eliminating source/drain-gate interspaces, while device B had the lowest R_{on} of 46.20 Ω·mm among reported 6-μm H-diamond MOSFETs with a gate dielectric prepared at high temperature (≥ 300 °C). A simple model of I_D was used to analyze the physics of this behavior. The average breakdown field was about 0.72 MV/cm for device A and 10.8 MV/cm for device B.

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(Zeyang Ren and Qi He contributed equally to this work.)

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ZEYANG REN received the B.Eng. and Ph.D. degrees in microelectronics and solid state electronics from Xidian University, Xi'an, China, in 2014 and 2018, respectively. His current research interest includes wide gap-band semiconductor materials and devices.

QI HE received the B.Eng. degree from Xidian University, Xi'an, China, where he is currently pursuing the Ph.D. degree with the School of Microelectronics.

JIAMIN XU received the B.Eng. degree from Xidian University, Xi'an, China, where he is currently pursuing the M.S. degree with the School of Microelectronics.

GUANSHENG YUAN received the B.S. degree from the Shandong University of Science and Technology, Qingdao, China, in 2014. He is currently pursuing the M.S. degree with the School of Microelectronics, Xidian University, Xi'an, China.

JINFENG ZHANG received the B.S. degree in electronic science and technology and the Ph.D. degree in microelectronics and solid state electronics from Xidian University, Xi'an, China, in 2000 and 2006, respectively. Her research interests include diamond and III–V nitride semiconductor materials and devices.

JINCHENG ZHANG (Member, IEEE) received the M.S. and Ph.D. degrees from Xidian University, Xi'an, China, in 2001 and 2004, respectively. He is currently a Professor with Xidian University. His current research interests include wide gap-band semiconductor GaN and diamond materials and devices.

KAI SU received the B.S. degree from the Harbin Institute of Technology, in 2010, and the M.S. degree in microelectronics from Sichuan University, in 2013. He is currently pursuing the Ph.D. degree with the School of Microelectronics, Xidian University, Xi'an, China.

YUE HAO (Senior Member, IEEE) is currently a Professor of microelectronics and solid state electronics with Xidian University, Xi'an, China. He is the Academician of the Chinese Academy of Sciences. His current research interests include wide gap-band materials and devices, advanced CMOS devices and technology, semiconductor device reliability physics, and failure mechanism and organic electronics.