

Received January 14, 2020, accepted February 15, 2020, date of publication March 11, 2020, date of current version March 20, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2980039

Learning Localized Spatial Material Properties of Substrates in Ultra-Thin Packages Using Markov Chain Monte Carlo and Finite Element Analysis

CHERYL SELVANAYAGAM^{1,2}, PHAM LUU TRUNG DUONG¹,
AND NAGARAJAN RAGHAVAN¹, (Member, IEEE)

¹Engineering Product Development, Singapore University of Technology and Design, Singapore 487372

²Advanced Micro Devices, Inc. (AMD), Package Engineering, Singapore 469032

Corresponding author: Cheryl Selvanayagam (cheryl_selavanayagam@mymail.sutd.edu.sg)

This work was supported by the Economic Development Board of Singapore (EDB) and Advanced Micro Devices, Inc. (AMD) under the Industry Postgraduate Program (IPP) under Grant IGIPAMD1801.


ABSTRACT Thinned silicon dies and thin substrates using thin core and coreless structures have enabled thin packages. For robust manufacturing and reliability of these parts, solving the warpage problem is key. While current finite element methodologies can provide some insights at the design stage, these simulations are only as accurate as the inputs such as the material properties and the stress-free temperatures. Electronic substrates are especially challenging to characterize and model as they are laminates consisting of a core with layers of resin and metal lines on either side. In this work, a hybrid approach using Markov Chain Monte Carlo (MCMC) and Finite Element Analysis (FEA) is used to learn the spatially varying properties of the substrate from Digital Image Correlation (DIC) measurements of the warpage. The analysis is carried out at room temperature and at an elevated temperature point. Image analysis on electrical artwork is also carried out to correlate the material properties to the substrate metal density. These results will be useful to package and substrate designers to understand how material properties vary over the substrate and how temperature and metal density affect material properties so that robust design for future packages to minimize warpage can be initiated by careful routing of metal lines depending on the locally desired properties of the stack.

INDEX TERMS Bayes method, finite element analysis, Markov Chain Monte Carlo (MCMC), material characterization, substrate, warpage.

I. INTRODUCTION

As consumers call for high performance mobile devices like laptops in thinner form factors, there is a push in the industry to make the electronic packages that go into them thinner. These thin packages need to be designed carefully as high warpage in these parts can lead to assembly and reliability issues like bump bridging and solder extrusion [1], [2]. Finite element analysis (FEA) would be a good tool for warpage prediction if accurate material properties were available. One study has shown that variation in package warpage measurements can be directly attributed to variation in the material properties of the bismaleimide triazine (BT) substrate [3]. The electronic substrate is inherently a composite material consisting of a core and alternating layers of

Ajinomoto Build-up Film (ABF) and copper metal lines on either side. The result is an anisotropic, spatially-varying, and temperature-dependent material that is cumbersome to characterize [3], [4], tedious to calculate analytically [5]–[7] and complex to model [8]. Several authors have demonstrated that FEA simulations with substrates modelled using trace mapping is the best method to model warpage accurately [9]–[13]. Trace mapping works by first importing the electrical artwork and then ‘superimposing’ it onto the elements of the metal layer in the FEA model. As a result, the volume fraction of the metal for each element is calculated and material properties are assigned accordingly. Regions of higher metal density would be assigned different material properties than regions of lower metal density. However, this method requires that the electrical artwork be available. During the design stage, this method is not feasible as the electrical artwork is often not even started. Clearly, an efficient method to determine

The associate editor coordinating the review of this manuscript and approving it for publication was Jiajie Fan .

substrate material properties is required where electrical artwork is not a prerequisite.

In one of the recent studies by Brandt *et al.*, material properties of different layers and interfaces in the solar cell have been predicted with good accuracy using a methodology which combines Bayesian inference with a physics-based model [14]. A similar approach is attempted here to address this problem. The results achieved using the Bayesian inference are very promising as will be evident in the sections that follow. In an earlier work of the team, we proposed a hybrid approach of using Markov Chain Monte Carlo (MCMC) and FEA to learn the material properties of the electronic substrate at locations along the package diagonal, which showed that the simulation error reduced by as much as two orders of magnitude [15].

In this work, the approach is extended to learn the material properties across the whole substrate and at two different temperatures as well. Understanding how the material properties of the substrate vary spatially and result in the observed warpage measurements will add to our understanding of the warpage phenomena and help us design better packages. In addition, the learned material properties are then correlated with the metal densities at different regions over the substrate to gain a better understanding of how metal densities affect material properties and warpage.

II. METHODOLOGY

The Bayesian inference approach uses each new evidence (experimental observation) to update the probability of a hypothesis. For this problem, the warpage model parameters are represented as a random vector (\mathbf{x}) with a prior distribution $\rightarrow p_0(\mathbf{x})$. Using Bayes' theorem, the posterior distribution of parameters given the observation (or likelihood), $L(\Upsilon|\mathbf{x})$ is

$$p(\mathbf{x}|\Upsilon) \propto L(\Upsilon|\mathbf{x})p_0(\mathbf{x}) \quad (1)$$

where Υ is the observed data.

Therefore, the posterior considers the observed data and refines our hypothesis about the distribution of the parameters. MCMC is a subset of this approach where evidence is collected by sampling the probabilistic space randomly [16], [17]. In this work, FEA simulations were carried out using random vectors of parameters generated by MCMC random sampling. The likelihood, $L(\Upsilon|\mathbf{x})$ is obtained from

$$L(\Upsilon|\mathbf{x}) = \frac{e^{-SS/(2v^2)}}{(2\pi v^2)^{n/2}} \quad (2)$$

where SS is the sum of squared error between the measurements and the FEA model output, v is the standard deviation of the measurement errors and n is the number of parameters. The MCMC analysis is carried out on MATLAB[®] using a toolbox developed by Haario *et al.* [18]. A short introduction to MCMC can be found in our previous work, where this approach is used to learn the material properties of the stiffener and different regions of the substrate [15].

As the objective of this work is to learn the spatially varying material properties of the substrate at two different temperatures, experimental measurements of warpage over the whole substrate and at two temperatures are required. In the next section the warpage measurements from digital image correlation (DIC) that are used in the MCMC analysis as the experimental observations (likelihood) will be presented.

III. DIGITAL IMAGE CORRELATION

DIC is a deformation measurement tool. A typical DIC setup consists of the camera to image the sample at certain time intervals, the speckled sample under external force or temperature loading and a computer for image correlation, speckle tracking and deformation measurement. The 2D version of this tool consists of one camera and can measure the in-plane deformation only. On the other hand, a 3D setup of this system consists of two or more cameras. As each camera captures different views of the sample, image processing and tracking can be used to measure in-plane and out-of-plane deformation at once, enabling curved surfaces to be measured as well. A speckle pattern on the sample is typically required for accurate measurements [19]. 3D DIC measurements were carried out on three package samples at two temperatures sequentially $\rightarrow 25^\circ\text{C}$ and 60°C . The temperature ramp rate used was about $40^\circ\text{C}/\text{min}$ to simulate the fast ramp rate of a typical reflow profile. The package sample has a body size of less than $40 \times 40 \text{ mm}^2$ with a total thickness of less than 1.5mm. The sample consists of a silicon die assembled onto an electronic substrate with a stiffener ring to control the warpage. In turn, the electronic substrate is a laminate consisting of the core and alternating layers of metal line and ABF. As we are interested in measuring the warpage of the whole package, the speckle pattern was applied on the back of the substrate. A sample speckle pattern can be found in our earlier publication [8]. The contour plot of a typical DIC result is shown in Fig. 1. Out-of-plane deformation of these parts was measured over four lines – two diagonal lines (AC and BD), one horizontal (FH) and one vertical line (EG) as shown in Fig. 1, in order to fully characterize the warpage of the part.

Line plots of the warpage measurements are shown in Figs. 2-4. Fig. 2 and 3 shows the warpage of all three samples (referred to as S1, S2 and S3), along each line, at room temperature and the elevated test temperature of 60°C respectively. The mean of the measurements from the three samples is represented by the dashed black line in both figures. From Fig. 2, in general, there is good agreement between the measurements from the three samples at room temperature, with the largest variability observed along the horizontal line F-H. Fig. 3 indicates that greater variability between the samples is observed at the higher temperature. This could be the result of different amount of residual stresses accumulated in each package during the assembly process, resulting in different amounts of stress relief and hence, different warpages.

For the MCMC analysis, the observation (likelihood) data used is the mean of the DIC measurements from the three

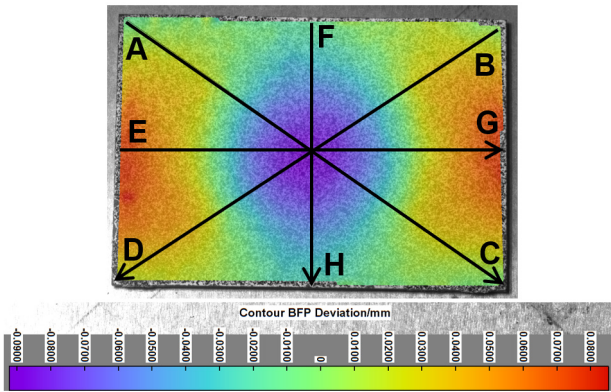


FIGURE 1. Contour plot of out-of-plane deformation from DIC. Four lines (A-C, B-D, F-H and E-G) drawn show locations along which warpage was extracted.

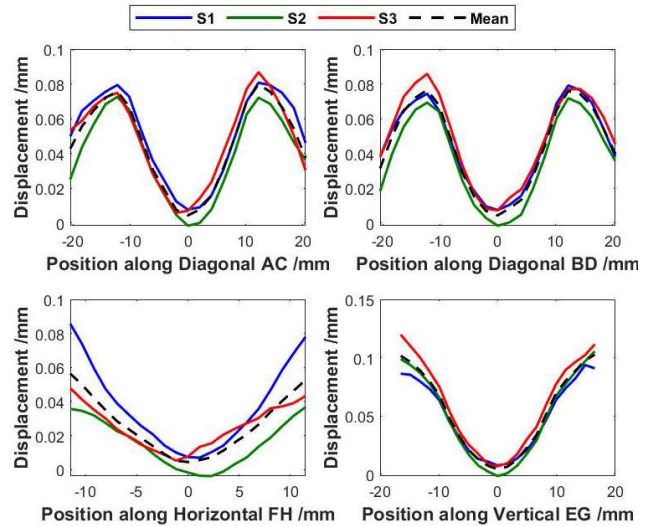


FIGURE 3. Warpage plots for three samples and the mean along four lines (A-C, B-D, F-H and E-G) at a higher temperature of 60°C.

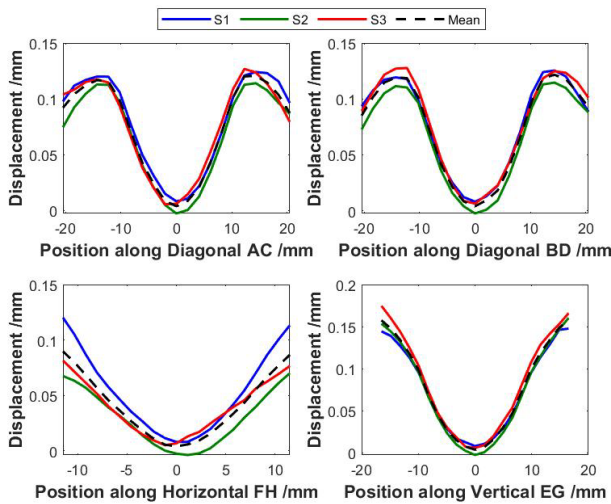


FIGURE 2. Warpage plots for three samples and the mean along four lines (A-C, B-D, F-H and E-G) at room temperature (25°C).

samples. This is shown in Fig. 4. It is clearly evident that warpage is higher at room temperature and decreases as temperature increases. Similar warpage shapes and trends are observed along all four lines.

IV. FEM AND MCMC MODEL DETAILS

A. FINITE ELEMENT ANALYSIS (FEA)

Typical FEA analysis for package warpage assumes that the package is symmetric about the two axes. Using symmetrical boundary conditions, the model size can be reduced by four times. However, in this case, there can be no assumption of symmetry as the objective is to determine material properties over the entire substrate. Therefore, a finite element model of the whole package was built on ANSYS® v19. The model consists of the silicon die, substrate, underfill and stiffener, as shown in Fig. 5(a). The loading condition used was a single step temperature ramp down from the stress-free temperature of 150°C to the temperature of interest (25°C or 60°C). The stress-free temperature was determined from warpage measurements, where the magnitude of the warpage is the smallest.

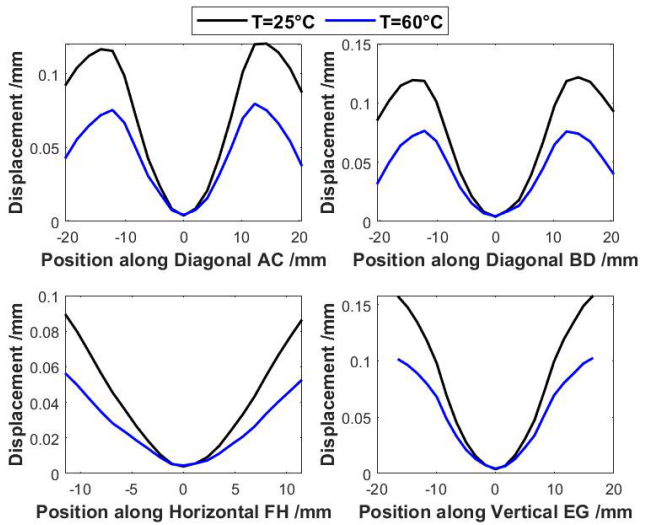


FIGURE 4. Comparison of the mean of the warpage plots of the three samples along four lines (A-C, B-D, F-H and E-G) at the two temperatures.

In order to learn the spatially-varying material properties of the substrate, the substrate was divided into nine parts as shown in Fig. 5(b). The model was parameterized such that each of the nine sections of the substrate can be assigned its own unique in-plane coefficient of thermal expansion (CTE) value. This approach of assigning each section its own unique CTE will allow the MCMC analysis to learn the material properties of the substrate that reflect the variation of copper density across the substrate.

A mesh convergence study is carried out to optimize the run-time of the warpage model to about 15 sec without compromising on the warpage simulation accuracy. The model is post-processed to extract warpage at the same locations as in the DIC measurements i.e. along the two diagonals and the central vertical and horizontal lines and output these values to a text file. Warpage contours from the simulations and

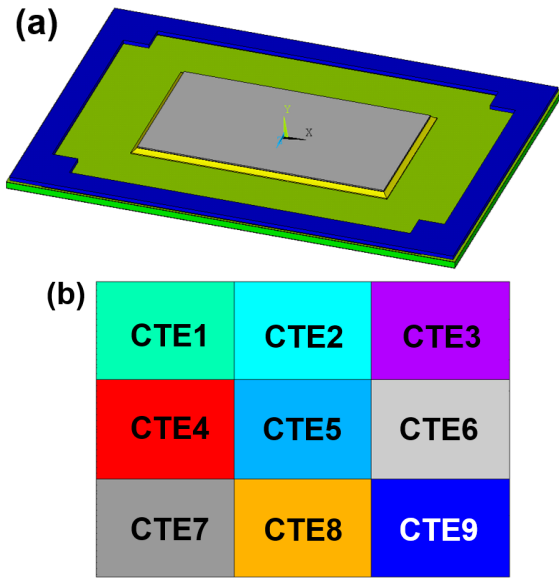


FIGURE 5. (a) FEM model of the whole package for warpage analysis and the corresponding (b) top view of the substrate showing the nine sections with unique CTE properties.

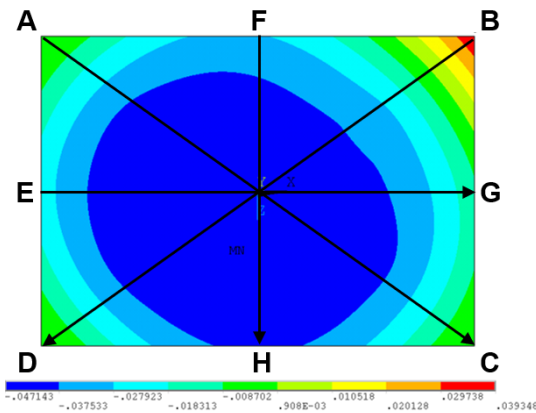


FIGURE 6. Warpage contour plot showing the four lines along which warpage data from the FEA model is extracted.

the lines along which the warpage is extracted are shown in Fig. 6. Fig. 7 shows the initial warpage plots from simulation when assuming uniform CTE of 14 ppm/°C for the whole substrate. As expected, there is a large discrepancy between the measured and simulated results. The total squared sum difference between measured and simulated results for the four curves is 9.9×10^{-2} .

B. MARKOV CHAIN MONTE CARLO (MCMC)

For this analysis, the equations governing the MCMC are similar to those in our previous work [10]. The only difference is that we are trying to fit to the measurements over four discrete lines, instead of just one. In order to accomplish this, the sum of squared error for each line is added together.

The relationship between the displacement $y_{i,l}$ and position $p_{i,l}$ is given by the FEM model in Eqn 3. Subscript i denotes

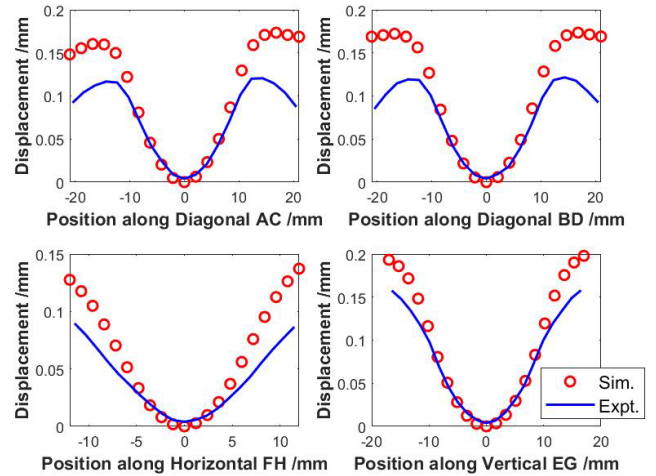


FIGURE 7. Displacement plot showing experimental measurements from DIC (blue line) and FEA simulations with initial assumed parameters (red circles) along the four lines (A-C, B-D, F-H, E-G). Relatively large SS between these two results of 9.9×10^{-2} is obtained.

the point along the line and l denotes the line.

$$y_{i,l} = f_{i,l}(p_{i,l}, \mathbf{x}), \quad i = 1, \dots, N, \quad l = 1, \dots, 4 \quad (3)$$

Here, $\mathbf{x} = (x_1, \dots, x_{n_p})$ is a vector of n_p parameters of the model. Given that the measurement of displacement data along each line $\Upsilon = \{z_{i,l} = y_{i,l} + \zeta_{i,l}\}, i = 1, \dots, N, l = 1, \dots, 4$ and errors, $\zeta_{i,l}$, are available, the total sum squared error is now given by:

$$SS(\mathbf{x}) = \sum_{l=1}^4 \sum_{i=1}^N (z_{i,l} - f_{i,l}(p_{i,l}, \mathbf{x}))^2 \quad (4)$$

V. RESULTS AND DISCUSSION

A. NINE-PARAMETER MODEL: IN-PLANE CTE AT DIFFERENT LOCATIONS ACROSS THE SUBSTRATE AT ROOM TEMPERATURE

A nine-parameter MCMC is executed to determine the spatially varying material properties in the substrate. This analysis is run for 2000 iterations. The total time taken for this analysis is about 9 hours. The convergence plot is shown in Fig. 8. Note that all the nine CTE values seem to have converged. The corresponding probability density plots are shown in Fig. 9.

The best estimate for CTE1 through CTE9 are determined to be 16.0, 14.8, 12.0, 10.7, 8.2, 11.2, 12.9, 15.1 and 14.9 ppm/°C respectively by averaging the latter values of the MCMC trials. These values are represented graphically in Fig. 10. Note that there is quite a wide variation in the CTE in the nine regions with variations of up to 50%. Similar to earlier work, it is worth noticing that the CTE increases from the center to the corner of the substrate.

Displacement plots of the experiment and simulation are shown in Fig. 11 using the optimum values of CTE obtained above. Also shown on this plot are the 5% and 95% quantiles for the 2000 iterations. The total squared sum of the difference between the experimental and simulated displacement curves across the four lines has now decreased from

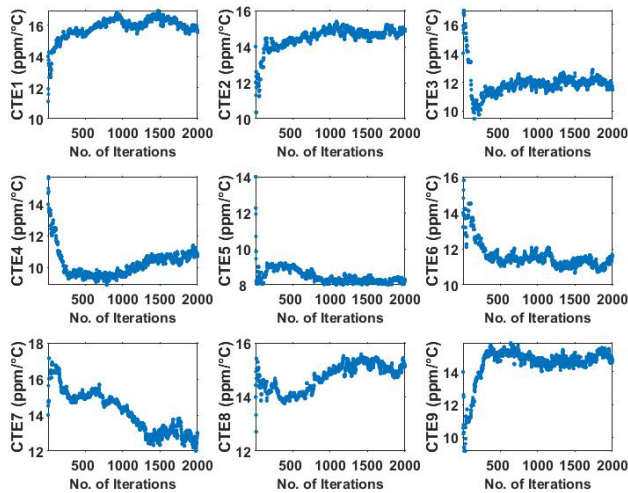


FIGURE 8. Convergence plot of the nine CTE parameter values across the substrate at room temperature over 2000 iterations.

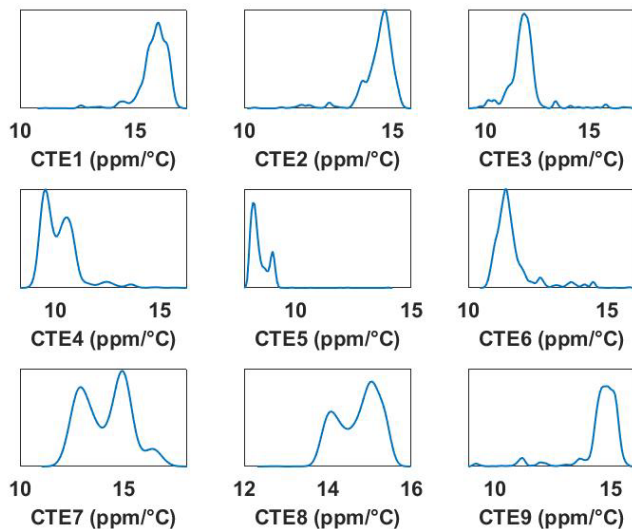


FIGURE 9. Probability density functions of the learnt nine CTE parameter values at room temperature post execution of the MCMC.

9.9×10^{-2} in the previous section to 3.2×10^{-3} , much more than an order of magnitude. This implies that an extremely good fit is achieved with the learnt material properties.

B. NINE-PARAMETER MODEL: IN-PLANE CTE AT DIFFERENT LOCATIONS ACROSS THE SUBSTRATE AT ELEVATED TEMPERATURE

The MCMC analysis is repeated to determine the material properties, this time at 60°C. The analysis is run for 1500 iterations and the total time taken for this analysis is about 6 hours. The convergence plot in Fig. 12 shows that the nine CTE values have converged satisfactorily. The corresponding probability density plots are shown in Fig. 13.

The best estimate for CTE1 through CTE9 is determined to be 16.1, 12.7, 10.2, 8.8, 8.0, 10.0, 12.2, 13.9 and 15.3 ppm/°C respectively by averaging the latter values of the MCMC trials. Again, these values are represented graphically in Fig. 14.

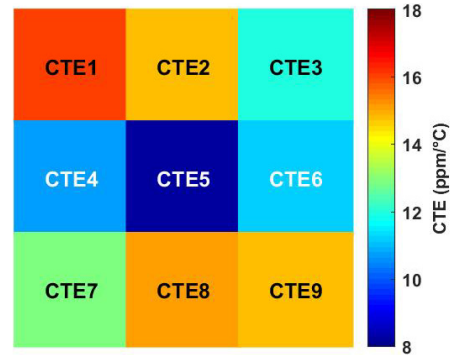


FIGURE 10. Graphical representation of optimum effective CTE values, as obtained from the MCMC analysis, indicating that the CTE clearly increases from the center to the corner of the substrate by as much as 50-100%.

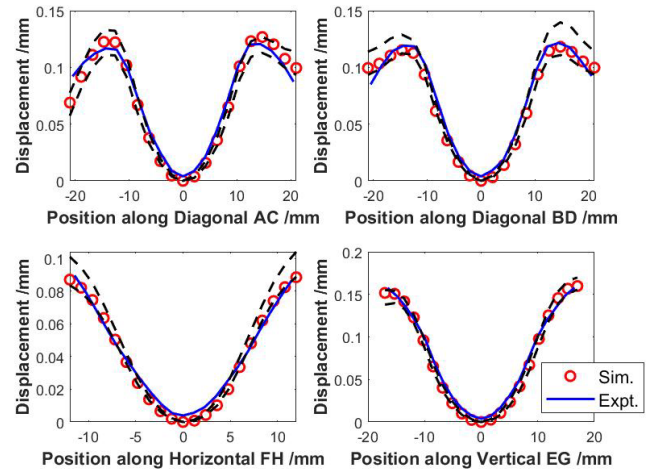


FIGURE 11. Displacement plot showing experimental measurements from DIC (blue line) and FEA simulations with optimized set of parameter values at room temperature (red circles) along the four lines (A-C, B-D, F-H, E-G). Significantly lower SS of 3.2×10^{-3} is obtained between these two results. The 5% and 95% quantiles for the 2000 simulation runs are also plotted (dashed black lines).

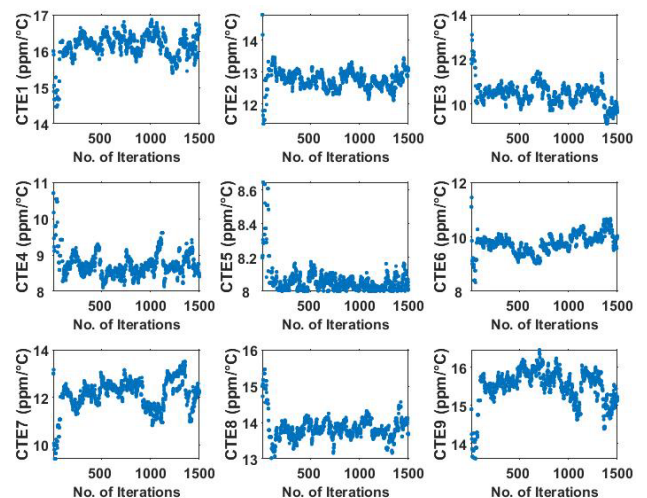


FIGURE 12. Convergence plot of the nine CTE parameter values across the substrate at 60°C over 1500 iterations.

Just as in the results for the room temperature, the CTE is again found to increase from the center of the substrate. This trend will be investigated further in the next

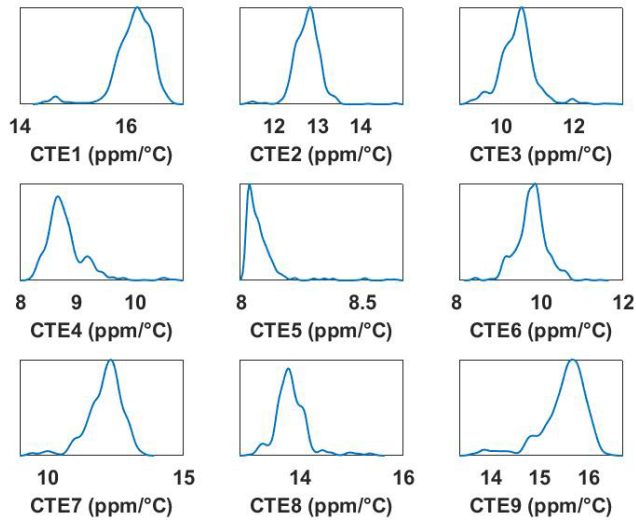


FIGURE 13. Probability density functions of the learnt nine CTE parameter values at 60°C post execution of the MCMC.

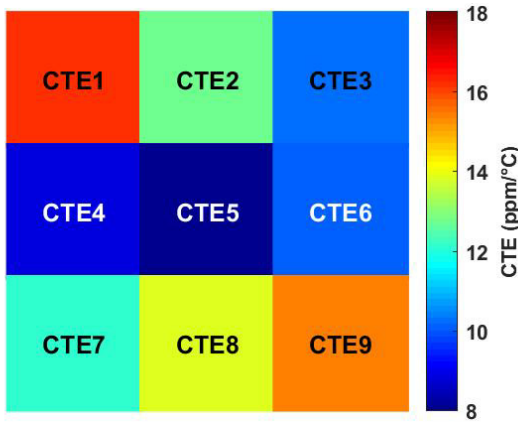


FIGURE 14. Graphical representation of CTE values at 60°C from the MCMC analysis, indicating that CTE increases from the center to the corner of the substrate.

section when we correlate the learnt material properties to the metal layer density. Displacement plots of the experiment and simulation are shown in Fig. 15 with the 5% and 95% quantiles for the 1500 iterations. The total squared sum of the difference between the experimental and simulated curves across the four lines is 3.7×10^{-3} . This is in the same range as that for the room temperature analysis. Again, an extremely good correlation between the simulated and experimental curves is achieved with the learnt material properties.

C. CORRELATION BETWEEN LEARNT MATERIAL PROPERTIES AND METAL LAYER DENSITIES

Though learning material properties of the substrate is found to be greatly useful in modeling the current design of the substrate and warpage accurately, the learnt material properties will not help in future robust design unless they can be correlated to the metal layer densities. Unfortunately, the software that generates the electrical artwork, Cadence®, is only able to output the metal densities of the whole layer and

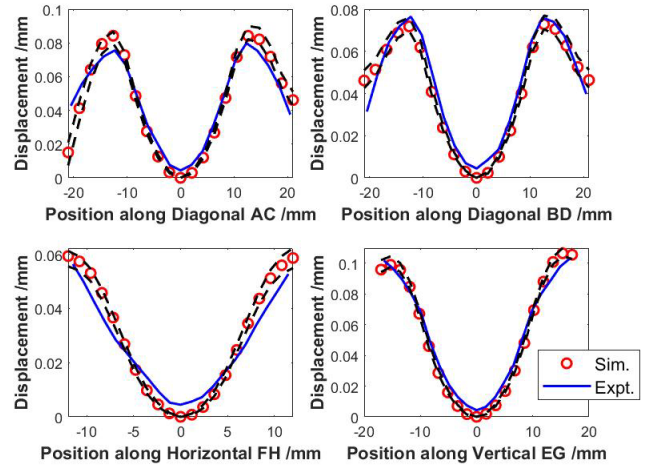


FIGURE 15. Displacement plot showing experimental measurements from DIC (blue line) and FEA simulations with optimized set of parameter values at 60°C (red circles) along the four lines (A-C, B-D, F-H, E-G). Significantly lower SS of 3.7×10^{-3} is obtained between these two results. The 5% and 95% quantiles for the 1500 simulation runs are also plotted (dashed black lines).

not subsections of the layer. In order to get this information, a code in Matlab® is written to carry out image analysis on the electrical artwork of each of the eight layers in the substrate and compute the metal densities based on counting of the white and black pixels. The metal density results from the code are then validated using similar data obtained from Cadence®. There is an error of about 6% in the copper density calculated by the Matlab® code, as compared to the Cadence® report for the first metal layer. This is possibly caused by the reduced resolution of the narrow trace lines in the imported image. Other layers with fewer lines have their areas calculated with an error of less than 3%.

With the validated code, image analysis is carried out to determine the copper density in each of the 8 metal layers, in each of the 3 by 3 cells (Fig. 5(b)) in the substrate, totaling 72 different regions. The metal density of each cell is determined by averaging the metal densities of the eight layers at that cell location. The plot of the extracted localized CTE determined from the MCMC analysis against the metal density determined for each cell from the Matlab® image analysis is shown in Fig. 16. Clearly, as the copper density in the cell increases, the corresponding effective CTE decreases. This is because the metal layer consists of copper, whose CTE is 17 ppm/°C, and ABF material of higher CTE (CTE > 20 ppm/°C). Therefore, with a higher metal content, the volume average of CTE is expected to be lower. A similar trend is observed at higher temperature as well. However, as indicated by the large scatter of the datapoints in the plot, the average copper density is not the only factor governing the CTE at each cell. Other factors such as copper layer pattern and the resulting anisotropy of the sample, residual stresses in the substrate and edge effects, to mention a few, also contribute to the local CTE of the sample and are not accounted for explicitly in this work.

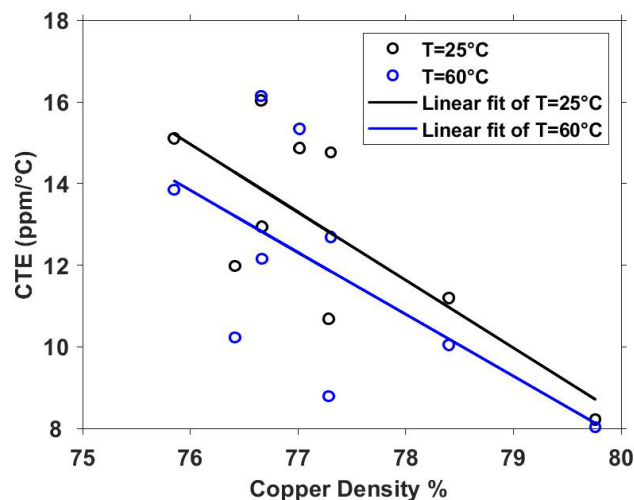


FIGURE 16. Plot of CTE against copper density percentage at room temperature and at 60°C, showing similar trends that further confirm the validity of our approach.

The substrate consists of three materials → core, ABF and copper metal. At the central cell of the substrate, the highest metal density and lowest CTE is found. This is because the core is significantly thicker than the ABF and metal layers. At the substrate center, the low CTE of the core material (CTE < 10 ppm/°C) easily dominates the material property of the cell. The outer cells in the periphery have higher CTEs, as in those regions, the accumulated effect of the ABF and copper layers plays a larger role in the deformation.

VI. CONCLUSION AND RECOMMENDATIONS

In this study, a hybrid approach of FEA and MCMC is proposed and used to calculate the spatially varying material properties (specifically, CTE) of the electronic substrate at two different temperatures. When the optimized local values of CTE from the MCMC routine are used in the FEA, excellent agreement with experimental measurements using DIC is obtained, indicating that the CTEs calculated using the methodology are indeed very accurate. The metal densities for each cell in the substrate were determined through image analysis of electrical artwork. It was found that the CTE is inversely proportional to the metal density. These results will be very useful for package designers to design future packages with better spatial planning so as to ensure much lower warpage. Though accurate, the hybrid approach of FEA and MCMC is still quite time-consuming, especially for larger FEA models.

In the future, we will attempt to replace the FEA model with a neural network as demonstrated by several authors [20], [21]. The neural network is a computational tool that learns the weights and biases between the input and output layers and then uses the learned parameters to make efficient predictions for other values in the parameter design space [22], [23], resulting in a significant speed up of simulation time. This would enable the number of MCMC iterations to increase well beyond 2000 in a fraction of the time.

In addition, this would also enable us to increase the number of parameters included in the analysis to better understand the factors (copper pattern, material property changes in constituent materials, residual stresses, etc.) that affect CTE and hence the warpage of the package.

The hybrid approach of using the MCMC and neural networks is the first step in realizing an inverse design model for electronic substrates. The next step would be to develop a model to link substrate characteristics like the number of layers and the material properties of the constituent materials to the material properties learned from the MCMC. With this framework in place, designers would be able to input a warpage profile and the model would return the necessary substrate characteristics (and perhaps the stack design, material choice and metal pattern density itself) that are required to achieve the desired warpage contour.

ACKNOWLEDGMENT

AMD, the AMD Arrow logo, and combinations thereof are trademarks of Advanced Micro Devices, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies. ©2019 Advanced Micro Devices, Inc. All rights reserved.

REFERENCES

- [1] C. Chee Meng, S. Stoeckl, H. Pape, F. Mun Yee, and T. Ai Min, "Effect of substrate warpage on flip chip BGA thermal stress simulation," in *Proc. 12th Electron. Packag. Technol. Conf.*, Singapore, Dec. 2010, pp. 500–504.
- [2] M. Kurashina, D. Mizutani, M. Koide, M. Watanabe, K. Fukuzono, and H. Suzuki, "Low warpage coreless substrate for large-size LSI packages," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf.*, San Diego, CA, USA, May 2012, pp. 1378–1383.
- [3] Q. Zhang, J. C. C. Lo, S. W. R. Lee, and W. Xu, "Determination of a meaningful warpage acceptance criterion for large PBGA components through the correlation with scattering in material properties," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, San Diego, CA, USA, May 2018, pp. 718–723.
- [4] Q. Zhang, J. C. C. Lo, S. W. R. Lee, W. Xu, and W. Yang, "Characterization of orthotropic CTE of BT substrate for PBGA warpage evaluation," in *Proc. 15th IEEE Intersociety Conf. Thermal Thermomech. Phenomena Electron. Syst. (ITherm)*, Las Vegas, NV, USA, May 2016, pp. 1312–1319.
- [5] L. Valdevit, V. Khanna, A. Sharma, S. Sri-Jayantha, D. Questad, and K. Sikka, "Organic substrates for flip-chip design: A thermo-mechanical model that accounts for heterogeneity and anisotropy," *Microelectron. Rel.*, vol. 48, no. 2, pp. 245–260, Feb. 2008.
- [6] P. Chen, P. Raghavan, K. Yazzie, and H. Fei, "On the effective coefficient of thermal expansion (CTE) of bilayer/trilayer in semiconductor package substrates," in *Proc. IEEE 65th Electron. Compon. Technol. Conf. (ECTC)*, San Diego, CA, USA, May 2015, pp. 1932–1937.
- [7] J. M. Hurley, "Estimating the engineering properties of electronic packaging materials," *IEEE Trans. Compon. Packag. Technol.*, vol. 31, no. 2, pp. 417–424, Jun. 2008.
- [8] C. Selvanayagam, R. Mandal, and N. Raghavan, "Comparison of experimental, analytical and simulation methods to estimate substrate material properties for warpage reliability analysis," *Microelectron. Rel.*, vols. 88–90, pp. 817–823, Sep. 2018.
- [9] B. Kim and B. Han, "Numerical/Experimental hybrid approach to predict warpage of thin advanced substrates," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, San Diego, CA, USA, May 2018, pp. 267–272.
- [10] P. Chen, Z. Ji, Y. Liu, C. Wu, N. Ye, and H. Takiar, "Warpage prediction methodology of extremely thin package," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, USA, May 2017, pp. 2080–2085.

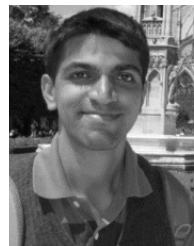
- [11] L. O. McCaslin, S. Yoon, H. Kim, and S. K. Sitaraman, "Methodology for modeling substrate warpage using copper trace pattern implementation," *IEEE Trans. Adv. Packag.*, vol. 32, no. 4, pp. 740–745, Nov. 2009.
- [12] M. Wang and B. Wells, "Substrate trace modeling for package warpage simulation," in *Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, Las Vegas, NV, USA, May 2016, pp. 516–523.
- [13] V. K. Yaddanapudi, S. Krishnaswamy, R. Rath, and R. Gandhi, "Validation of new approach of modelling traces by mapping mechanical properties for a printed circuit board mechanical analysis," in *Proc. IEEE 17th Electron. Packag. Technol. Conf. (EPTC)*, Singapore, Dec. 2015, pp. 1–6.
- [14] R. E. Brandt, R. C. Kurchin, V. Steinmann, D. Kitchaev, C. Roat, S. Levenco, G. Ceder, T. Unold, and T. Buonassisi, "Rapid photovoltaic device characterization through Bayesian parameter estimation," *Joule*, vol. 1, no. 4, pp. 843–856, Dec. 2017.
- [15] C. Selvanayagam, P. Luu Trung Duong, R. Mandal, and N. Raghavan, "Machine learning approach to improve accuracy of warpage simulations," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, Las Vegas, NV, USA, May 2019, pp. 834–841.
- [16] D. Gamerman and H. Lopes, *Markov Chain Monte Carlo*. New York, NY, USA: CRC Press, 2006.
- [17] D. P. Kroese, T. Taimre, and Z. I. Botev, *Handbook of Monte Carlo Methods, Wiley Series in Probability and Statistics*. New York, NY, USA: Wiley, 2011.
- [18] H. Haario, M. Laine, A. Mira, and E. Saksman, "DRAM: Efficient adaptive MCMC," *Statist. Comput.*, vol. 16, no. 4, pp. 339–354, Dec. 2006, doi: 10.1007/s11222-006-9438-0.
- [19] M. A. Sutton, "Digital image correlation for shape and deformation measurements," in *Springer Handbook of Experimental Solid Mechanics*, W. Sharpe, Ed. Boston, MA, USA: Springer, 2008.
- [20] W. Jianxin and Y. Xiaojun, "U-shaped part springback forecasting based on the finite element method and the neural network," in *Proc. Int. Conf. Comput., Control Ind. Eng.*, Wuhan, China, 2010, pp. 253–256.
- [21] Y. Fei, G. Pengdong, and L. Yongquan, "Bolt force prediction using simplified finite element model and back propagation neural networks," in *Proc. IEEE Inf. Technol., Neww., Electron. Autom. Control Conf.*, Chongqing, China, May 2016, pp. 520–523.
- [22] R. Rojas, *Neural Networks: A Systematic Introduction*. Berlin, Germany: Springer-Verlag, 1996.
- [23] C. F. Higham and D. J. Higham, "Deep learning: An introduction for applied mathematicians," *SIAM Rev.*, vol. 61, no. 3, pp. 860–891, Jan. 2019.



CHERYL SELVANAYAGAM received the bachelor's and master's degrees in mechanical engineering from the National University of Singapore (NUS). She has worked on material characterization and mechanical simulations at the A* STAR Institute of Microelectronics (IME), Singapore, and is currently a member of Technical Staff at Advanced Micro Devices (AMD), Singapore. She is currently pursuing the Ph.D. degree with the Singapore University of Technology and Design (SUTD). Her current research interest includes incorporation of machine learning algorithms with high fidelity finite element simulations for warpage minimization in ultrathin electronic packages.



PHAM LUU TRUNG DUONG received the B.S. and M.S. degrees in electrical engineering from Bauman Moscow State Technical University, in 2006 and 2008, respectively, and the Ph.D. degree in process control from Yeungnam University, South Korea, in 2013. He is currently a Senior Research Scientist with the Engineering Product Development (EPD) Pillar, Singapore University of Technology and Design (SUTD). His research interests include PID control, model predictive control, stochastic systems, prognostics and health management and uncertainty quantification.



NAGARAJAN RAGHAVAN (Member, IEEE) received the Ph.D. degree from the Division of Microelectronics, Nanyang Technological University (NTU), Singapore, in 2012. He was a Postdoctoral Fellow with the Massachusetts Institute of Technology (MIT), Boston, and IMEC, Belgium, in joint association with the Katholieke Universiteit Leuven (KUL). He is currently an Assistant Professor with the Singapore University of Technology and Design (SUTD), Engineering Product Development (EPD) Pillar. His work focuses on reliability assessment, characterization and lifetime prediction of nanoelectronic devices as well as material design for reliability, inverse design, physics informed machine learning, uncertainty quantification and prognostics and health management of electronic systems. He was a recipient of the IEEE Electron Device Society (EDS) Early Career Award for 2016, Asia-Pacific recipient for the IEEE EDS Ph.D. Student Fellowship in 2011, and the IEEE Reliability Society Graduate Scholarship Award in 2008. To date, he has authored/coauthored more than 180 international peer-reviewed publications and five invited book chapters as well. He serves as the General Chair for the IEEE IPFA 2020 at Singapore and has consistently served on the review committee for various IEEE journals and conferences including IRPS, IIRW, IPFA, and ESREF. He is currently serving as an Associate Editor for IEEE Access. He was an invited member of the IEEE GOLD committee, from 2012 to 2014.

...