IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 24, 2020, accepted March 8, 2020, date of publication March 11, 2020, date of current version March 24, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2980080

Hybrid Internal Vth Cancellation Rectifiers for RF Energy Harvesting

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This work was supported by the King Fahd University of Petroleum and Minerals under Project SF191-EE-540.

ABSTRACT This paper presents two Internal Threshold Voltage (IVC) cancellation schemes for rectifiers used in RF energy harvesting: N-stage IVC based rectifier and IVC based rectifier with Self Vth Cancellation (SVC). The presented rectifiers reduce the threshold voltage of the transistors and deliver a high-rectified output voltage at an input frequency of 402MHz. Tanner TSPICE simulation tool in 0.18μm TSMC CMOS technology is used to confirm the functionality of the proposed designs. Simulation results show that the proposed design is superior to the previously published works in reducing the MOSFET threshold voltage and delivering a rectified high output voltage at an input voltage of 200mV and frequency of 402 MHz.

INDEX TERMS RF energy harvesting, threshold compensation, internal Vth cancellation, CMOS rectifier.

I. INTRODUCTION

Energy harvesting is the process of extracting electrical energy from the available sources in the environment including solar, thermal, mechanical, fluid and Radio Frequency (RF) energy. In the recent years, the interest in RF energy harvesting as a promising substitute for a battery has increased rapidly. This can be attributed to the wide range of applications for wireless power transmission in areas like Radio Frequency Identification (RFID), biomedical devices, and wireless sensor networks is increasing. A typical RF energy harvesting system shown in Fig.1 consists of the antenna which receives incident power, a matching network for maximizing the power transfer and minimizing the signal reflection from the load, an RF-to-DC rectifier which is mostly responsible for the performance of energy harvesting system, storage devices which could be batteries or capacitors, and the load.

Typically, the power density for RF energy source ranges between 0.01 to 0.1μW/cm^2, which is the lowest among other sources such as vibration and thermal [2]. For instance, the maximum power received for a free space distance of 40m is 7μW and 1μW for frequencies of 900MHz and 2.4GHz respectively. Another important factor playing a role in the received power is the distance as shown in Fig.2.

The associate editor coordinating the review of this manuscript and approving it for publication was Sun Junwei.

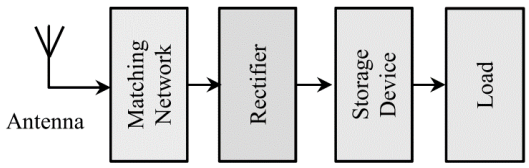

FIGURE 1. Block diagram of a typical RF energy harvesting [1].

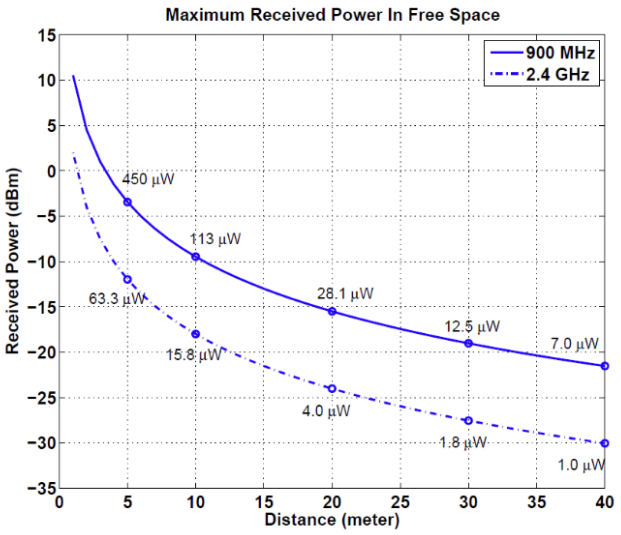

FIGURE 2. Maximum received power in free space versus distance [2].

Table 1 summarizes the experimental data obtained from different RF sources varying in frequency, power, and distance with the amount of harvested energy [3].

TABLE 1. Experimental data of RF energy harvesting.

Source	Source Power (W)	Frequency (MHz)	Distance (m)	Energy Harvested Rate (μW)
Isotropic RF transmitter	4	902-928	15	5.5
Isotropic RF transmitter	1.78	868	25	2.3
Isotropic RF transmitter	3	915	27	2
TX91501 Powercaster transmitter	3	915	5	189
TX91501 Powercaster transmitter	3	915	11	1
KING-TV tower	960k	674-680	4.1k	60

CMOS technology is widely used in the design of rectifiers for RF energy harvesting. Due to the very small RF energy density, the input voltage amplitude after the matching impedance does not typically reach 300mV which is lower than the threshold voltage of the MOS transistor even though the matching impedance network is also used to boost the voltage induced by the antenna [4]. Researchers proposed different topologies to reduce the threshold voltage. Some of them reduce the threshold voltage using the body effect [3], [5]. Other techniques compensate the threshold voltage using an external auxiliary circuit to generate gate bias voltage [6]–[8]. In [9], auxiliary transistors are used to enhance the forward conduction and also to reduce the leakage of current.

Some techniques use bootstrapping circuit by charging up the bootstrapping capacitors to apply it to the gate of the main rectifying pMOS transistors [10]. In [11], a high-speed comparator is used to control the reverse leakage current. Self-Vth cancellation (SVC) is used in [12] to bias the gate by the output voltage of the rectifier itself in order to decrease the threshold voltage of the transistor by the same amount of the output DC voltage. In [13], clamper circuits were used to insert a negative DC level to bias the gates of the main rectifying pMOS devices during its conduction state.

Another approach to reducing the threshold voltage of a MOS transistor is by injecting some charges on its gate oxide. It could be done by applying a high voltage to the gate causing charges to be trapped in the oxide due to the tunneling effect. However, this approach has two main drawbacks. The trapped electrons will be released gradually over time and temperature which makes it not reliable for the long term. In addition, it has an additional fabrication cost [14].

Some schemes use advanced technologies such as zero threshold voltage MOS. However, it is not available in the standard CMOS process and requires additional fabrication cost. Also, it has zero V_{th} for a small current range [15]. Schottky diode-based rectifiers are also used because of their low forward-voltage drop of about 150mV which makes it suitable for ultra-low power applications [16]. In this design, a 10-stage rectifier using Schottky diodes is proposed. It achieves an output voltage of 1.55V with an input voltage of 200 mV and it achieves an output voltage of 1.60V with an input voltage as low as 100 mV at 7.2 MHZ. The multiple stages were added in the design to boost up the voltage across the rectifier. However, Schottky diodes require additional fabrication steps because of the manufacturing incompatibility with the standard CMOS process which results in high cost. The design in [17] is based on the Villard voltage doubler circuit. The cross-coupled rectifier is another commonly used topology circuit due to its small on-resistance and dynamic compensating of the threshold voltage.

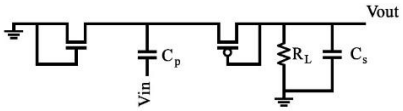

FIGURE 3. The conventional CMOS rectifier.

In this paper, two new IVC based CMOS rectifiers suitable for RF energy harvesting are proposed. The two designs reduce the threshold voltage of the transistors and deliver a high-rectified output voltage at an input frequency of 402MHz.

The rest of the paper is organized as follows: The two proposed rectifiers analysis and simulation results are presented in section II. The paper conclusion is presented in Section III.

II. PROPOSED DESIGN

A. N-STAGE IVC BASED RECTIFIER

Starting from the conventional CMOS rectifier shown in Fig. 3, the output voltage can be described as:

$$V_{out} = 2V_p - V_{drop} \tag{1}$$

where V_{out} is the output voltage, V_p is the peak RF input voltage and V_{drop} is the voltage losses due to mainly the threshold voltages of the nMOS and pMOS transistors.

Therefore, it is obvious from equation (1) that the threshold voltage is the main cause of the decrease of the output voltage. By reducing the threshold voltage, not only the output voltage is maximized but also it becomes suitable for low-power applications. In the case of using N-stage charge pump schemes, the voltage drop is multiplied by the number of stages as expressed in (2).

$$V_{out} = N(2V_p - V_{drop}) \tag{2}$$

However, the output voltage is lower in practice with the increase of the number of stages due to the increasing threshold voltage of the nMOS transistor which is another problem. In the standard CMOS process, the bulk of nMOS must be connected to the lowest potential (ground in this design). Therefore, with the increasing number of stages, the voltage

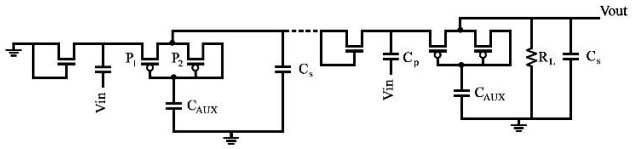

FIGURE 4. Proposed N-stage IVC based rectifier with nMOS transistors.

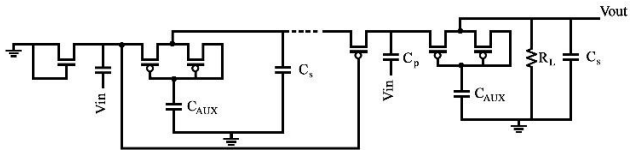

FIGURE 5. Proposed N-stage IVC based rectifier with pMOS transistors.

difference between the bulk and the source will increase which causes a higher threshold voltage. The relationship between the threshold voltage and the voltage difference V_{SB} is known as the body effect and it is given by:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\,|\emptyset_F| + V_{SB}} - \sqrt{2\emptyset_F}) \tag{3}$$

where γ is the body effect coefficient, $\emptyset_F$ is the surface potential of MOS transistor, V_{TH0} is the threshold voltage when $V_{SB} = 0$ and V_{SB} is the source-bulk voltage.

To tackle the first problem, an IVC scheme is used in the proposed design as shown in Fig. 4. It reduces V_{drop} by internally compensating for V_{thp} using an auxiliary pMOS added to the main pMOS and a capacitance C_{AUX} connected from the common gate node to ground for each stage. Therefore, the output voltage can be simplified as:

$$V_{out} = \frac{1}{2}(V_p + (V_{thp1} - V_{thp2}) + V_{AUX}) + V_p - V_{thn} \tag{4}$$

$$V_{out} = \frac{3}{2}V_p + \frac{1}{2}V_{AUX} + \frac{1}{2}(V_{thp1} - V_{thp2}) - V_{thn} \tag{5}$$

where V_{AUX} is the voltage across C_{AUX}.

And for N stages,

$$V_{out} = N(\frac{3}{2}V_p + \frac{1}{2}V_{AUX} + \frac{1}{2}(V_{thp1} - V_{thp2}) - V_{thn}) \tag{6}$$

Equation (6) shows that this arrangement can decrease V_{drop} by compensating the threshold voltages of pMOS transistors which results in enhancing the DC extraction ability. However, there is still the threshold voltage of nMOS transistors which is the second problem, not only because it degrades the output voltage, but also because of its contribution to e body effect problem.

One way to eliminate the body effect is by using deep n-well layer with the nMOS transistors. However, this requires an adopted fabrication process and cannot be implemented in standard CMOS [4].

The proposed solution to overcome this issue is to replace all the nMOS devices, except the first stage, by pMOS transistors as shown in Fig.5. The gate of the pMOS transistor is biased by the former stage. This scheme solves two problems. The first one is the body effect problem since we can connect

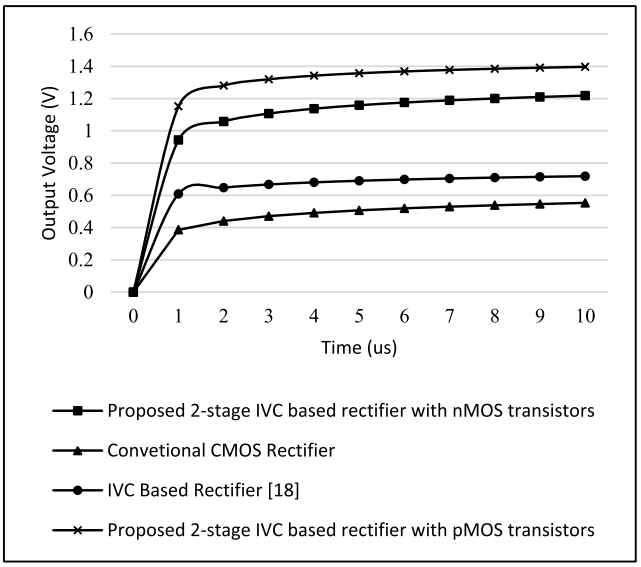

FIGURE 6. Comparison of different IVC based rectifiers with the proposed schemes in two stages.

the bulk to the source in the standard CMOS process. The second one is the threshold voltage which will be compensated by the former stage bias.

Therefore, the output voltage can be simplified as:

$$V_{out} = \frac{3}{2}V_p + \frac{1}{2}V_{AUX} + \frac{1}{2}\left(V_{thp1} - V_{thp2}\right) + (V_{bias} - V_{thn}) \tag{7}$$

And for N stages,

$$V_{out} = N\left(\frac{3}{2}V_p + \frac{1}{2}V_{AUX} + \frac{1}{2}\left(V_{thp1} - V_{thp2}\right) + (V_{bias} - V_{thn})\right) \tag{8}$$

III. SIMULATION RESULTS

The proposed design was simulated using Tanner TSPICE in 0.18μm TSMC CMOS technology. Drawn gate length and width of rectifier MOS transistors are 0.4μm and 40μm for n-MOS transistors and 0.4μm and 120μm for p-MOS transistors. Fig 6 demonstrates a comparison of different IVC based rectifiers with the proposed two stages schemes at input voltage 0.55V and at a frequency of 402MHz suitable for Medical Implant Communication Systems(MICS). It is clear from the plot that the proposed N stages IVC based deliver a higher voltage than the other schemes. Moreover, the proposed scheme with pMOS transistors deliver even a higher voltage than the proposed scheme with nMOS transistors which is expected from the previous equations. Fig 7 demonstrates a comparison of different stages of the proposed scheme with pMOS transistors. It is evident from the plot that more stages will produce a higher DC output voltage. The design was simulated for temperature analysis. Fig 8 is demonstrating a plot of IVC based rectifier with pMOS transistors in two stages for different temperatures. It is clear from the plot that the variation in the output voltage to the variation in the temperature is very small.

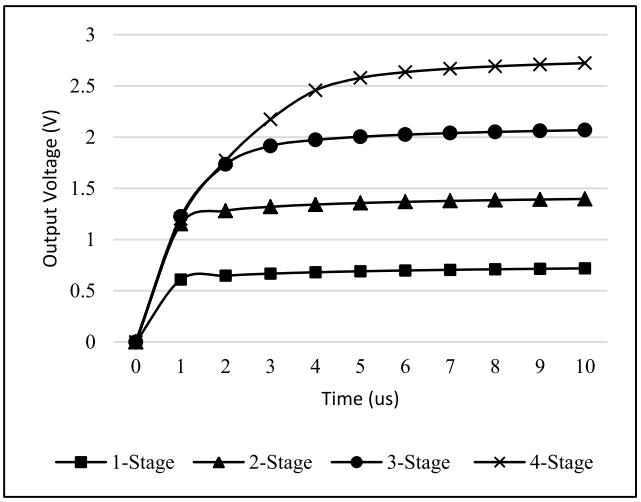

FIGURE 7. Comparison of different stages of the proposed IVC based rectifier using pMOS transistors.

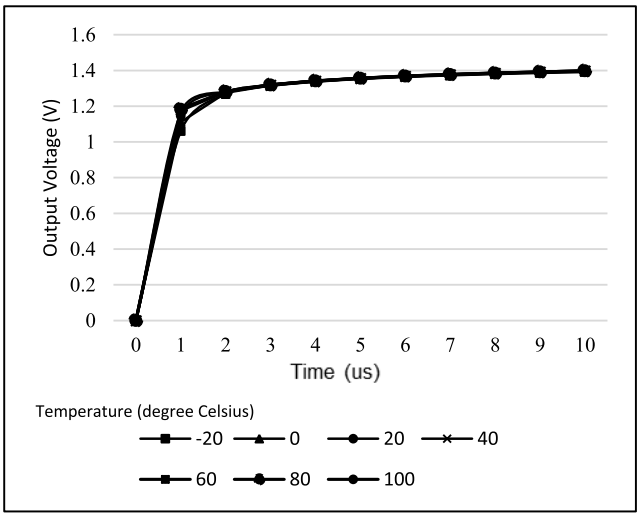

FIGURE 8. Temperature analysis for IVC based two stages rectifier using pMOS transistors.

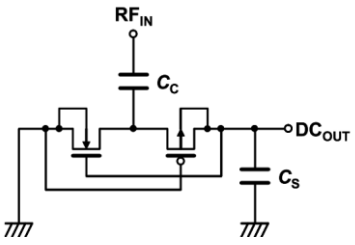

FIGURE 9. Self-Vth-cancellation (SVC) rectifier scheme [13].

A. IVC BASED RECTIFIER WITH SELF VTH CANCELLATION (SVC)

Self-Vth cancellation (SVC) shown in Fig. 9 is used in [12] to bias the gate by the output voltage of the rectifier. This configuration will decrease the threshold voltage of the transistor by the same amount of the output DC voltage.

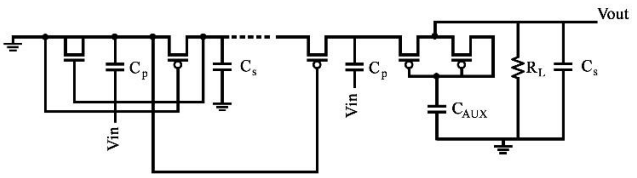

FIGURE 10. The proposed IVC based rectifier with SVC.

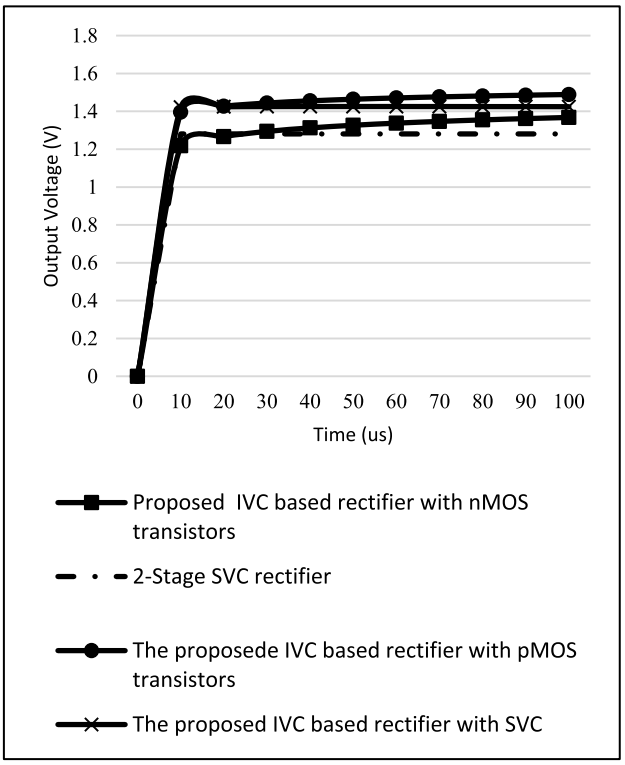

FIGURE 11. Comparison of the proposed rectifiers with other rectifier.

Although N-stage SVC could be used to boost the output voltage, a better solution is to cascade it with IVC circuits, as proposed in Fig. 10. The circuit of Fig. 10 was simulated with RF input voltage of 200mV at a frequency of 402MHz. The simulation results shown in Fig. 11 demonstrates a comparison of the proposed rectifier with the other rectifiers. It is clear from the plot that the proposed IVC based rectifiers are superior to the recent published rectifier.

IV. CONCLUSION

Two internal threshold voltage cancellation schemes for rectifiers used in RF energy harvesting have been proposed: N-stage IVC based rectifier and IVC based rectifier with self Vth cancellation (SVC). The developed rectifiers reduce the threshold voltage, solve the body effect problem, and deliver a high rectified output voltage at an input voltage of 200mV and frequency of 402MHz.

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