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# A New Single-Phase AC Voltage Converter With Voltage Buck Characteristics for Grid Voltage Compensation

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**ABSTRACT** Voltage sags and swells are the major problems of the power distribution system that arise due to uneven distribution of the single-phase and nonlinear loads. They severely degrade the power quality and may cause the failure of the equipment at the user's side. The voltage sag and swell issues are compensated by operating the AC voltage controllers with bipolar voltage gain characteristics. In these converters, high switching voltage and current, and a large number of switching devices are the main issues that cause unwanted power losses and result in reduced efficiency of the system. High voltage stresses may cause device failure due to the increase in *dv/dt* rating. The large count of switching devices results in high cost and high conversion losses. So here, we propose a novel AC converter with fewer switching devices that reduces switching voltage and current to have low conversion losses. The amplitude of the output is governed through the direct PWM control (DPWM) of one switch that controls the switching state of the other switch indirectly called indirect PWM control switch (IDPWM). The detailed analysis of the proposed converter is carried out to compare its performance with the existing converters. MATLAB/Simulink environment-based simulation results are proved through the experimental results obtained by developing a hardware prototype.

**INDEX TERMS** Bipolar voltage gain, power distribution system, power quality, PWM control, switching and conduction losses, switching voltage, voltage sag and swell.

## I. INTRODUCTION

Distributed energy resources (DRs) are an integral part of the power generating system realized with the decentralization approach. This approach ensures flexibility and reduces its dependency on the conventional power network. The growing rate of DRs is very fast nowadays [1], but along with enormous advantages, they have many technical limitations [2]. Their operation is more feasible if they operate in conventional (grid) mode as well as in autonomous (island) mode. So, their operating modes can be employed in micro-grids [3]. The operation of micro-grids in autonomous mode has many power quality concerns due to extensive use of the nonlinear loads, power electronic processors, and variation in the outputs of the renewable resources [4]. They are also caused by the rapid and uneven load distribution [5], [6]. The causes of power system disturbances can be split into three categories: the one is related to characteristics of the renewable resources; the second one is associated with solid-state electronic devices; the third one is linked with the reactive power demand. These types result in voltage fluctuation, harmonics, and voltage sags/swells, respectively. Several standards are developed to address and tackle these problems [7]. These issues can solve with proper monitoring and suitable compensation techniques [8].

The voltage sag/swell is one of the critical issues of the power system, especially for the sensitive loads connected at the consumer end. It also increases the unwanted line losses and tripping problem of the protective systems. A reduction in the line RMS voltage in the range of 90% to 10% results in voltage sag while the voltage swell has arisen once the line RMS voltage is boosted from 110% to 180% [9], [10].

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These two issues cause the under- and over-voltage problems, respectively. They can disturb the production progression and result in production shortage and economic loss. To maintain the power quality of the supplied voltage at the consumer end is the most challenging problem in the current power distribution scenario [11], [12]. Normally, these issues are resolved by employing the dynamic voltage restorers (DVRs) connected at the consumer's ends.

The DVRs can be realized with semiconductor devices realized on flexible ac transmission system (FACTS) devices, including the static-var compensators (SVC), unified power flow controllers (UPFC), and distributed static compensator (DSTATCOM) [13]. The series compensators based on FACTS devices are realized as a DVR to improve the transient and steady-state voltage stability [14]–[21]. It includes the voltage source converter (dc-to-ac) connected in series with the line to supply the required power for voltage compensation. Various control techniques are introduced for the proper operation of DVR, as reported in [22]–[24]. More emphasis is given on in-phase and pre-sage compensation [25]. However, these techniques employed high rating storage devices as their realization require high real power injection. Various techniques based on the energy optimization principle are developed for deep voltage sag having a longer duration [26]–[28]. They reduce the capacity of the energy-storing devices by lowering the required injected power during the compensation period. The voltage sag is characterized by a phase jump due to the difference in the impedance ratio of the line and source. So, the solution with the above strategies makes the situation worse. Besides, they facilitate the voltage regulation of the injected voltage without considering the power quality issues.

The problem of the limited capacity of the energy-storing devices is resolved in dual converters (ac-to-dc). They include two conversion stages, namely rectification, and inversion. They have the capability of regulating both the voltages and frequencies. They are realized with different topologies for various applications [29]–[32]. The rectification mode normally is realized with a diode converter to reduce the circuit cost and complexity. With this arrangement, the input current desirable in some applications cannot be controlled. The output conversion stage is implemented with dc-to-ac converters, where their output voltage and frequency are controlled through various PWM techniques. The presence of the dc-link capacitor is the main issue for the system's reliability. It also causes a poor power quality problem in the input current of the front-end rectifier, resulting in poor input power factor. Complex circuit arrangement and switching sequences are to be employed to tackle this problem. So, this power conversion topology is not favorable for voltage compensation as it is complex, and has high conversion losses and cost.

The direct ac-to-ac voltage compensating topologies are more attractive over sizeable dc-to-ac converters and dual converters due to simple conversion having no dc-link capacitors or energy storing devices. They get attention in the applications that only require voltage control. The traditional ac voltage controllers are implemented by using the thyristors as switching devices, but their output is highly distorted due to high harmonics. The power quality is improved in high switching frequency direct ac-to-ac converters implemented in buck, boost, and buck-boost fashion [19], [33]. They have a risk of short-circuiting due to current commutation issues [34], and their output can only be regulated with unipolar manners. So, they cannot be realized both for voltage sag and swell compensation. Four additional thyristors are used to change their unipolar voltage features to bipolar. This solution is not feasible as it increases the overall volume and conversion losses. It also faces a reliability problem. The Z-source converters are another approach for bipolar voltage characteristics, but they require the snubber circuits to avoid the problems initiated by the current commutation [35]. The safe commutation with bipolar voltage features is ensured in [36] by employing the switching cell arrangement. It uses a large count of passive components and switching devices. The conduction of the switching devices is reduced in the converter topology reported in [37], as shown in Fig. 1(a). This topology is realized with six MOSFET-diode pairs, and at any time during its operation, only two pairs conduct that lowers the conduction losses. However, its gating sequences are non-symmetrical during its non-inverting and inverting operation. Also, its operating modes can only be realized in buck-boost fashion. So, its switching losses are high due to high switching voltages and currents. A new current commutation strategy is introduced in [38] by changing the bidirectional current conduction features of the MOSFETs to unidirectional. This is achieved by reverse biasing its body diode with a series connection of another diode having abrupt recovery characteristics. Besides, their operation in inverting and non-inverting modes are non-identical that makes the switching scheme complex, but its non-inverting operation has low switching voltage and switching current. All its operating modes are realized with the conduction of three MOSFET-diode pairs (see Fig. 1(b)), resulting in high conduction losses as in [37]. Its inverting mode can only be realized in a buck-boost manner that has the problem of high switching voltage and current. This problem is tackled in [39], [40] by lowering the switching voltages and currents to reduce the switching losses. The inverting and non-inverting operating modes are identical, but their conduction losses remain the same as in [38], as each of their operating modes requires the conduction of three MOSFET-diode pairs

To overcome the drawbacks suffered by [37], [38], this research, therefore, introduces an alternate ac-to-ac buck topology (see Fig. 2) having inverting and non-inverting features with the conduction of the fewer switching devices (two MOSFET-diode pairs) that reduce its footprint. The unwanted switching and conduction losses are also reduced with low switching voltage and currents. Its all-operating modes have similar operating behavior. Low count of the switching devices results in low losses and low cost as each controlled switching device requires one isolated dc voltage

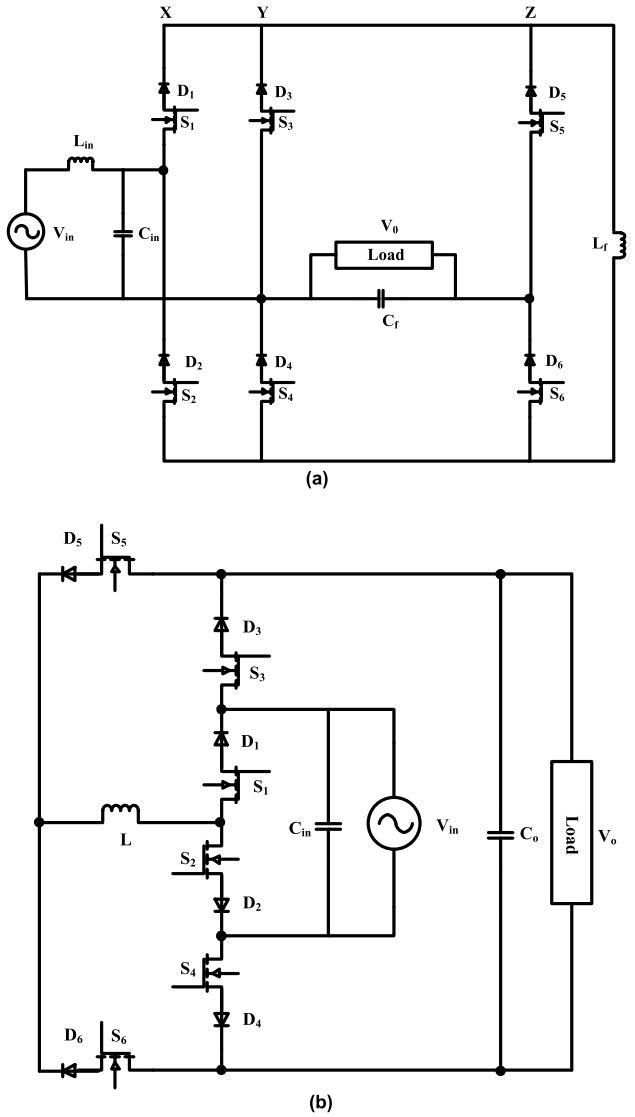


**FIGURE 1.** A single-phase AC-to-AC converter proposed in (a) [37] and (b) [38].

source and one gate driving circuit. Their cost is higher than that of the controlled switch. The effectiveness of the proposed topology is proved through the comparison of the performance parameters with that of the existing topologies for a voltage gain of '0.5'. The analysis demonstrates that switching voltage and switching current of the proposed topology is lesser 50 % than that of the converter reported in [37] and the inverting operation of converter in [38]. This results in lower conversion losses.

The organization of this article is as follows. Section II demonstrates the proposed topology with its operating modes. Its dynamic modeling is formulated in Section III, and comparison with existing topologies is given in Section IV. Section V describes the power quality of the output voltage. The validity of the developed topology is explored through the simulation and practical results in Section VI. Section VII highlights the conclusion.

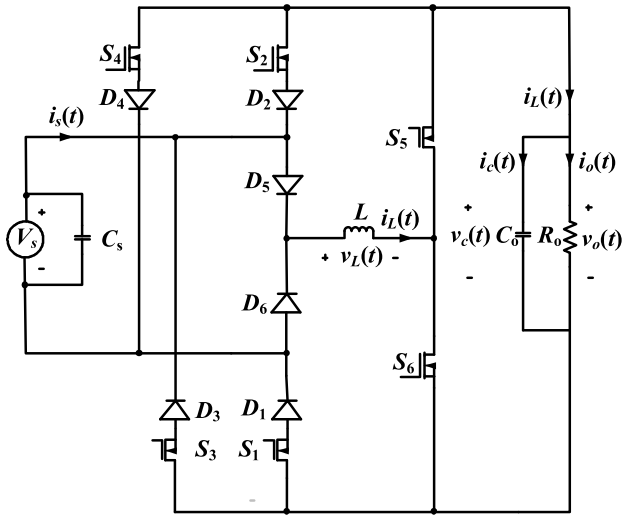


**FIGURE 2.** The proposed converter configuration.

## II. THE PROPOSED CONVERTER CONFIGURATION

Fig. 2 depicts the electrical circuit diagram of the proposed topology that may be employed as a dynamic voltage restorer (DVR) in the power system to mitigate the voltage disturbances such as voltage sags and swells. It is made up of only six diodes and MOSFETs pairs along with one inductor ($L$) and two capacitors ($C_S$ and $C_o$), for input and output, respectively. The power MOSFET is chosen as a switching unit to get the advantage of its low on-state resistance and high switching speed. However, its body diode limits its switching speed due to its poor reverse characteristics. This problem is tackled by connecting a fast recovery diode in its series that changes its bidirectional current conduction characteristics to unidirectional. This arrangement also increases its operating reliability as it avoids the problem of current commutation. During all its operating modes, the input power is transferred to load through one filtering inductor and two diodes and MOSFETs. It also ensures the no current commutation issue initiated by switching devices operated in a complementary manner. So, owning to the absence of these issues, the requirement of the blanking time or snubbing circuits is eliminated. The switching frequency of the high-frequency switching devices is selected high; therefore, the instantaneous value of the input voltage is assumed to be quasi-constant during each switching interval.

The operating principle of the suggested topology is split into non-inverting and inverting modes, as tabulated in Table 1, which also gives the detail of the switching algorithm and the operating modes.

### A. OPERATION IN NON-INVERTING MODE

The voltage gain of the output voltage is required to be positive for voltage sag compensation so that the injected voltage should be added in the input voltage to increase the overall voltage at the required level. The low and high-frequency switching signals to achieve in-phase voltage are shown in Fig. 3(a). The switching signals $x_1$ and $x_2$ are

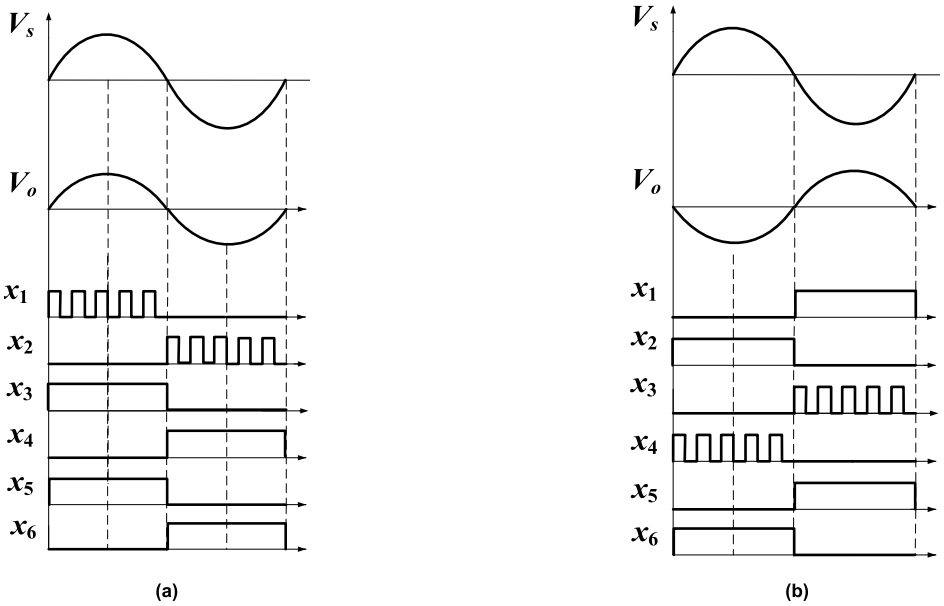


**FIGURE 3.** PWM switching schemes for (a) non-inverting operation and (b) inverting operation.

**TABLE 1.** Modes of operation.

| Mode | Line Voltage Polarity | Output Voltage Polarity | Proposed Converter Application |
|---|---|---|---|
| A | Positive | Positive | Sag Compensator |
| B | Negative | Negative | Sag Compensator |
| C | Positive | Negative | Swell Compensator |
| D | Negative | Positive | Swell Compensator |

high-frequency PWM signals that control the output voltage through the duty cycle control ($k$) with respect to switching period ($T$) in the positive and negative input voltage, respectively. The control signals ($x_1$ to $x_6$) govern the switching behavior of switches $S_1$ to $S_6$. How the in-phase output voltage regulation is achieved through the duty cycle control is explored in mode 1 and 2 with the help of the current conduction path highlighted in Figs. 4(a), (b), and (c), (d) during the positive and negative input voltage, respectively.

**Mode 1:** This mode is initiated during the positive input voltage with the PWM switching of the controlled switch $S_1$. During the PWM time interval [0-$kT$], the current conducted by switches $S_1$, $S_5$, and diodes $D_1$, $D_5$ transfers the power from input to output, as highlighted in Fig. 4(a). The controlled switch $S_3$ always remains in the on-state to avoid the current interruption of the filtering inductor. However, it cannot conduct as the diode $D_3$ is reverse biased at input voltage level $V_s$. It becomes forward bias in the time interval [$kT$-$T$] once the PWM switch $S_1$ is turned off. During this period, the stored power of the filtering inductor is delivered to load via a highlighted path formed by switches $S_3$, $S_5$ and diodes $D_3$ and $D_5$, as demonstrated in Fig. 4(b). The switching of the controlled switch $S_1$ governs the turn-on and turn-off states of the switch $S_3$.

**Mode 2:** In the negative half cycle of the line voltage, during the PWM interval [0-$kT$] of switch $S_2$, the source power is supplied to the load through the path of Fig. 4(c) that is developed with the conduction of the semiconductor devices $S_2$, $S_6$, $D_2$, and $D_6$. The turn-on switch $S_4$ is in non-conducting states as the diode $D_4$ is in reverse blocking mode with '$V_s$' reverse voltage. It only conducts in the time interval [$kT$-$T$] once the PWM control switch $S_2$ changes its operating state from 'on' to 'off' to isolate the line from the load. The stored energy of the filtering inductor is released toward output once a current conducting path is developed due to the conduction of the semiconductor devices $S_4$, $S_6$, $D_4$, and $D_6$, as exposed in Fig. 4(d).

### B. OPERATION IN INVERTING MODE

The problem of the voltage swell is tackled if the voltage gain of the output voltage is negative so that injected voltage can be subtracted from the line voltage to decrease the overall voltage at the safe level. The detail of its operation is discussed in mode 3 and mode 4 for positive and negative line voltage, respectively.

**Mode 3:** The inverting output voltage during the positive value of the line voltage is accomplished with the PWM control of switch $S_4$. During its PWM switching interval [0-$kT$], the switching devices $S_4$, $S_6$, $D_4$, and $D_5$ facilitate the output to connect with the input through filtering inductor '$L$' as shown in Fig. 4(e). The controlled switch $S_2$ remains in the on position to avoid the problem of the current interruption of the filtering inductor. Its series-connected diode $D_2$ remains reverse biased until the source is isolated from the circuit in the PWM switching interval [$kT$-$T$]. During this time interval, the stored energy in the filtering inductor is transmitted toward the output via the path facilitated by the conducting semiconductor devices $S_2$, $S_6$, $D_2$, and $D_5$ as can be viewed in Fig. 4(f). The turn on and off switching of the controlled switch $S_2$ is governed through the forward and reverse biasing

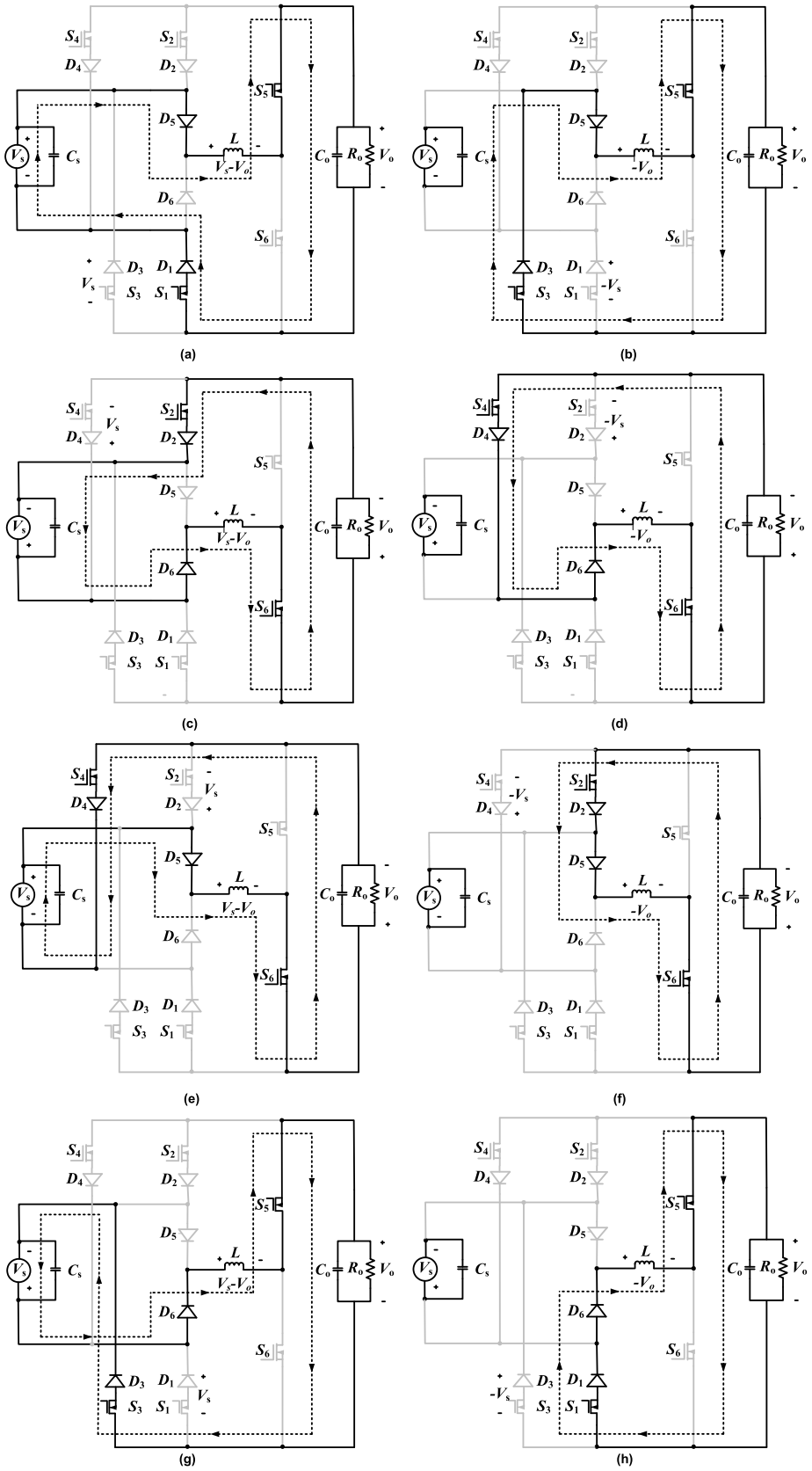


**FIGURE 4.** Current highlighted paths during (a) to (d) non-inverting operation and (e) to (h) inverting operation.

of its series-connected diode $D_2$ that is controlled with the switching action of the controlled switch $S_4$.

**Mode 4:** The high-frequency PWM operation of the controlled switch $S_3$ realizes the buck operation of the proposed topology in inverting mode with the negative input voltage. During the PWM turn-on interval [0-$kT$], the input power is transmitted towards the output through by current conducting path made with the turn-on operation of the semiconductor devices $S_3$, $S_5$, $D_3$ and $D_6$ as depicted in Fig. 4(g). The controlled switch $S_1$ maintains its off state until the diode $D_1$ becomes forward biased in the turn off interval [$kT$-$T$] of the controlled switch $S_3$. In this interval, the energy stored by the inductor is brought at the output side via the highlighted current conducting path formed by the semiconductor devices $S_1$, $S_5$, $D_1$, and $D_6$ as shown in Fig. 4(h).

## III. DYNAMIC MODELING OF THE PROPOSED TOPOLOGY

It is clear from the analysis of Section II (see also Fig. 4) that in each switching interval, two transistors and two diodes conduct to realize the required operation. The inductor current $i_L(t)$ and capacitor voltage $v_o(t) = v_C(t)$ are chosen as the state variables to develop the dynamic modeling of the proposed circuit during non-inverting and inverting operation with the positive and negative input voltage.

Assume that $r_d$, $r_m$ and $r_L$ represent the internal resistance of the conducting diode, the conducting transistor, and the filtering inductor, respectively. As all diodes and transistors have similar characteristics, so their internal resistances are equal. The sum of these internal resistances of the filtering inductor and the switching devices may be added as they are connected in series in each operating mode. That is to say

$$R_L = r_L + 2r_m + 2r_d$$

where $R_L$ represents the total resistance offered by the current conduction path during each operating mode.

### A. DYNAMIC MODELING DURING NON-INVERTING OPERATION

The dynamic behavior for the non-inverting operation of the proposed topology for positive input voltage during the PWM turn-on and turn-off intervals can be derived by applying the KVL in Figs. 4(a) and (b) respectively.

$$L\frac{di_L(t)}{dt} = -ki_L(t)R_L - kv_o(t) + v_s(t) \quad (1)$$

$$L\frac{di_L(t)}{dt} = -(1-k)i_L(t)R_L - (1-k)v_o(t) \quad (2)$$

In the same way, the application of KCL at the output node of Figs. 4(a) and (b) respectively gives

$$C_o\frac{di_o(t)}{dt} = ki_L(t) - ki_o(t) \quad (3)$$

$$C_o\frac{di_o(t)}{dt} = (1-k)i_L(t) - (1-k)i_o(t) \quad (4)$$

where

$$i_o(t) = \frac{v_o(t)}{R_o}$$

The dynamic behavior in matrix form during PWM turn-on and turn-off intervals using (1) to (4), thus results in

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_o} & \frac{-1}{R_oC_o} \end{bmatrix}\begin{bmatrix} ki_L(t) \\ kv_o(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s(t) \quad (5)$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_o} & \frac{-1}{R_oC_o} \end{bmatrix}\begin{bmatrix} (1-k)i_L(t) \\ (1-k)v_o(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_s(t) \quad (6)$$

The state-space average modeling of the non-inverting operation is developed in (7) by adding the right-hand side of (5) and (6).

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_o} & \frac{-1}{R_oC_o} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{k}{L} \\ 0 \end{bmatrix} v_s(t) \quad (7)$$

Similarly, the dynamic behavior in matrix form can be realized during PWM turn-on and turn-off intervals for its non-inverting operation for negative input voltage and is expressed by

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_o} & \frac{-1}{R_oC_o} \end{bmatrix}\begin{bmatrix} ki_L(t) \\ kv_o(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s(t) \quad (8)$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_o} & \frac{-1}{R_oC_o} \end{bmatrix}\begin{bmatrix} (1-k)i_L(t) \\ (1-k)v_o(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_s(t) \quad (9)$$

This results in the state-space averaged model for this operation as

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_o} & \frac{-1}{R_oC_o} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{k}{L} \\ 0 \end{bmatrix} v_s(t) \quad (10)$$

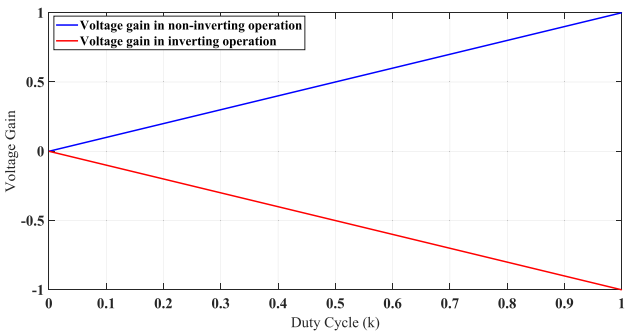


**FIGURE 5.** Relationship between voltage gain and duty cycle.

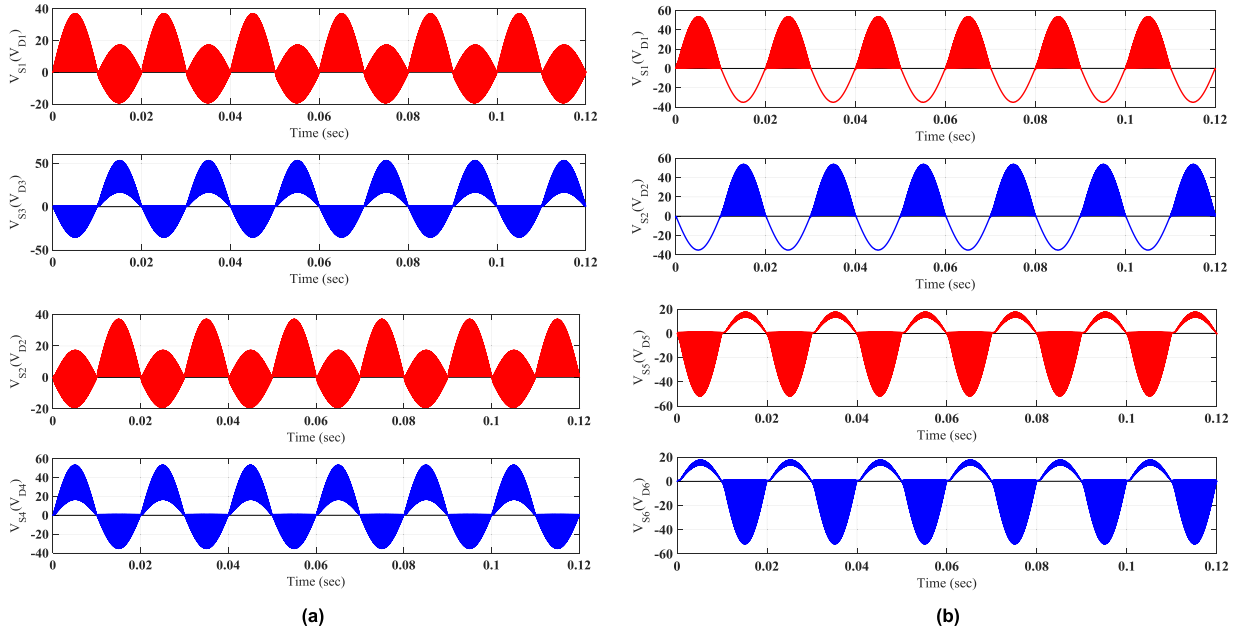


**FIGURE 6.** Switching voltage waveforms offered by (a) the proposed topology and (b) the converter in [37].

### B. DYNAMIC MODELING DURING INVERTING OPERATION

By following the same pattern of calculations, (11) and (12) show the inverting state-space representation of the inductor current and capacitor voltage for positive and negative input voltage, respectively.

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{1}{L} \\ \frac{-1}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} ki_L(t) \\ kv_o(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s(t) \quad (11)$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{1}{L} \\ \frac{-1}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} (1-k)i_L(t) \\ (1-k)v_o(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_s(t) \quad (12)$$

The average states-space modeling of the inverting operation is realized by (13).

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{1}{L} \\ \frac{-1}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{k}{L} \\ 0 \end{bmatrix} v_s(t) \quad (13)$$

In the steady-state condition, the voltage and current transfer ratio of the proposed topology with the non-inverting and inverting operation are realized in (14) and (15) by ignoring the internal resistances ($r_L$, $r_m$, $r_d$) and the derivative terms of (7) and (13).

$$\begin{cases} V_o = kV_s \\ I_o = I_L \end{cases} \quad (14)$$

$$\begin{cases} V_o = -kV_s \\ I_o = -I_L \end{cases} \quad (15)$$

From (14) and (15), it is clear that the voltage gain is a function of duty cycle '$k$' for non-inverting and inverting operation, ignoring the internal resistances of the switching devices and filtering components. The variation in the voltage gain with respect to duty cycle control $k$ is shown in Fig. 5.

## IV. ANALYSIS AND COMPARISON

This section includes a detailed analysis of the proposed topology in terms of switching voltage and currents, conduction, and switching losses. These performance parameters are then compared with the existing topologies in [37], [38].

### A. SWITCHING VOLTAGES

The high-frequency switching voltages determine the switching losses. The switching voltage of the high-frequency switching devices $S_1$, $S_2$, $S_3$, $S_4$, $D_1$, $D_2$, $D_3$, and $D_4$ are depicted in Fig. 4. During the non-inverting operation with the positive input voltage, for the voltage gain of '0.5', the controlled switches $S_1$ and $S_3$ operate in DPWM and IDPWM modes having the switching voltage of '$+V_S$' and '$-V_S$' respectively. In the negative interval of the input voltage, this control scheme is shifted to the controlled switches $S_2$ and $S_4$ with the switching voltage of '$+V_S$' and '$-V_S$' respectively. In the same manner, during the inverting operation with the positive input voltage, the controlled switches $S_4$ and $S_2$ operate as DPWM and IDPWM control with switching voltage of '$+V_S$' and '$-V_S$'. This control is transferred to the switches $S_3$ and $S_1$ during the period of the negative input voltage with the switching voltage of '$+V_S$' and '$-V_S$'. It means that once a controlled switch operates as a DPWM

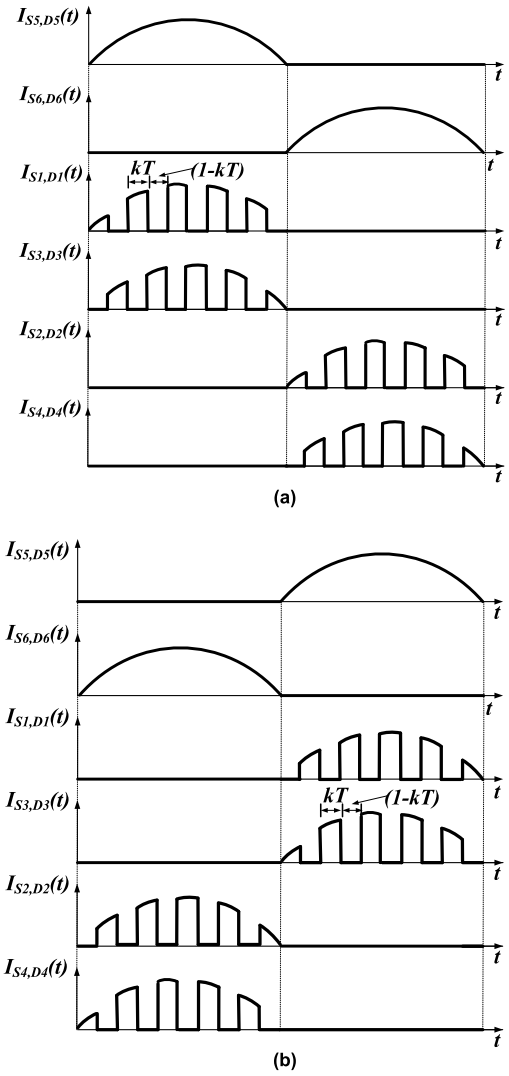


**FIGURE 7.** Switching current waveforms during (a) non-inverting operation and (b) inverting operation.

manner, its series-connected diode is always forward bias. Then switching voltage between drain and source ($V_{ds}$) is changed '$V_S$' to '0' and '0' to '$V_S$' during its turn-on and turn-off PWM intervals, respectively. In the IDPWM control operation, the series-connected MOSFET is always in on state to ensure continuous inductor's current, the reverse switching voltage ($V_{dr}$) of the hyper-fast diode is switched from '$V_S$ ' to '0' and '0' to '$V_S$' during its turn-on and turn-off PWM intervals respectively. Therefore, the switching voltage of the switching devices during all operating modes of the proposed topology never exceeds the input voltage level. This ensures the low switching losses and low *dv*/*dt* problem. Also, these voltage stresses are independent of the voltage gain of the converter.

The switching voltage in all the operating modes of [37] and the inverting mode of [38] is increased to $V_s + V_o$. It depends on the voltage gain of the converter as the output voltage is directly related to the voltage gain. A comparison of the switching voltages in the form of MATLAB/Simulink based simulation results offered by the proposed topology and the converter in [37], for a voltage gain of '0.5' is presented in Fig. 6, thus validating the superiority of the proposed topology in terms of switching voltage.

### B. SWITCHING CURRENTS

As there is no interruption in the inductor current, so the peak value of the inductor current passes through the switching devices during their conduction periods. The switching current waveforms of the conducting devices of all operating modes are depicted in Fig. 7(a) and (b) by ignoring the ripple current.

Fig. 7(a) depicts the waveforms of the switching currents during the non-inverting operation of the input voltage. As can be viewed from Figs. 4(a) and (b) that switching devices $S_5$, $D_5$ and $S_2$, $D_2$, $S_4$, $D_4$ remain in the conducting and non-conducting states throughout the positive half cycle of the input voltage, respectively. Therefore, the current conducted by the turn-on and turn-off devices is equal to instantaneous inductor current and zero, respectively. As the pair of the switching devices, $S_1$-$D_1$ and $S_3$-$D_3$ operate in DPWM and IDPWM manner, so they conduct the current in a complementary fashion, as can be seen in Fig 7(a).

During the negative half cycle of the line voltage, the switching devices $S_6$, $D_6$ remain on, and $S_5$, $D_5$ remain off. The switching devices $S_2$-$D_2$ and $S_4$-$D_4$ operate in the DPWM and IDPWM manner.

The average values of the switching currents during non-inverting operation, thus, can be calculated from (16) to (18).

$$\begin{cases} I_{S5,D5}(avg) = \dfrac{1}{2\pi}\displaystyle\int_0^{\pi} I_{L(p)} sin(\omega t) d\omega t = \dfrac{I_{L(p)}}{\pi} \\ I_{S6,D6}(avg) = \dfrac{1}{2\pi}\displaystyle\int_{\pi}^{2\pi} -I_{L(p)} sin(\omega t) d\omega t = \dfrac{I_{L(p)}}{\pi} \end{cases} \tag{16}$$

$$\begin{cases} I_{S1,D1}(avg) = \dfrac{1}{2\pi}\displaystyle\int_0^{\pi} kI_{L(p)} sin(\omega t) d\omega t = \dfrac{kI_{L(p)}}{\pi} \\ I_{S3,D3}(avg) = \dfrac{1}{2\pi}\displaystyle\int_0^{\pi} (1-k) I_{L(p)} sin(\omega t) d\omega t \\ = \dfrac{(1-k)I_{L(p)}}{\pi} \end{cases} \tag{17}$$

$$\begin{cases} I_{S2,D2}(avg) = \dfrac{-1}{2\pi}\displaystyle\int_{\pi}^{2\pi} kI_{L(p)} sin(\omega t) d\omega t = \dfrac{kI_{L(p)}}{\pi} \\ I_{S4,D4}(avg) = \dfrac{-1}{2\pi}\displaystyle\int_{\pi}^{2\pi} (1-k) I_{L(p)} sin(\omega t) d\omega t \\ = \dfrac{(1-k)I_{L(p)}}{\pi} \end{cases} \tag{18}$$

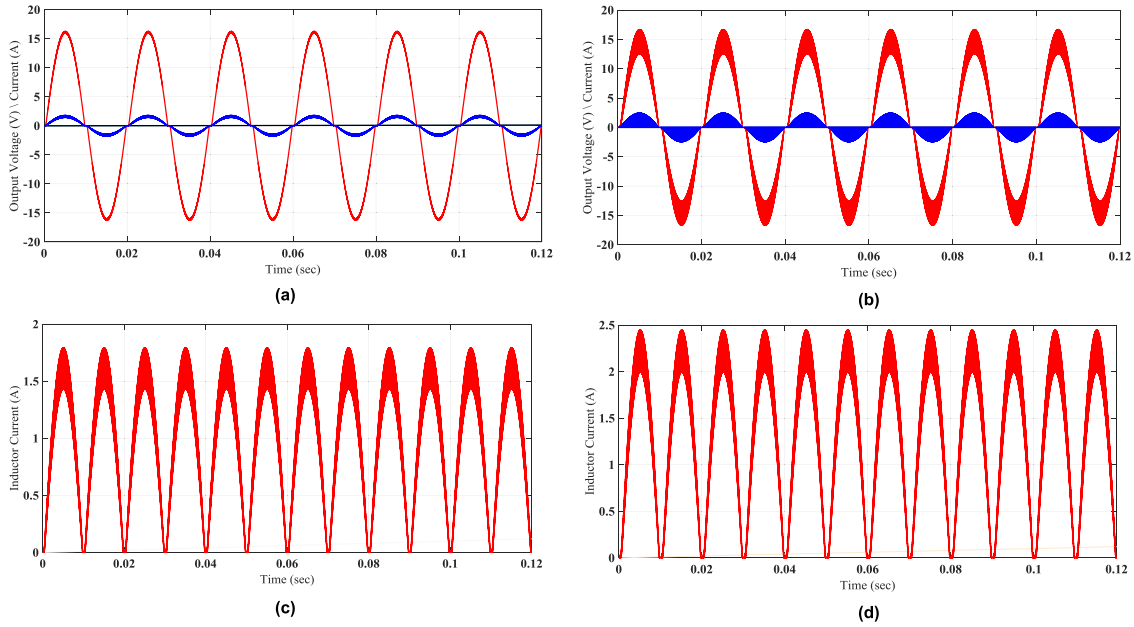


**FIGURE 8.** Input and inductor current waveforms offered by (a) & (c) the proposed topology and (b) & (d) the converter in [37].

And the RMS values of the switching currents are calculated from (19) to (21).

$$\begin{cases} I_{S5,D5}(rms) = \sqrt{\dfrac{1}{2\pi}\displaystyle\int_{0}^{\pi}\left(I_{L(p)}sin(\omega t)\right)^2 d\omega t} = \dfrac{I_{L(p)}}{2} \\ I_{S6,D6}(rms) = \sqrt{\dfrac{-1}{2\pi}\displaystyle\int_{\pi}^{2\pi}\left(I_{L(p)}sin(\omega t)\right)^2 d\omega t} = \dfrac{I_{L(p)}}{2} \end{cases} \tag{19}$$

$$\begin{cases} I_{S1,D1}(rms) = \sqrt{\dfrac{1}{2\pi}\displaystyle\int_{0}^{\pi}\left(kI_{L(p)}sin(\omega t)\right)^2 d\omega t} = \dfrac{kI_{L(p)}}{2} \\ I_{S3,D3}(rms) = \sqrt{\dfrac{1}{2\pi}\displaystyle\int_{0}^{\pi}\left((1-k)I_{L(p)}sin(\omega t)\right)^2 d\omega t} \\ = \dfrac{(1-k)I_{L(p)}}{2} \end{cases} \tag{20}$$

$$\begin{cases} I_{S2,D2}(rms) = \sqrt{\dfrac{-1}{2\pi}\displaystyle\int_{\pi}^{2\pi}\left(kI_{L(p)}sin(\omega t)\right)^2 d\omega t} = \dfrac{kI_{L(p)}}{2} \\ I_{S4,D4}(rms) = \sqrt{\dfrac{-1}{2\pi}\displaystyle\int_{\pi}^{2\pi}\left((1-k)I_{L(p)}sin(\omega t)\right)^2 d\omega t} \\ = \dfrac{(1-k)I_{L(p)}}{2} \end{cases} \tag{21}$$

where $I_{L(p)}$ is the peak value of the inductor current and is computed by

$$I_{L(p)} = \frac{\sqrt{2}P_o}{V_o} \tag{22}$$

Similarly, the switching current waveforms during the inverting operation of the proposed topology are shown in Fig. 7(b). It should be noted that DPWM and IDPWM control of the switching devices $S_1$ and $S_3$ in non-inverting operation during positive input voltage is shifted to switching devices $S_4$ and $S_2$, respectively. During this mode, the current through the switching devices $S_5$-$D_5$ and $S_6$-$D_6$ becomes zero and instantaneous inductor current, respectively. In the same way for the inverting operation during negative input voltage, the DPWM and IDPWM switching control is employed to the switching devices $S_3$ and $S_1$, respectively.

The mathematical calculations performed regarding switching currents can be validated by simulation results as well. The peak value of the switching currents is similar to the peak value of the inductor current which depends on the peak value of the output current and the value of the duty cycle control. In a voltage step-down operation implemented with buck mode, the peak value of the inductor current is the same as the peak value of the output current, i.e., $I_{L(p)} = I_{o(p)}$. But, in the buck-boost mode of [37], [38] for the voltage step-down operation with the same voltage gain, the inductor peak current is computed as $I_{L(p)} = I_{o(P)}/(1-k) = 1.5I_{o(p)}$. Fig. 8 compares the simulation results of the inductor current of the proposed topology with that of the converter in [37] for a voltage gain of '0.5'. As already pointed out that the values of the switching currents are similar to their corresponding inductor currents. Therefore, the peak value of the switching currents in the proposed converting topology is low as its peak inductor current is low. This is confirmed from the simulation results of Fig. 9. It can be seen from Fig. 9 that the peak value in the simulation current waveforms of the proposed topology is 1.6 A, but in the simulation current waveforms of [37], their peak values are raised to 2.4 A.

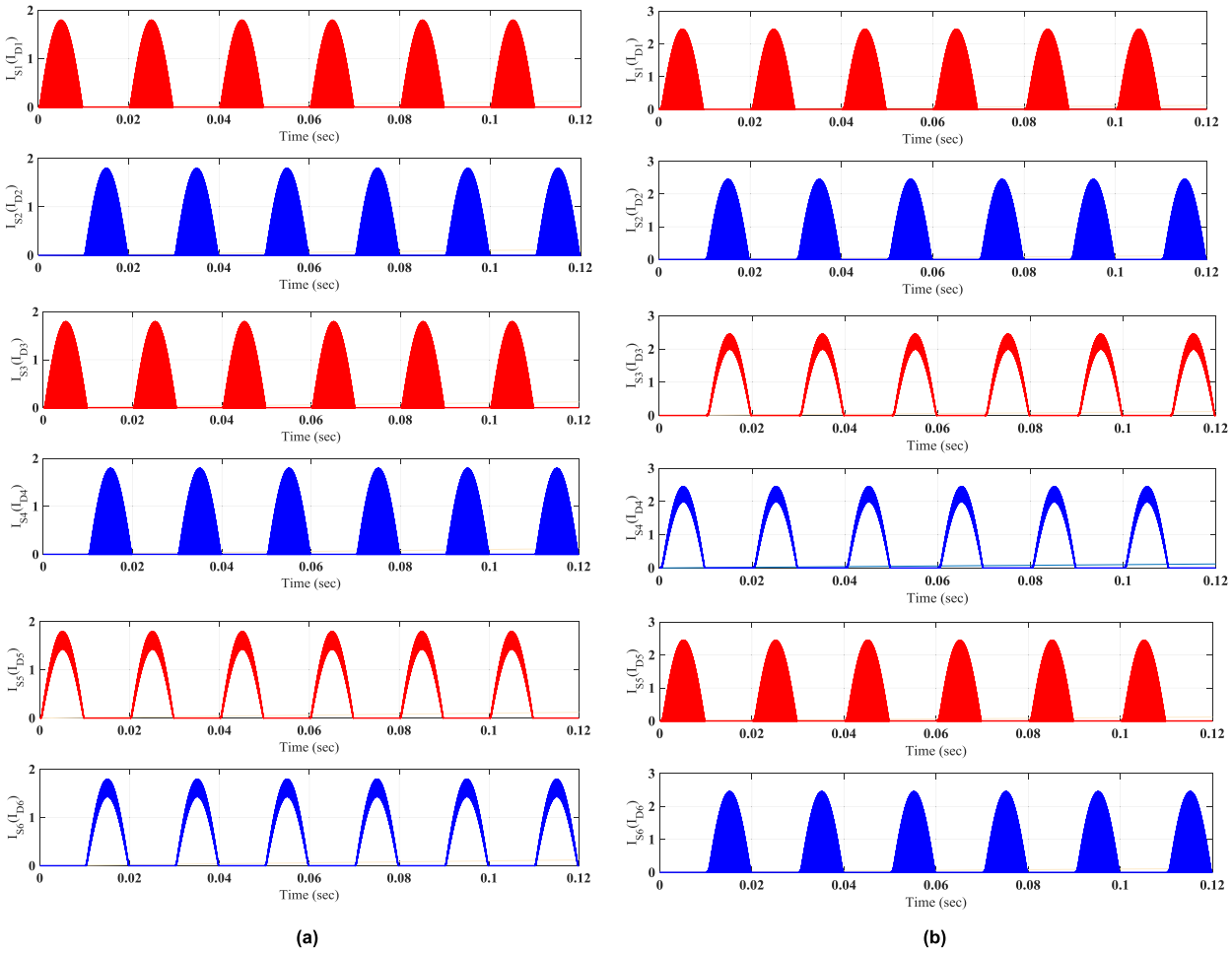


**FIGURE 9.** Switching currents offered by (a) the proposed topology and (b) the converter in [37].

### C. POWER LOSSES

The conversion losses include the power losses of the filtering components, conduction losses, blocking losses, and switching losses. The power losses of the filtering inductor and capacitor depend on their parasitic resistances, and blocking losses are directly related to the leakage current of the switching devices. These losses are normally negligible. The major contribution of the conversion losses comes from conduction and switching losses.

#### 1) CONDUCTION LOSSES

These losses occur during the current conduction intervals of the switching devices. They are the sum of the losses caused by the MOSFETs and diodes. These losses depend on their conduction currents ($I_m$, $I_d$), internal resistances ($r_m$, $r_d$), and forward voltage ($V_f$) of the switching devices. The conduction losses of a MOSFET and a diode are computed in (23) and (24), respectively.

$$P_{C(m)} = \frac{1}{T}\int_0^T r_m I_m^2 dt \tag{23}$$

$$P_{C(d)} = \frac{1}{T}\int_0^T \left(V_f I_d + r_d I_d^2\right) dt \tag{24}$$

As already remarked, in each switching interval of all operating modes of the proposed topology, two diodes and two MOSFETs conduct the current $I_{L(p)}$ that is equal to peak output current $I_{o(p)}$. The total conduction losses of a MOSFET and a diode operating at low output frequency can be realized in (25) by assuming the sinusoidal output current.

$$P_C = \frac{V_f I_{o(p)}}{\pi} + \frac{I_{o(p)}^2 (r_m + r_d)}{4} \tag{25}$$

The conduction losses of the DPWM and IDPWM controlled devices are formulated in (26) and (27), respectively.

$$P_C = \frac{kV_f I_{o(p)}}{\pi} + \frac{kI_{o(p)}^2 (r_m + r_d)}{4} \tag{26}$$

$$P_C = \frac{(1-k)V_f I_{o(p)}}{\pi} + \frac{(1-k)I_{o(p)}^2 (r_m + r_d)}{4} \tag{27}$$

Remember that in each cycle of the input voltage, two controlled switches operate at a low output frequency, two

as DPWM and two as IDPWM manner. Therefore, the total conduction losses of all switching devices in one cycle of the input voltage are computed in (28).

$$P_{C(proposed)} = \frac{4V_f I_{o(p)}}{\pi} + I^2_{o(p)}(r_m + r_d) \tag{28}$$

However, the total conduction losses of the converter in [38] during inverting buck mode, and non-inverting buck-boost mode of [37] were calculated to be in (29) and (30) respectively.

$$P_{C[38]} = \frac{6V_f I_{o(p)}}{\pi(1-k)} + \frac{3I^2_{o(p)}(r_m + r_d)}{2(1-k)^2} \tag{29}$$

$$P_{C[37]} = \frac{4V_f I_{o(p)}}{\pi(1-k)} + \frac{I^2_{o(p)}(r_m + r_d)}{(1-k)^2} \tag{30}$$

Therefore, the proposed topology has the advantage of low power losses in the conduction intervals of the semiconductor devices, due to low conduction currents.

### 2) SWITCHING LOSSES

The switching characteristics of a MOSFET and a diode are nonlinear, thus making the calculations complex. This issue is tackled by applying the linear approximation during their rising and falling intervals. These losses in a MOSFET are directly linked with the switching frequency ($f_s$), switching voltage ($V_{ds}$), current ($I_{ds}$), turn on ($t_r$), and off ($t_f$) time intervals and output capacitance ($C_{os}$) [41]. The switching losses of a MOSFET are approximated by ignoring the effect of the output capacitance.

$$P_{sw(m)} = \frac{1}{8} V_{ds} I_{ds} f_s (t_r + t_f)$$

The switching losses of a diode are normally ignorable during its turn-on transition, but its turn-off transition ($t_{rr}$) contributes to these losses [41] as depicted in (31). These losses are related to maximum reverse current ($I_{rm}$), reverse voltage ($V_{dr}$), switching frequency ($f_s$) and reverse recovery time ($t_{rr}$).

$$P_{sw(d)} = \frac{1}{2\pi} V_{dr} I_{rm} f_s t_{rr} \tag{31}$$

In each cycle of the input voltage, two MOSFETS and two diodes operate at a high frequency, so the total switching losses in this interval for the suggested work and converting topology reported in [38] during the inverting operation, and in [37] during the non-inverting and inverting operation are realized in (32) and (33) respectively.

$$P_{sw(proposed)} = \frac{1}{4} V_{s(p)} I_{o(p)} f_s (t_r + t_f) + \frac{1}{\pi} V_{s(p)} I_{r(p)} f_s t_{rr} \tag{32}$$

$$P_{sw([38])} = \frac{1}{4(1-k)} (V_{s(p)} + V_{o(p)}) I_{o(p)} f_s (t_r + t_f) + \frac{1}{\pi} (V_{s(p)} + V_{o(p)}) I_{r(p)} f_s t_{rr} \tag{33}$$

For any value of the duty ratio, the switching losses of the proposed topology are low, as it has low switching voltage and current.

**TABLE 2. Comparison of performance parameters with 50% duty cycle control.**

| Performance Parameters | | Proposed Topology | Topology in [38] | Topology in [37] |
|---|---|---|---|---|
| Switching Voltages | | $V_s(t)$ | $\frac{3}{2}V_s(t)$ | $\frac{3}{2}V_s(t)$ |
| Switching Currents | Avg. | $\frac{I_L}{2\pi}$ | $\frac{I_L}{2\pi}$ | $\frac{I_L}{2\pi}$ |
| | RMS | $\frac{I_L}{4}$ | $\frac{I_L}{4}$ | $\frac{I_L}{4}$ |
| Conduction Losses | | $\frac{4V_f I_{o(p)}}{\pi}$ $+I^2_{o(p)}(R_m + R_d)$ | $\frac{9V_f I_{o(p)}}{\pi}$ $+\frac{27I^2_{o(p)}(R_m + R_d)}{8}$ | $\frac{6V_f I_{o(p)}}{\pi}$ $+\frac{9I^2_{o(p)}(R_m + R_d)}{4}$ |
| Switching Losses | | $\frac{1}{4}V_{s(p)} I_o f_s (t_r + t_f)$ $+\frac{1}{\pi}V_{s(p)} I_{r(p)} f_s t_{rr}$ | $\frac{9}{16}V_{s(p)} I_{o(p)} f_s (t_r + t_f)$ $+\frac{3}{2\pi}V_{s(p)} I_{r(p)} f_s t_{rr}$ | $\frac{9}{16}V_{s(p)} I_{o(p)} f_s (t_r + t_f)$ $+\frac{3}{2\pi}V_{s(p)} I_{r(p)} f_s t_{rr}$ |

**TABLE 3. Average power losses of the switching devices.**

| Switching Devices | Power Losses ($W$) in Proposed Topology | Power Losses ($W$) in [37] |
|---|---|---|
| $S_1$ and $D_1$ | 0.2215 | 0.2069 |
| $S_2$ and $D_2$ | 0.2215 | 0.2069 |
| $S_3$ and $D_3$ | 0.2214 | 0.6224 |
| $S_4$ and $D_4$ | 0.2214 | 0.6224 |
| $S_5$ and $D_5$ | 0.4428 | 0.4156 |
| $S_6$ and $D_6$ | 0.4428 | 0.4156 |
| Total Losses | 1.7714 | 2.4898 |

In summary, Table 2 depicts the comparative analysis during the inverting mode.

Simulation results (see Fig. 10), simulated for parameter values of Table 3 and a peak value of output current of 1.6 A, also confirm the mathematically calculated switching losses for the proposed and existing topologies, for a voltage gain of 0.5. The comparison validates the low conversion losses in the proposed converter than that of [37], as can be observed from the peaks of waveforms shown in Fig. 10. This is due to the low value of the switching currents and switching voltages for the same operating condition.

To gain more clarity, the instantaneous power losses waveforms having high peak values have high average power losses. Average power losses in the proposed topology are low than that of the converter in [37] as its instantaneous power losses waveforms have a low peak, as depicted in Fig. 10. The average power losses are recorded or measured in Simulink based environment and are tabulated in Table 3.

The average power losses computed mathematically using (28) and (30) for the proposed topology and the converter in [37], respectively, for an equal voltage gain of '0.5', are plotted in Fig. 11 with respect to the load (output) current. It can be viewed that average power losses computed mathematically and obtained from simulation results are almost the same (see the result for the output current of 1.6 A as highlighted in Fig. 11).

Therefore, the power losses analysis based on mathematically computed results and simulated values depict that the proposed topology has low conversion losses.

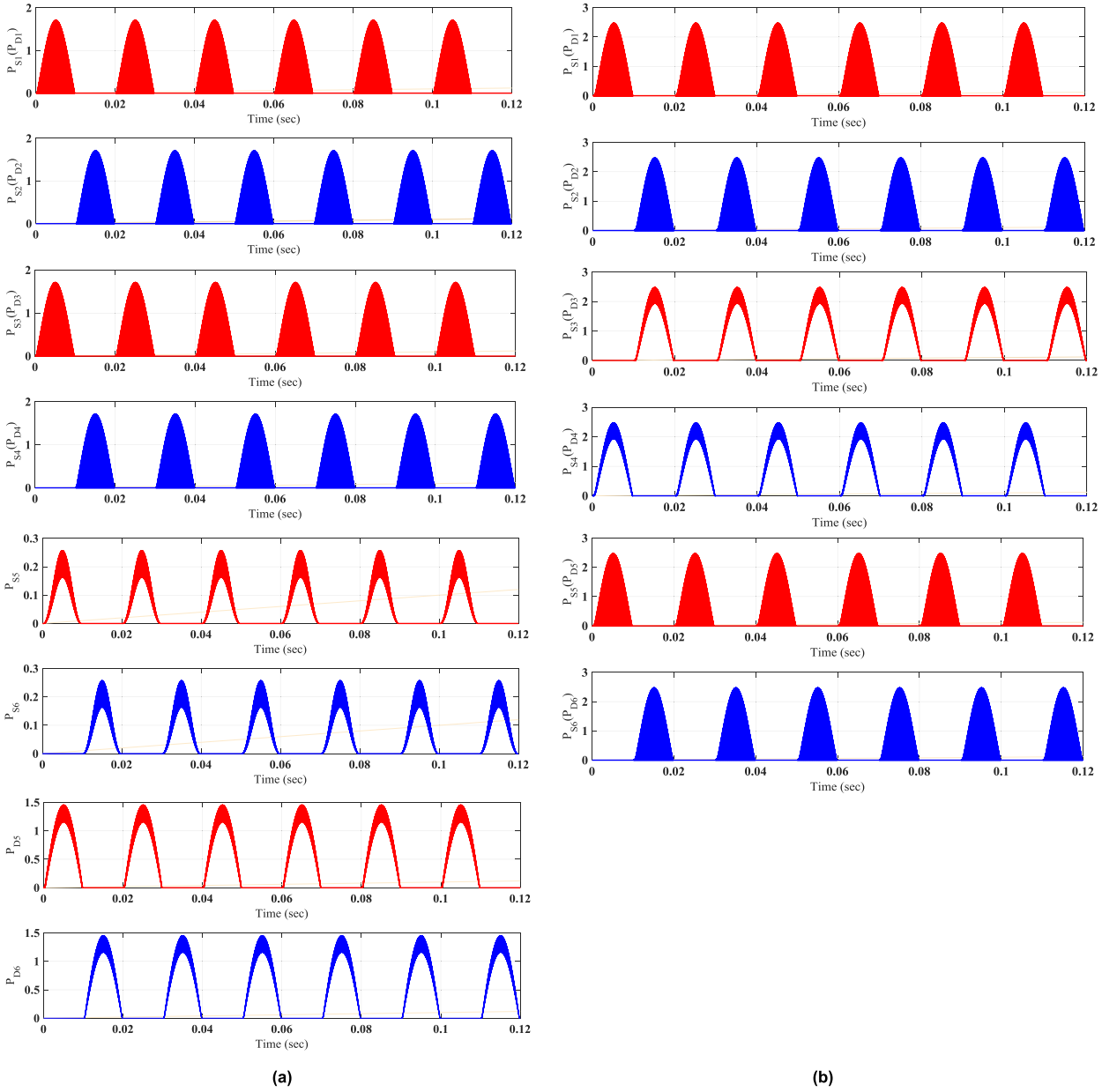


**FIGURE 10.** Switching losses offered by (a) the proposed topology and (b) the converter in [37].

## V. POWER QUALITY ANALYSIS OF THE OUTPUT VOLTAGE

This analysis is based on the ideal sinusoidal input voltage and ideal filtering behavior [42]. Fig. 12(a) displays the waveforms of the input voltage, square wave, and resultant output voltage waveform obtained through the switching action. This output $V_H(\omega t)$ is applied at the input of an LC filter, as depicted in Fig. 12 (b).

Mathematically speaking, the input voltage is given by

$$V_S(\omega t) = V_m sin(\omega t) \tag{34}$$

Here $V_m$ and $\omega$ are the peak value and angular frequency of the input voltage, respectively.

The Fourier of a square wave with duty cycle control '$k$' is computed in (35).

$$g(\omega_s t) = k + \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin(n\pi k) \cos(n\omega_s t - n\pi k) \tag{35}$$

where $\omega_s$ is the angular switching frequency of the control signal.

The resultant output voltage of the converter is approximated as follows.

$$\begin{aligned} V_H(\omega t) &= V_S(\omega t) * g(\omega_s t) \\ &= kV_m \sin(\omega t) + \sum_{n=1}^{\infty} \frac{V_m}{n\pi} \sin(n\pi k) \sin(n\omega_s t) \end{aligned} \tag{36}$$

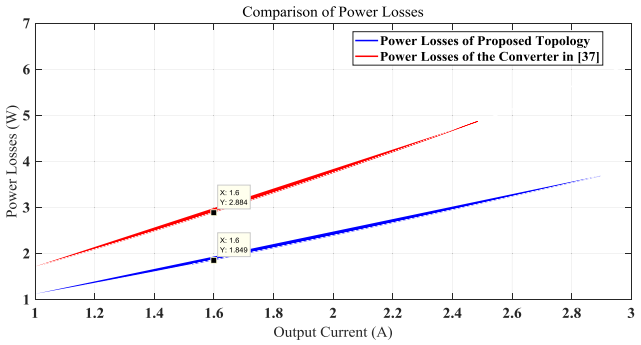


**FIGURE 11.** Power losses vs. load current.

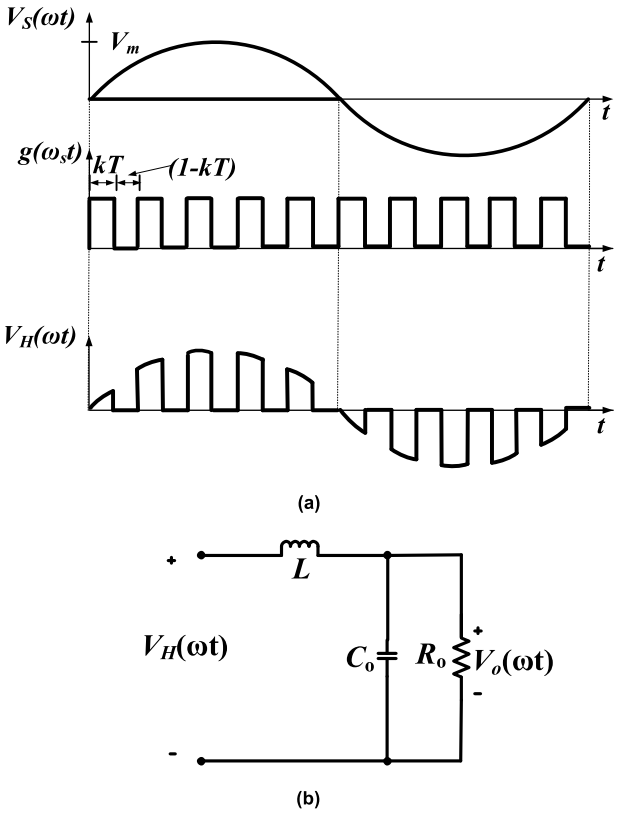


**FIGURE 12.** (a) Input voltage chopped at switching frequency; (b) LC filter.

The following expression illustrates the relationship between the voltage fundamental component at output $V_{o(f_o)}$ and output voltage of the converter $V_{H(f_o)}$ by assuming that load is purely resistive and output filter has ideal characteristics.

$$V_{H(f_o)} = \frac{kV_m}{\sqrt{2}}, V_{o(f_o)} = \frac{-jX_{Co}R_o}{jR_o(X_L - X_{Co}) + X_L X_{Co}} V_{H(f_o)} \tag{37}$$

where $R_o$ is the output resistance; $X_{Co}$ and $X_L$ are the capacitive and inductive reactance of the filtering network.

And

$$V_{H(f_o)} = \frac{kV_m}{\sqrt{2}} \tag{38}$$

At fundamental frequency, as $X_{Co} \gg R_o \gg X_L$, this implies

$$V_{o(f_o)} \cong V_{H(f_o)} \tag{39}$$

In the same manner, their harmonics components are related as

$$V_{o(hn)} = \frac{-jX_{Co(n\omega_S)}}{jR_o(X_{L(n\omega_S)} - X_{Co(n\omega_S)}) + X_{L(n\omega_S)}X_{Co(n\omega_S)}} V_{H(hn)} \tag{40}$$

where

$$X_{Co(n\omega_S)} = \frac{1}{(n\omega_S \pm \omega)C_o}, \quad X_{L(n\omega_S)} = (n\omega_S \pm \omega)L$$

and

$$V_{H(hn)} = \frac{V_m \sin(kn\pi)}{\sqrt{2}n\pi}$$

By applying the approximation $n\omega_S \pm \omega \cong n\omega_S$, we have

$$X_{Co(n\omega_S)} \cong \frac{1}{n\omega_S C_o}, \quad X_{L(n\omega_S)} \cong n\omega_S L$$

As $X_{Co(n\omega_S)} \ll R_o \ll X_{L(n\omega_S)}$

$$V_{o(hn)} = V_{H(hn)} \frac{R_o X_{Co(n\omega_S)}}{\sqrt{R_o^2(X_{L(n\omega_S)} - X_{Co(n\omega_S)})^2 + (X_{L(n\omega_S)}X_{Co(n\omega_S)})^2}} \tag{41}$$

$$V_{o(hn)} \cong \frac{X_{Co(n\omega_S)}}{X_{L(n\omega_S)}} V_{H(hn)} \tag{42}$$

The THD of the output voltage is computed by

$$THD_{Vo}(\%) = \frac{100}{V_{o(f_o)}} \sqrt{\sum_{n=1}^{\infty} V_{o(hn)}^2} \tag{43}$$

By putting the values from (39) and (42) into (43), we have

$$THD_{Vo}(\%) = \frac{\sqrt{2}}{k\pi\omega_S^2 LC_o} \sqrt{\sum_{n=1}^{\infty} \frac{\sin(n\pi k)^2}{n^6}} \times 100 \tag{44}$$

Equation (44) can be further approximated by ignoring the higher terms as

$$THD_{Vo}(\%) \cong \frac{\sin(\pi k)}{k\pi\omega_S^2 LC_o} \times 100 \tag{45}$$

At $G_V = 0.5$

$$THD_{Vo(buck-boost)} \cong 1.29 THD_{Vo(buck)} \tag{46}$$

Therefore, the THD of the output voltage realized with buck operation instead of buck-boost operation is low as this operating mode has low ripples in the inductor current and capacitor voltage. The output voltage waveforms with their FFT analysis depicted in Fig. 13 demonstrate the improved power quality in the output voltage of the proposed topology as it has low ripples in the output voltage than that of the converter in [37], for a voltage gain of 0.5.

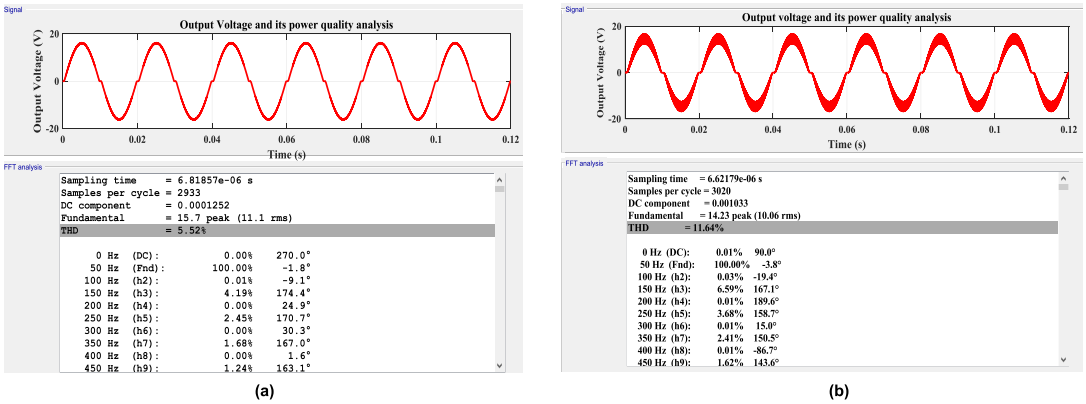


**FIGURE 13.** The power quality of the output voltage of (a) the proposed topology and (b) the converter in [37].

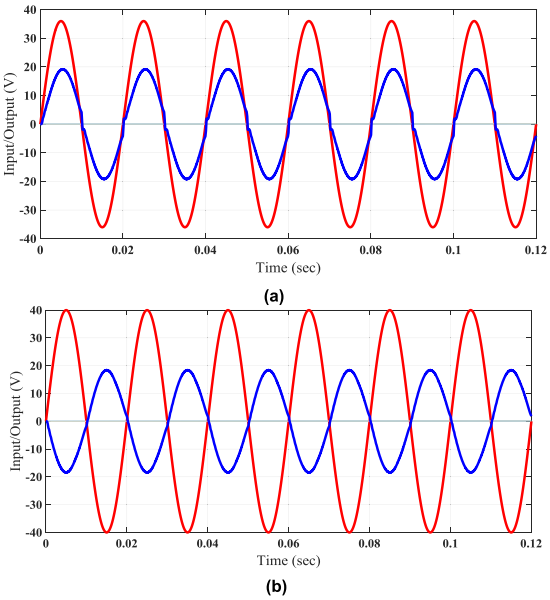


**FIGURE 14.** Waveforms of the input (red) and output (blue) voltages of the suggested converter operating in (a) non-inverting mode and (b) inverting mode.

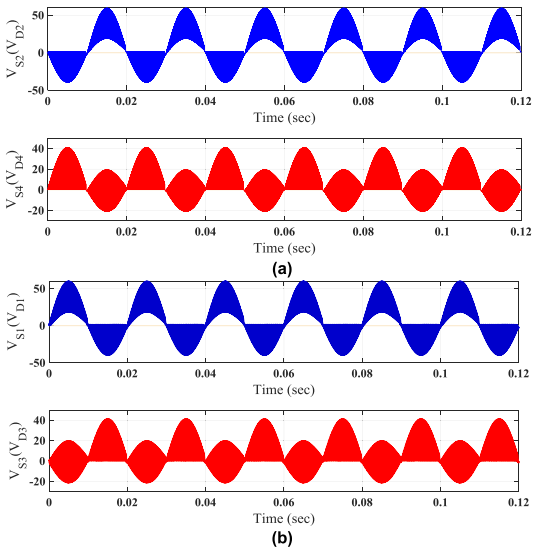


**FIGURE 15.** Voltage waveforms of the switching devices in inverting mode: (a) $S_2(D_2)$, $S_4$ $(D_4)$, (b) $S_1(D_1)$, $S_3$ $(D_3)$.

Specifically speaking, the proposed topology shows an improved THD (5.52%, in our case) compared to the other topology. This THD of 5.52% lies in the vicinity of the allowable THD, according to IEEE Standard. The effect of the generation of the harmonic distortion will be tolerable.

## VI. RESULTS

The proposed converter's scheme is simulated in MATLAB/Simulink which is then validated through the practical results. The peak value of the input voltage is set to 36 V at 50 Hz input frequency. The output voltage is regulated to 18 V peak at an input frequency through the 50% PWM duty cycle control. The filtering inductor and capacitors are taken 1 $mH$, and 4.7 $\mu F$ (output) and 1 $\mu F$ (input), respectively, to improve the quality of the output voltage and current. The parameters used for simulation and practical results throughout the paper are summarized in Table 4.

**TABLE 4.** Parameters values for simulation and practical results.

| Parameters | Values |
|---|---|
| Switching frequency ($f_s$) | 25 kHz |
| Peak input voltage ($V_p$) | 36 V |
| Input (output) frequency | 50 Hz |
| Output voltage gain | 0.5 |
| Load resistance ($R_L$) | 10 Ω |
| Output filtering capacitor | 4.7$\mu F$ |
| Filtering inductor | 1 $mH$ |
| Diode internal voltage ($V_d$) | 0.8 V |
| Diode internal resistance ($R_d$) | 0.006 Ω |
| MOSFET internal resistance ($R_m$) | 0.08 Ω |

### A. SIMULATION RESULTS

The simulation waveforms in the Simulink environment of the input voltage, output voltage, and high-frequency switching voltage of the suggested scheme operating in non-inverting and inverting modes are recorded. Figs. 14(a) and (b) depict the input-output voltage

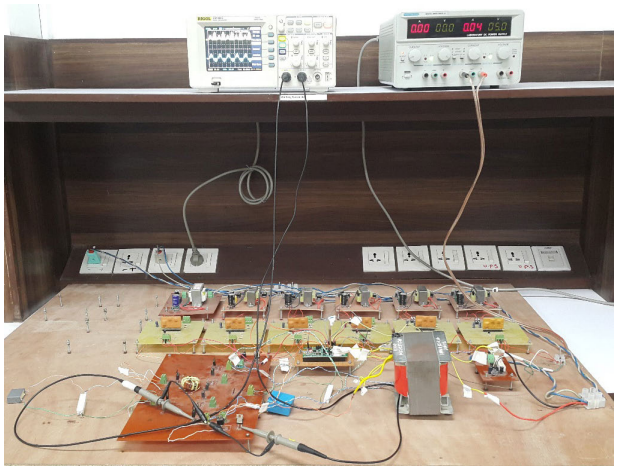

**FIGURE 16.** Practical setup of the proposed topology.

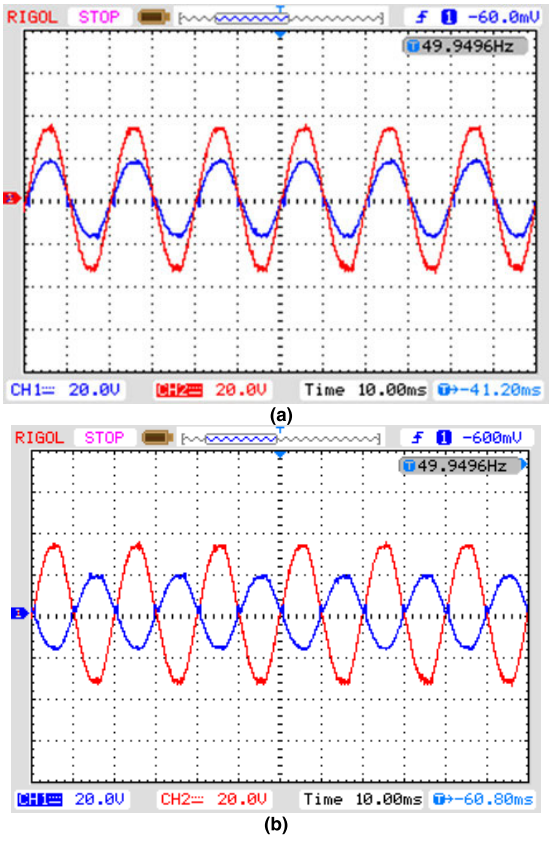


**FIGURE 17.** Practically recorded waveforms of input (red) and output (blue) voltages of the proposed converter operating during (a) non-inverting mode and (b) inverting mode.

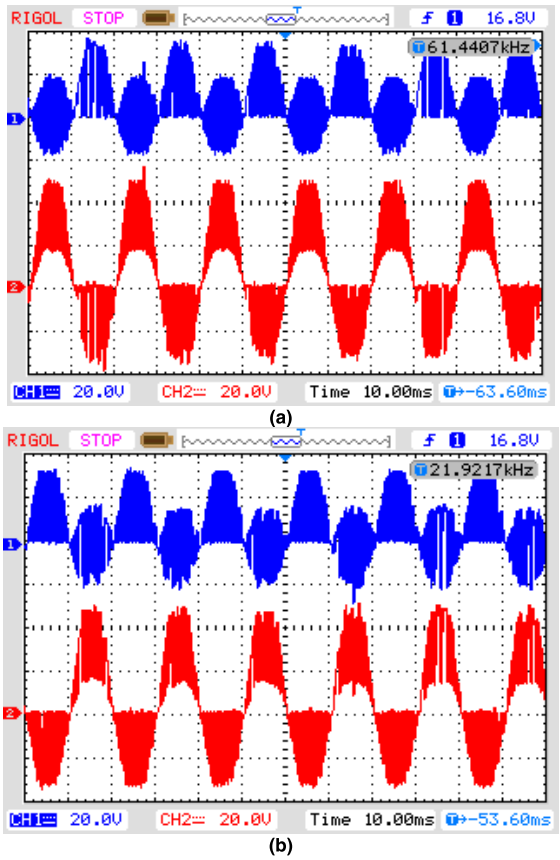


**FIGURE 18.** Practically recorded voltage waveforms of the switching devices in non-inverting modes: (a) $S_1$ ($D_1$), $S_3$ ($D_3$), (b) $S_2$($D_2$), $S_4$ ($D_4$).

waveforms. The input-output voltage is in-phase in non-inverting and out-of-phase in inverting operation. The amplitude of the output voltage is half in both cases as the duty cycle of the switching devices is set to 0.5. The non-inverted voltage is added in the line voltage to increase the line voltage, while the inverted voltage decreases the line voltage once it is added to it.

The high-frequency switching voltages across the controlled switches $S_1$, $S_3$, $D_1$, $D_3$ during the positive input voltage and across $S_2$, $S_4$, $D_2$, $D_4$ during the negative input voltage for non-inverting operation have already been demonstrated in Section IV. They are restricted to the input voltage. Figs. 15(a) and (b) illustrate the switching voltage during the inverting buck operation. This operation is realized through the high-frequency switching action of the switching devices $S_2$, $S_4$, $D_2$, $D_4$ for positive input voltage and $S_1$, $S_3$, $D_1$, $D_3$ for negative input voltage. The switching voltages of '$+V_S$' and '$-V_S$' are developed across the switching devices $S_3(D_3)$, $S_4(D_4)$ and $S_1(D_1)$, $S_2(D_2)$ respectively.

Therefore, the switching voltage during the high-frequency transition never exceeds the source's during the inverting and non-inverting operation. But the high-frequency switching voltage in the inverting operation of the converter in [38] and all operating modes of [37] is increased to $V_S + V_o$. This results in high switching voltage, and complicates *dv/dt* problem.

### B. PRACTICAL RESULTS

A practical prototype displayed in Fig. 16 is designed and developed for further validation of the proposed topology. It is tested for the same specifications mentioned in the simulation part for input-output voltage and switching voltage waveforms with duty cycle control of '0.5'. The practical setup is developed with six MOSFETs (IRF840) as a controlled

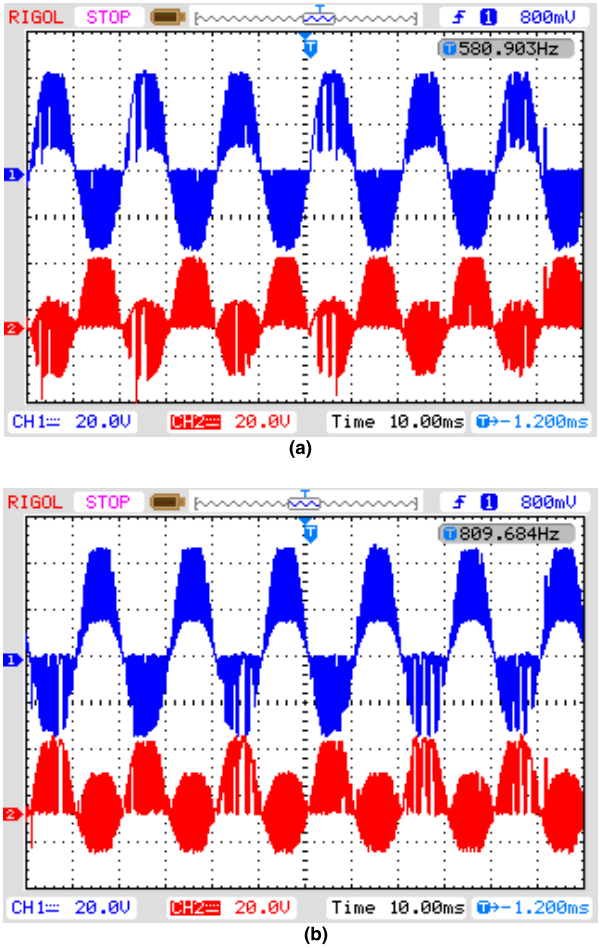


**FIGURE 19.** Practically recorded voltage waveforms of the switching devices in inverting modes: (a) $S_1(D_1)$, $S_3$ $(D_3)$, (b) $S_2(D_2)$, $S_4$ $(D_4)$.

switch, six-series connected hyper-fast diodes (RHRG3060), six GDCs (EXB840) with six isolated dc power supplies, and one ZCD that synchronizes the gating signals generated by STM microcontroller with the input voltage. One isolating step down transformer is utilized to bring the applied voltage at a safe level of the tested prototype.

To verify the non-inverting and inverting characteristics of the proposed topology, the prototype is tested for a positive and negative voltage gain of '0.5'. The resulted output voltages with the reference of input voltage are practically plotted on the Rigol oscilloscope (DS1052E) in Fig. 17(a) and (b) for in-phase and out-of-phase output voltage operation, respectively.

The noninverted operation is realized to increase the line voltage for voltage sag compensation. The inverted operation decreases the line voltage that is increased by the voltage swell issue. The non-inverted and inverted operation is governed through the sequences of the control signals while their voltage's magnitudes are adjusted by controlling the duty cycle control of the high-frequency switching devices. The practically recorded switching voltage waveforms during the non-inverting and inverting operation are displayed in Figs. 18 and 19, respectively. They validate that low switching voltage in all operating modes ensures low switching losses and *dv/dt* issues across the semiconductor devices.

All the practically recorded results match the simulation results obtained from the Simulink environment and mathematically computed values. This validates the effectiveness of the proposed topology.

## VII. CONCLUSION

This research develops a novel ac-to-ac converter topology having bipolar voltage gain for grid voltage compensation. It reduces the switching voltages and switching currents by 50% than that of the existing converters for a voltage gain of 0.5. Reduction in switching voltage ensures low switching losses. At any instant of time of its operation, each of its operating modes can be realized with the conduction of one high and one low switching frequency controlled device. The low switching currents and the conduction of a fewer number of switching devices lower the conduction losses significantly. Its non-inverting and inverting operation is identical, ensuring the same switching algorithm for both operations. It also ensures the low ripples in the output voltage, thus ensuring the improved power quality. Reduction in the unwanted conversion losses results in improved conversion efficiency. The mathematically computed performances are compared with the existing topology to validate the effectiveness of the suggested research. The computed and compared results are verified through the simulated and practically recorded results.

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