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Three-Level T-Type Inverter Fault Diagnosis and Tolerant Control Using Single-Phase Line Voltage

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ABSTRACT This study combines extension theory and chaos theory to create a three-level T-type inverter fault diagnosis system that uses single-phase line voltage signals. First, the three-level T-type inverter single-phase line voltage output waveform was measured when faults occurred separately in 12 power transistors. Subsequently, the Lorenz master–slave dynamic error transformation was used to obtain the chaos eye coordinates, which functioned as fault characteristics. Fault diagnosis involved extension theory–based fault categorization. Specifically, fault characteristic values were adopted as the input signal to determine the correlation between chaos eyes coordinates and transistor fault, thereby locating faulty transistors. In summary, this study established a low-cost and fast-operating inverter fault diagnosis system. The system integrates detection results with inverter fault-tolerant control to enable the constant operation of inverters in power generation without derating, thereby greatly enhancing system reliability. Finally, the reliability of the smart fault diagnosis system and fault-tolerant control was verified through measurement results.

INDEX TERMS Chaos theory, extension theory, fault diagnosis, fault-tolerant control, T-type inverter.

I. INTRODUCTION

The current growth of the renewable energy and electric vehicle industries—particularly in relation to grid-connected photovoltaic systems, power factor correction devices, and electric vehicle engines—has led to greater attention being paid to low withstand voltage, high efficiency power inverters; such growth has resulted in fruitful developments in multilevel inverter technology [1]–[5]. Multilevel inverters are primarily applied in high-power environments. However, because these inverters require a large number of power transistors, fault detection for these transistors is difficult. To increase equipment reliability and maintain the continual operation of the inverter's power transistor components during the occurrence of a fault, scholars around the globe have improved upon the fault detection mechanisms [6]–[15] and fault-tolerant control functions [16]–[19], [19]–[26] of multilevel inverters.

Current fault detection and diagnosis technologies include model-based methods, expert systems, and machine learning. Despite being viable, model-base methods [6]–[8] reference the values of the snubber capacitance and balance resistor, both of which are difficult to obtain. Furthermore, model-based methods are limited by its presence of parasitic elements, the functioning of which necessitates certain assumptions and limitations. Alternatively, although expert systems can repair relevant systems, they are costly because the construction of a comprehensive diagnosis system, prior to operation, require experts [9], [10]. Another method is neural networks, the most popular machine learning technique [11] that imitates the human brain. Neural networks can easily update data models through backpropagation and, through the use of its hidden layers, are less reliant on feature engineering. However, machine learning has longer operation times because the processing of huge learning datasets is required before accurate decisions can be made [12]–[15]. Although current fault-tolerant control methods [16]–[22] allow for continued operation after the occurrence of faults, operation occurs under derating conditions. Therefore, these current methods are unsuitable for some fault conditions. A study [23] only discussed the fault tolerance in neutral point switches but did not mention how three-level T-type inverters should operate when faults occur in the upper and lower arms. Other studies [24], [19] that discussed the fault tolerance of three-level T-type inverters after the occurrence of upper and lower arm faults determined that during fault tolerance, the

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inverter must operate under derating conditions and output two-level voltage waveforms, thus increasing the total harmonic distortion [25]. Therefore, system fault diagnosis and tolerance require further development.

The author of this study has investigated fault diagnosis and tolerant control in three-level T-type inverters [26]. However, this previous study was limited by difficulties from the complex computation and fault diagnosis processes. These processes required the extraction (and application) of values from the three-phase voltage lines using the Lorenz master–slave dynamic error transformation, which rendered the study unable to distinguish fault conditions between the 12 switches. Additionally, the fault detection and diagnosis mechanism developed in that study could only perform fault-tolerant control for faults occurring in the upper and lower arms. Therefore, this study proposed a new fault diagnosis and tolerant control system that remedies the aforementioned problems.

This study first extracted the voltage waveform data during occurrences of a power transistor fault and conducted master–slave chaotic dynamic error transformation on the extracted data to obtain the chaos eyes for each fault switch. Subsequently, the characteristics of the chaos eye coordinates are employed in extension theory for fault diagnosis and for detecting the locations of faulty power transistors. Figure 1 displays the system framework.

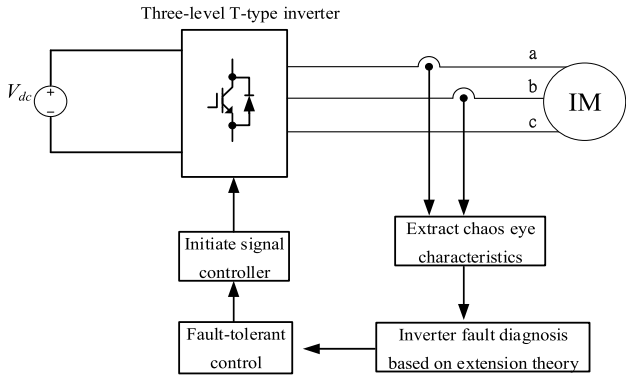


FIGURE 1. Fault diagnosis system framework of three-level T-type inverter.

II. FAULT CHARACTERISTICS OF THE THREE-LEVEL T-TYPE INVERTER

Figure 2 displays the three-level T-type inverter framework. Inverter faults are distinguished into short circuit and open switch faults [27]. Short circuit faults primarily occur during conditions of drive signal errors, overvoltage, or overheating. These conditions cause switch components to be pierced through. Short circuits rapidly generate a large electrical current, severely damaging the circuit. Therefore, hardware methods were adopted to detect faults and conduct fault tolerance [28]. By comparison, open circuit faults generally occur when no triggering signal is given or when the switch drive circuit malfunctions; such faults prevent the

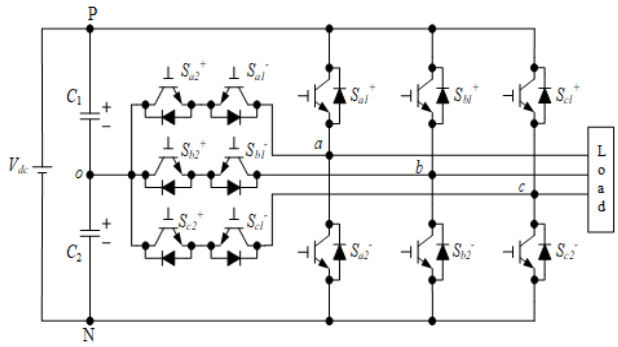


FIGURE 2. Three-level T-type inverter framework.

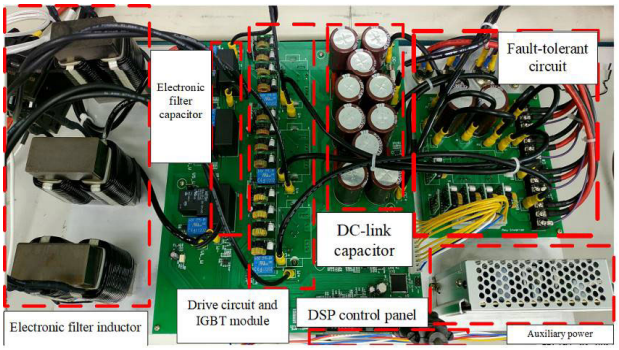


FIGURE 3. Experimental hardware circuits of the three-level T-type inverter.

switch from activating and transmitting the current. Although short-duration open circuit faults do not cause severe damage, output voltage quality is degraded and circuit distortion is produced, thereby causing potential faults in other components [29].

Figure 3 displays the three-level T-type inverter used in this study. To provide stable DC power, the input end included 10 680 μF/400 V electrolytic capacitors, which were connected in two serial-connected parallel power circuits, each of which comprised five capacitators. Subsequently, 12 insulated gate bipolar transistors (IGBTs) were adopted to compose a T-type inverter framework. To filter out the high-frequency signal output of the inverter and convert the output into low-frequency sine waves, the three-level T-type inverter used a two-level low-pass filter for wave filtration. The filter capacitor, inductor, and effective output voltage values were 10 μF/250 V, 1.6 mH/16 A, and 220 V, respectively. This study analyzed the power output for each switch fault instance. Through analysis and observation, this study determined that under regular operation, the inverter output waveform is a balanced three-phase current.

For instance, Figure 4 displays the output line voltage waveform when the inverter work frequency was 60 Hz and no power transistor faults have occurred. The figure illustrates the equal size and shape of the voltage waves, together with the 120° phase angle difference between each wave, thereby demonstrating the general characteristics of the three-phase balance. These characteristics may change if faults occur in

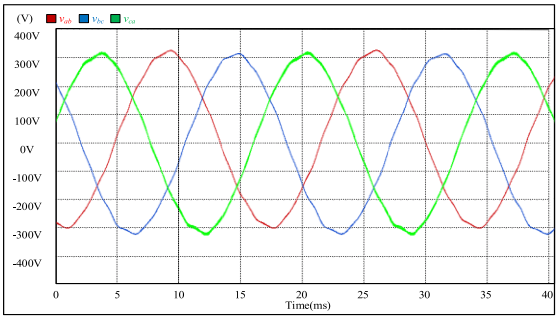


FIGURE 4. Output line voltage waveforms v_{ab}, v_{bc}, and v_{ca} when the inverter work frequency was 60 Hz under standard operation.

any of the switches. Figure 5(a) reveals that if a fault occurs in inverter switch S_{a1}^{+}, the a phase output voltage waveform, v_{ab}, becomes distorted. Figure 5(b) and 5(c) reveal that if a fault occurs in switches S_{b2}^{+} or S_{b1}^{-}, the line voltage waveform v_{bc} becomes distorted. Figure 5(d) reveals that relative to the waveform during regular operation conditions, the detected c phase line voltage waveform, v_{ca}, was significantly different during fault occurrences in switch S_{c2}^{-}.

III. CHAOS THEORY AND EXTENSION THEORY

A. DYNAMIC ERRORS IN MASTER-SLAVE CHAOS SYNCHRONIZATION

Pecora and Carrol (1990) proposed the concept of synchronization in chaotic system theory [30]. Generally, if two or more chaotic systems are situated in the same time frame, their motion trajectories will be identical. The synchronized chaotic system comprises a master system and slave system, which is described in (1) and (2), respectively. However, if the default value settings of the master and slave systems are different, the two systems' trajectories will differ. This study included a controller in the slave system to configure the slave system into tracking the master system; such tracking can then be used to synchronize the trajectories of the two systems. This tracking system is termed the chaotic synchronization system.

$$S_{master} = \left\{ \begin{array}{l} \dot{x}_1 = f_1(x_1, x_2, \ldots, x_n) \\ \dot{x}_2 = f_2(x_1, x_2, \ldots, x_n) \\ \quad \vdots \\ \dot{x}_n = f_n(x_1, x_2, \ldots, x_n) \end{array} \right\} \tag{1}$$

$$S_{slave} = \left\{ \begin{array}{l} \dot{y}_1 = f_1(y_1, y_2, \ldots, y_n) \\ \dot{y}_2 = f_2(y_1, y_2, \ldots, y_n) \\ \quad \vdots \\ \dot{y}_n = f_n(y_1, y_2, \ldots, y_n) \end{array} \right\} \tag{2}$$

where $f_n(x_1, x_2, \ldots, x_n)$ are nonlinear equations.

The method of chaotic synchronization employed in this study, which uses the dynamic error between the master and slave systems, was similar to that used in a previous study [31]. Therefore, instead of using the controller in the master–slave synchronization system, this study subtracted (1) from (2) to generate the dynamic error equation in (3). This dynamic error equation can be used to establish a characteristic equation in (4).

$$\left\{ \begin{array}{l} e_1 = y_1 - x_1 \\ e_2 = y_2 - x_2 \\ \quad \vdots \\ e_n = y_n - x_n \end{array} \right\} \tag{3}$$

$$\left\{ \begin{array}{l} \dot{e}_1 = f_1(y_1, y_2, \ldots, y_n) - f_1(x_1, x_2, \ldots, x_n) \\ \dot{e}_2 = f_2(y_1, y_2, \ldots, y_n) - f_2(x_1, x_2, \ldots, x_n) \\ \quad \vdots \\ \dot{e}_n = f_n(y_1, y_2, \ldots, y_n) - f_n(x_1, x_2, \ldots, x_n) \end{array} \right\} \tag{4}$$

If systems with different parameters are coupled together without the controller, errors may occur in the coupled system. Therefore, this study employed two similar Lorenz systems [32], L_{master} and L_{slave}, which are described in (5) and (6), respectively.

$$L_{master} = \left\{ \begin{array}{l} \dot{x}_1 = \alpha(x_2 - x_1) \\ \dot{x}_2 = \beta x_1 - x_1 x_3 - x_2 \\ \dot{x}_3 = x_1 x_2 - \gamma x_3 \end{array} \right\} \tag{5}$$

$$L_{slave} = \left\{ \begin{array}{l} \dot{y}_1 = \alpha(y_2 - y_1) \\ \dot{y}_2 = \beta y_1 - y_1 y_3 - y_2 \\ \dot{y}_3 = y_1 y_2 - \gamma y_3 \end{array} \right\} \tag{6}$$

The baseline and testing values were input into the master and slave systems, respectively. α, β, and γ are adjustable parameters and were set to be $\alpha = 10$, $\beta = 28$, and $\gamma = 8/3$ for both systems. The dynamic error equation can be acquired by subtracting (5) with (6); its matrix is presented in (7).

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \end{bmatrix} = \begin{bmatrix} -\alpha & \alpha & 0 \\ \beta & -1 & 0 \\ 0 & 0 & -\gamma \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} + \begin{bmatrix} 0 \\ -y_1 y_3 \\ y_1 y_2 \end{bmatrix} + \begin{bmatrix} 0 \\ x_1 x_3 \\ x_1 x_2 \end{bmatrix} \tag{7}$$

where $e_1 = y_1 - x_1$, $e_2 = y_2 - x_2$, $e_3 = y_3 - x_3$.

The values for $\dot{e}_1$, $\dot{e}_2$, and $\dot{e}_3$ can be obtained from the aforementioned Lorenz master–slave system. This study adopted $\dot{e}_1$ and $\dot{e}_2$ to generate a dynamic error trajectory map, which is displayed in Figure 6. The chaos eyes were established as the two centers of gravity in the trajectory map, with their coordinates serving as the characteristic value for the inverter diagnosis.

After the line voltage was input into the Lorenz master–slave dynamic error system, two chaotic trajectories—one under regular operating conditions and the other when a fault occurred in switch S_{a1}^{+}—were obtained (Figures 7 and 8, respectively). The chaos eye coordinates in Figures 7(a) and 8(a) are [C_1: (−1.8170, −2.2083); C_2: (1.8240, −3.1845)] and [C_1: (−1.2392, −2.3343); C_2: (1.4652, −12.4135)], respectively, indicating that the y-coordinate values of the chaos eyes of the voltage waveforms v_{ab} exhibited considerable differences before and after fault occurrence. These differences may have been caused by

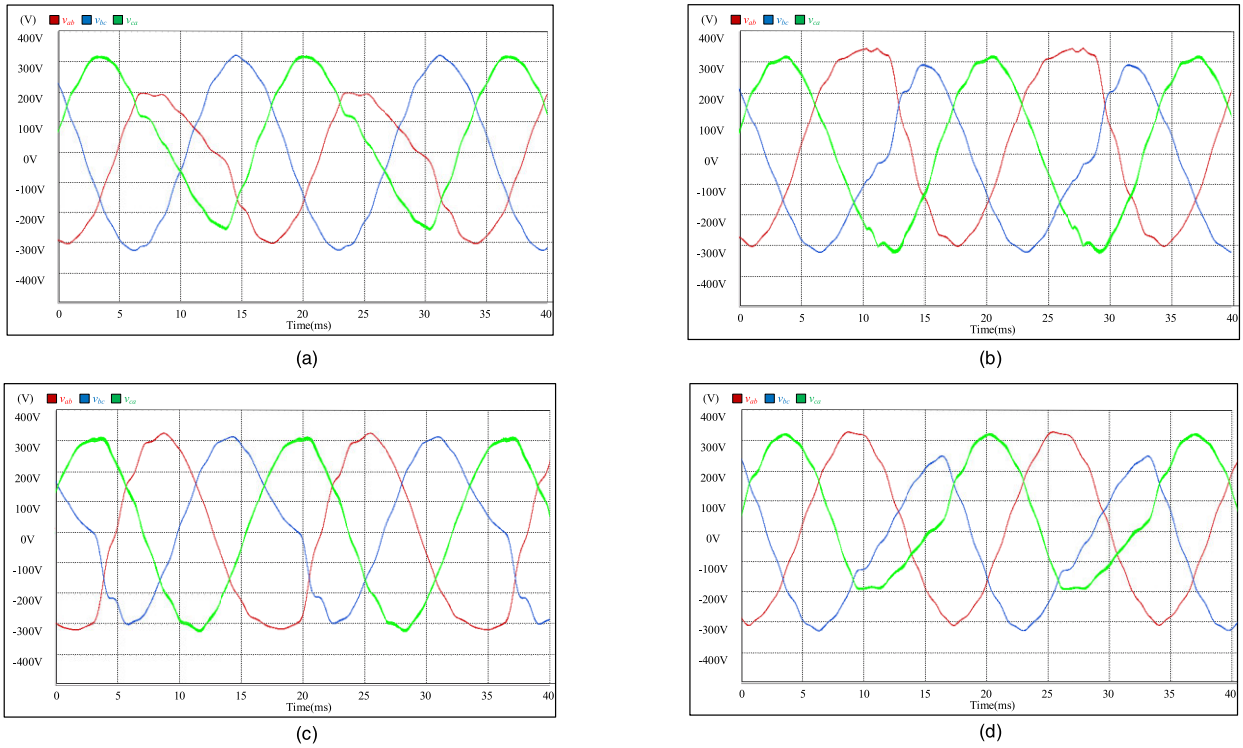


FIGURE 5. Output line voltage waveforms when the inverter work frequency was 60 Hz and the faults occur at the following switches: (a) S_{a1}^{+}, (b) S_{b2}^{+}, (c) S_{b1}^{-}, and (d) S_{c2}^{-}.

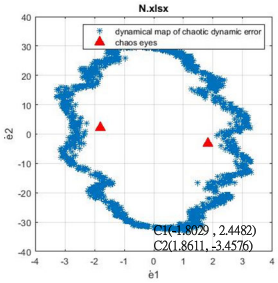


FIGURE 6. Chaos eyes and chaotic trajectory.

faults occurring in switch S_{a1}^{+}. This study adopted the voltage waveform values under similar operation frequencies as the fault diagnosis input value. After the conversion of the chaotic synchronization system, the chaos eye coordinates C_1 and C_2 were used as fault characteristics. However, the chaos eye coordinates of the v_{ab} voltage waveform will differ if a fault occurs in other transistors. Furthermore, chaos eye coordinates, being situated in a range, are not stabilized. Therefore, extension theory is required for fault diagnosis to confirm which switch is at fault.

B. EXTENSION THEORY

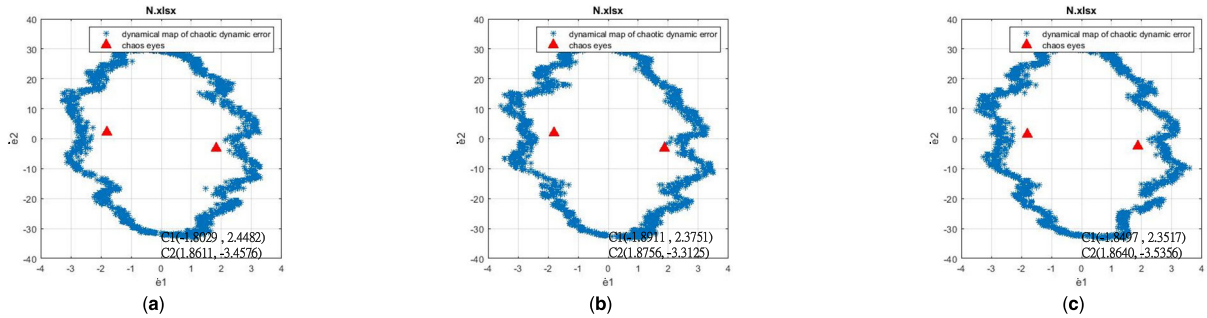
Extension theory was first proposed by a Chinese scholar, Professor Tsai Wen, in 1983. The theory analyzes the extensionality of objects and adopts a qualitative and quantitative approach to investigate and resolve dilemmas between objects. Matter-element theory and extension mathematics are the two pillars of extension theory. Matter-element theory describes the extensionality and transformation characteristics of matter elements, whereas extension mathematics uses extension sets and correlation functions as algorithm cores [17]. Extension theory expresses matter object information in the form of matter-element models and employs matter-element transformations to express the conversion relationship between object quantity and object quality. Correlation functions are then adopted to clearly determine the degree of influence exerted by qualitative and quantitative characteristics.

1) CONCEPT OF EXTENSION THEORY

Extension theory solves problems by representing objects with matter-element models. Equation (8) displays the numeric function of the matter-element model.

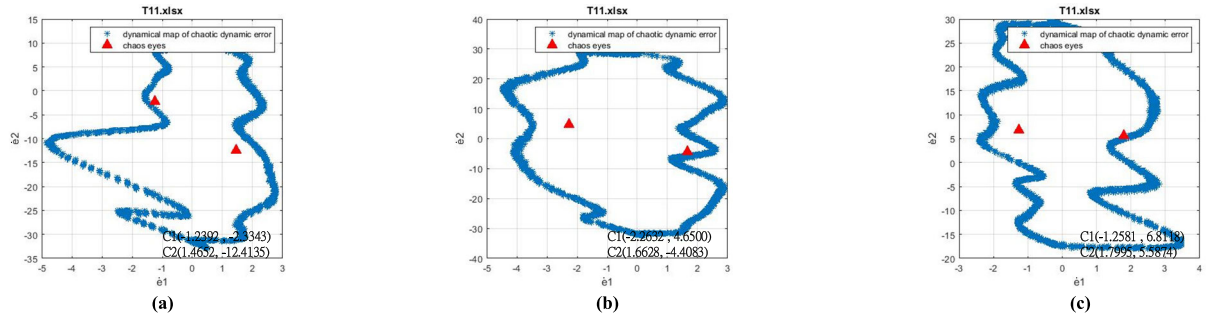
$$R = (N, C, V) \tag{8}$$

In the equation, R represents the basic element of the object, also known as the matter element. The three elements constituting the matter element, N, C, and V, represent the object's name, characteristics, and characteristic value, respectively. Extension theory states that if the matter-element characteristic is not a single variable, the characteristics should be represented by x characteristics and x corresponding characteristic values. In this instance, the characteristics and characteristic values should be represented in the vector forms $C = [c_1, c_2, \ldots, c_x]$ and $V = [v_1, v_2, \ldots, v_x]$, respectively. Therefore, the extension



(a) (b) (c)

FIGURE 7. Line voltage chaotic trajectories when inverter work frequency was 60 Hz under standard operation: (a) v_{ab}, (b) v_{bc}, (c) v_{ca}.



(a) (b) (c)

FIGURE 8. Line voltage chaotic trajectories when inverter work frequency was 60 Hz and when a fault occurred in the switch S_{a1}^{+}: (a) v_{ab}; (b) v_{bc}; (c) v_{ca}.

matter-element function in (8) can be rewritten as (9).

$$R = \begin{bmatrix} R_1 \\ R_2 \\ \vdots \\ R_x \end{bmatrix} = \begin{bmatrix} N, & c_1, & v_1 \\ & c_2, & v_2 \\ & \vdots & \vdots \\ & c_x, & v_x \end{bmatrix} \tag{9}$$

If the characteristic value is within a range, that range is termed the classical domain and is included in the neighborhood domain. If the domains $F_0 =< a, b >$, $F=< d, e >$, $F_0 \in F$, and f represent any point in domain F, the corresponding matter elements in $F_0 =< a, b >$ can be represented as (10).

$$R_0 = (F_0, C_i, V_i) = \begin{bmatrix} F_0, & c_1, & < a_1, b_1 > \\ & c_2, & < a_2, b_2 > \\ & \vdots & \vdots \\ c_x, & < a_x, & b_x > \end{bmatrix} \tag{10}$$

where C_i is the characteristics of F_0 and V_i is the characteristic value of C_i (i.e., the classical domain). Equation (11) displays the matter elements of object F, namely R_F.

$$R_F = (F, C_j, V_j) = \begin{bmatrix} F, & c_1, & < d_1, & e_1 > \\ & c_2, & < d_2, & e_2 > \\ & \vdots & & \vdots \\ & c_x, & < d_x, & e_x > \end{bmatrix} \tag{11}$$

where C_j and V_j are the characteristics and characteristic values of F, respectively. Therefore, V_j represents the neighborhood domain.

2) DISTANCE AND LOCATION VALUES

Classical mathematics focuses on the distance between two points. By contrast, extension theory computes the distance between one point within the real field and the domain, which is expressed as a function and written in (12).

$$\phi(f, F_0) = \left| f - \frac{v_a + v_b}{2} \right| - \frac{v_b - v_a}{2} \tag{12}$$

In addition to analyzing the relationship between points and domains, an analysis of the relationship between points and that between domains is crucial. Let $F_0 =< v_a, v_b >$ and $F =< v_d, v_e >$ be two domains in the real field between the domains F_0 and F. Therefore, the distance value from point f to the domains F_0 and F is

$$D(f, F_0, F) = \begin{cases} \phi(f, F) - \phi(f, F_0), & f \notin F_0 \\ -1, & f \in F_0 \end{cases} \tag{13}$$

3) CORRELATION FUNCTION

The correlation function, presented in (14), is the division between the distance and location values.

$$K(f) = \frac{\phi(f, F_0)}{D(f, F_0, F)} \tag{14}$$

The correlation function attains its maximum value when the elementary correlation function $f = [v_a + v_b]/2$

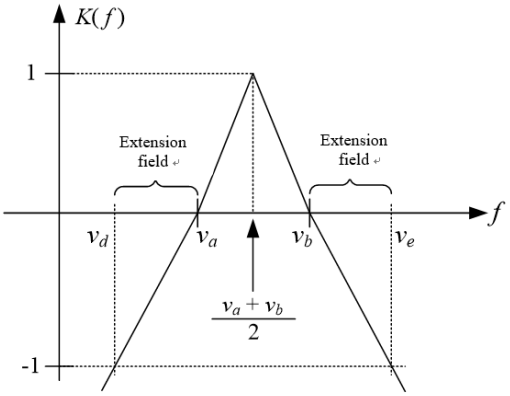


FIGURE 9. Elementary correlation function.

is satisfied, as illustrated in Figure 9. When $K(f) < -1$, $K(f) > 0$, and $-1 < K(f) < 0$, point f is not in domain F, in domain F_0, and in the extension field, respectively.

IV. EXTENSION THEORY-BASED INVERTER FAULT DIAGNOSIS

A. FAULT DIAGNOSIS METHOD

The proposed fault diagnosis method first employs chaos theory to acquire the dynamic error trajectory of the line voltage waveforms. The Lorenz dynamical system equations are then used to extract the chaos eye values, which serve as the characteristic values. Finally, extension theory is used to classify the fault incident into fault types and determine whether faults have occurred in the three-level inverter. The extension theory–based fault diagnosis process is as follows.

Step 1: To establish the matter-element model, chaos eye coordinates (C_1 and C_2) located on the voltage chaos trajectory maps of each transistor failure scenario are used as characteristics.

$$R_g = (F, C, V_p) = \begin{bmatrix} F_0 & C_1 & < x_1, y_1 > \\ & C_2 & < x_2, y_2 > \end{bmatrix}, \quad g = 1, 2, \ldots, 13 \tag{15}$$

Step 2: The chaos eye coordinates of the faulty transistor to be determined, namely C_1 and C_2, are entered as inputs. The matter-element model is as follows.

$$R_{\text{new}} = \begin{bmatrix} F_{\text{new}} & C_1 & V_{\text{now1}} \\ & C_2 & V_{\text{new2}} \end{bmatrix} \tag{16}$$

Step 3: The characteristics (C_1 and C_2) and the corresponding weights (W_1, W_2, W_3, and W_4) are determined. These weights represent the importance of each characteristic. In this study, $W_1 = W_3 = 0.15$ and $W_2 = W_4 = 0.35$.

Step 4: The degree of correlation between the fault characteristics and each fault category is computed.

$$\lambda_g = \sum_{j=1}^{2} W_j K_{gj}, \quad g = 1, 2, \ldots, 13 \tag{17}$$

TABLE 1. Codes for fault types.

Fault state	Type
Fault did not occur	F_0
Fault occurred in switch S_{a1}^+	F_1
Fault occurred in switch S_{a1}^-	F_2
Fault occurred in switch S_{a2}^+	F_3
Fault occurred in switch S_{a2}^-	F_4
Fault occurred in switch S_{b1}^+	F_5
Fault occurred in switch S_{b1}^-	F_6
Fault occurred in switch S_{b2}^+	F_7
Fault occurred in switch S_{b2}^-	F_8
Fault occurred in switch S_{c1}^+	F_9
Fault occurred in switch S_{c1}^-	F_{10}
Fault occurred in switch S_{c2}^+	F_{11}
Fault occurred in switch S_{c2}^-	F_{12}

Step 5: After the computation, characteristics are assigned (as belonging) to the fault category it has the largest correlation value with. In doing so, these fault characteristic can be used to determine which transistor is faulty.

To identify the faulty power transistor, the fault categories were divided into the following 12 switch fault states: S_{a1}^+, S_{a1}^-, S_{a2}^+, S_{a2}^-, S_{b1}^+, S_{b1}^-, S_{b2}^+, S_{b2}^-, S_{c1}^+, S_{c1}^-, S_{c2}^+, and S_{c2}^-. After including the state in which no switch faults occurred, the 13 fault categories are displayed in Table 1.

To increase diagnostic efficiency, this study established 13 fault conditions, which differ by the single-phase line voltage in the extension matter-element models. Diagnosis speed is increased because the system only has to consider the single-phase line voltage. This study adopted v_{ab} as the fault diagnosis signal and constructed a new type of fault diagnosis system. The system fault diagnosis process is displayed in Figure 10.

B. FAULT DIAGNOSIS RESULTS

Figures 11 and 12 display the measured chaos trajectory maps of v_{ab} during regular system operation and when faults occurred in the 12 switches, respectively. This study exclusively used the chaos trajectory maps of v_{ab} as the reference for fault diagnosis. Upon obtaining the chaos trajectory maps, the chaos eyes were then used as fault diagnosis

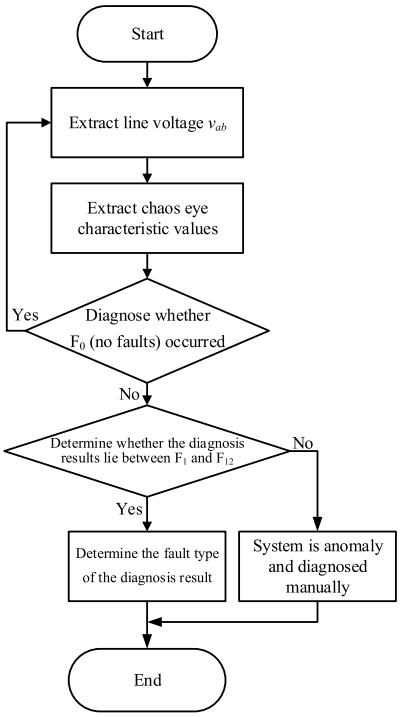


FIGURE 10. Fault diagnosis process involving only the single-phase line voltage.

TABLE 2. Measured chaos eye characteristic values of v_{ab} when the inverter operated at 60 Hz.

Fault Category	Characteristic values of the v_{ab} chaos eyes			
	C_1 (x-axis)	C_1 (y-axis)	C_2 (x-axis)	C_2 (y-axis)
F_0	-1.8308	1.9935	1.9673	-4.5685
F_1	-1.2227	-3.4996	1.4417	-11.4781
F_2	-1.363	-6.7133	1.1404	-10.7648
F_3	-1.1765	8.9421	1.2862	4.8655
F_4	-1.4381	10.2815	1.1928	2.2773
F_5	-1.2729	6.1066	1.8293	4.7317
F_6	-1.5539	10.3856	1.6251	3.8971
F_7	-1.6578	-5.3968	1.5543	-13.3752
F_8	-1.8461	-6.6006	1.2712	-7.4623
F_9	-2.1751	3.9242	1.674	-4.9344
F_{10}	-1.4959	2.0018	2.0737	-4.4605
F_{11}	-2.1033	2.9209	1.4255	-3.6922
F_{12}	-1.7095	2.4033	2.1019	-5.1572

characteristics. The chaos eye coordinates of each fault condition are listed in Table 2.

After the chaos eye coordinates were input into the fault diagnosis system, the diagnosis results were obtained in Table 3. The third testing dataset in Table 3 was extracted from the occurrence of a fault in the S_{a1}^{-} switch (fault type F_2). After the fault was recognized by the fault diagnosis system, the fault data were determined to be most highly correlated, among the 13 fault types, with fault type F_2 (correlation degree = 0.90314). Therefore, the system recognized

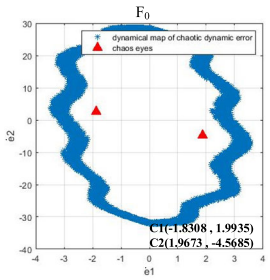


FIGURE 11. Measured chaos trajectory maps of v_{ab} under normal operation.

the fault as an F_2 fault, and by referencing Table 1, it was revealed that the fault occurred in switch S_{a1}^{-}. The correlation degree in Table 3 indicate that all fault diagnoses for each dataset were accurately distinguished. Furthermore, this study included a ±5% deviation into the testing samples. The results, displayed in Table 4, revealed that the system correctly recognized fault conditions and fault types even after this deviation was included in the testing information. In summary, this study's proposed a fault diagnosis system only requires the extraction of single-phase line voltage data, thereby increasing diagnostic accuracy and efficiency.

The proposed chaos theory– and extension theory–based inverter fault diagnosis system can identify the location of faulty power transistors in three-level T-type inverters. Furthermore, the system has fault tolerance functions, thereby reducing the influence of noise signals, and does not require a learning process.

The measurement results reveal that the proposed diagnosis method can correctly diagnose fault types despite noise interference. Compared with current three-level T-type inverter fault diagnosis systems [26], the proposed fault diagnosis system only requires extracting single-phase line voltage data for analysis, which reduces system operation times. In addition to references from the literature, the proposed fault diagnosis system covers normal operation and fault occurrences in S_{a1}^{-}, S_{a2}^{+}, S_{b1}^{-}, S_{b2}^{+}, S_{c1}^{-}, S_{c2}^{+}. Therefore, this system can accurately distinguish all switch fault types in three-level T-type inverters, thus demonstrating its reliability.

V. THREE-LEVEL T-TYPE INVERTER FAULT-TOLERANT CONTROL

Some applications require greater equipment reliability. To maintain stable output voltages, thus increasing reliability, fault tolerance functions are often included in systems such as the three-level T-type inverter. Furthermore, during the occurrence of switch faults, three-level inverters do not require systems to operate under derating conditions.

Figure 13 displays the circuit framework of the fault-tolerant control of the proposed system. Compared with standard three-level inverters, the three-level T-type inverter includes four additional TRIACs and three IGBTs. The circuit is connected by connecting three TRIAC semiconductor switches over the fault-tolerant arm neutral point, namely

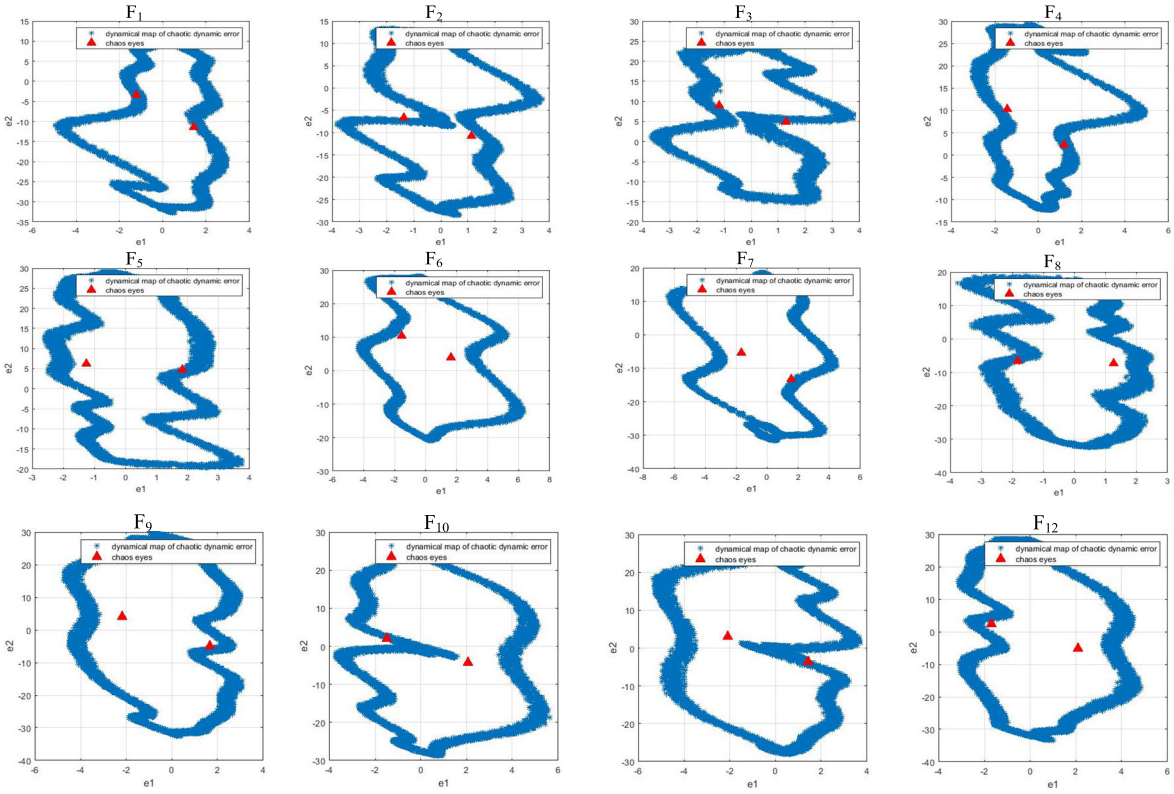


FIGURE 12. Measured chaos trajectory maps of v_{ab} during the 12 of fault type.

TABLE 3. Recognition results of different switch faults using v_{ab} data when the inverter operated at 60 Hz.

Fault type	Fault correlation degree													Recognition result
	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8	F_9	F_{10}	F_{11}	F_{12}	
F_0	**0.8885**	-0.25845	-0.28715	-0.33287	-0.28589	-0.13211	-0.17919	-0.14067	-0.07239	0.244073	0.770325	0.037558	0.389133	F_0
F_1	-0.43636	**0.76351**	0.143866	-0.22121	-0.36718	-0.30387	-0.39185	0.153027	-0.21123	-0.40484	-0.31359	-0.31039	-0.4298	F_1
F_2	-0.50829	0.18588	**0.90314**	-0.34862	-0.27594	-0.41216	-0.48432	-0.02416	0.233139	-0.52453	-0.38888	-0.48221	-0.46424	F_2
F_3	-0.6351	-0.32831	-0.42675	**0.8036**	0.021268	0.176231	-0.10587	-0.64111	-0.52984	-0.55829	-0.59172	-0.48517	-0.64051	F_3
F_4	-0.43446	-0.38661	-0.23042	0.130874	**0.61004**	-0.18657	0.323037	-0.44159	-0.35392	-0.44238	-0.31994	-0.36622	-0.40608	F_4
F_5	-0.42033	-0.31113	-0.451	0.391671	-0.2159	**0.83132**	0.001369	-0.49996	-0.61658	-0.3245	-0.31399	-0.46941	-0.43625	F_5
F_6	-0.37346	-0.43799	-0.45899	-0.04095	0.379536	-0.08216	**0.56682**	-0.31657	-0.48716	-0.32957	-0.27528	-0.38635	-0.36569	F_6
F_7	-0.31942	0.122075	-0.02361	-0.50523	-0.42261	-0.45155	-0.25462	**0.79653**	-0.08088	-0.33147	-0.2889	-0.30921	-0.28984	F_7
F_8	-0.25853	-0.18364	0.419687	-0.4055	-0.28481	-0.52854	-0.40425	0.032718	**0.70642**	-0.32983	-0.34416	-0.26712	-0.23229	F_8
F_9	0.159621	-0.20403	-0.30811	-0.28365	-0.27734	-0.14806	-0.1123	-0.14616	-0.15349	**0.81378**	0.026733	0.153548	0.292923	F_9
F_{10}	0.621836	-0.1737	-0.13907	-0.27947	-0.14721	-0.06666	-0.16976	-0.19129	-0.20851	0.240044	**0.7252**	-0.11746	0.581446	F_{10}
F_{11}	0.237728	-0.12113	-0.28517	-0.21551	-0.24314	-0.23312	-0.18445	-0.15541	-0.04332	0.25527	0.161381	**0.72555**	0.016398	F_{11}
F_{12}	0.16036	-0.24043	-0.23707	-0.32648	-0.2312	-0.17049	-0.14654	-0.09177	-0.08377	-0.00702	0.199214	0.212345	**0.46304**	F_{12}

T_a, T_b, and T_c. This implementation enables the system to activate one TRIAC semiconductor switch during the occurrence of a switch fault. In doing so, the faulty arm can be connected and remain separated from the fault-tolerant control during normal operation, thereby preventing the faulty arm from interfering with the operation of the main circuit. Additionally, switches S_{t1}^{+} and S_{t2}^{-} can conduct T_t and the corresponding TRIAC semiconductor switch when faults occur in

TABLE 4. Recognition results of different switch faults after adding a ±5% deviation into the input data when the inverter operated at 60 Hz.

Fault type	Deviation	Fault correlation degree													Recognition result
		F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8	F_9	F_{10}	F_{11}	F_{12}	
F_0	5%	0.889272	-0.268	-0.29827	-0.34211	-0.30599	-0.17227	-0.2478	-0.18455	-0.06252	0.307574	0.710135	0.035862	0.518086	F_0
	-5%	0.666274	-0.24643	-0.27247	-0.32354	-0.24771	-0.09329	-0.10045	-0.07298	-0.10533	0.180604	0.622434	0.110972	0.267922	
F_1	5%	-0.42834	0.710953	0.107611	-0.28954	-0.38256	-0.28359	-0.36252	0.298458	-0.20662	-0.39996	-0.31004	-0.3228	-0.40875	F_1
	-5%	-0.47859	0.827695	0.274775	-0.16388	-0.33482	-0.35464	-0.5837	-0.04231	-0.16622	-0.45044	-0.54103	-0.36711	-0.4874	
F_2	5%	-0.4415	0.205457	0.710489	-0.39463	-0.22536	-0.48472	-0.41087	0.097365	0.258515	-0.48394	-0.33068	-0.41553	-0.40499	F_2
	-5%	-0.48717	0.121269	0.828239	-0.34905	-0.27255	-0.40344	-0.47418	-0.02738	0.3093	-0.50708	-0.3678	-0.47079	-0.44111	
F_3	5%	-0.60692	-0.25209	-0.49096	0.501111	0.036432	0.047551	0.148568	-0.52595	-0.61178	-0.51594	-0.48335	-0.45379	-0.59854	F_3
	-5%	-0.65307	-0.34141	-0.46534	0.748091	0.080079	0.173542	-0.23104	-0.6798	-0.5672	-0.55861	-0.97254	-0.48297	-0.67298	
F_4	5%	-0.44631	-0.40811	-0.29787	0.042568	0.683795	-0.20602	0.31354	-0.43309	-0.33936	-0.46034	-0.33314	-0.3728	-0.42097	F_4
	-5%	-0.50588	-0.3636	-0.21551	0.238987	0.49849	-0.11856	0.203255	-0.50739	-0.45073	-0.48896	-0.38231	-0.43515	-0.47309	
F_5	5%	-0.40364	0.888814	0.212735	-0.28515	-0.37854	-0.26174	-0.33892	0.200834	-0.2061	-0.36667	-0.28538	-0.31677	-0.386	F_5
	-5%	-0.45624	0.666784	0.321365	-0.1684	-0.33887	-0.33911	-0.57605	-0.12955	-0.16511	-0.42032	-0.57026	-0.33679	-0.46682	
F_6	5%	-0.46374	0.207698	0.889049	-0.38645	-0.22169	-0.45626	-0.44234	0.070763	0.29521	-0.50073	-0.35136	-0.44762	-0.4223	F_6
	-5%	-0.51062	0.129405	0.66669	-0.33988	-0.31936	-0.38779	-0.50265	0.013376	0.175326	-0.52227	-0.38651	-0.49407	-0.4772	
F_7	5%	-0.60735	-0.29056	-0.42029	0.889061	0.127649	0.284207	0.134886	-0.58071	-0.51997	-0.54282	-0.48021	-0.46123	-0.60073	F_7
	-5%	-0.65346	-0.38759	-0.37771	0.66663	0.24279	0.242898	-0.17588	-0.72647	-0.56922	-0.56517	-1.0604	-0.51515	-0.67496	
F_8	5%	-0.44032	-0.43564	-0.30341	0.088327	0.889012	-0.20333	0.386691	-0.42976	-0.34182	-0.45672	-0.32431	-0.37474	-0.41299	F_8
	-5%	-0.49599	-0.38653	-0.21388	0.274259	0.666704	-0.11709	0.175296	-0.50188	-0.449	-0.48569	-0.37432	-0.43621	-0.45458	
F_9	5%	-0.41038	0.731614	0.076395	-0.30572	-0.38197	-0.26068	-0.34061	0.323749	-0.23321	-0.37858	-0.29325	-0.32791	-0.38956	F_9
	-5%	-0.46234	0.707007	0.235101	-0.16937	-0.34288	-0.33853	-0.54912	-0.01726	-0.18898	-0.4311	-0.47032	-0.34465	-0.47004	
F_{10}	5%	-0.4859	0.22984	0.766852	-0.37118	-0.22821	-0.45121	-0.45476	0.050152	0.197018	-0.51441	-0.3723	-0.45654	-0.44205	F_{10}
	-5%	-0.53067	0.146904	0.777234	-0.32606	-0.3245	-0.40371	-0.51389	-0.10136	0.260361	-0.53465	-0.40545	-0.50451	-0.50276	
F_{11}	5%	-0.61228	-0.27925	-0.44943	0.696494	0.059043	0.113921	0.08596	-0.5661	-0.54915	-0.5407	-0.48648	-0.45805	-0.60353	F_{11}
	-5%	-0.65792	-0.37736	-0.40408	0.748652	0.136638	0.238541	-0.29196	-0.71612	-0.55985	-0.56842	-1.01585	-0.51228	-0.67749	
F_{12}	5%	-0.40969	-0.40881	-0.31154	0.039601	0.49809	-0.23197	0.329801	-0.39889	-0.30159	-0.42645	-0.29347	-0.33315	-0.38427	F_{12}
	-5%	-0.46731	-0.3644	-0.17828	0.230325	0.463587	-0.14113	0.195375	-0.47825	-0.41175	-0.4583	-0.34642	-0.39928	-0.42789	

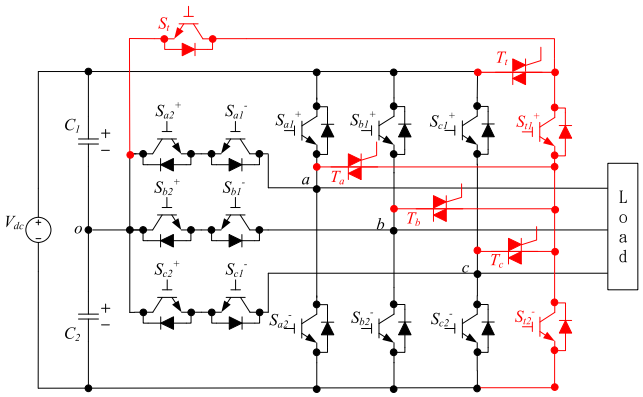


FIGURE 13. Three-level T-type inverter fault-tolerant control circuit.

the switches that are situated in the upper and lower arms (i.e., S_{x1}^+ or S_{x2}^-, x represents a, b or c). Therefore, by transmitting switch fault activation signals to switches S_{t1}^+ and S_{t2}^-, the two switches can function as a substitute for the faulty switch, thereby performing fault-tolerant control. In addition, the system adopts S_t and S_{t1}^+ as a substitute for the middle arm during fault occurrences in the middle arm.

A. FAULT-TOLERANT CONTROL ANALYSIS

Figure 14 displays the fault-tolerant control process. After the fault diagnosis system identifies the fault location, the system conducts fault-tolerant control in accordance with the fault location. For example, if the fault location is in the switch in the upper or lower arms (i.e., S_{x1}^+ or S_{x2}^-), the system simultaneously deactivates the arms where the faults occurred while conducting T_x and T_t, thereby connecting the fault-tolerant arm to the faulty location. Subsequently, the system transfers the pulse width modulation (PWM) control signal of the faulty switch to the fault-tolerant switch (i.e., transferring S_{x1}^+ to S_{t1}^+ and S_{x2}^- to S_{t2}^-), thereby completing the fault-tolerant control process. If faults occur in the middle arm, the system simultaneously deactivates the two switches bridging over the neutral point (i.e., S_{x1}^- and S_{x2}^+) and activates T_x to connect the fault-tolerant arm to the fault component. Subsequently, the faulty PWM control signal of the faulty switch is transmitted to the fault-tolerant switch (i.e., transferring S_{x1}^- to S_{t1}^+ and S_{x2}^+ to S_t), thus completing the fault-tolerant control process.

Figure 15 shows the fault-tolerant control process when an open circuit fault occurs in S_{a1}^+. First, the system turns-off the switches in the faulty arm (S_{a1}^+ and S_{a2}^-) and conducts T_a and T_t to connect the faulty arm to the faulty component. Subsequently, the PWM control signal of the faulty switch is transmitted into the fault-tolerant switch (i.e., transferring S_{a1}^+ to S_{t1}^+ and S_{a2}^- to S_{t2}^-), thus completing the fault-tolerant control process.

Figure 16 shows the process when an open switch fault occurs in the middle arm (S_{b1}^-). First, the system disables the control signals of the two switches (S_{b1}^- and S_{b2}^+) that are

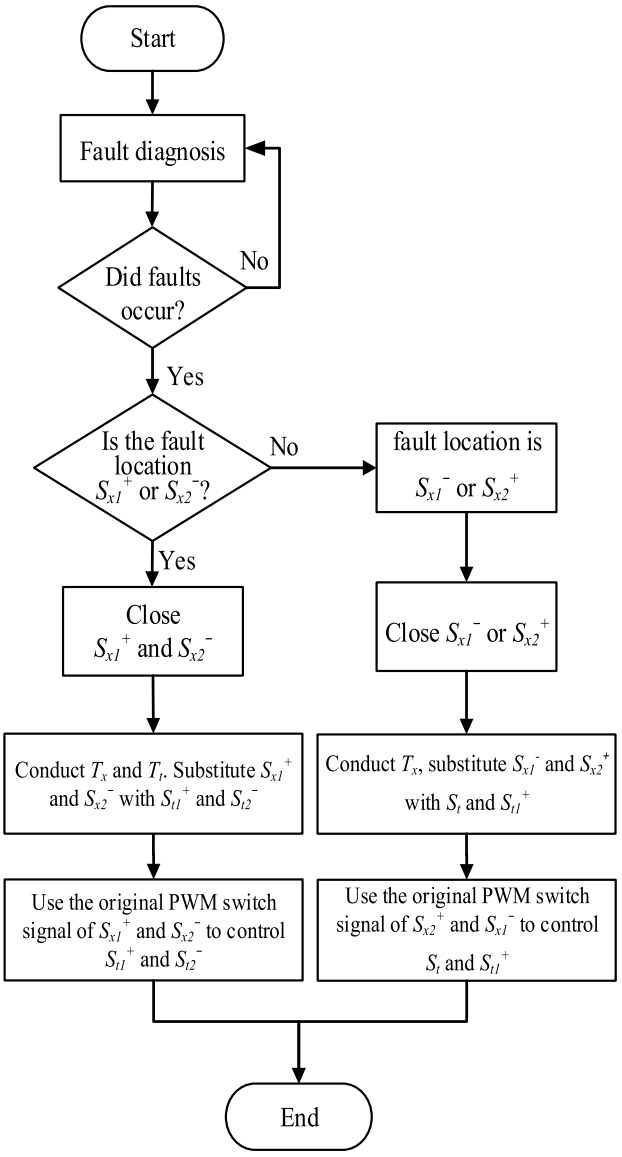


FIGURE 14. Fault-tolerant control system process.

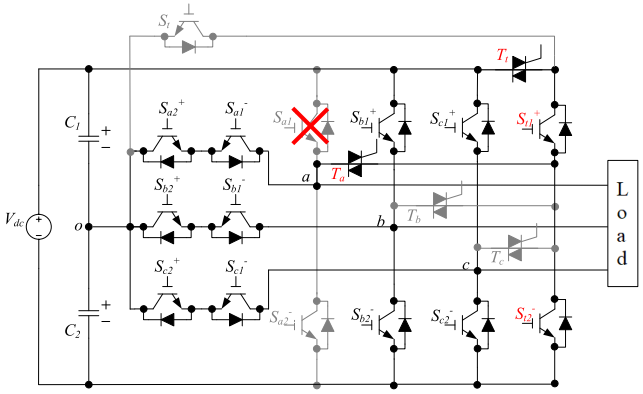


FIGURE 15. Fault-tolerant control during an S_{b1}^{-} open switch fault.

connected to the neutral point and conducts T_b to connect the fault-tolerant arm to phase b. Subsequently, the system transfers the PWM control signals of S_{b2}^{+} and S_{b1}^{-} to the

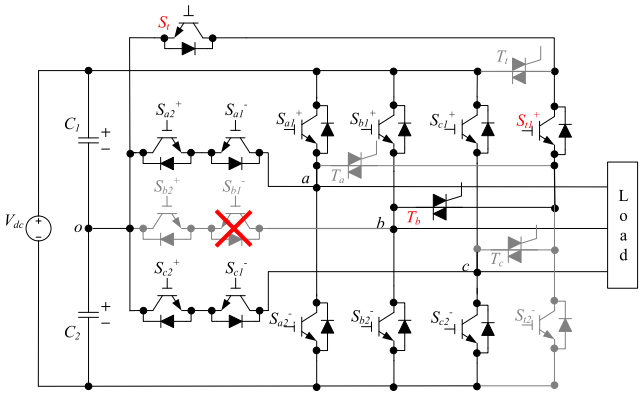


FIGURE 16. Fault-tolerant control during an S_{b2}^{+} open switch fault.

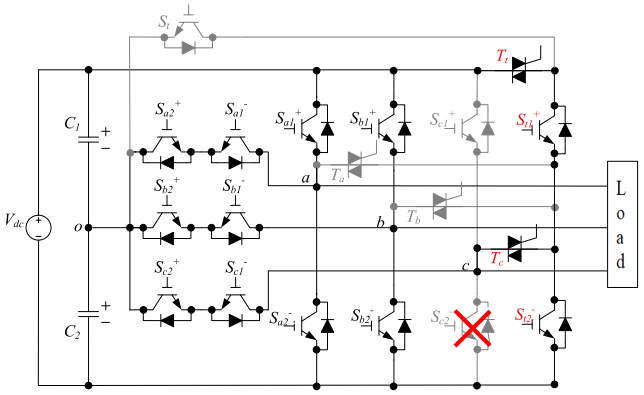


FIGURE 17. Fault-tolerant control during an S_{c2}^{-} open switch fault.

fault-tolerant switch (i.e., transferring S_{b1}^{-} to S_{t1}^{+} and S_{b2}^{+} to S_t), thereby completing the fault-tolerant control process. This process enables the system to maintain normal operation and keeps the quality of the power supply at acceptable levels.

Figure 17 shows the process when an open switch fault occurs in S_{c2}^{-}. First, the system turns-off the switches on the faulty arms (i.e., S_{c1}^{+} and S_{c2}^{-}) and conducts T_c and T_t to connect the faulty tolerant arm to phase c. Subsequently, the system transfers the PWM control signal of the faulty switches to the fault-tolerant switches (i.e., transferring S_{c1}^{+} to S_{t1}^{+} and S_{c2}^{-} to S_{t2}^{-}), thereby completing the fault-tolerant control process. This process enables the system to maintain normal operation and keeps the quality of the power supply at acceptable levels.

B. MEASUREMENT RESULTS FOR THE FAULT-TOLERANT CONTROL

This study used switches S_{a1}^{+}, S_{b1}^{-}, and S_{c2}^{-} to the test fault-tolerant control performance during fault occurrences. The fault was set to occur at 0.04 s, and the fault-tolerant control was set to activate at 0.12 s. Waveforms were observed to verify the efficiency of the proposed fault-tolerant method.

Figure 18 illustrates the fault-tolerant control results during an S_{a1}^{+} open switch fault. Specifically, when the fault occurred in S_{a1}^{+} at 0.04 s, the waveform of the line voltages v_{ab} and v_{ca} exhibited notable changes. These changes

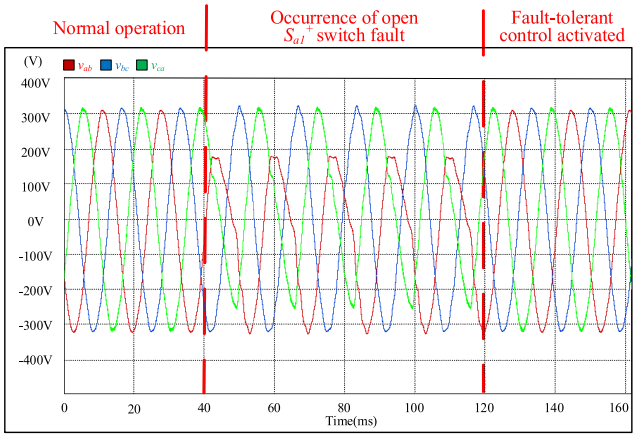


FIGURE 18. Measurement results for the fault-tolerant control during an S_{a1}^{+} open circuit fault.

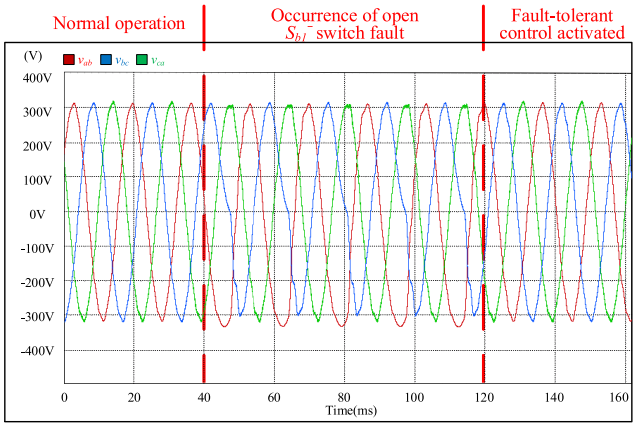


FIGURE 19. Measurement results for the fault-tolerant control during an S_{b1}^{-} open circuit fault.

persisted until 0.12 s, which was when the fault-tolerant control was activated—where T_a and T_t were conducted to connect the fault-tolerant arm to the faulty phase. The PWM control signal of the faulty switch was subsequently transferred to the fault-tolerant switch (i.e., the transfers of S_{a1}^{+} to S_{t1}^{+} and S_{a2}^{-} to S_{t2}^{-}). After the completion of the fault-tolerant control process, the output voltage waveforms returned to normal, and the balance of the three phases was maintained.

Figure 19 shows the measurement results for the fault-tolerant controls when an S_{b1}^{-} open switch fault occurred. The figure reveals that after the occurrence of a fault at S_{b1}^{-} at 0.04 s, the line voltage waveforms v_{ab} and v_{bc} exhibited considerable change. This change persisted until 0.12 s, which was when the fault-tolerant control was activated—where T_b was conducted, and the fault-tolerant arm was connected to the faulty phase. The PWM control signals for S_{b2}^{+} and S_{b1}^{-} were subsequently transferred to the fault-tolerant switches (i.e., the transfers of S_{b1}^{-} to S_{t1}^{+} and S_{b2}^{+} to S_t). After the completion of the fault-tolerant control process, the output voltage waveform returned to normal, and the balance of the three phases was maintained.

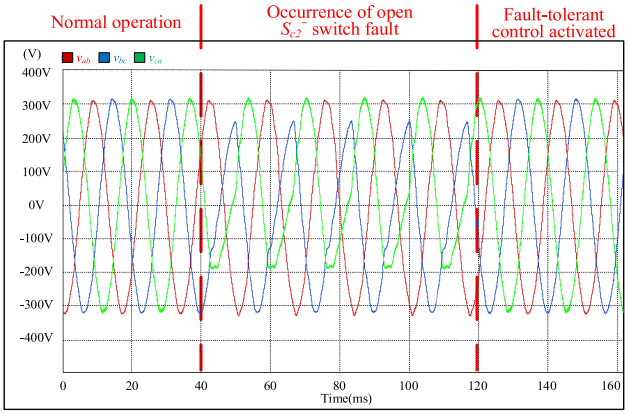


FIGURE 20. Measurement results for the fault-tolerant control during an S_{c2}^{-} open circuit fault.

Figure 20 displays the measurement results for the fault-tolerant control when an S_{c2}^{-} open switch fault occurred. The figure reveals that after the occurrence of a fault at S_{c2}^{-} at 0.04 s, the line voltage waveforms v_{bc} and v_{ca} exhibited considerable change. This change persisted until 0.12 s, which was when the fault-tolerant control was activated—where T_c and T_t were conducted to connect the fault-tolerant arm to the faulty phrase c. The PWM control signal of the faulty switch was subsequently transferred, by the system, to the fault-tolerant switch (i.e., the transfers of S_{c1}^{+} to S_{t1}^{+} and S_{c2}^{-} to S_{t2}^{-}). After the completion of the fault-tolerant control process, the output voltage waveform returned to normal, and the balance of the three phases was maintained.

VI. CONCLUSION

This study proposed an inverter fault diagnosis system that combines chaos theory with extension theory. The system identifies the location of faulty power transistors in three-level T-type inverters. When provided with single-phase voltage data, the system can accurately detect the locations of faulty switches. In addition, the fault diagnosis system does not require the undergoing of a learning process. The system consists of an internal fault tolerance function, thus lowering the influence of noise signals. When faults occur in any of the inverter's switches, the proposed fault-tolerant control strategy can immediately conduct fault-tolerant control using three IGBTs and four externally installed TRIAC semiconductor switches. This design enables the system to adjust the inverter circuit framework and maintain a constantly balanced three-phase voltage output, thereby greatly improving the power supply reliability of three-level T-type inverters. Finally, the measurement results revealed that the proposed inverter fault diagnosis system can correctly diagnose fault types, even under noise interference, as well as the location of faulty switches. The system was determined to be able to adopt fault diagnosis strategies to maintain consistent output voltage amplitudes for fault occurrences at any switch, thereby verifying the feasibility of the proposed fault-tolerant control method.

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