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Control Design and Performance Analysis of a Double-Switched LLC Resonant Rectifier for Unity Power Factor and Soft-Switching

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ABSTRACT This paper presents and analyzes an AC-DC power converter structure, which is comprised of a Power Factor Correction (PFC) module and a LLC resonant DC-DC converter module. This converter only uses two switches, and requires three less diodes and one less switch compared to popular LLC resonant converter solutions. Compared to its conventional counterpart, the rectifier of interest has high energy efficiency while a smaller size, owing to the soft-switching in the LLC resonant converter. Detailed theoretical analyses are conducted in this study, followed by software simulation and hardware experimentation, which demonstrate that the single stage double-switched (DS)-LLC rectifier is able to realize unity power factor and a wide output range, indicating its effectiveness and applicability.

INDEX TERMS AC-DC converter, power factor correction, LLC resonant converter.

I. INTRODUCTION

Due to unique advantages, LED lighting has been recognized as the most promising fourth-generation lighting solution, which has seen rapid development in recent years [1]–[3].

However, low efficiency and high cost are deemed the biggest problems in current LED drivers, especially for high-frequency operations. LLC resonant converter can realizes Zero Voltage Switch (ZVS) turn-on of switching transistor, Zero Current Switch (ZCS) turn-off of rectifier diode for wide-range inputs and loads [4], [5], low voltage stress of switching transistors and rectifier diodes [6], [7] and low switching loss, which can eliminate the reverse recovery problem of the rectifier diode, reduce the diode loss and improve the efficiency of the converter [8]. With these favorable features, LLC resonant converters are often used as LED drivers in high-frequency conditions.

Usually, a rectifier is placed before the LLC resonant converter. The single-phase AC-DC converters with isolated transformers have been widely applied to LED power supplies [9] as shown in Fig. 1(a). As a result, the diode rectifiers draw highly distorted current from the AC power source, leading to a poor input power factor (PF) [10], as shown in Fig. 1(b). Additionally, the traditional Switch Mode Power Supply (SMPS) with a rectifier bridge connected with the power grid suffers the distortion of the input current and generates a large number of harmonics, which deteriorates the input PF and can cause electromagnetic interferences (EMI) [11].

In order to reduce the harmonics and EMI pollution to the power grid, a pre-stage Boost PFC circuit can be introduced and connected with the diode bridge to shape the input AC current to be sinusoidal and in phase with the AC voltage [12]–[14].

Compared to other PFC solutions, the Boost PFC topology, as shown in Fig. 2 [15]–[17], has many advantages, such as simple structure, high PF and low EMI [18]–[20]. Thus it has had the widest adoption in the LED lighting industry [21]. As shown in Fig. 3, combined with a traditional LLC resonant converter, PFC function and a wide output range can be

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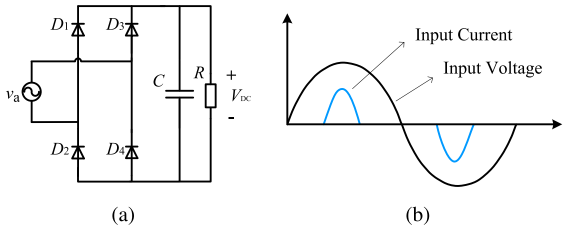


FIGURE 1. (a) Traditional diode rectifier with a capacitor connected at the DC output side. (b) Input voltage and current waveforms of the traditional diode rectifier.

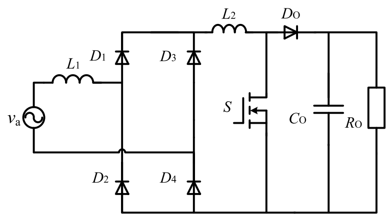


FIGURE 2. Traditional Boost PFC converter.

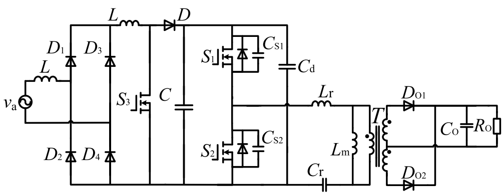


FIGURE 3. Traditional rectifier with PFC functions and LLC resonant converter.

achieved, and the voltage stress of the two power switches is proven to be reduced. Thus this topology has served as a prevailing LED lighting driver candidate [21], [22].

However, the above converter structure is normally composed of a diode bridge rectifier, a PFC stage and a DC-DC LLC resonant converter, which bears the disadvantages of needing too many switches, high component cost and energy waste. The same problem happens to the circuits such as [23] and [24], both of which use too many diodes, causing unnecessary energy loss due to forward voltage drop. It is therefore important to introduce a new converter topology that can solve these shortcomings whilst having a simple structure with fewer components.

Aware of the above issues, in this paper, we present and analyze a single-stage Double-Switched LLC AC-DC resonant converter that requires fewer components and has higher energy efficiency. This topology only requires two switches, which is realized through the pre-stage Boost topology and the LLC resonant converter sharing two common switches. The DS-LLC AC-DC resonant converter can realize both PFC and LLC functions with two fewer diodes compared with the converters in [23], [24]. Thus the original double-stage structure is reduced into a single-stage AC-DC topology. In addition, the number of diodes used in this converter is also smaller than that in the conventional topology. In order to verify the functionality and effectiveness of the DS-LLC

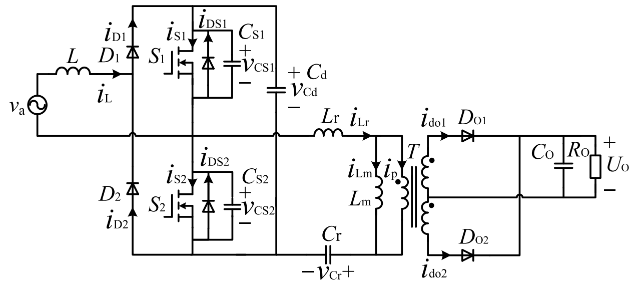


FIGURE 4. Topology of double-switched LLC resonant AC-DC converter.

resonant converter, simulation and experimentation are conducted in this study, which show great agreement with theoretical analyses, demonstrating the superiority of the presented converter over the conventional ones and also its wide applicability in energy conversion.

The remainder of the paper is organized as follows. In Section II, the working principle of the DS-LLC resonant converter is detailed, followed by the description of power factor correction function by this converter in Section III. Then, the matching design of switching frequency and the closed-loop design is elaborated in Section IV and Section V, respectively. Simulation and experimentation are presented in Section VI. Lastly, this paper concludes in Section VII.

II. WORKING PRINCIPLE OF OF THE DS-LLC CONVERTER

The DS-LLC resonant AC-DC converter is shown Fig. 4, and its working principle is analyzed as follows.

A. TOPOLOGY OF DS-LLC AC-DC RESONANT CONVERTER

As shown in Fig. 4, the converter is composed of a single-phase PFC circuit and a DC-DC LLC resonant converter, which collectively achieve unity PF correction, a wide output range and at the same time AC-DC conversion. Therein, the PFC circuit comprises an inductor L, two switches S_1 and S_2 (including their body diodes and capacitors), two diodes D_1 and D_2, and a linking capacitor C_d, whereas the isolated DC-DC LLC resonant converter is composed of two shared switches S_1 and S_2, a resonant capacitor C_r, a transformer T, two rectifier diodes D_{O1}, D_{O2} and an output capacitor filter C_O. A transformer T contains the magnetizing inductor L_m and leakage inductor L_r. With two shared switches being ON and OFF, the introduced converter can realize both PFC and LLC functions.

Compared to the traditional topology which consists of a pre-stage Boost topology and the LLC resonant converter, this topology has the following advantages:

- A simpler structure of bridgeless boost PFC to obtain high PF;
- One less power switch since PFC circuit stage shares a pair of switches with the LLC resonant converter stage;
- High energy efficiency achieved by soft-switching in the LLC resonant stage;

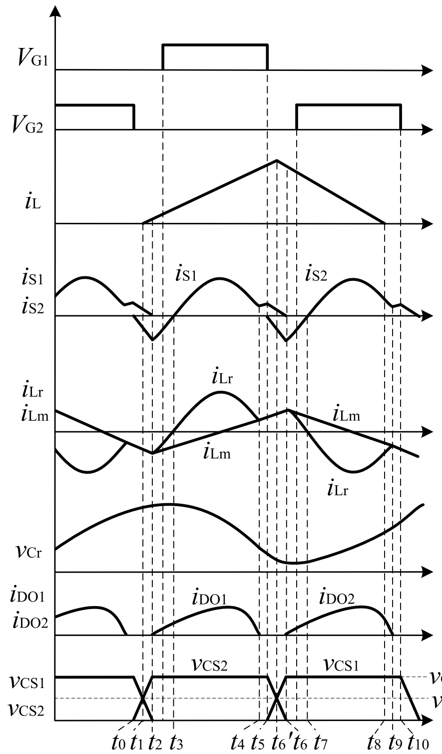


FIGURE 5. Time-domain operations of the DS-LLC AC-DC converter with PFC.

- A wide output range achieved by pulse frequency modulation(PFM) control which can be applied to step-load change and stabilize the output voltage;
- A very compact structure and artful design: a resonant capacitor is added to resonate with the resonant inductor which is integrated with the transformer on the magnetic core, so the magnetizing inductor and leakage inductor in the transformer are fully utilized.

B. TIME-DOMAIN OPERATIONS AND OPERATION MODES

Time-domain operations of the DS-LLC AC-DC conversion system are shown in Fig. 5, wherein there are ten operation modes for the positive half cycle as shown in Fig. 6. The arrow shows the reference current directions. TABLE 1 shows switches' ON-OFF statuses in the ten operation modes. Detailed analysis of each mode is described as follows.

Mode 1 (**$t_0 < t < t_1$**)**:** Positive half-cycle begins at $t = t_0$, when the switches S_1 and S_2 are off. The diodes D_1 and D_2 are off, and the equivalent circuit is shown as Fig. 6(a). The current flowing into inductor L_m, namely i_{Lm}, is equal to the current of resonant inductor L_r, namely i_{Lr}. L_m starts to resonate with L_r and C_r, and the primary current of the transformer T, namely $i_p = 0$. Then, diodes D_{O1} and D_{O2} turn off due to the endured negative voltage. The output is insulated by transformer T. In loop $C_O - R_O$, capacitor C_O produces energy, which is consumed by load R_O. The resonant current i_{Lr} charges the parasitic capacitor of switch S_2, namely C_{S2}, and discharges the parasitic capacitor of S_1, namely C_{S1}, creating ZVS conditions [25], [26].

TABLE 1. Switching states.

Mode	S_1	S_2	D_1	D_2	D_{O1}	D_{O2}
Mode 1	OFF	OFF	OFF	OFF	OFF	OFF
Mode 2	OFF	OFF	ON	OFF	OFF	OFF
Mode 3	OFF	OFF	ON	OFF	ON	OFF
Mode 4	ON	OFF	ON	OFF	ON	OFF
Mode 5	ON	OFF	ON	OFF	OFF	OFF
Mode 6	OFF	OFF	ON	OFF	OFF	OFF
Mode 7	OFF	OFF	ON	OFF	OFF	ON
Mode 8	OFF	ON	ON	OFF	OFF	ON
Mode 9	OFF	ON	OFF	OFF	OFF	ON
Mode 10	OFF	OFF	OFF	OFF	OFF	OFF

Mode 2 (**$t_1 < t < t_2$**)**:** At $t = t_1$, when the voltage of C_{S1}, i.e., v_{CS1}, is smaller than the input voltage v_a, diode D_1 turns on, and the inductor L starts absorbing energy and enduring voltage ($v_a - v_{CS1}$). The equivalent circuit is shown as Fig. 6(b). Then, v_{CS1} decreases to 0 at $t = t_2$ and Mode 2 completes.

Mode 3 (**$t_2 < t < t_3$**)**:** The equivalent circuit of Mode 3 is shown in Fig. 6(c), when v_{CS1} decreases to 0 at $t = t_2$. The free-wheel diode of S_1, namely D_{S1}, is turned on, which results in Zero-Voltage-Switching (ZVS) turn-on of S_1. The driving signal of S_1 is on but S_1 is still off because of the clamped diode D_{S1}. At the same time, the diode D_{O1} is turned on and primary voltage of T is clamped at nU_O, i.e., n (voltage ratio of T) times of output voltage. Then, the magnetizing inductor L_m absorbs energy under the primary voltage nU_O. L_r and C_r are in resonance, and one can obtain $i_p = i_{Lr} - i_{Lm}$. Inductor L absorbs energy and endures voltage v_a. When the resonant current i_{Lr} changes from negative to 0, Mode 3 completes.

Mode 4 (**$t_3 < t < t_4$**)**:** At $t = t_3$, Mode 4 as shown in Fig. 6(d) starts. i_{Lr} increases from 0 to positive and S_1 is turned on. Inductor L keeps absorbing energy and enduring voltage v_a and L_m keeps absorbing energy under the primary voltage nU_O. L_r and C_r are in resonance; meanwhile, D_1 is on, energy is transferred from C_d to R_O. Mode 4 finishes when $i_{Lm} = i_{Lr}$.

Mode 5 (**$t_4 < t < t_5$**)**:** At $t = t_4$, $i_{Lm} = i_{Lr}$, then L_m, L_r and C_r resonate. D_{O1} and D_{O2} endure negative voltage and then turn off. The output is insulated by transformer T. C_O charges load R_O, as shown in Fig. 6(e). Meanwhile, the inductor L absorbs energy from the input source.

Mode 6 (**$t_5 < t < t_6$**)**:** At $t = t_5$, S_1 and S_2 are turned off, D_{O1} and D_{O2} are also off. The current of inductor L_m is equal to the current of resonant inductor L_r, and L_m starts to resonate with L_r and C_r. C_O produces energy to load R_O. Resonant current i_{Lr} charges the parasitic capacitor C_{S1}, and C_{S2} discharges. At $t = t_6'$, v_{CS1} becomes larger than the

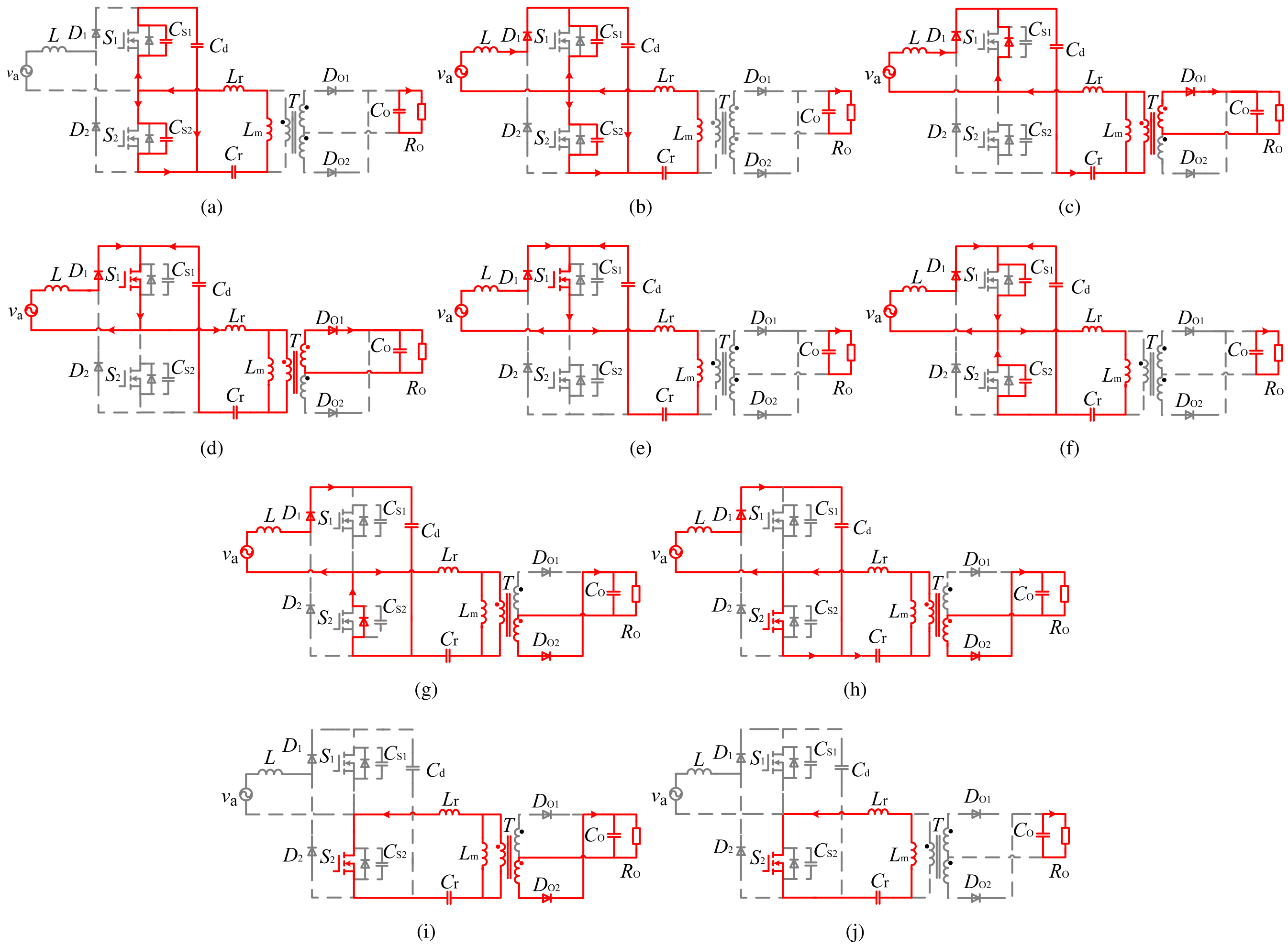


FIGURE 6. Equivalent circuit diagrams in each operating mode for the positive cycle of input voltage: (a)-(j) correspond to Modes 1-10 respectively(please refer to Fig. 4 for all voltage and current notations in the analysis).

input voltage v_a, and inductor L releases energy and endures voltage ($v_{CS1} - v_a$). Then, when C_{S2} discharges and v_{CS2} decreases to 0, D_{S2} is turned on and Mode 6 ends.

Mode 7 ($t_6 < t < t_7$)**:** In the time-domain operation curves in Fig. 5 at $t = t_6$, D_{S2} turns on, which meets the operating condition for ZVS. The driving signal of S_2 is on but S_2 is still off because of the clamped diode D_{S2}. The corresponding equivalent circuit is shown in Fig. 6(g), wherein inductor L produces energy to C_d under the voltage ($v_{Cd} - v_a$). Meanwhile, D_{O2} is turned on, and the primary voltage of T is clamped at $-nU_O$ and L_m rises linearly. L_r and C_r are in resonance and one can obtain $i_p = i_{Lr} - i_{Lm}$. Then, when the resonant current i_{Lr} decreased to 0, Mode 6 completes.

Mode 8 ($t_7 < t < t_8$)**:** At $t = t_7$ as shown in Fig. 6(h), $i_{Lr} = 0$ and begins to decrease to be negative. Then, S_2 is turned on, and D_{O2} is also on. Similar to Mode 7, the primary voltage of T is clamped at $-nU_O$ and releases energy to L_m. L_r and C_r are in resonance. In the meantime, i_{Lr} goes through L_m and the primary side of T, and then transfers energy to R_O. L releases energy to C_d. When i_L decreases to 0 and D_1 endures negative voltage and turns off, Mode 8 finishes.

Mode 9 ($t_8 < t < t_9$)**:** As shown in Fig. 6(i) at $t = t_8$, $i_L = 0$ and L_m and the primary side of T transfer energy to R_O. When i_{Lm} reaches i_{Lr}, Mode 9 completes.

Mode 10 ($t_9 < t < t_{10}$)**:** As shown in Fig. 6(j), at $t = t_9$, $i_{Lm} = i_{Lr}$ and L_m begins to take part in resonance. D_{O1} and D_{O2} endure negative voltages and turn off. The output is insulated by transformer T, and C_O charges load R_O.

III. POWER FACTOR CORRECTION OF THE DS-LLC RESONANT CONVERTER

Since a large number of articles have elaborated how LLC resonant converter works in the secondary resonant region such as [27]–[29], this section mainly focuses on the realization of the PFC function. In order to ensure successful power factor correction, it is necessary to increase the inductor current from zero to the peak value and then decrease the inductor current from the peak value to zero within one cycle [30], [31]. Since the implementation of the LLC resonant function requires a constant duty cycle of 0.5, the inductor current needs to be reduced to zero in fixed duty cycle.

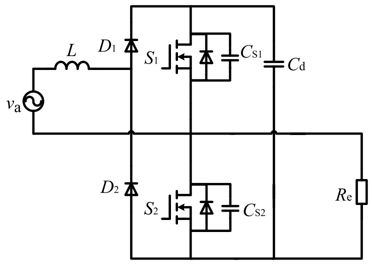


FIGURE 7. The equivalent topology of pre-stage converter.

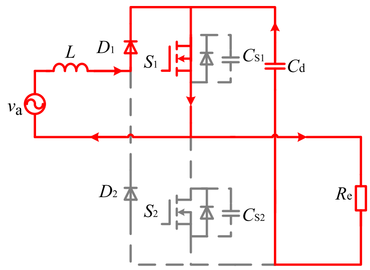


FIGURE 8. Operation of the converter when the switch S_1 is turned on and the S_2 is turned off.

Since the LLC resonant converter is equivalent to a load connected to the pre-stage Boost PFC converter, the following LLC resonant converter is simplified as a resistive load in order to explain the realization of PFC, as shown in the Fig. 7. Because the dead zone is much smaller than one switching cycle, the dead zone is ignored. Taking the positive half cycle as an example, when the switch S_1 is turned on and the S_2 is turned off, the operation of the converter is shown in Fig. 8, and the relationship between inductor current and the input voltage can be expressed as:

$$v_a = v_L = L\frac{di_L}{dt} = \frac{Li_{Lp}}{d_1 T_S}, \tag{1}$$

$$\frac{dv_{Cd}}{dt} = -\frac{v_{Cd}}{R_e C_d}, \tag{2}$$

where i_L is the inductor current, u_L is the inductor voltage, T_S is the switching period, v_{Cd} is the voltage of the linking capacitor, and d_1 is the duty cycle during which the inductor current increases. We can obtain that the peak value of the inductor current i_{LP} is

$$i_{LP} = \frac{v_a}{Lf_S} d_1, \tag{3}$$

where f_S is the switching frequency.

When switch S_2 is turned on and S_1 is turned off, the operation of the converter is as shown as Fig. 9, and the relationship between inductor current and output voltage of the pre-stage can be expressed as:

$$v_a = u_L + v_{Cd} = L\frac{di_L}{dt} + v_{Cd} = -\frac{Li_{LP}}{d_2 T_S} + v_{Cd}, \tag{4}$$

$$U_{Re} = 0, \tag{5}$$

where d_2 is the duty cycle during which inductor current decreases to zero and U_{Re} is the voltage across R_e.

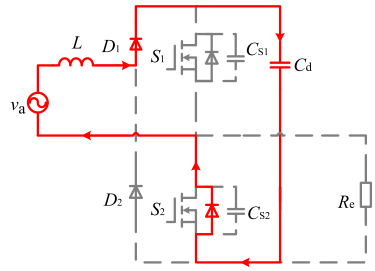


FIGURE 9. The operating state of the converter when the switch S_2 is turned on and the S_1 is turned off.

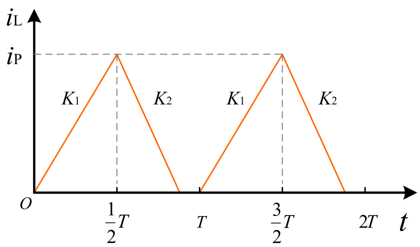


FIGURE 10. The inductor current.

The magnitude of the drop in the inductor current is thus:

$$-i_{LP} = \frac{v_a - v_{Cd}}{Lf_S} d_2. \tag{6}$$

From (3) and (6), we can get

$$d_2 = \frac{U_m \sin \omega t}{v_{Cd} - U_m \sin \omega t} d_1, \tag{7}$$

where $v_a = U_m \sin \omega t$.

From the above equations, if PFC is implemented, we will have

$$d_2 < d_1 = 0.5, \tag{8}$$

namely

$$\frac{U_m \sin \omega t}{v_{Cd} - U_m \sin \omega t} d_1 < 0.5. \tag{9}$$

Simplifying formula (9), we can have

$$v_{Cd} > 2U_m \sin \omega t. \tag{10}$$

Equation (10) indicates that to ensure the functionality of the PFC module, the voltage across the linking capacitor v_{Cd} must be at least twice the peak value of the input voltage v_a, i.e.,

$$v_{Cd} > 2U_m. \tag{11}$$

In other words, because the slope of the inductor current is proportional to the voltage across it, as shown in the Fig. 10, when the inductor current rises, the slope K_1 is calculated as,

$$K_1 = \frac{U_m \sin \omega t}{L}, \tag{12}$$

and when the inductor current drops, its slope K_2 is

$$K_2 = \frac{U_m \sin \omega t - v_{Cd}}{L}. \tag{13}$$

Since the duty cycle is constantly 0.5, to ensure the implementation of PFC, it should be ensured that $K_1 < -K_2$, i.e.,

$$v_{Cd} > 2U_m. \tag{14}$$

Therefore, to ensure the PFC module is functional, the inductor current should be reduced by adjusting v_{Cd}, that is, the energy stored in the inductor is transferred to the linking capacitor v_{Cd}. The following relationship shows the v_{Cd} and other factors, and the average input power of every switching cycle during the positive half-frequency cycle is:

$$P_{in} = \frac{2}{T}\sum_{n=1}^{N} U_m \sin(\pi n/N) i_{LP}(d_1 + d_2)T_S/2, \tag{15}$$

where $N = T/2T_S$, T is the period of input voltage.

Substituting (3) and (7) into (15), we can have:

$$P_{in} = \frac{1}{T}\sum_{n=1}^{N} \frac{v_{Cd}U_m^2 \sin^2(\pi n/N)}{v_{Cd} - U_m \sin(\pi n/N)} d_1^2 T_S^2/L. \tag{16}$$

Since $v_{Cd} = U_{Re}$, and T_S is small enough relative to T, (16) can be expressed as,

$$P_{in} = \frac{v_{Cd}d_1^2}{2\pi Lf_S}\int_0^{\pi} \frac{(U_m \sin \omega t)^2}{v_{Cd} - U_m \sin \omega t} d\omega t. \tag{17}$$

Since the linking capacitor C_d only supplies energy to the load when S_1 is turned on and S_2 is turned off, the output power is obtained as,

$$P_{out} = \frac{v_{Cd}^2}{2R_e}. \tag{18}$$

Suppose the efficiency is 1, namely $P_{in} = P_{out}$; one can have

$$\frac{v_{Cd}d_1^2}{2\pi Lf_S}\int_0^{\pi} \frac{(U_m \sin \omega t)^2}{v_{Cd} - U_m \sin \omega t} d\omega t = \frac{v_{Cd}^2}{2R_e}. \tag{19}$$

Simplifying (19) yields:

$$d_1^2 = \frac{\pi Lf_S v_{Cd}}{R_e} \frac{1}{\int_0^{\pi} \frac{(U_m \sin \omega t)^2}{v_{Cd} - U_m \sin \omega t} d\omega t} = 0.5^2. \tag{20}$$

It can be seen from (20) that when the load R_e and frequency f_S are constant, if the converter is able to realize the PFC function, the critical value of L is,

$$L = \frac{R_e}{8\pi U_m f_S}\int_0^{\pi} \frac{(U_m \sin \omega t)^2}{2U_m - U_m \sin \omega t} d\omega t. \tag{21}$$

When R_e, f_S,v_a are fixed, the relationship between L and v_{Cd} is shown as Fig. 11.

Therefore, in order to ensure the realization of PFC, it is necessary to employ inductor values below the critical value of L.

The LLC resonant converter module can be viewed an impedance. When the LLC resonant converter runs in

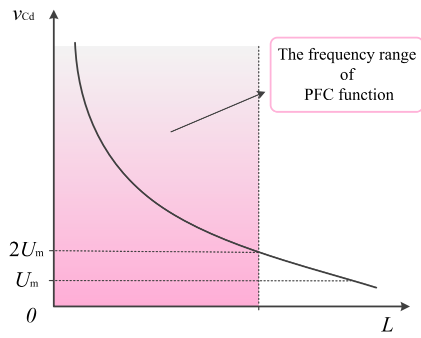


FIGURE 11. The relationship between L and v_{Cd}.

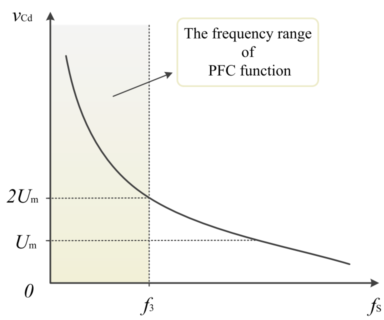


FIGURE 12. The relationship between f_S and v_{Cd}.

ZVS or ZCS conditions, it can be regarded as an inductive impedance $Z = R + jX$, so when applying the above theory, equation (18) can be converted to

$$P_{out} = \frac{v_{Cd}^2}{2|Z|}\cos\varphi_z, \tag{22}$$

where $\varphi_z = \arctan(X/R)$.

The relation between v_{Cd} and L can be analyzed with a similar procedure.

IV. FREQUENCY MATCHING

Since the LLC resonant converter works in a wide frequency range, the switching frequency f_S may affect the realization of the PFC in pre-stage PFC module. Therefore, before carrying out the simulation and experiment, it is necessary to match the frequency range in which the two functions can be implemented simultaneously. From (21), the relationship between the switching frequency f_S and v_{Cd} is shown in Fig. 12:

According to the working condition of the PFC in the Boost topology, the voltage of the linking capacitor v_{Cd} should be at least twice as large as the peak value of the input voltage v_a, namely U_m. Therefore, in order to ensure the implementation of PFC and LLC resonant function, the range of frequency f_S can be selected is $f_2 < f_S < \min[f_1, f_3]$ (assuming $f_2 < f_3 < f_1$), where $f_1 = 1/(2\pi\sqrt{L_r C_r})$, $f_2 = 1/(2\pi\sqrt{(L_r + L_m)C_r})$, f_3 is the critical frequency of the Boost PFC module:

$$f_3 = \frac{|Z|}{8\pi U_m L \cos\varphi_z}\int_0^{\pi} \frac{(U_m \sin \omega t)^2}{2U_m - U_m \sin \omega t} d\omega t. \tag{23}$$

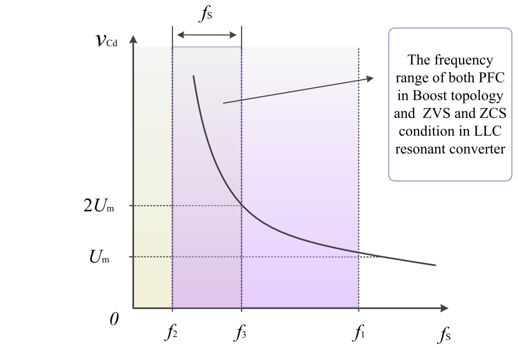


FIGURE 13. The range of frequencies to ensure the simultaneous implementation of pre-stage Boost PFC and the function of the LLC resonant converter.

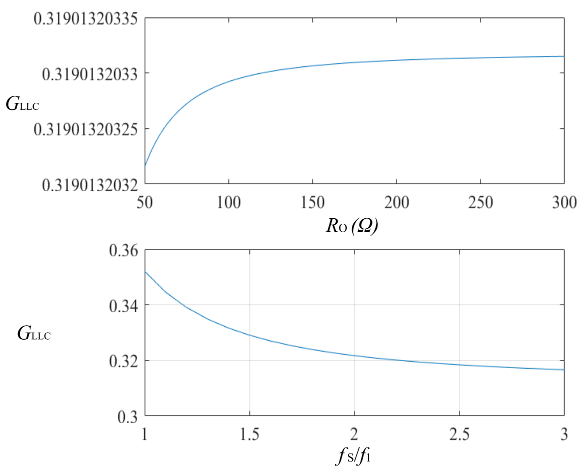


FIGURE 14. Relationship between gain G_{LLC} and frequency f_S and load R_O.

The frequency range that can be selected is shown in Fig. 13.

V. CLOSED-LOOP DESIGN OF THE DS-LLC RESONANT CONVERTER

Since the load often changes, it is necessary to design a control method to stabilize the output voltage in order to adapt to wide output range. According to [32], [33], based on FHA, we can obtain the gain of the LLC resonant converter as:

$$G_{LLC} = \frac{1}{2n}\frac{1}{\sqrt{(1+k-\frac{k}{(\frac{f_S}{f_1})^2})^2 + Q^2((\frac{f_S}{f_1})^2 - \frac{1}{(\frac{f_S}{f_1})^2})^2}}, \tag{24}$$

where $k = L_r/L_m$, $Q = (2\pi f_1 L_r)/(n^2 R_O)$.

Here, $Q = 0.195$, and the relationship between G_{LLC} and load R_O is shown in the Fig. 14 with the relationship between G_{LLC} and switching frequency f_S shown in the same figure.

The voltage across the linking capacitor v_{Cd} in the pre-stage PFC converter decreases as frequency f_S increases. Therefore, when load R_O changes, the switching frequency f_S can be changed to ensure gain G_{LLC} is constant, and consequently the output voltage U_O is constant.

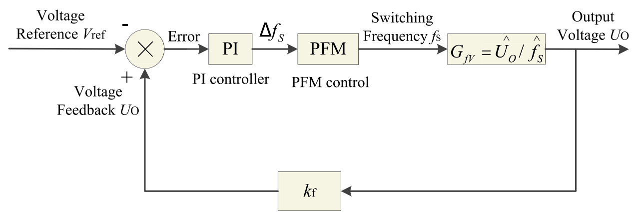


FIGURE 15. Control of the DS-LLC resonant converter($k_f = 1$).

The control based on pulse frequency modulation(PFM) is designed as shown in Fig. 15. Through small signal analysis, the open-loop transfer function of the output voltage G_{fV} is obtained as:

$$G_{fV} = \frac{b_2 s^2 + b_1 s}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}, \tag{25}$$

where

$$\begin{cases} b_1 = -[8000 v_{Cd}\omega^4 L^3 f_S k f_1(1+k-kf_1/f_S)/(2\pi f_S^2) \\ \quad + 8000 v_{Cd}\omega^4 L^3 f_S Q^2 (f_S/f_1 - f_1/f_S) \\ \quad \cdot [1/(2\pi f_1) + f_1/(2\pi f_S^2)]] \\ \quad /n[(1+k-kf_1/f_S)^2 + Q^2(f_S/f_1 - f_1/f_S)^2]^{3/2}, \\ b_2 = r_{CO} C_O b_1, \\ a_0 = 32 v_{Cd} U_m \omega^3 - 16 U_m^2 \omega^2 - 16 v_{Cd}^2 \omega^4, \\ a_1 = a_0/(Q f_S) + R_O C_O a_0, \\ a_2 = 32 v_{Cd} U_m \omega - 32 v_{Cd}^2 \omega^2 + a_0/f_S^2 + R_O C_O a_0/(Q f_S), \\ a_3 = R_O C_O a_0/(f_S^2) + (32 v_{Cd} U_m \omega - 32 v_{Cd}^2 \omega^2)/(Q f_S) \\ \quad + R_O C_O (32 v_{Cd} U_m \omega - 32 v_{Cd}^2 \omega^2), \\ a_4 = (32 v_{Cd} U_m \omega - 32 v_{Cd}^2 \omega^2)/f_S^2 \\ \quad + [R_O C_O (32 v_{Cd} U_m \omega - 32 v_{Cd}^2 \omega^2)]/(Q f_S), \\ a_5 = [R_O C_O (32 v_{Cd} U_m \omega - 32 v_{Cd}^2 \omega^2)]/f_S^2. \end{cases} \tag{26}$$

Term r_{CO} is the parasitic resistance of the output capacitor C_O. The frequency—domain simulation results are shown in Fig. 16. The uncompensated loop gain described in blue lines indicates a poor system response. Therefore, a PI compensator is used to increase the dynamic response, and the preferred crossover frequency of the output voltage loop is chosen as 1/9 of the stable switching frequency, namely 8.9kHz. The transfer function of the PI compensator is

$$G_P(s) = k_p + \frac{k_i}{s}, \tag{27}$$

where k_p and k_i are the proportional and integral gains. The parameters of the PI compensated loop gain are chosen as $k_p = 2.24 \times 10^{12}$ and $k_i = 1.44 \times 10^{17}$. The compensated loop gain of the output voltage loop is shown in Fig. 16 in red lines. It can be seen that the compensated loop gain has a crossover frequency of 8.92kHz with a phase margin of 50.3°, which indicates a better dynamic response.

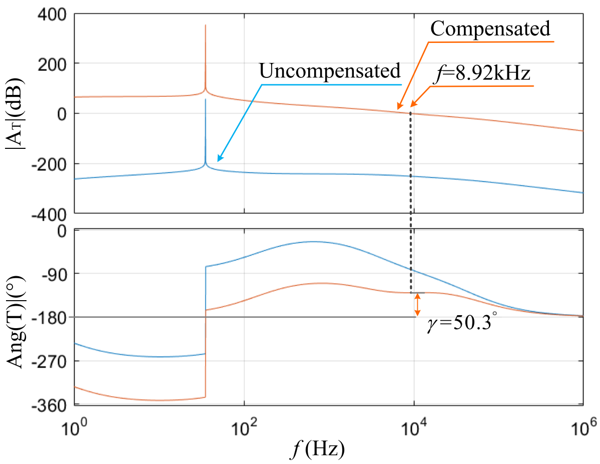


FIGURE 16. Frequency response of the output voltage loop.

TABLE 2. Simulation parameters of LLC resonant converter.

Input voltage v_a	60V(50Hz)
Input power P_{in}	100W
Transformer ratio n	17:12:12
Resonant inductor L_r	78μH
Resonant Capacitor C_r	32nF
Magnetizing inductor L_m	620μH
Rated switching frequency f_S	80kHz
Rated output voltage U_O	100V
Rated voltage of the linking capacitor v_{Cd}	300V
Range of output voltage U_O	90V-150V
Range of voltage of the linking capacitor v_{Cd}	270V-320V

VI. SIMULATION AND EXPERIMENTATION

In order to verify the functionality of the DS-LLC resonant AC-DC converter, simulation is conducted using PSIM software. Simulation parameters of the LLC converter are shown in TABLE 2.

According to (17), in order to ensure the realization of PFC, the expression of the critical Boost inductor L can be obtained as:

$$L = \frac{d_1^2}{\pi P_{in} f_S} \int_0^{\pi} \frac{(U_m \sin \omega t)^2}{2 - \sin \omega t} d\omega t \approx 50\mu\text{H}. \tag{28}$$

Therefore, we set the Boost inductor L value as 47μH.

A. SIMULATION RESULTS

As shown in Fig. 17, the DS-LLC resonant converter can realize Boost PFC function, where the input AC current is sinusoidal and in phase with the AC voltage. In the magnified figure, the rising slope of the input current is smaller than the absolute value of the falling slope. Therefore, the inductor current can fall to zero in the second half of the switching cycle after rising in half a switching cycle, meaning that the PFC is realized, which is consistent with the theory.

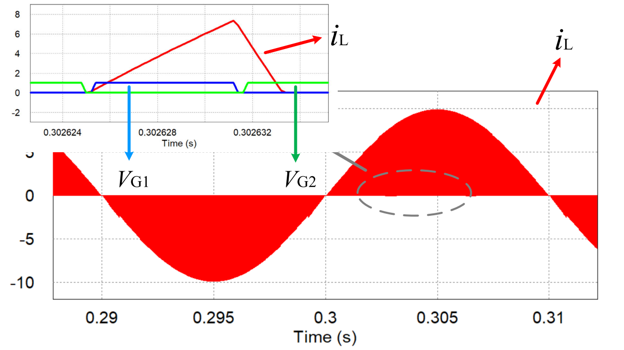


FIGURE 17. Simulation results of the DS-LLC resonant converter for Boost PFC verification.

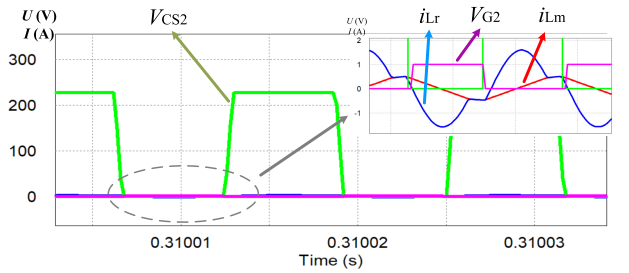


FIGURE 18. Simulation results for ZVS of switch S_2.

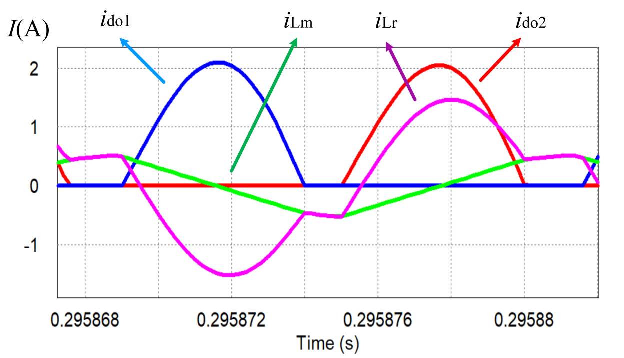


FIGURE 19. Simulation results for ZCS of rectifier diodes D_{O1} and D_{O2}.

With the LLC resonant converter, the DS-LLC resonant converter realizes ZVS of MOS transistors S_1 and S_2, as shown in Fig. 18. The source-drain voltages of the switches S_1 and S_2 drop to zero before the rising edge of the driving voltage V_{GS}, indicating that the switches S_1 and S_2 achieve zero-voltage-switch turn-on. Besides, zero-current-switch turn-off is realized in both rectifier diodes D_{O1} and D_{O2} on the secondary side of transformer, as shown in Fig. 19. The diodes D_{O1} and D_{O2} on the secondary side of the transformer are alternately turned on, and both of them are turned on after the current of the other one drops to zero, achieving zero-current-switch turn-off.

The above simulation results verify the function of the PFC and LLC resonant converter.

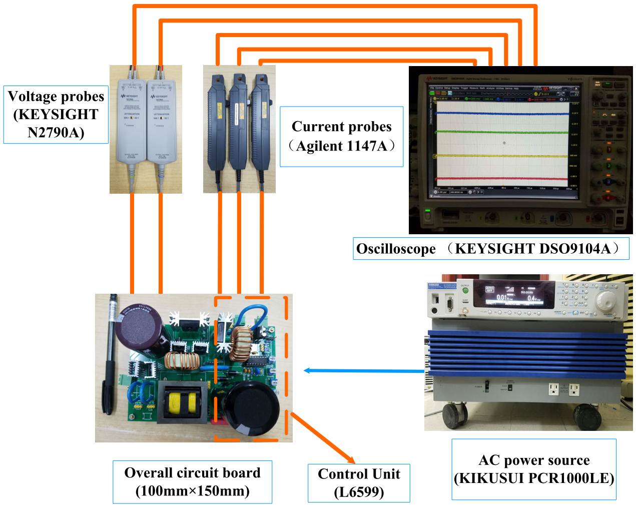


FIGURE 20. The experimental condition.

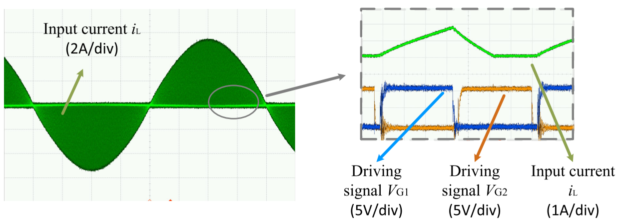


FIGURE 21. Boost PFC experiment results of the DS-LLC resonant converter.

B. EXPERIMENTATION

With the same parameters used in the simulation, the corresponding experiments based on IC L6599 and STM32F103 are conducted in a prototype established in this study, which is shown in Fig. 20.

The experimental results of the PFC function are shown in Fig. 21, where it can be observed that the Boost PFC function is achieved. Refining the waveform, it can be seen that the rising slope of the input current is smaller than the absolute value of the falling slope, which is consistent with the theory and the simulation results, and is also key to the successful realization of the PFC.

Figs. 22 and 23 show the waveform of the realization of ZVS condition in switches S_2 (the ZVS condition in switches S_1 is the same as S_2) and the ZCS of rectifier diodes D_{O1} and D_{O2} on the secondary side of the transformer, which proves the soft switching functionality of these switches.

On the same parameters, we conducted a step-load-change experiment. The load changes from 60 Ω to 100 Ω (where the maximum voltage when the load is 60 Ω and the frequency is minimum is equal to the minimum voltage when the load is 100 Ω and the frequency is maximum). As shown in Fig. 24, when a sudden change occurs in the load, the output voltage can be adjusted quickly by the PFM control to stabilize the voltage. The result of this experiment well verifies the wide output range feature of this converter, because the output voltage is adjusted by the switching frequency f_S and

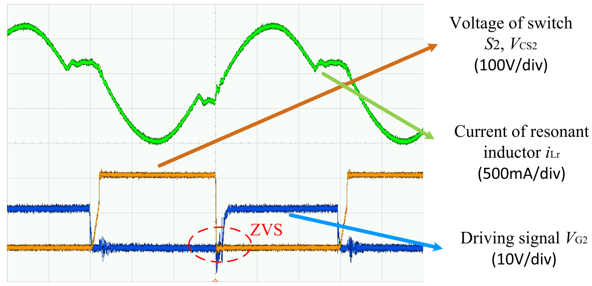


FIGURE 22. ZVS verification of the DS-LLC resonant converter in LLC resonant operation.

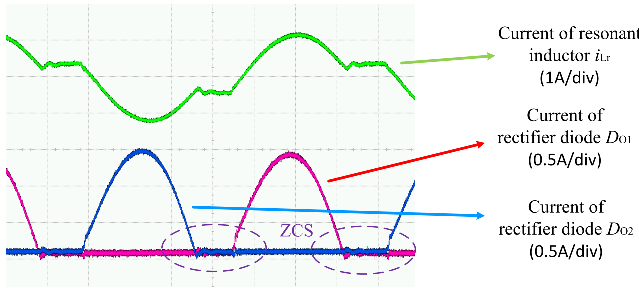


FIGURE 23. ZCS verification of the DS-LLC resonant converter in LLC resonant operation.

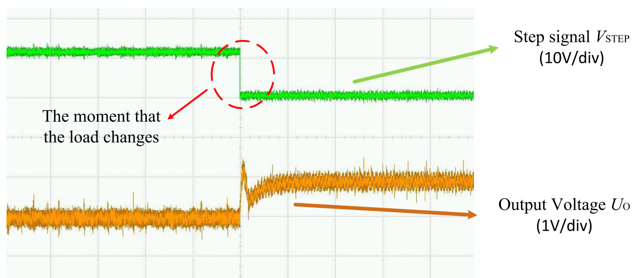


FIGURE 24. Experiment result of step load change.

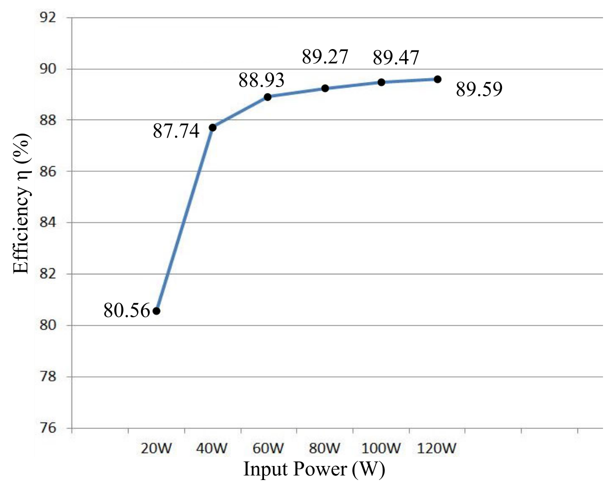


FIGURE 25. The relationship between input power and efficiency.

then stabilized at the voltage levels before the load changes. In other words, we can get different voltage level by adjusting the switching frequency f_S, hence a wide output range.

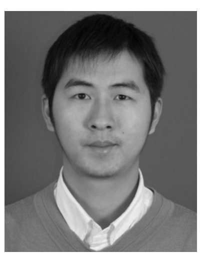
The efficiency of the LLC resonant converter is shown in Fig. 25. Therefore, the experiment results are consistent with the simulation and theory, and have shown the functionality and advantages of this converter.

VII. CONCLUSION

In this paper, we have presented and analyzed a single-stage double-switched AC-DC power converter, which has soft-switching functions for power switches, nearly unity power factor and a wide output range. In particular, two switches are shared by the PFC converter and the LLC resonant converter for size reduction and cost saving. Detailed analyses, including operational modes, mathematical deduction of the Boost PFC, the frequency matching design and the closed-loop control design, have been presented in this paper. Finally, simulation and experimental results have well verified the feasibility and effectiveness of the introduced converter, which is envisioned to have wide applicability in the LED driver industry.

REFERENCES

[1] G. Zhang, Z. Li, B. Zhang, and W. A. Halang, "Power electronics converters: Past, present and future," *Renew. Sustain. Energy Rev.*, vol. 81, pp. 2028–2044, Jan. 2018.
[2] Y. Hu, L. Huber, and M. M. Jovanović, "Single-stage, universal-input AC/DC LED driver with current-controlled variable PFC boost inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1579–1588, Mar. 2012.
[3] X. Liu, X. Li, Q. Zhou, and J. Xu, "Flicker-free single-switch quadratic boost LED driver compatible with electronic transformers," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3458–3467, May 2019.
[4] Z. Fang, J. Wang, S. Duan, K. Liu, and T. Cai, "Control of an LLC resonant converter using load feedback linearization," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 887–898, Jan. 2018.
[5] H. Wang and Z. Li, "A PWM LLC type resonant converter adapted to wide output range in PEV charging applications," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3791–3801, May 2018.
[6] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. APEC. 17th Annu. IEEE Appl. Power Electron. Conf. Exposit.*, vol. 2, Mar. 2002, pp. 1108–1112.
[7] Y. Shen, W. Zhao, Z. Chen, and C. Cai, "Full-bridge LLC resonant converter with series-parallel connected transformers for electric vehicle on-board charger," *IEEE Access*, vol. 6, pp. 13490–13500, 2018.
[8] H. Wang, Y. Chen, Y. Qiu, P. Fang, Y. Zhang, L. Wang, Y.-F. Liu, J. Afsharian, and Z. Yang, "Common capacitor multiphase LLC converter with passive current sharing ability," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 370–387, Jan. 2018.
[9] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.
[10] C.-K. Lee, S. Kiratipongvoot, and S.-C. Tan, "High-Frequency-Fed unity power-factor AC–DC power converter with one switching per cycle," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2148–2156, Apr. 2015.
[11] T. S. Key and J.-S. Lai, "Comparison of standards and power supply design options for limiting harmonic distortion in power systems," *IEEE Trans. Ind. Appl.*, vol. 29, no. 4, pp. 688–695, Jul. 1993.
[12] K. I. Hwu, Y. T. Yau, and Y. C. Chang, "Full-digital AC-DC converter with PFC based on counting," *IEEE Trans Ind. Informat.*, vol. 11, no. 1, pp. 122–131, Feb. 2015.
[13] K. Schenk and S. Cuk, "A single-switch single-stage active power factor corrector with high quality input and output," in *Proc. Rec. 28th Annu. IEEE Power Electron. Spec. Conf. Formerly Power Conditioning Spec. Conf. Power Process. Electron. Spec. Conf.*, vol. 1, Jun. 1997, pp. 385–391.
[14] W. Qi, S. Li, H. Yuan, S.-C. Tan, and S.-Y. Hui, "High-Power-Density single-phase three-level flying-capacitor buck PFC rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10833–10844, Nov. 2019.
[15] K. H. Leung, K. H. Loo, and Y. M. Lai, "Unity-Power-Factor control based on precise ripple cancellation for fast-response PFC preregulator," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3324–3337, Apr. 2016.
[16] R. Goswami, S. Wang, and Y. Chu, "Design of an active differential mode current filter for a boost power factor correction AC-DC converter," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Sep. 2015, pp. 4375–4382.
[17] H.-C. Chen, C.-Y. Lu, G.-T. Li, and W.-C. Chen, "Digital current sensorless control for dual-boost half-bridge PFC converter with natural capacitor voltage balancing," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 4074–4083, May 2017.
[18] Z. Chen, P. Yang, G. Zhou, J. Xu, and Z. Chen, "Variable duty cycle control for quadratic boost PFC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4222–4232, Jul. 2016.
[19] J.-S. Kim, S.-H. Lee, W.-J. Cha, and B.-H. Kwon, "High-efficiency bridgeless three-level power factor correction rectifier," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1130–1136, Feb. 2017.
[20] C. Zhao, J. Zhang, and X. Wu, "An improved variable on-time control strategy for a CRM flyback PFC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 915–919, Feb. 2017.
[21] J.-I. Baek, J.-K. Kim, J.-B. Lee, H.-S. Youn, and G.-W. Moon, "A boost PFC stage utilized as half-bridge converter for high-efficiency DC–DC stage in power supply unit," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7449–7457, Oct. 2017.
[22] H. Wu, X. Zhan, and Y. Xing, "Interleaved LLC resonant converter with hybrid rectifier and variable-frequency plus phase-shift control for wide output voltage range applications," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4246–4257, Jun. 2017.
[23] S.-Y. Chen, Z. R. Li, and C.-L. Chen, "Analysis and design of single-stage AC/DC *LLC* resonant converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1538–1544, Mar. 2012.
[24] H. Ma, Y. Li, Q. Chen, L. Zhang, and J. and Xu, "A single-stage integrated boost-*LLC* AC–DC converter with quasi-constant bus voltage for multichannel LED street-lighting applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1143–1153, Sep. 2018.
[25] L. Zhao, Z. Luo, Z. Fan, and Y. Shi, "A dual half bridge converter with hybrid rectifier for DC power supply in railway systems," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4579–4587, May 2020.
[26] L. Zhao, F. Li, Z. Zhuang, Z. Li, and Z. Luo, "A dual half-bridge converter with current doubler rectifier," *IEEE Trans. Ind. Electron.*, to be published.
[27] Z. Hu, L. Wang, H. Wang, Y.-F. Liu, and P. C. Sen, "An accurate design algorithm for *LLC* resonant converters—Part I," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5435–5447, Aug. 2016.
[28] X. Fang, H. Hu, F. Chen, U. Somani, E. Auadisian, J. Shen, and I. Batarseh, "Efficiency-oriented optimal design of the LLC resonant converter based on peak gain placement," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2285–2296, May 2013.
[29] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985–1995, Apr. 2012.
[30] X. Zhang and J. W. Spencer, "Analysis of boost PFC converters operating in the discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3621–3628, Dec. 2011.
[31] H. Luo, J. Xu, Y. Luo, and S. Jin, "A digital pulse train controlled high power factor DCM boost PFC converter over a universal input voltage range," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2814–2824, Apr. 2019.
[32] H.-N. Vu and W. Choi, "A novel dual full-bridge *LLC* resonant converter for CC and CV charges of batteries for electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2212–2225, Mar. 2018.
[33] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle, and W. G. Dunford, "An *LLC* resonant DC–DC converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5437–5445, Dec. 2013.



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