

Comprehensive Design of Device Parameters for GaN Vertical Trench MOSFETs

SHUANG LIU¹, XIUFENG SONG¹, JINCHENG ZHANG¹, (Member, IEEE), SHENGLI ZHAO¹, (Member, IEEE), JUN LUO², HONG ZHANG¹, YACHAO ZHANG¹, WEIHANG ZHANG¹, (Member, IEEE), HONG ZHOU¹, (Member, IEEE), ZHIHONG LIU¹, (Senior Member, IEEE), AND YUE HAO¹, (Senior Member, IEEE)

¹State Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, China

²The Testing Center, Sichuan Institute of Solid-State Circuits, China Electronics Technology Group Corporation (CETC), Chongqing 400060, China

Corresponding authors: Jincheng Zhang (jchzhang@xidian.edu.cn) and Shenglei Zhao (slzhao@xidian.edu.cn)

This work was supported in part by the National Key Research and Development Program under Grant 2016YFB0400100, and in part by the National Key Science & Technology Special Project under Grant 2017ZX01001301.

ABSTRACT In this work, device parameters for GaN vertical trench MOSFETs have been investigated systematically to further improve the device characteristics. The n^- GaN drift layer, the p^+ GaN layer and the trench gate are designed and optimized systematically using Silvaco ATLAS 2-D simulation, in order to get the best trade-off between V_{BR} and specific on-resistance R_{on} . Three-terminal breakdown curves, the electron concentration, current density and electric field strength distributions have been presented to analyze the breakdown characteristics. The correlations between different parameters and different initial conditions are considered, and the eight parameters are optimized comprehensively. After the final optimization, record high FOM of 4.8 GW/cm², V_{BR} of 2783 V, average electric field E_{drift} of 1.98 MV/cm and a low R_{on} of 1.6 m Ω ·cm² are obtained for drift layer thickness of 14 μ m. The product of the thickness L_p and doping density N_p of p^+ GaN layer can determine the breakdown mechanism, and punch through mechanism would occur when $L_p \cdot N_p$ is lower than a certain value. The results indicate there exists large optimization room for fabricated GaN vertical trench MOSFETs, and the device characteristics can be further improved through the methodology in this paper for high power and high voltage applications.

INDEX TERMS GaN vertical trench MOSFETs, breakdown voltage, specific on-resistance, power figure-of-merit (FOM).

I. INTRODUCTION

GaN-based devices are considered to be candidates for power electronic applications due to wide bandgap, high breakdown field strength, high electron mobility and high 2DEG density. Compared with GaN lateral high-electron-mobility transistor (HEMT) device, GaN vertical MOSFETs possess higher current density, lower specific on-resistance R_{on} and lower current collapse. GaN-based current aperture vertical electron transistors (CAVETs) and vertical trench MOSFETs are typical GaN vertical structures. Although the CAVET structure shows excellent current performance due to the high conductivity of a two-dimensional electron gas (2DEG), the vertical trench MOSFETs are easier to achieve intrinsically normally-off operation [1]-[2] and do not need the regrowth

of AlGaIn/GaN layers. The vertical trench MOSFET with a threshold voltage of 3.7 V and a specific on-resistance of 9.3 m Ω ·cm² has been reported in 2008 [3]. Then, trench MOSFETs with a 13 μ m drift layer and hexagonal trench gate layout were fabricated, obtaining a threshold voltage of 3.5 V, breakdown voltage of 1250 V, specific on-resistance of 1.8 m Ω ·cm², and power figure of merit (FOM) of 0.868 GW/cm² as shown in TABLE 1 [4]. In situ oxide, GaN interlayer-based vertical trench MOSFET (OG-FET) has been proposed to enhance the channel electron mobility and reduce on resistance [5]-[12]. For OG-FET, the breakdown voltage was increased to 1435 V by utilizing novel double field-plated structure. The specific on-resistance is 2.2 m Ω ·cm², leading to a high FOM of 0.891 GW/cm², which is the highest FOM value of GaN vertical trench MOSFETs [13]. Considering the thickness of the drift layer is 15 μ m, the average breakdown electric field is less than

The associate editor coordinating the review of this manuscript and approving it for publication was N. Prabaharan¹.

TABLE 1. Comparison of GaN lateral HEMTs and vertical MOSFETs.

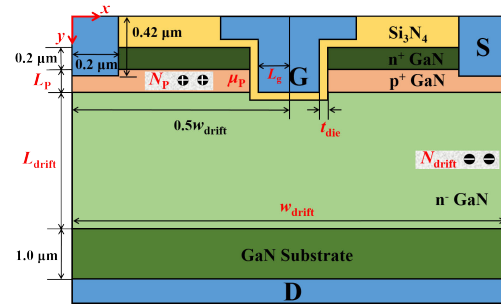
Reference	Device Structure	V_{BR} (kV)	R_{on} ($m\Omega \cdot cm^2$)	FOM (GW/cm^2)
[16]	InAlN/GaN MOSHEMTs	3	4.25	2.1
[17]	AlGaIn/GaN HEMTs	10.4	186	0.582
[18]	AlGaIn/GaN/GaN: C HEMTs	0.942	0.39	2.3
[4]	GaN vertical Trench MOSFETs	1.25	1.8	0.868
[10]	GaN OG-FET	0.9	8.2	0.0988
[13]	GaN OG-FET with Double Field Plates	1.4	2.2	0.891
[14]	GaN-on-Si Quasi- vertical MOSFETs	0.645	6.8	0.0612
[15]	GaN-on-Si Fully- vertical MOSFETs	0.52	5	0.0541

1 MV/cm. Recently, GaN vertical trench MOSFETs with a 4 μm drift layer based on the silicon substrate were fabricated, obtaining a breakdown voltage of 520 V, specific on-resistance of 5 $m\Omega \cdot cm^2$ and FOM of 0.0541 GW/cm^2 [14], [15]. Although plenty of studies have been carried out on GaN vertical trench MOSFETs, the breakdown voltage and FOM for GaN vertical trench MOSFETs are lower than those for GaN lateral HEMTs. A high breakdown voltage of 3000 V and FOM of 2.1 GW/cm^2 were achieved in InAlN/GaN MOSHEMTs [16], and these values are higher than those for all GaN vertical trench MOSFETs. A record high breakdown voltage of 10.4 kV for GaN-based HEMTs has been achieved by increasing gate-drain spacing [17]. In addition, the lowest specific on-resistance of 0.39 $m\Omega \cdot cm^2$ and the highest Power figure of merit FOM of 2.3 GW/cm^2 were achieved in AlGaIn/GaN/GaN: C HEMTs [18].

In order to improve the breakdown voltage and FOM for GaN vertical trench MOSFETs, it is necessary to further optimize structures and parameters of trench MOSFETs. Especially the n^- GaN drift layer, the p^+ GaN layer and the trench gate are the main regions that decide the specific on-resistance and breakdown voltage. However, the key parameters of GaN vertical trench MOSFETs have not been fully investigated until now, which is very important for achieving high breakdown voltage, low specific on-resistance and high FOM.

In this work, the key parameters of trench MOSFETs, including the thickness of drift layer L_{drift} , the doping density of drift layer N_{drift} , the length of drift layer w_{drift} , the thickness of p^+ GaN L_p , the doping density of p^+ GaN N_p , the channel electron mobility μ_p , the thickness of gate dielectric t_{die} and the length of gate L_g , have been designed and optimized systematically using 2-D simulation. The whole simulation procedure includes three parts, in which the trade-off of V_{BR} and R_{on} have been investigated. Firstly, by optimizing the n^- GaN drift layer with different initial conditions, the optimal results that $L_{drift} = 14 \mu m$, $N_{drift} = 7 \times 10^{15} cm^{-3}$, and $w_{drift} = 5 \mu m$ are obtained. Then based on the optimal parameters of drift layer, the product of the thickness and

doping density of p^+ GaN layer ($L_p \cdot N_p$) can determine the breakdown mechanism. Device breakdown induced by punch through would occur when $L_p \cdot N_p$ is lower than a certain value. With a reasonable channel mobility $\mu_p = 50 cm^2/V \cdot s$, the optimal results are $L_p = 310 nm$, $N_p = 2 \times 10^{18} cm^{-3}$. Finally, a high FOM of 4.8 GW/cm^2 and gate-drain average breakdown electric field of 1.98 MV/cm are obtained through optimizing the trench gate.

**FIGURE 1. Cross-sectional structure of GaN vertical trench MOSFETs.**

II. DEVICE STRUCTURE AND CALIBRATION OF SIMULATION MODELS

The cross-sectional structure of the GaN trench MOSFETs discussed in this paper is shown in Fig. 1, which include eight parameters for the n^- GaN drift layer, the p^+ GaN channel layer and the trench gate. Based on n^+ GaN substrate, the trench MOSFET epitaxial structure includes n^- GaN drift layer, p^+ GaN channel layer and n^+ GaN layer. Gate trench is obtained by etching the n^+ GaN and p^+ GaN region under the gate. Si_3N_4 is utilized to form gate dielectric, and gate electrode metal is nickel metal with a work function of 5.15 eV. In addition, both the drain electrode and the source electrode are ohmic contacts, and contact resistance model is considered.

The doping density of the n^+ GaN layer is set as $2 \times 10^{18} cm^{-3}$ to form ohmic contact with the source electrode, and the n^+ GaN layer serves as a conductive layer. The acceptors of the p^+ layer in this paper are completely ionized. The thickness of the n^+ GaN layer is 200 nm. The highly doped n^+ GaN substrate's thickness is 1 μm . Trench MOSFET device has a length of w_{drift} in the x direction, and the distance between the two source electrodes is $(w_{drift}-0.4) \mu m$. The active region is composed of x direction between the two source electrodes and a direction perpendicular to the x - y plane, and the area of the active region is $(w_{drift}-0.4) \times 10^{-8} cm^2$. The channel mobility of trench MOSFETs was limited by material damage caused in the process of etching for the gate trench and the high impurity scattering due to the heavily doped p^- GaN. The reported electron channel mobilities in conventional trench MOSFETs are between 4-89 $cm^2/V \cdot s$, and the channel mobility in OG-FET devices can be improved to 185 $cm^2/V \cdot s$ by regrowth of the channel [19]. Based on these experimental results, the channel electron mobility is discussed in the second part.

TABLE 2. Parameters for the low field mobility model.

Parameters	Value	Unit
MU1N.FMCT	55	cm ² /V·s
MU2N.FMCT	100	cm ² /V·s
NCRITN.FMCT	2e17	cm ⁻³
ALPHAN.FMCT	1.0	--
MUIP.FMCT	3	cm ² /V·s
MU2P.FMCT	170	cm ² /V·s
NCRITP.FMCT	3e17	cm ⁻³
ALPHAP.FMCT	2.0	--

TABLE 3. Parameters for the trap model.

Parameters	Value	Unit	Description
e.level	2.85/1.75 /0.5	eV	Energy of the discrete trap level
density	1e13	cm ⁻³	Maximum density of states of the trap level
degen	1	--	Degeneracy factor of the trap level used to calculate the density
sign	1e-15/1e-15 /1e-13	cm ²	Capture cross section of the trap for electrons
sigp	1e-15	cm ²	Capture cross section of the trap for holes

All the work in this paper is based on the two-dimensional simulator of Silvaco-Atlas, using the reported experimental result [20] of GaN trench MOSFETs to calibrate the model codes. Main parameters are consistent with the reported experimental result. The results after calibration are shown in Fig. 2, and the specific on-resistance estimated from the linear region at $V_{DS} = 0.5$ V and $V_{GS} = 50$ V is 12.78 mΩ·cm². The models considered in this simulation include field dependent mobility (FLDMOB), the SRH recombination model, the Auger recombination model, the trap model [21], the low field mobility model, the impact ionization model, and the source contact resistance of 1.4 Ω·mm. After calibration with the reported experimental result of GaN trench MOSFETs, the parameters of important models are determined and presented in TABLE 2 and TABLE 3. The energy level of $E_C-1.75$ eV and $E_C-0.5$ eV are for the deep donor, and $E_C-2.85$ eV is for the deep acceptor.

III. SIMULATION RESULTS AND DISCUSSION

In order to obtain the reasonable parameters of GaN trench MOSFETs, the simulation process consists of three parts. Firstly, optimize the thickness, the doping density and the length of the n⁻ GaN drift layer with different initial values. Then, based on the optimal parameters of drift layer, the thickness, the doping density, and the channel electron mobility of p⁺ GaN are discussed with different initial values. Finally, effects of the gate dielectric thickness and the gate length for the trench gate on the device performance are studied.

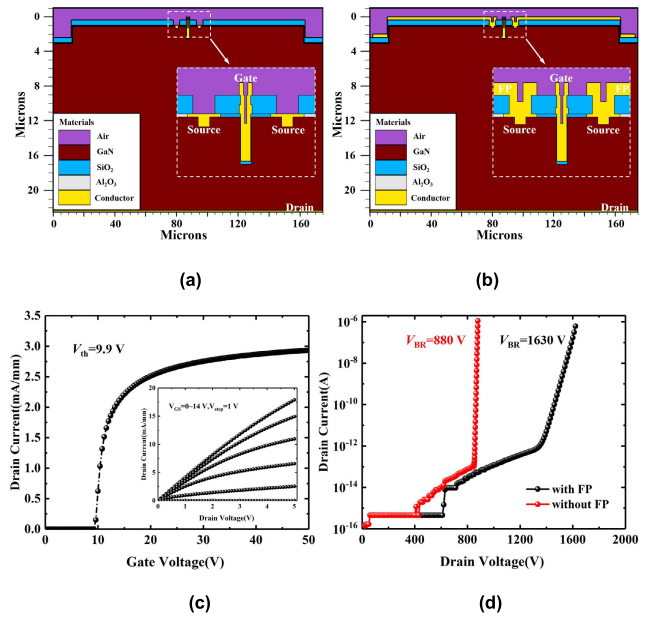


FIGURE 2. Schematic cross section of calibrated trench MOSFETs (a) without and (b) with field-plate edge termination. (c) Transfer and output curves of calibrated trench MOSFETs with field-plate edge termination. (d) Breakdown curves at $V_{GS} = 0$ V of calibrated trench MOSFETs.

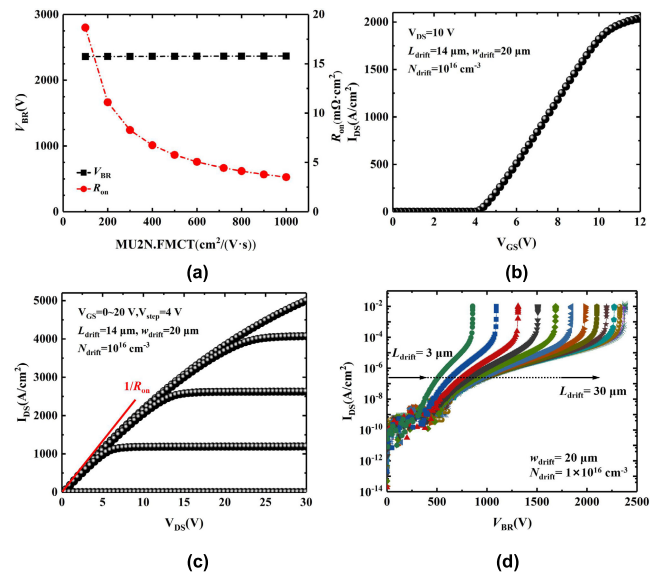


FIGURE 3. (a) V_{BR} and R_{on} as a function of the MU2N.FMCT parameter. (b) Transfer and (c) output curves of the MOSFET with $L_{drift} = 14$ μm. (d) Breakdown curves of MOSFETs at $V_{GS} = 0$ V with different thicknesses of the n⁻ GaN drift layer.

A. DISCUSSION AND OPTIMIZATION FOR THE n⁻ GaN DRIFT LAYER

Fig. 3(a) shows the V_{BR} and R_{on} as a function of MU2N.FMCT parameter, and R_{on} decrease significantly with the increase of the drift layer's electron mobility. The electron mobility parameter of MU2N.FMCT is set to 720 cm²/V·s according to the latest literature [14]. Transfer and output characteristics of the GaN vertical trench MOSFETs are shown in Fig. 3(b) and 3(c). The threshold voltage in this paper is defined as the gate voltage with I_{DS} reaching

5 A/cm². As shown in Fig. 3(b), the threshold voltage is 4.1 V for $L_{\text{drift}} = 14 \mu\text{m}$, and the threshold voltages of the MOSFETs discussed in this part are all 4.1 V due to the same p⁺ GaN parameters. The maximum output current and the specific on-resistance R_{on} is 5.0 kA/cm² and 4.44 mΩ·cm² respectively as shown in Fig. 3(c).

The breakdown characteristics of the trench MOSFETs with different thicknesses of the n⁻ GaN drift layer are shown in Fig. 3(d). The breakdown voltage was defined as the voltage at which $I_{\text{DS}} = 10^{-2}$ A/cm². When the thickness L_{drift} is set as 3 μm, V_{BR} is 857 V. With the increase of L_{drift} , V_{BR} increases significantly and almost saturates at 14 μm. When the thickness increases to 30 μm, a high breakdown voltage of 2380 V is obtained.

As shown in Fig. 4(a) and 4(c), V_{BR} increases and saturates at a certain value as L_{drift} increases with different initial conditions. In contrast, V_{BR} decreases with the increases of N_{drift} as shown in Fig. 4(e). However, the increase of L_{drift} or decrease of N_{drift} without limitation is meaningless, which would lead to a large increase in R_{on} . Fig. 4(g) shows that as the length increases from 5 μm to 24 μm, the breakdown voltage changes from 2825 V to 2820 V. The length of the drift layer has no effect on the breakdown voltage of the device, but the reduction in length results in the reduction of the active area and R_{on} . Power figure of merit $\text{FOM} = V_{\text{BR}}^2/R_{\text{on}}$ and average electric field between gate and drain electrodes E_{drift} can be used as a criterion to optimize L_{drift} . As shown in Fig. 4(b), 4(d), 4(f) and 4(h), E_{drift} decreases as L_{drift} and N_{drift} increase, while the increase of w_{drift} has no effect on E_{drift} . In the process of optimizing L_{drift} and N_{drift} with different conditions, the FOM value has a peak value at $L_{\text{drift}} = 14 \mu\text{m}$ and $N_{\text{drift}} = 7 \times 10^{15} \text{ cm}^{-3}$, respectively. When the drift layer length increases from 5 μm to 24 μm, the FOM value decreases from 3.96 GW/cm² to 1.1 GW/cm². During the comprehensive analysis on the n⁻ GaN drift layer, the idea of gradually optimizing L_{drift} , N_{drift} and w_{drift} has been adopted to obtain the optimal structural parameters of the n⁻ GaN drift layer. The optimal parameters of the n⁻ GaN drift layer are that $L_{\text{drift}} = 14 \mu\text{m}$, $N_{\text{drift}} = 7 \times 10^{15} \text{ cm}^{-3}$, $w_{\text{drift}} = 5 \mu\text{m}$. The corresponding results are $V_{\text{BR}} = 2824 \text{ V}$, $R_{\text{on}} = 2.01 \text{ m}\Omega\cdot\text{cm}^2$, $\text{FOM} = 3.96 \text{ GW/cm}^2$, $E_{\text{drift}} = 2.01 \text{ MV/cm}$.

In order to study the breakdown mechanism for different L_{drift} , the electron concentration distribution is shown in Fig. 5(a). With $V_{\text{DS}} = V_{\text{BR}}$, the electron depletion region is extended to the n⁺ GaN substrate for the MOSFET with $L_{\text{drift}} = 3 \mu\text{m}$. The limitation of the depletion region results from the low thickness of n⁻ GaN drift layer and the high doping density of n⁺ GaN substrate. In comparison, the depth of depletion region can be improved to 14 μm and 15 μm for the MOSFETs with $L_{\text{drift}} = 14 \mu\text{m}$ and 20 μm at the breakdown voltages. It can be found that the depletion thickness of 14 μm in the drift layer accounts for the largest proportion of the entire drift region. Fig. 5(b) shows the current density distributions of the vertical trench MOSFETs at $V_{\text{DS}} = V_{\text{BR}}$, and the impact ionization produces electron-hole pairs. The

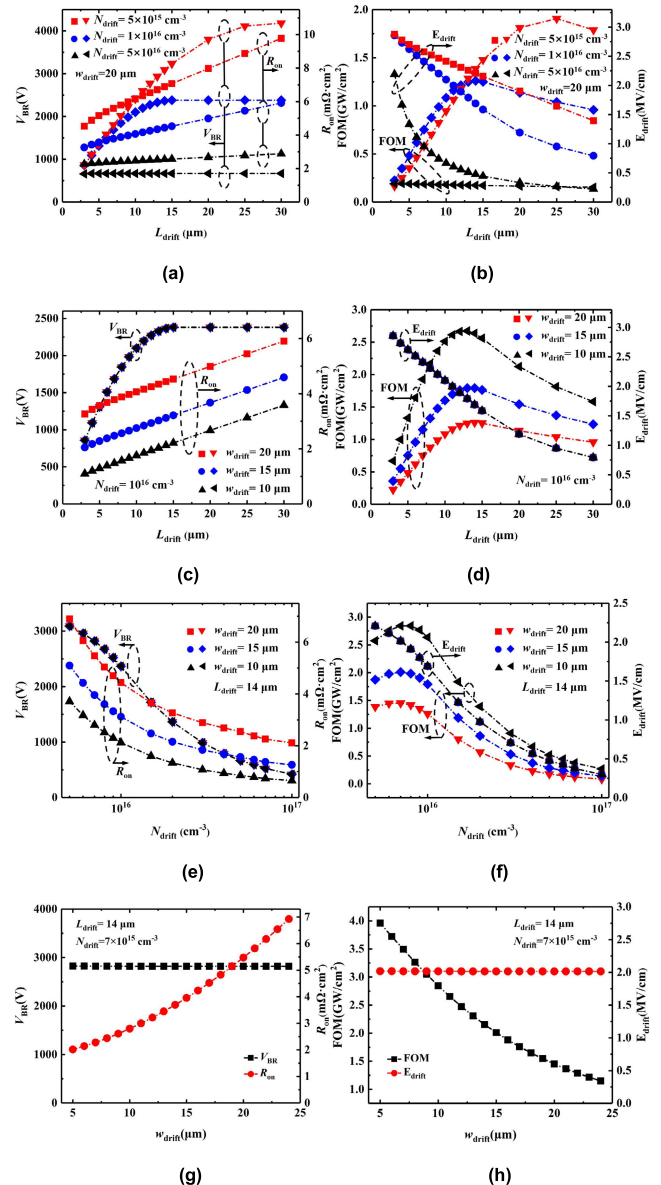


FIGURE 4. V_{BR} and R_{on} as a function of the n⁻ GaN drift layer thickness with different (a) N_{drift} and (c) w_{drift} . Power FOM and E_{drift} as a function of the n⁻ GaN thickness with different (b) N_{drift} and (d) w_{drift} . (e) V_{BR} , R_{on} and (f) FOM, E_{drift} as a function of the n⁻ GaN drift layer doping density with different w_{drift} . (g) V_{BR} , R_{on} and (h) FOM, E_{drift} as a function of the n⁻ GaN drift layer length w_{drift} .

electron current mainly flows vertically to the drain electrode, while the hole current flows to the source electrode along the p⁺ GaN layer.

As shown in Fig. 5(c) and 5(d), there are two electric field peaks in the device, which exists at the PN junction and the trench gate corner, respectively. Compared with the electric field peak of the PN junction, the electric field peak of the trench corner reaches the 3.3 MV/cm earlier. For $L_{\text{drift}} = 3 \mu\text{m}$, the electric field strength drops sharply after the depletion region reaches the n⁺ substrate. For $L_{\text{drift}} = 20 \mu\text{m}$, when the depletion region extends to 14 μm in the drift layer, the electric field strength drops to zero sharply. Therefore, 14 μm drift layer is enough to obtain high breakdown voltage.

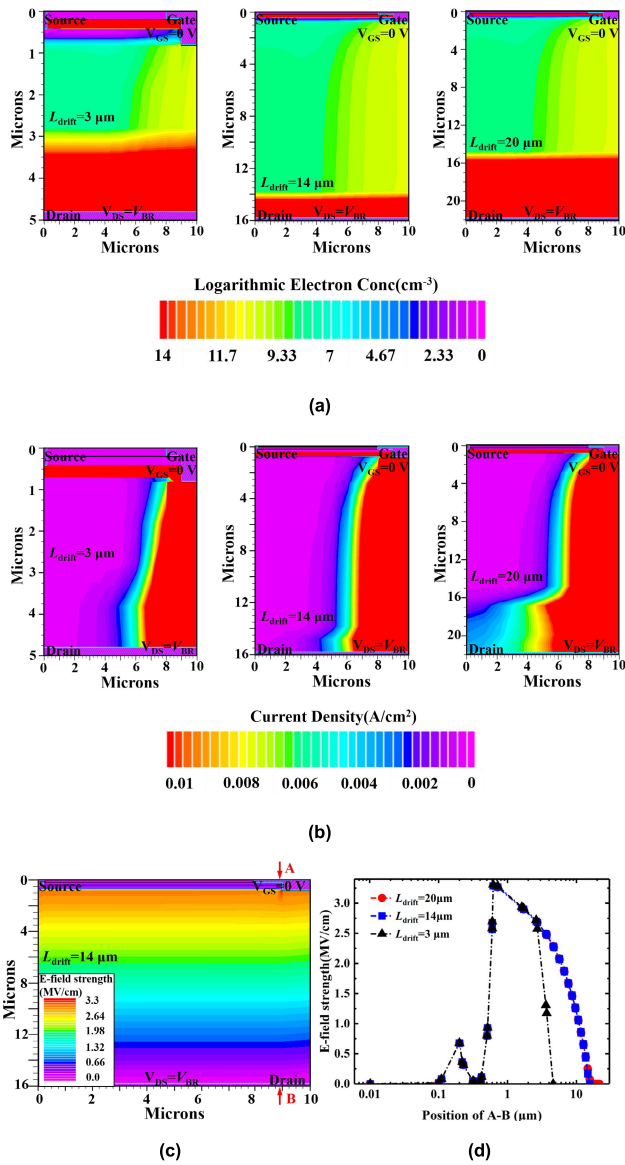


FIGURE 5. (a) Logarithmic electron concentration and (b) current density distributions of trench MOSFETs with different drift layer thicknesses at $V_{GS} = 0$ V and $V_{DS} = V_{BR}$. (c) E-field strength distributions of trench MOSFETs with drift layer thickness of $14 \mu\text{m}$ at $V_{GS} = 0$ V and $V_{DS} = V_{BR}$. (d) E-field strength distributions of trench MOSFETs along A-B as a function of different drift layer thicknesses at the breakdown voltages.

B. DISCUSSION AND OPTIMIZATION FOR THE p^+ GaN LAYER

Based on the optimal parameters of the n^- GaN drift layer, the parameters optimization for the p^+ GaN layer has been carried out in this section. Firstly, the thickness of the p^+ GaN layer L_p is optimized with different initial conditions of N_p and μ_p . Then, with the optimal thickness of the p^+ GaN layer, the p^+ GaN layer doping density N_p with different μ_p is discussed. Finally, the effect of channel electron mobility on the device characteristics is investigated.

As shown in Fig. 6 (a) and 6(c), V_{BR} increases and saturates at a certain value as L_p increases with different initial

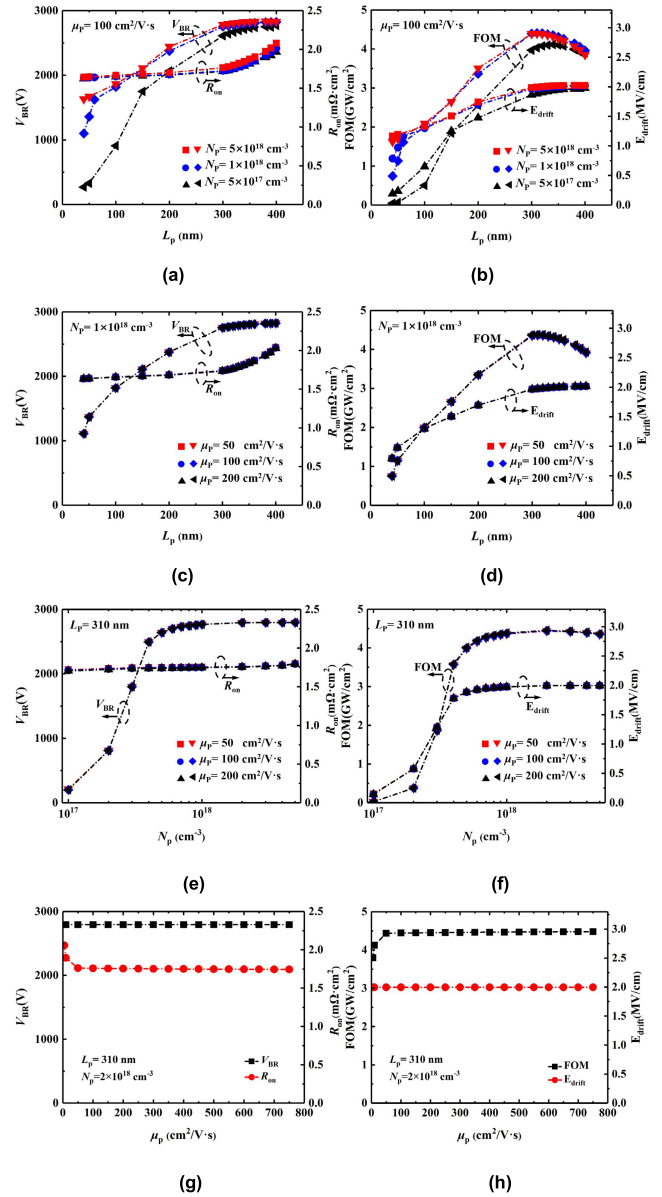


FIGURE 6. V_{BR} and R_{ON} as a function of the p^+ GaN thickness with different (a) N_p and (c) μ_p . Power FOM and E_{drift} as a function of the p^+ GaN thickness with different (b) N_p and (d) μ_p . (e) V_{BR} , R_{ON} and (f) FOM, E_{drift} as a function of the p^+ GaN doping density with different μ_p . (g) V_{BR} , R_{ON} and (h) FOM, E_{drift} as a function of the channel electron mobility μ_p . (All μ_p is set by the value of MUN2.FMCT, in fact the maximum mobility of the extracted p^+ GaN layer is limited to $117.9 \text{ cm}^2/\text{V}\cdot\text{s}$).

conditions, while R_{ON} increases as L_p increases. Fig. 6(b) and 6(d) show the optimal L_p is 310 nm, which is corresponding to the highest FOM. Since the thickness of the drift layer is maintained at $14 \mu\text{m}$, the change in E_{drift} is consistent with the trend of V_{BR} . During the change of μ_p , the breakdown voltage remains constant at 2795 V. Fig. 6(f) shows that the maximum FOM can be achieved at $N_p = 2 \times 10^{18} \text{ cm}^{-3}$, and the corresponding E_{drift} is 1.99 MV/cm.

The effect of μ_p on R_{ON} needs to be discussed according to the actual situations. For 1.2 kV applications, the channel mobility increasing from 4-89 $\text{cm}^2/\text{V}\cdot\text{s}$ to 185 $\text{cm}^2/\text{V}\cdot\text{s}$

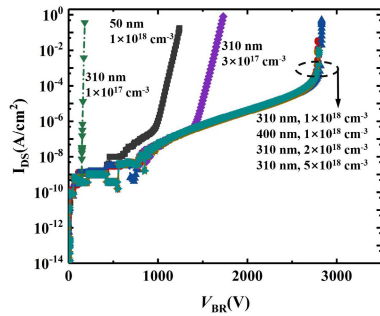


FIGURE 7. Breakdown curves of MOSFETs at $V_{GS} = 0$ V with different thicknesses and doping densities of p^+ GaN layer.

can reduce R_{on} effectively [19]. In this work, the simulated devices are targeted at the 2 kV-3 kV applications and the drift layer is quite thick, so the total resistance is mainly contributed by resistance of the drift layer. Therefore, μ_P has little effect on the total resistance in this case. In addition, if μ_P is particularly low, the channel resistance will accounts for a large proportion of the total resistance even in high-voltage applications.

Although a high channel electron mobility of $750 \text{ cm}^2/\text{V}\cdot\text{s}$ is set, the maximum channel electron mobility in simulation results is limited to $117.9 \text{ cm}^2/\text{V}\cdot\text{s}$ due to the limitation of the high doping density of the p^+ GaN. For the mobility of $5 \text{ cm}^2/\text{V}\cdot\text{s}$, $100 \text{ cm}^2/\text{V}\cdot\text{s}$ and $750 \text{ cm}^2/\text{V}\cdot\text{s}$ in Fig. 6(g) and 6(h), the actual ranges of mobility in the channel are $4.6\text{-}5 \text{ cm}^2/\text{V}\cdot\text{s}$, $31.3\text{-}59 \text{ cm}^2/\text{V}\cdot\text{s}$, and $41\text{-}117.9 \text{ cm}^2/\text{V}\cdot\text{s}$, and the corresponding R_{on} are $2.06 \text{ m}\Omega\cdot\text{cm}^2$, $1.76 \text{ m}\Omega\cdot\text{cm}^2$, and $1.74 \text{ m}\Omega\cdot\text{cm}^2$, respectively. The optimized FOM value reaches $4.43 \text{ GW}/\text{cm}^2$, and optimal parameters of the p^+ GaN layer are $L_p = 310 \text{ nm}$, $N_p = 2 \times 10^{18} \text{ cm}^{-3}$, and $\mu_p = 50 \text{ cm}^2/\text{V}\cdot\text{s}$. The corresponding results are $V_{BR} = 2795 \text{ V}$, $R_{on} = 1.76 \text{ m}\Omega\cdot\text{cm}^2$, $\text{FOM} = 4.44 \text{ GW}/\text{cm}^2$, and $E_{drift} = 1.99 \text{ MV}/\text{cm}$.

Two breakdown mechanisms exist in vertical trench MOSFETs, namely avalanche breakdown and punch-through breakdown. The product of the thickness and doping density of p^+ GaN layer ($L_p \cdot N_p$) can determine the breakdown mechanism, and punch through mechanism would occur when $L_p \cdot N_p$ is lower than a certain value ($L_p = 310 \text{ nm}$ and $N_p = 10^{17} \text{ cm}^{-3}$, $L_p = 50 \text{ nm}$ and $N_p = 10^{18} \text{ cm}^{-3}$, $L_p = 310 \text{ nm}$ and $N_p = 3 \times 10^{17} \text{ cm}^{-3}$) as shown in Fig. 7. When $L_p \cdot N_p$ is high enough, the breakdown mechanism can be changed to avalanche breakdown. The breakdown curves of punch through increase gradually with the increase of drain voltage after the inflexion points. In contrast, the breakdown curves of avalanche breakdown increase immediately after the inflexion points. In order to investigate the effect of N_p and L_p on the breakdown mechanism, analysis and discussion are carried out as follows.

Fig. 8 shows the electron concentration, the current density and the electric field strength distributions of the GaN vertical trench MOSFETs with different p^+ GaN thicknesses at $V_{DS} = V_{BR}$. For $L_p = 50 \text{ nm}$, the breakdown mechanism is

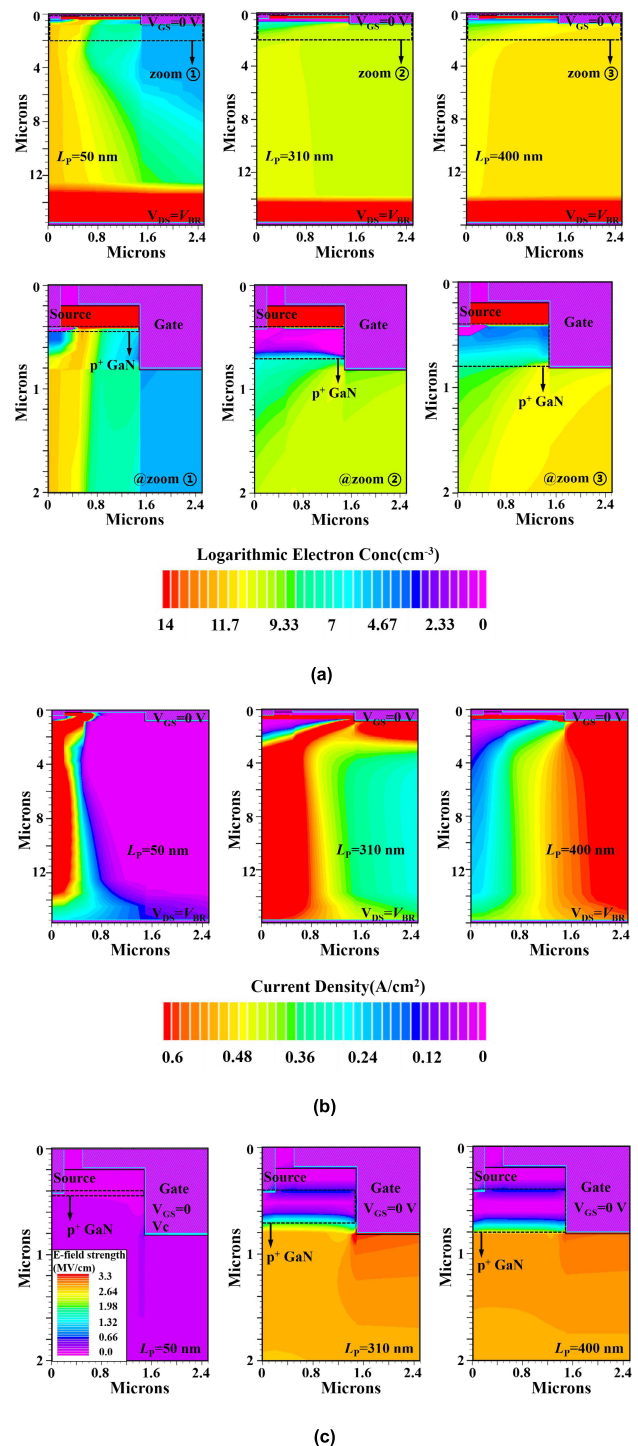


FIGURE 8. (a) Logarithmic electron concentration, (b) current density, and (c) E-field strength distributions of trench MOSFETs with different thicknesses of p^+ GaN at $V_{GS} = 0$ V and $V_{DS} = V_{BR}$. The p^+ GaN layer doping density is 10^{18} cm^{-3} .

punch through, and current flows from the source electrode directly to the drain electrode. For $L_p = 310 \text{ nm}$ or 400 nm , the breakdown mechanism is avalanche breakdown, and large number of electron-hole pairs are produced at the gate corner, leading to the electron current from gate corner to the drain electrode and hole current from gate corner to the source

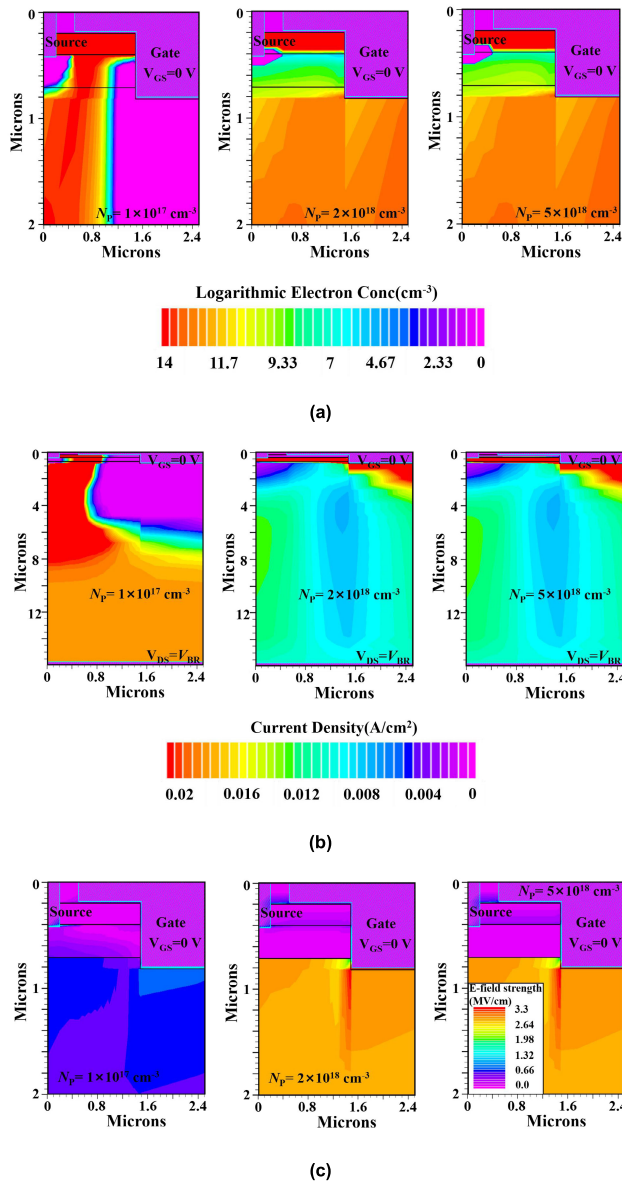


FIGURE 9. (a) Logarithmic electron concentration, (b) current density, and (c) E-field strength distributions of trench MOSFETs with different doping densities of p⁺ GaN at $V_{GS} = 0 \text{ V}$ and $V_{DS} = V_{BR}$. The p⁺ GaN layer thickness is 310 nm.

electrode. As shown in Fig. 8(c), the electric field strength of the punch-through breakdown does not reach the critical electric field strength value of GaN. In contrast, electric field peak is located at the gate corner for avalanche breakdown, and the electric field peak can reach the critical electric field of 3.3 MV/cm.

The effect of p⁺ GaN doping density on the breakdown mechanism is shown in Fig. 9. For a low N_p , such as $1 \times 10^{17} \text{ cm}^{-3}$, punch through occurs and current flows from the source electrode directly to drain electrode. For a high N_p such as $2 \times 10^{18} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, the breakdown mechanism changes to avalanche breakdown, and large number of electron-hole pairs are produced at the gate corner, leading to a large electron current and hole current. The effect

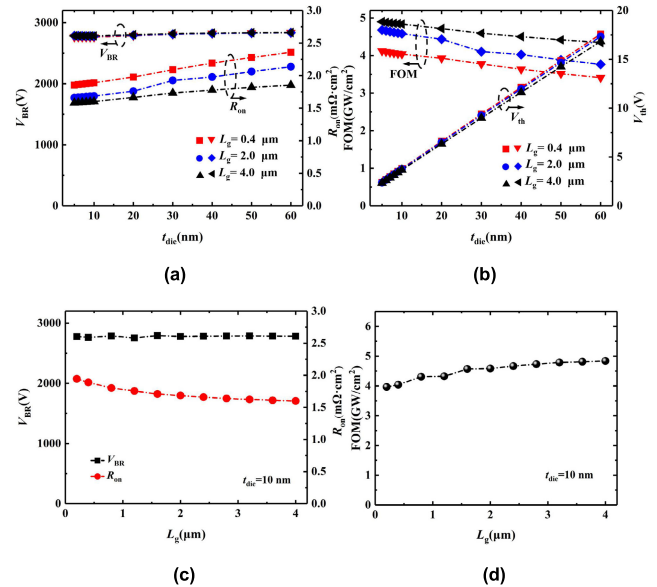


FIGURE 10. (a) V_{BR} , R_{on} and (b) Power FOM, V_{th} as a function of the gate dielectric thickness with different L_g . (c) V_{BR} , R_{on} and (d) Power FOM as a function of L_g .

of p⁺ GaN doping density on the breakdown mechanism is similar to that of p⁺ GaN thickness. High V_{BR} and high electric field can be achieved in the case of high N_p by avalanche breakdown. According to Fig. 8 and Fig. 9, product of L_p and N_p can determine the breakdown mechanism. By increasing L_p or N_p , the punch-through mechanism can be avoided so that high V_{BR} and FOM can be obtained. However, threshold voltage or other device characteristic parameters may be influenced and should be considered in the design process of L_p and N_p .

C. DISCUSSION AND OPTIMIZATION FOR THE TRENCH GATE

Compared with the optimization of the n⁻ GaN drift layer and the p⁺ GaN layer, the optimization near the trench gate also has a great impact on the device performance. The optimization of the gate dielectric thickness t_{die} and gate length L_g has been considered in this part.

As shown in Fig. 10(a), under different initial conditions of the gate length, the increase of the gate dielectric thickness has no effect on the breakdown voltage. However, it will increase the specific on-resistance of the device, leading to the reduction of FOM as shown in Fig. 10(b). The threshold voltage increases from 2.40 V to 17.58 V with the gate dielectric increases from 5 nm to 60 nm. For $t_{die} = 10 \text{ nm}$, R_{on} reduces from 1.95 mΩ·cm² to 1.60 mΩ·cm² and V_{BR} changes from 2777 V to 2783 V for gate length increasing from 0.2 μm to 4 μm. The FOM value has a maximum value of 4.8 GW/cm² when the gate length is 4 μm, and the threshold voltage is 3.68 V. The corresponding results are $V_{BR} = 2782 \text{ V}$, $R_{on} = 1.60 \text{ m}\Omega\cdot\text{cm}^2$, $\text{FOM} = 4.8 \text{ GW/cm}^2$, and $E_{drift} = 1.98 \text{ MV/cm}$.

In order to investigate the reason for the reduction of R_{on} with increasing of t_{die} and L_g , the local electron

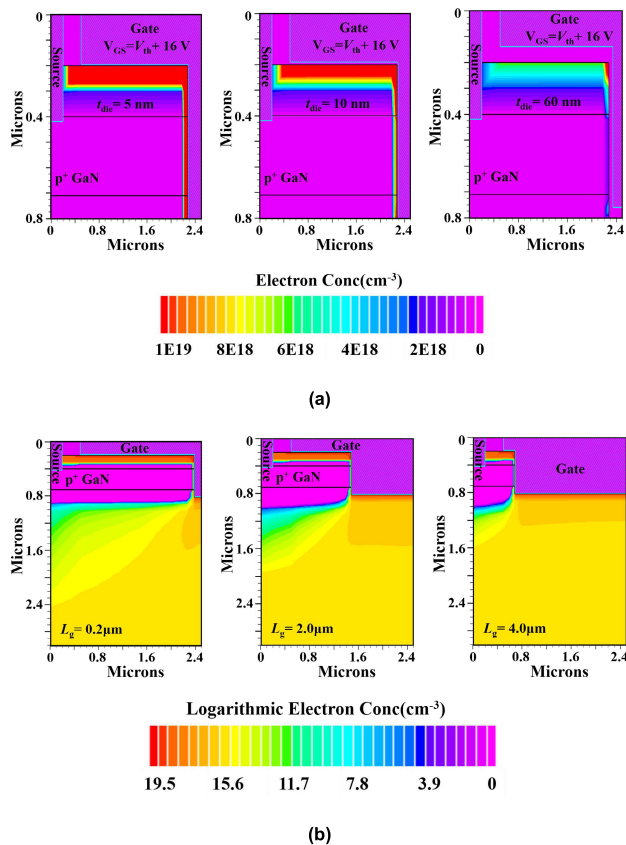


FIGURE 11. (a) Local electron concentration distribution of trench MOSFETs with different t_{die} at $V_{DS} = 20$ V. (b) Local logarithmic electron concentration distribution of trench MOSFETs with different L_g at $V_{DS} = 20$ V.

concentration distributions of different t_{die} and L_g are shown in Fig. 11. When the gate dielectric thickness changes from 5 nm to 10 nm and then to 60 nm, the corresponding R_{on} increases from $1.65 \text{ m}\Omega\cdot\text{cm}^2$ to $1.68 \text{ m}\Omega\cdot\text{cm}^2$, and then to $2.13 \text{ m}\Omega\cdot\text{cm}^2$. For on-state condition, the increase of the gate dielectric thickness would reduce the gate capacitance and the electron concentration of the channel layer, leading to a larger R_{on} . With the gate length increasing from $0.2 \mu\text{m}$ to $2 \mu\text{m}$, and then to $4 \mu\text{m}$, the current channel width is expanded effectively. As a result, R_{on} decreases from $1.88 \text{ m}\Omega\cdot\text{cm}^2$ to $1.68 \text{ m}\Omega\cdot\text{cm}^2$, and then to $1.60 \text{ m}\Omega\cdot\text{cm}^2$. There is little room to further reduce R_{on} because the length of the drift layer has been optimized to $5 \mu\text{m}$, and the gate length can not exceed this value.

According to the optimization of n^- GaN drift layer, p^+ GaN channel layer and the trench gate, the power FOM can achieve a record high value of $4.8 \text{ GW}/\text{cm}^2$, which is much higher than $0.891 \text{ GW}/\text{cm}^2$ for fabricated GaN vertical trench MOSFETs and $2.3 \text{ GW}/\text{cm}^2$ for GaN lateral HEMTs. Consequently, there exists large room for optimization of fabricated GaN vertical trench MOSFETs.

IV. CONCLUSION

In this work, the n^- GaN drift layer, the p^+ GaN layer, and the trench gate are designed and optimized systematically

using 2-D simulation, in order to investigate V_{BR} and power FOM enhancement potential for GaN vertical trench MOSFETs. The whole simulation procedure includes three parts, in which the trade-off of V_{BR} and R_{on} has been investigated. During the optimization process, the correlations between different parameters and different initial conditions are considered. When the product of the thickness and doping density of the p^+ GaN layer is high enough, the breakdown mechanism can be changed from punch through to avalanche breakdown. Finally, R_{on} and FOM can be further improved through the optimization of the gate dielectric thickness and the gate length. A record high FOM of $4.8 \text{ GW}/\text{cm}^2$, and V_{BR} of 2783 V are obtained for $L_{drift} = 14 \mu\text{m}$, $N_{drift} = 7 \times 10^{15} \text{ cm}^{-3}$, $w_{drift} = 5 \mu\text{m}$, $L_p = 310 \text{ nm}$, $N_p = 2 \times 10^{18} \text{ cm}^{-3}$, $\mu_p = 50 \text{ cm}^2/\text{V}\cdot\text{s}$, $t_{die} = 10 \text{ nm}$ and $L_{gate} = 4 \mu\text{m}$. V_{BR} and FOM of fabricated GaN vertical trench MOSFETs can be further improved by the optimization methodology for high power and high voltage applications.

ACKNOWLEDGMENT

(Shuang Liu and Xiufeng Song contributed equally to this work.)

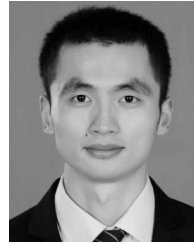
REFERENCES

- [1] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET: Part I—History, technology, and prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 674–691, Mar. 2017.
- [2] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017.
- [3] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-based trench gate metal oxide semiconductor field-effect transistors on GaN bulk substrates," *Appl. Phys. Express*, vol. 1, no. 1, Jan. 2008, Art. no. 011105.
- [4] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "1.8 $\text{m}\Omega\cdot\text{cm}^2$ vertical GaN-based trench metal-oxide-semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Appl. Phys. Express*, vol. 8, no. 5, Apr. 2015, Art. no. 054101.
- [5] C. Gupta, C. Lund, S. H. Chan, A. Agarwal, J. Liu, Y. Enatsu, S. Keller, and U. K. Mishra, "In situ oxide, GaN interlayer-based vertical trench MOSFET (OG-FET) on bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 353–355, Mar. 2017.
- [6] C. Gupta, A. Agarwal, S. H. Chan, O. S. Koksaldi, S. Keller, and U. K. Mishra, "1 kV field plated in-situ oxide, GaN interlayer based vertical trench MOSFET (OG-FET)," in *Proc. 75th Annu. Device Res. Conf. (DRC)*, South Bend, IN, USA, Jun. 2017, pp. 1–2.
- [7] W. Li, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, and H. G. Xing, "600 v GaN vertical V-trench MOSFET with MBE regrown channel," in *Proc. 75th Annu. Device Res. Conf. (DRC)*, Bend, IN, USA, Jun. 2017, pp. 1–2.
- [8] D. Ji, C. Gupta, A. Agarwal, S. H. Chan, C. Lund, W. Li, M. A. Laurent, S. Keller, U. K. Mishra, and S. Chowdhury, "First report of scaling a normally-off in-situ oxide, GaN interlayer based vertical trench MOSFET (OG-FET)," in *Proc. DRC*, South Bend, IN, USA, Jun. 2017, pp. 1–2.
- [9] W. Li, H. G. Xing, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, and D. Jena, "Development of GaN vertical trench-MOSFET with MBE regrown channel," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2558–2564, Jun. 2018.
- [10] D. Ji, W. Li, A. Agarwal, S. H. Chan, J. Haller, D. Bisi, M. Labrecque, C. Gupta, B. Cruse, R. Lal, S. Keller, U. K. Mishra, and S. Chowdhury, "Improved dynamic RON of GaN vertical trench MOSFETs (OG-FETs) using TMAH wet etch," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1030–1033, Jul. 2018.

- [11] D. Ji, C. Gupta, A. Agarwal, S. H. Chan, C. Lund, W. Li, S. Keller, U. K. Mishra, and S. Chowdhury, "Large-area *in-situ* oxide, GaN interlayer-based vertical trench MOSFET (OG-FET)," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 711–714, May 2018.
- [12] C. Gupta, S. H. Chan, A. Agarwal, N. Hatui, S. Keller, and U. K. Mishra, "First demonstration of AlSiO as gate dielectric in GaN FETs; applied to a high performance OG-FET," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1575–1578, Nov. 2017.
- [13] D. Ji, C. Gupta, S. H. Chan, A. Agarwal, W. Li, S. Keller, U. K. Mishra, and S. Chowdhury, "Demonstrating >1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices," in *IEDM Tech. Dig.*, Dec. 2017, pp. 4–9.
- [14] C. Liu, R. Abdul Khadar, and E. Matioli, "GaN-on-Si quasi-vertical power MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 71–74, Jan. 2018.
- [15] R. Abdul Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully vertical GaN-on-Si power MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 443–446, Mar. 2019.
- [16] H. S. Lee, D. Piedra, M. Sun, X. Gao, S. Guo, and T. Palacios, "3000-V 4.3-mΩ·cm² InAlN/GaN MOSHEMTs With AlGaIn Back Barrier," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 982–984, Jul. 2012.
- [17] M. Yanagihara, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "Recent advances in GaN transistors for future emerging applications," *Phys. Status Solidi A*, vol. 206, no. 6, pp. 1221–1227, Jun. 2009.
- [18] E. Bahat-Treidel, F. Brunner, O. Hil, E. Cho, J. Wurfl, and G. Trankle, "AlGaIn/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low R-ON×A," *IEEE Electron Device Lett.*, vol. 57, no. 11, pp. 3050–3058, Nov. 2010.
- [19] D. Ji, W. Li, and S. Chowdhury, "A study on the impact of channel mobility on switching performance of vertical GaN MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4271–4275, Oct. 2018.
- [20] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV," *Appl. Phys. Express*, vol. 7, no. 2, Jan. 2014, Art. no. 021002.
- [21] H. Hanawa, H. Onodera, A. Nakajima, and K. Horio, "Numerical analysis of breakdown voltage enhancement in AlGaIn/GaN HEMTs with a high-k passivation layer," *IEEE Electron Device Lett.*, vol. 61, no. 3, pp. 699–775, Mar. 2014.



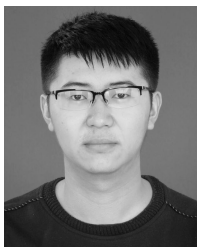
JINCENG ZHANG (Member, IEEE) received the M.S. and Ph.D. degrees from Xidian University, Xi'an, China, in 2001 and 2004, respectively. He is currently a Professor with Xidian University, Xi'an. His current interests include wide bandgap semiconductor GaN and diamond materials and devices. He has authored and coauthored more than 200 journal and conference papers.



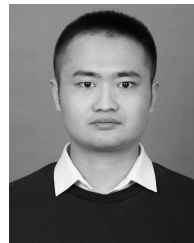
SHENGLI ZHAO (Member, IEEE) received the Ph.D. degree from Xidian University, Xi'an, China, in 2015. He is currently an Associate Professor with the School of Microelectronics, Xidian University. His research interests include GaN-based power devices and integrated circuits.



JUN LUO received the Ph.D. degree from Xidian University, Xi'an, China, in 2018. He is currently a Senior Engineer with the Sichuan Institute of Solid-State Circuits, China Electronics Technology Group Corporation. His research interests include the Si-based and GaN-based power electronics and microelectronics reliability.



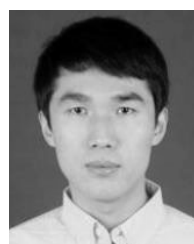
SHUANG LIU received the B.S. degree from the Xi'an University of Technology, Xi'an, China, in 2018. He is currently pursuing the Ph.D. degree in GaN power devices with Xidian University, Xi'an.



HONG ZHANG received the M.S. degree from Xidian University, Xi'an, China, in 2019. His research interest includes fabrication and characterization analysis of GaN-based high electron-mobility transistors.



XIUFENG SONG received the B.S. degree from Xidian University, Xi'an, China, in 2018, where he is currently pursuing the Ph.D. degree in GaN power devices.



YACHAO ZHANG received the B.S. and Ph.D. degrees in electronic science and technology from Xidian University, in 2012 and 2017, respectively. His current research interest includes the simulation, modeling, fabrication, and characterization of III-V electronic materials and devices.



WEIHANG ZHANG (Member, IEEE) received the B.S. degree in electronic science and technology from Xidian University, Xi'an, China, in 2013, where he is currently pursuing the Ph.D. degree with the School of Microelectronics. His current research interest includes the fabrication, characterization, and reliability analysis of GaN-based power devices.



ZHIHONG LIU (Senior Member, IEEE) received the B.Sc. degree from Nankai University, China, in 2001, the M.Eng. degree from the Institute of Semiconductors, Chinese Academy of Sciences, China, in 2004, and the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2011. From 2007 to 2011, he was a Research Associate with the Temasek Laboratories at NTU. In 2011, he joined the Singapore-MIT Alliance for Research and Technology (SMART) Center, as a Postdoctoral Associate, and was promoted to a Research Scientist, in 2014, and a Principal Research Scientist, in 2016. In 2019, he joined Xidian University, China, as a Professor. His current research interests include GaN and other wide bandgap semiconductors based microwave, mmWave, THz devices and MMICs, and also power electronic devices and circuits.



wide bandgap GaN and ultrawide bandgap β -Ga₂O₃-based FETs for both DC and RF applications.

HONG ZHOU (Member, IEEE) received the Ph.D. degree from Purdue University, in May 2017. From June 2017 to February 2018, he held a postdoctoral position at the University of California at Berkeley. He is currently a Professor with the School of Microelectronics, Xidian University. He has authored or coauthored more than 60 journal and conference papers. His research focuses on fabrication, electrical and thermal measurement, and modeling of negative-capacitance Si FETs,



YUE HAO (Senior Member, IEEE) is currently a Professor of microelectronics and solid state electronics with Xidian University, Xi'an, China. His current interests include wide bandgap materials and devices, advanced CMOS devices and technology, semiconductor device reliability physics and failure mechanism, and organic electronics. He has authored or coauthored more than 300 journal and conference papers. He is a member of the Chinese Academy of Sciences, China.

...