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Common-Mode Stability Test and Design Guidelines for a Transformer-Based Push-Pull Power Amplifier

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ABSTRACT We report design guidelines for a transformer-based push-pull power amplifier (PA) with a systematic stability test carried out in the complex frequency domain. By detecting the right half-plane zeros of the impedance matrix's determinant, the common-mode (CM) instability in a differential PA were accurately estimated with the established frequencies from the analysis. In the stability test, the parasitic series coupling capacitance of the input transformer and the parasitic inductance from the gate (base) biasing line were identified as the two primary mechanisms of the CM instability in a transformer-based PA contingent on stability. Based on the analysis of the instability mechanisms, useful stabilization methods were proposed and discussed for a robust push-pull PA design with a well-balanced performance. An onboard transformer-based push-pull PA was implemented for the verification purpose, and the effects of parasitic inductance on the stability had been investigated. The simulated and measured results corresponded well with the proposed analysis.

INDEX TERMS Common mode, power amplifiers, stability analysis, transformers.

I. INTRODUCTION

Over the past decades, modern wireless communications have led to the significant advancement of microwave / millimeter-wave circuits. In modern power amplifier (PA) designs, transformers have been widely used in implementing a differential amplifier with better performance and less size occupancy [1], [2]. In the microwave / millimeter-wave regime, a high-performance amplifier with excellent stability is essential for reliable operation in various environments. Although Rollet's k-Δ test and μ-test, which are mostly based on a single-ended configuration [3], have been widely used in traditional microwave circuit designs, these stability tests are not directly applicable when estimating the stability of differential circuits due to common-mode (CM) oscillation.

The prevalence of a differential amplifier in common-source (CS) configurations is owing to its distinct benefits. The differential pair combines the power of two active devices to a load, thereby helping to release the voltage stress on the device's drains. It is a well-balanced structure when its push-pull operation implies the natural two-pole property of an AC signal which maximizes the combining efficiency, mitigates CM interference and noise, and facilitates circuit layout owing to the symmetry structure. Therefore, the differential pair is commonly used as the unit cell when output power combining is exploited for a higher output power [1], [2], [4]. However, it is well known that a CM oscillation can be triggered in a differential amplifier at a high frequency if the losses in the path of any feedback loop are not significant enough to guarantee robust stability. Moreover, the transistor itself has feedback capacitances, i.e., the gate-to-drain capacitance (C_{gd}) in the CS configuration, which degrades the stability. Notably, the CM oscillation must be carefully investigated for an amplifier coupled with transformers.

For a robust differential amplifier design, it is necessary to detect instability and stabilize the network in the early stages of the design. Small-signal analysis has proved to be efficient in detecting most of the sources of instability in the circuit while utilizing only a slight computation effort [5], [6]. However, there still exist unstable points that only appear under

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a specific level of RF input [7], and a small-signal analysis cannot detect these oscillations. Though transient simulation is an efficient method to view the unwanted behaviors of a circuit in a large-signal regime, it requires considerable computing resources for complex designs [8]. To check its stability properly, designers should excite perturbations in the circuit, e.g., by introducing a step function in the supply as well as bias nodes. Detecting instability by harmonic balance (HB) simulation has also proved to be a promising solution, although the conventional HB simulator widely used in commercial CAD tools generally experiences difficulty in detecting instability [7]. However, by applying some additional conditions or techniques, the HB simulator can be a useful tool to detect unwanted oscillations [9], [10].

Even though instability in a design can be detected by a CAD tool, it is quite a complex task because designers need to thoroughly determine the root causes of the instability to fix the design effectively and to have a good trade-off between stabilization and other performances. For a comprehensive approach, tailored analyses are necessary for specific circuit topologies. Essential contributions to the stabilization of various circuit structures can be found in [11]–[13]. Multi-branch (or multi-device) paralleled PA has gained considerable interest from researchers. Since the multi-branch structure uses power dividers and combiners between PA stages, it faces potential odd-mode instability that has been investigated carefully both in the small-signal and large-signal domains [5], [6], [10].

On the contrary, there has been little information on the CM stability analysis of differential amplifier structures up until now. In [13], the authors disclosed that a bypass capacitor connected to a non-ideal ground could lead to instability in push-pull amplifiers. In our analysis, we show that a differential amplifier can suffer from CM instability due to the gate inductance from the biasing line as well as the parasitic series coupling capacitance between the two coils of the input transformer.

We present analytical expressions for evaluating the stability of a transformer-based push-pull PA through a small-signal analysis in the complex-frequency ($s = \sigma + j\omega$) domain to establish useful guidelines. Based on the general small-signal stability criteria, the conditions of instability can be summarized for the detection of the right half-plane zeros of the impedance matrix's determinant. The analysis corresponded very well with the results from the CAD tools for a 180-nm CMOS. From the example design, the root causes of the CM oscillation are identified, and design guidelines are presented by considering the stability criterion with a small-signal model. Various components are gradually investigated to verify their effects on the stability of the push-pull structure and are compared with corresponding simulations. Finally, an on-board push-pull amplifier was fabricated to verify the vulnerability of the structure and the applicability of the presented stabilization methods.

The oscillation mechanisms are discussed in Section II, and a detailed analysis of the simplified small-signal model is explained and verified with a SPICE simulation in Section III. Section IV deals with the various methods of stabilizing the transformer-based push-pull PA. Next, an experimental example of the instability in the push-pull structure is given in Section V, followed by conclusions on the study.

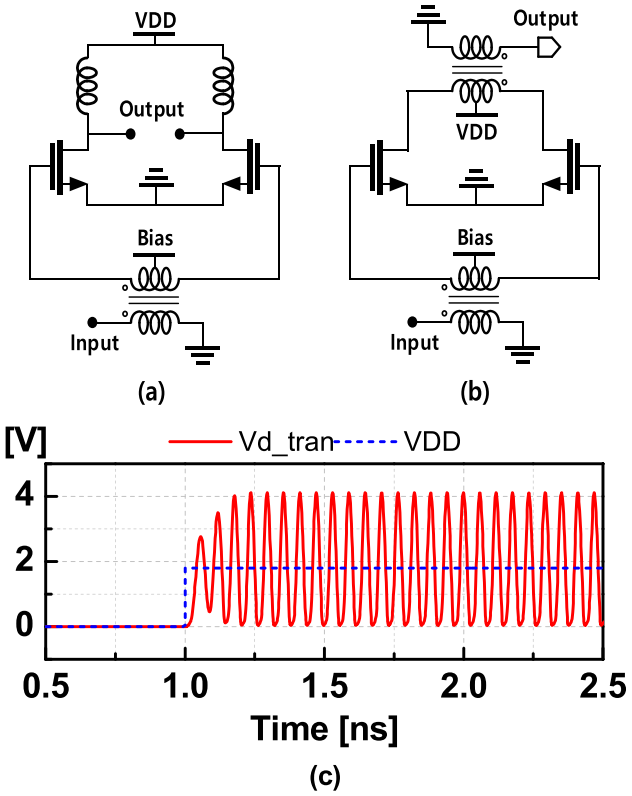


FIGURE 1. (a) A pseudo-differential amplifier, (b) a push-pull amplifier, and (c) the simulated oscillation of the drain voltage of a transistor in a push-pull structure after turning on the supply voltage at 1ns when no input is introduced.

II. THE CM OSCILLATION MECHANISM IN A DIFFERENTIAL AMPLIFIER

There are two widely used differential pair configurations in the microwave regime depending on the output configuration: one is a pseudo-differential pair, and the other is a push-pull amplifier, as illustrated in Fig. 1(a), and Fig. 1(b), respectively. Although a differential CS amplifier has some distinct advantages as stated, CM oscillation can occur due to a careless microwave amplifier design since the differential load is not shown to the transistor pair [13]. Instead, the small parasitic series resistance of the inductive coils contributing as the primary loss mechanism of the CM signal makes the structure prone to instability. Moreover, C_{gd}, along with the input impedance of the source, creates a positive feedback network for the amplifier design, leading to unwanted oscillations when a triggering signal appears. Fig. 1(c) shows a transient simulation of a differential push-pull PA using a 180-nm 1P6M CMOS technology. The simulation shows that the amplifier oscillates at 1 ns after providing the supply voltage without an input signal.

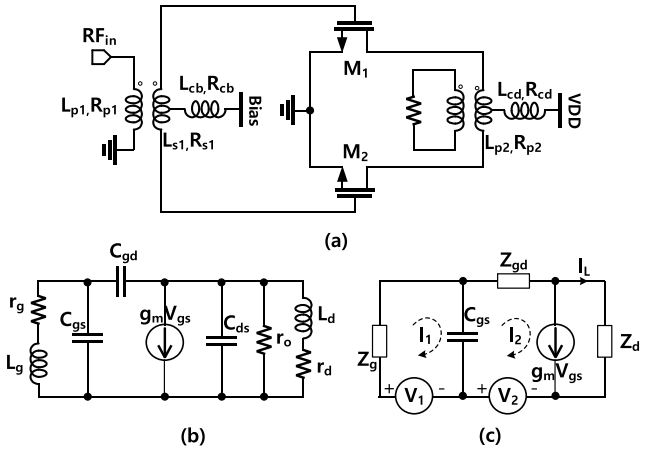


FIGURE 2. (a) A schematic of push-pull amplifier, (b) the small-signal common-mode half-circuit of the PA, and (c) a simplified version of the circuit in (b).

In the transient simulation, the self-oscillation grows exponentially but is compressed quickly to a specific level due to the gain compression of the active device in the large-signal domain. Since oscillation itself naturally constitutes large-signal behavior, a stability analysis to attain more accurate results should be considered in the large-signal domain where the active devices play as non-linear components in the circuit. However, in the case of the unstable mechanism mentioned earlier, the small-signal analysis proved to be more effective since it is more intuitive with less complexity. In [10], the analysis of the odd-mode oscillation in multi-branch amplifiers revealed that the threshold value of the stabilization resistor (R_{stab}) is even stricter in the small-signal region than in the large-signal one. Therefore, in the present approach, the small-signal model can provide useful guidelines for a stable differential PA design.

III. THE SMALL-SIGNAL ANALYSIS OF THE PUSH-PULL POWER AMPLIFIER

A. CM INSTABILITY CRITERIA IN PUSH-PULL PAS

A simplified schematic of a push-pull PA with a transformer at the input and biasing circuit is illustrated in Fig. 2(a). The transformer-based balun transforms the single-ended input to the differential signal for the balanced pair of transistors. The bias voltage for the transistor's gate is delivered through the CM center tap of the secondary coil of the input transformer where the bias line has a parasitic inductance L_{cb}. Similarly, the power supply also sees a CM inductor (L_{cd}) before being delivered to the center tap of the primary coil of the output transformer where L_{s1} represents and L_{p2} stands for the inductive winding of the output transformer. Note that all inductive coils have a resistive loss which is represented by the corresponding resistors. Moreover, to arrive at intuitive and mathematically tractable results, the low-frequency lumped model is used for transformers, and transistors are modeled by simplifying lumped elements as shown in Fig. 2(b). Herein, the parasitic capacitance between two coils of the transformers is neglected for simplicity, and it will be considered later in section IV-B.

Since the instability occurs in common mode, it can be investigated with the half-circuit, as shown in Fig. 2(b). Here, $L_g = 2L_{cb} + L_{s1}/2$, $r_g = 2R_{cb} + R_{s1}/2$, $L_d = 2L_{cd} + L_{p2}/2$, and $r_d = 2R_{cd} + R_{p2}/2$, while the transistor is modeled using a voltage-controlled current source with a transconductance of g_m combined with three capacitors: C_{gs}, C_{ds}, and C_{gd} and output resistor r_o. The load and the source impedances are not shown in the CM oscillation. A simplified circuit of Fig. 2(b) is exhibited in Fig. 2(c) with the two pseudo-voltages V_1 and V_2 for triggering. Furthermore, Z_g represents $r_g + sL_g$, Z_{gd} stands for $1/sC_{gd}$, and Z_d includes $1/sC_{ds}//r_o//(sL_d + r_d)$. Subsequently, in the complex-frequency (s) domain, the impedances can be expressed as

$$Z_g = sL_g + r_g; Z_{gd} = \frac{1}{sC_{gd}}$$
$$Z_d = \frac{1}{sC_{ds} + \frac{1}{r_o} + \frac{1}{sL_d + r_d}}. \quad (1)$$

Using Kirchhoff's voltage and current laws for the circuit in Fig. 2(c) and by noting that the current flow through Z_L is $I_L = I_2\text{-}g_m V_{gs}$, we can obtain network equations in the form of a matrix as

$$[Z][I] = [V], \quad (2)$$

where $\boldsymbol{Z}$, $\boldsymbol{I}$, and $\boldsymbol{V}$ represent the impedance, the circulating current, and the voltage matrices, respectively, which are given by

$$Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}; \quad I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}; \quad V = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \quad (3)$$

In Fig. 2(c), the elements in the impedance matrix can be calculated as

$$z_{11} = Z_g + Z_{gs}; Z_{12} = -Z_{gs}$$
$$z_{21} = -\left(Z_{gs} + Z_d Z_{gs} g_m\right)$$
$$z_{22} = Z_{gd} + Z_{gs} + Z_d + Z_d Z_{gs} g_m, \quad (4)$$

where $Z_{gs} = 1/(sC_{gs})$. The circuit can be excited by applying delta functions to V_1 and V_2 to check the current responses in the circuit. In the s domain, the delta function is expressed as unity; then the circulating currents can be calculated as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{\det(Z)} \begin{bmatrix} z_{22} & -z_{12} \\ -z_{21} & z_{11} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \end{bmatrix}. \quad (5)$$

If the expression of the currents in the s domain contains right half-plane poles (RHPs), its transformation to the time domain will contain oscillations growing exponentially, resulting in an unstable design. Note that the expressions for the poles do not depend on the triggering matrix [$\boldsymbol{V}$]. There are two cases when this can happen: $det(\boldsymbol{Z})$ has a right half-plane zero (RHZ), or an element of the $\boldsymbol{Z}$ matrix has RHPs. However, the operands of the $\boldsymbol{Z}$-matrix's elements, i.e. z_{ij} (i, j=1,2), are formed by either merely impedances of

passive branches or a real value g_m, thus they cannot contain RHPs. Therefore, we can envisage a situation when a given circuit becomes unstable if $det(\mathbf{Z})$ contains RHZs and the imaginary part of the zeros comprises the angular frequencies of the oscillations. The expression of $det(\mathbf{Z})$ is given by

$$\det(Z) = z_{11}z_{22} - z_{21}z_{12}. \tag{6}$$

By replacing (1) to (4), and using (6), we can obtain the following equation when r_o is large enough to be ignored, i.e.

$$\det(Z) = \frac{A(s)}{B(s)} = \frac{a_4s^4 + a_3s^3 + a_2s^2 + a_1s + 1}{s^2C_{gd}C_{gs}(s^2C_{ds}L_d + sC_{ds}r_d + 1)}, \tag{7}$$

where

$$\begin{aligned} a_4 &= L_gL_dC_{gds} \\ a_3 &= (r_dL_g + r_gL_d)C_{gds} + g_mC_{gd}L_dL_g \\ a_2 &= L_dL_gC_{gds} + L_g(C_{gs} + C_{gd}) + L_d(C_{ds} + C_{gd}) \\ &\quad + g_mC_{gd}(r_dL_g + L_dr_g) \\ a_1 &= r_g(C_{gs} + C_{gd}) + r_d(C_{ds} + C_{gd}) + g_mC_{gd}r_dr_g \\ C_{gds} &= (C_{gs}C_{ds} + C_{gd}C_{ds} + C_{gd}C_{gs}) \end{aligned} \tag{8}$$

The solution to $A(s) = 0$ gives us the zeros of $det(\mathbf{Z})$. It is known that RHZs always come in pairs given as $s = \alpha \pm j\omega$ in A(s), which is a quartic function. Thus, it may potentially have two pairs of solutions that give two oscillation frequencies.

Let us consider the circuit in Fig. 2(b) by choosing the drain inductance (L_d) of 250 pH. If it has an effective quality factor (Q_e) of 10 at 10 GHz (the Q_e at a particular frequency is calculated using $Q_e = \omega L_d/r_d$), the parasitic drain resistance (r_d) is 1.57 Ω. The gate inductance (L_g) and gate parasitic resistance (r_g) were chosen to be the same as for the drain inductance: L_g = 250 pH and r_g = 1.57 Ω. These inductances are from the routing lines as well as the CM inductance of the input balun used for biasing the transistor. Under given bias conditions, the small-signal parameters of the NMOS device of 90 × 0.18 μm was extracted as C_{ds} = 52.9 fF, C_{gs} = 99.7 fF, C_{gd} = 29.4 fF, g_m = 38.7 mS, and r_o = 549 Ω. Using the equation for $A(s)$ in (7), we can see four zeros in $A(s)$: $s_{12} = 40.93 \times 2\pi(-0.34 \pm j)$ Grad/s and $s_{34} = 23.46 \times 2\pi(0.15 \pm j)$ Grad/s, which means that the circuit oscillates at F = 23.46 GHz. If r_o is taken into account, the calculated F shifts to 23.49 GHz.

Stability analysis in the complex-frequency domain (s) is more advantageous in checking stability compared with that based on a small-signal analysis in the real-frequency domain (ω) in [13]. It can be seen that the expression in (2) is similar to equation (11) in [13], albeit we used the current branch matrix in the s domain. Indeed, in (2), if $det(\mathbf{Z}) = 0$ at a certain point $s = s_0$, then $[\boldsymbol{I}]$ will have a nonzero solution at s_0 even for $[V(s = s_0)] = [\boldsymbol{0}]$. If s_0 is not located on the left half-plane, we will have a mathematically unstable solution at s_0. The explicit solution of $[\boldsymbol{I}]$ should be derived to find its physical meaning. Deploying the idea by using $j\omega$ instead of s prevents us from reaching a complete solution since $det(\mathbf{Z}(s = j\omega))$ includes a real part and an imaginary one which generally cannot be zero simultaneously. Therefore, solving only the equation of the real part equal to zero, i.e., $Real\{det(\mathbf{Z}(j\omega))\} = 0$, leads to a solution of oscillation frequencies deviating from the values obtained by using the s domain. Moreover, the additional task of calculating the input impedance is required to verify the instability.

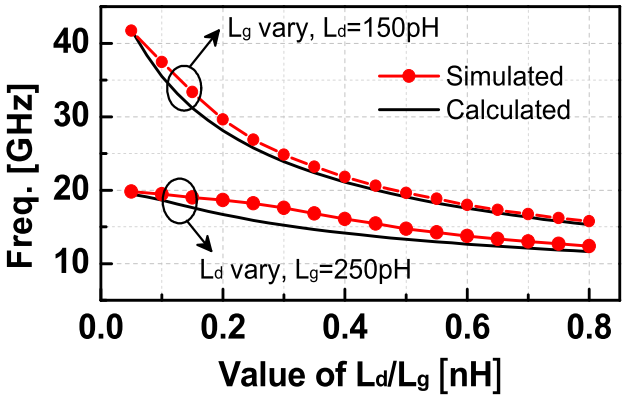


FIGURE 3. Calculated and simulated oscillation frequencies versus L_g or L_d.

B. VERIFICATION WITH A SPICE SIMULATION

The analysis presented in the previous section was verified using the single stage PA shown in Fig. 2(a) where 180-nm 1P6M CMOS technology was used in the simulation. Transient simulation with the circuit was carried out using the same bias conditions in the time domain, and the drain voltage was transformed to the signal in the frequency domain using a fast Fourier transform.

We obtained F = 25.81 GHz, which was slightly higher than the calculated one. It should be noted that the calculated CM oscillation frequency was quite similar to the simulated value with the simplified small-signal model of the MOS transistor even though the MOS behaves as a non-linear component when the oscillation starts since it is operating in the large-signal domain.

IV. DESIGN GUIDELINES FOR THE AMPLIFIER STABILIZATION

A. THE EFFECT OF CM INDUCTANCE ON STABILITY

We investigated the effects of parasitic inductance and resistance on the CM oscillation frequency to establish useful design guidelines. In the simulation, we selected several NMOS devices of different sizes to check the validity of the proposed analysis. The parasitic resistance of each inductor was chosen such that its Q_e was 10 at 10 GHz. Fig. 3 illustrates the variation of the oscillation frequency versus L_g or L_d, where L_g = 250 pH when the NMOS device size was 180×0.18 μm or L_d = 150 pH when it was 90×0.18 μm. The simulated and calculated values corresponded well with each other for the different device sizes, which indicates that the

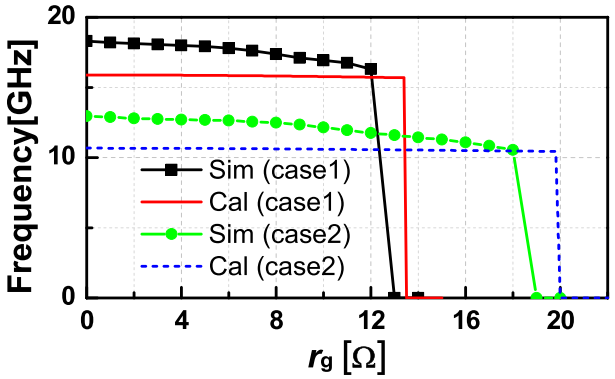


FIGURE 4. Calculated and simulated oscillation frequencies versus r_g: Case 1: Lg = Ld = 250 pH and Case 2: Lg = Ld = 500 pH.

proposed analysis method using the small-signal half-circuit was accurate and useful for estimating the essential behavior of CM oscillation.

It is noteworthy that L_d, L_g, and C_{gd} are the components mainly taking charge in forming the positive feedback for the active device. Both in the simulation and calculation, the oscillation turns off if either L_d or L_g becomes zero or infinite. When $L_g = 0$ and $r_g = 0$, the active device becomes inactive, and thus no oscillation can remain since the gate voltage becomes zero. When there is no gate inductance (i.e., L_g is infinite), the drain voltage (V_d) and the gate voltage (V_g) are in phase due to a capacitive divider formed by C_{gd} and C_{gs}, as shown in Fig. 2(b). Therefore, no oscillation can remain in this case as well.

In a real case scenario, the CM inductances L_d and L_g always exist, thereby degrading amplifier stability. Therefore, we investigated several ways of preventing CM oscillation. Fig. 4 presents a comparison between the simulated and calculated oscillation frequencies as a function of r_g for two cases: $L_g = L_d = 250$ pH and $r_d = 1.57$ Ω, and $L_g = L_d = 500$ pH and $r_d = 3.14$ Ω. As expected, the oscillation frequency depended weakly on r_g, and the oscillation stopped when r_g was larger than a specific value, $R_{g,off}$. In the same way, increasing r_d also improved the stability of the amplifier. However, r_d should be kept as small as possible for improved efficiency since the drain current is conducted throughout it. In this case, a decoupling capacitor can be included in the center tap of the winding inductor at the drain to resonate out the CM coil inductance L_d. To achieve better stability, degrading quality factor of the bypass capacitor is also possible by applying additional resistance in series with it.

The bias resistor can usually be chosen to be much larger than the range of $R_{g,off}$ so that the oscillation can be turned off effectively. In this case, the effect of the bias path on the CM oscillation is only minor and can be ignored. However, in the case of bipolar-junction-transistor (BJT) amplifiers, the base bias resistor should be kept small enough to conduct the DC base current. The minimum required gate (base) resistance ($R_{g(b),off}$) was calculated and compared to the simulation results, as shown in Fig. 5.

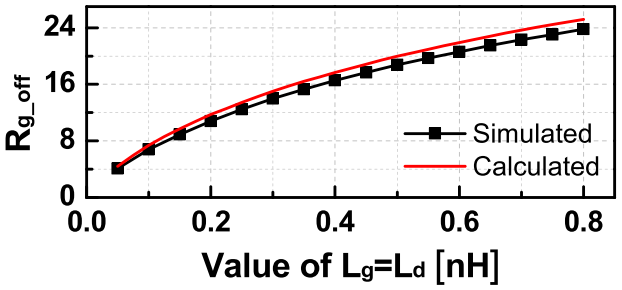


FIGURE 5. Calculated and simulated gate resistances which prohibited the unstable oscillations ($r_d = (2\pi \times 10G \times L_d)/10$).

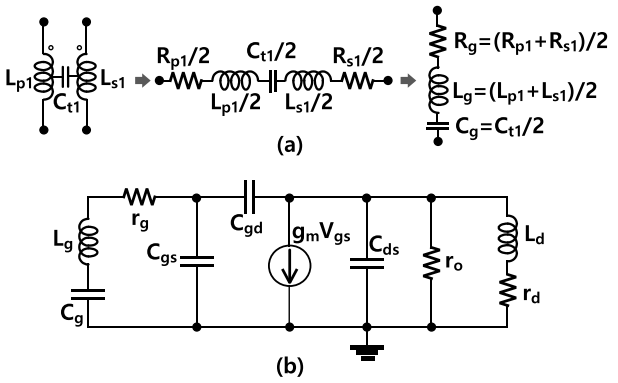


FIGURE 6. (a) The parasitic capacitance between the two coils of the input transformer and (b) the small-signal CM half-circuit of the PA.

B. THE EFFECT OF THE COUPLING CAPACITANCE BETWEEN THE COILS

Typically, two coils are placed in proximity to achieve strong magnetic coupling to obtain a high-efficiency on-chip transformer. The narrow gap between the two coils results in significant parasitic capacitance between the two windings even though it is distributed over the entire length of the two winding coils. We can use a lumped capacitor connected between two central points of the two coils to investigate its effect on the stability of the circuit, as depicted in Fig. 6(a).

It is interesting to observe that the push-pull amplifier may experience instability because of the capacitance between the two coils of the input transformer. The series coupling capacitor between the two coils of the input transformer (C_{t1}) can form a closed path for the CM oscillation. Let us add a gate capacitor ($C_g = C_{t1}/2$) to the half-circuit of the CM operation, as shown in Fig. 6b. When we ignore the bias path, the gate resistor and inductor can now be calculated as $r_g = (R_{s1} + R_{p1})/2$ and $L_g = (L_{s1} + L_{p1})/2$ (Fig. 2(a)). The analysis in the previous section can be applied when substituting Z_g given in (1) by

$$Z_g = sL_g + r_g + \frac{1}{sC_g}. \tag{9}$$

Using the new Z_g to calculate the elements of the impedance matrix $\mathbf{Z}$ given in (4) and then replacing these values in (6), we can obtain a new expression for the numerator of $det(\mathbf{Z})$, represented by $A(s)$. As an example, if $L_g = 300$ pH, $L_d = 200$ pH, r_g and r_d are chosen so that the Q_e of their inductance is 15 at 20 GHz, $C_{t1} = 150$ fF, and the MOS

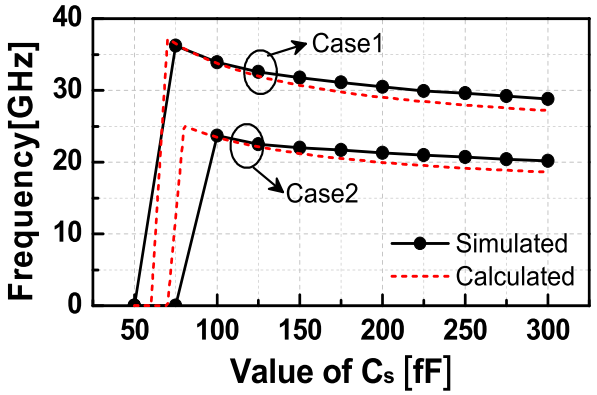


FIGURE 7. The calculated and simulated oscillation frequencies versus Cg: *Case 1*: L_g = 300 pH, L_d = 200 pH and *Case 2*: L_g = 600 pH, L_d = 400 pH.

transistor size is 90 × 0.18μm with C_{ds} = 52.9 fF, C_{gs} = 99.7 fF, C_{gd} = 29.4 fF, g_m = 38.7 mS, and r_o = 549 Ω, the solutions of the equation $A(s) = 0$ are $s_{12} = 2\pi \times 44.3 \times (-0.32 \pm j)$ Grad/s and $s_{34} = 2\pi \times 30.72\text{G} \times (0.06 \pm j)$ Grad/s. Thus, there is a CM oscillation at the frequency of 30.72 GHz. The simulation results showed an oscillation at 31.62 GHz, which is slightly higher than the calculated value.

Fig. 7 contains a plot of the variation in oscillation frequency versus C_{t1} for two cases: L_g = 300 pH, r_g = 2.51 Ω, L_d = 200 pH, and r_d = 1.67 Ω and L_g = 600 pH, r_g = 5.02 Ω, L_d = 400 pH, and r_d = 3.34 Ω. The calculated and simulated values were a good match, both showing that the CM oscillation stopped when C_{t1} was smaller than a certain value. For example, for case 2, when the calculated C_{t1} = 70 fF, the oscillation was not triggered while the minimum series value in the simulation was around 75–100 fF.

It should be noted that even though the resistive losses in the system might have been significant enough to turn off the oscillation, the small damping factor in the solution forecasted considerably long settling time of the PA, which should be avoided. To further prevent instability, we can increase the resistive loss by increasing r_d and r_g or decrease the capacitive coupling by reducing C_g. However, these component values should not be set as a trade-off in a practical design. Thus, any additional resistors must be avoided in the signal path to guarantee the high efficiency of the designed PA.

C. SERIES RC FEEDBACK NETWORK

Using a resistive feedback network by connecting a resistor (R_{fb}) between the gate and the drain of the transistor can compress the gain of the system, which helps to mitigate instability. The feedback resistor is typically connected in series with a capacitor (C_{fb}) to provide the ability to bias the gate and the drain independently, as illustrated in Fig. 8. The calculation of this case with the previous method is still applicable if Z_{gd} in (1) is replaced by

$$Z_{gd} = \frac{\frac{1}{sC_{gd}}\left(\frac{1}{sC_{fb}} + R_{fb}\right)}{\frac{1}{sC_{gd}} + \frac{1}{sC_{fb}} + R_{fb}}. \tag{10}$$

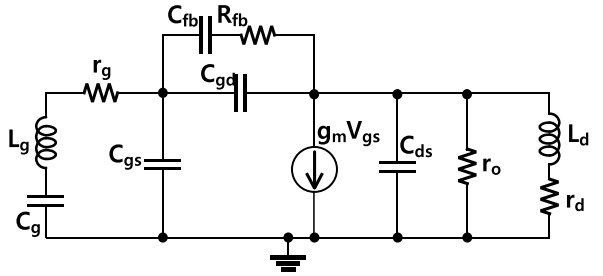


FIGURE 8. A schematic of common-mode half-circuit push-pull amplifier with RC feedback circuit (the bias circuit is hidden).

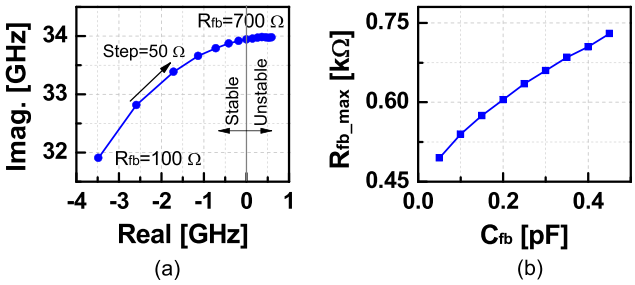
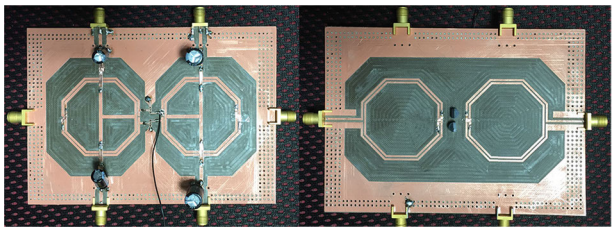


FIGURE 9. (a) The root locus of the point causing instability versus the value of R_{fb}. (b) The simulated maximum value of R_{fb} required to turn off oscillation.

The expression of Z_g is still the same as in (9). The numerator of $det(\mathbf{Z})$, i.e. $A(s)$, is now a quintic polynomial with an additional real zero. For example, if L_g = 300 pH, r_g = 2.51 Ω, L_d = 200 pH, r_d = 1.67 Ω, C_g = 100 fF, C_{fb} = 200 fF, R_{fb} = 800 Ω, and the MOS transistor size is 90 × 0.18 μm with the parameters given in the previous section, the solutions of the equation $A(s) = 0$ are $s_{12} = 2\pi \times 46.28 \times (-0.27 \pm j)$ Grad/s, $s_{34} = 2\pi \times 33.71 \times (0.03 \pm j)$ Grad/s, and $s_5 = -1.16 \times 10^{10}$ rad/s. This means that there is a CM oscillation at 33.71 GHz, which is close to the simulation value of 33.67 GHz.

By using the small-signal analysis, the root locus of the system-pole (or the zero of $det(\mathbf{Z})$) that causes instability in the circuit is plotted as a function of R_{fb} as shown in Fig. 9(a). To suppress the oscillation, the value of R_{fb} should be smaller than a specific value, $R_{fb(max)}$, to provide a large enough loss between two *LC* tanks at input and output ports as depicted in Fig. 8. Meanwhile, R_{fb} must be chosen to be large enough for a better closed-loop gain. In addition, R_{fb} should not be too small to provide valid resistive feedback for a meaningful power gain. Otherwise, an oscillation occurs at a lower frequency as C_{fb} is effectively added to C_{gd}. Also, it would significantly reduce the power efficiency as well as the gain of the PA if the RC feedback is configured with a small R_{fb} and a large C_{fb}. Therefore, proper selection of R_{fb} is essential for a robust PA design with well balanced RF performance. Fig. 9(b) shows the maximum value of R_{fb} ($R_{fb(max)}$) required to stabilize the circuit depending on the value of C_{fb}. Different from r_g and r_d, the critical point of maintaining oscillation depends weakly on R_{fb} since R_{fb} is not in the main path that



(a) (b)

FIGURE 10. The on-board push-pull amplifier. (a) the front side and (b) the back side.

creates the CM oscillation. This results in a relatively large error in calculating $R_{\mathrm{fb(max)}}$ using small-signal analysis as compared to the value seen from large-signal simulation for suppressing the instability. Therefore, it is recommended to be conservative in selecting $R_{\mathrm{fb(max)}}$ in a practical design.

Based on our analysis, the principle of the RC feedback was applied in designing an X-band PA in 65-nm CMOS [1]. With proposed analysis results, careful biasing routing line with the series resistor was applied as well [1], [2]. To avoid the CM mode instability of the push-pull configuration, a single-pull amplifier was designed in 180-nm CMOS [14]. A series RC feedback network was also applied between gate and drain of the NMOS to provide stable operation with improved bandwidth, which confirmed the validity of the proposed stability test and the established design guidelines in various CMOS technology nodes.

V. EXPERIMENTAL VERIFICATION

It is difficult to validate the established design guidelines using a fully integrated PA in CMOS technology. Instead, the on-board push-pull amplifier presented in Fig. 1b was implemented using a high-frequency BJT (2N3904) with a cut-off frequency of 300 MHz. The implemented PA is shown in Fig. 10. The onboard input and output transformers were implemented with a center-tap option so that it could be soldered to any extra inductor to change the CM inductances (L_{g} and L_{d}) of the amplifier for verification purposes. At first, each center tap was shorted to GND, as can be seen on the front of the push-pull amplifier in Fig. 10a. It should be noted that noise from the bias line would affect the amplifier if the bypass capacitors were absented. Moreover, the structure balance would be broken at the operating frequency regime. The applied bypass capacitor was 100 μF, which was large enough to be considered as a short circuit in the MHz-range (e.g., at 1 MHz, a 100 μF capacitor has a reactance of 1.6E-3 Ω). The collector voltage waveform of each transistor was directly probed and measured with a digital oscilloscope (Keysight DSOX6002A).

With the original design of the onboard transformers, the CM inductances were so small that the active devices did not sustain any oscillations. However, when L_{g} and L_{d} were increased with the extra inductors connected to the center tap, it led to instability in the PA under various ranges of bias points. Fig. 11 presents the measurement setup where the transistors were biased with base current $I_{\mathrm{b}} = 0.058$ mA

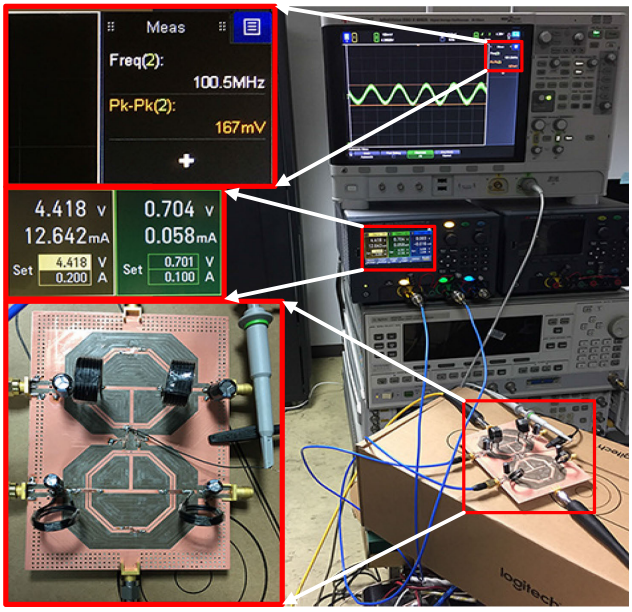
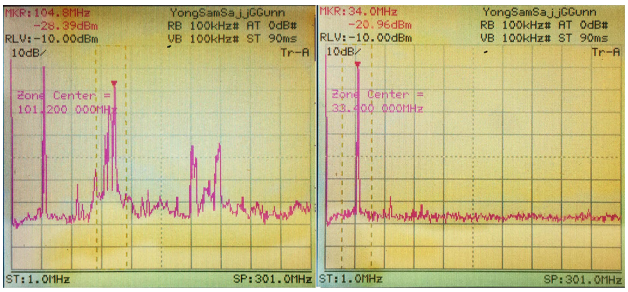


FIGURE 11. Measurement of common mode oscillation in the push-pull amplifier.



(a) (b)

FIGURE 12. Output spectrum before stabilization (a) and after stabilized by using a 50 Ω resister at the base bias line.

and collector current $I_{\mathrm{c}} = 12.6$ mA under stable conditions. At this bias point, the amplifier had a 7-dB small-signal gain. When we measured the oscillation, the input and output were terminated with 50 Ω. On the oscilloscope, a sinusoidal voltage swing was observed at the transistor's collector with a frequency of around 100 MHz and a peak-to-peak swing of 167 mV. The output spectrum of the unstable amplifier is given in Fig. 12(a) with $P_{in} = -28$ dBm at 33 MHz. It can be seen that the signal was disturbed by unwanted spurious tones at around 100 MHz along with their second harmonics from the CM oscillation. Following the proposed design guidelines, the amplifier was stabilized as expected by using a base resistor of 50 Ω (the measured output spectrum is presented in Fig. 12(b)).

VI. CONCLUSION

We presented an advanced common-mode (CM) stability analysis of the transformer-based power amplifier (PA) based on a small-signal model in the complex frequency domain.

The analysis carried out in the complex frequency domain proved its validity in predicting the oscillation frequency with high accuracy, which was compatible with the SPICE simulation. With the proposed stability test, it was shown that a biasing line connected to the gate could induce instability and the parasitic capacitance between the two coils of an input transformer could severely degrade the CM stability of the PA under test. Design guidelines were discussed for the biasing line and the RC feedback network to get better stability for a transformer-based push-pull PA. The analysis was verified experimentally by implementing an onboard transformer-based push-pull amplifier in the MHz-range. The CM stability test and design guidelines developed in this work could apply to general linear time-invariant circuits to check their stability effectively.

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