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Original Approach Toward Three-Phase Indirect Matrix Converters Through Hybrid PWM Modulation and DSP Implementation

AMIRA AMMAR^{1,2}, (Member, IEEE), HADI Y. KANAAN¹, (Senior Member, IEEE),
NAZIH MOUBAYED², (Senior Member, IEEE),
MAHMOUD HAMOUDA³, (Member, IEEE),
AND KAMAL AL-HADDAD⁴, (Life Fellow, IEEE)

¹Faculty of Engineering–ESIB, CST, Saint Joseph University, Beirut 11-0514, Lebanon

²Faculty of Engineering, CRSI, LaRGES, Lebanese University, Beirut, Lebanon

³Research Laboratory LATIS, ENISO, University of Sousse, Sousse, Tunisia

⁴GREPCI, École de Technologie Supérieure (ETS), Université du Québec, Montréal, QC H3C 1K3, Canada

Corresponding author: Amira Ammar (ammar.h.amira@gmail.com)

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ABSTRACT Power electronic matrix converters are converters carrying out just one solitary transitional stage. AC-AC conversion automatism in matrix converters is attained through the exploitation of bidirectional controllable power switches associated with a structural matrix. The indirect matrix converter is an alternating preference to the direct matrix converter embodied by AC-DC converter and DC-AC inverter. In this paper, an assemblage of Pulse Width Modulation categories is used to control the dual stages of IMC. AC-DC converter is modulated through the well-known space vector algorithm, while DC-AC inverter is modulated through a novel algorithmic conception referred to as the digital scalar algorithm. Comparative analysis between the conventional DSVPM modulation and the novel proposed modulation technique is escorted demonstrating that the latter is facilely comprehended and simply put into real-time practice. This paper comes forward with digital signal processor real-time enforcement, conceived for indirect matrix converter. Uniting both original approaches into one topological system entrained a significant decrease of 38% in real-time computation assesses. Throughout the paper, it is well proven that the proposed solution results in high-quality input/output waveforms, and averts from servicing supplementary devices that trigger silicon devices' gates. Numerous experimental enquires within the delivered research reveal advantageous aspects of the contemporary approach from overall simplicity to entire effectiveness.

INDEX TERMS Computation burden, distributed power, grid-connected converter, matrix converters, real-time implementation, scalar modulation, space vector modulation, unity displacement factor operation.

I. INTRODUCTION

Matrix converters are AC-AC power topologic converters that receive electrical signals characterized by fixed voltage, magnitude, and frequency from the input AC grid source. Their role is then to deliver electrical signals characterized by variable voltage, magnitude, and frequency to the output AC load. Less demand for energy storage devices makes the valuation of the converter high. Matrix converters hold multiple enticing distinguishing features over customary AC-AC power topologic converters. The considerably advantageous

feature of MC is the capacitor-free aspect. The absence of massive electrolytic polarized capacitors, that are of confined lifespan, from the converter elicits compact design, reliable circuitry, and enhanced power density structure. The additional favorable feature is the admirable quality of input/output grid/load current and voltage waveforms. Possessing a manageable input power factor is feasible due to the existence of bidirectional power switches. The drawback of MC topologies is the restricted output/input voltage magnitude transfer ratio [1]–[4].

Indirect matrix converters are improved substitutes of matrix converters developed to comply with the needs of industrial claims. The topology is composed of two separate

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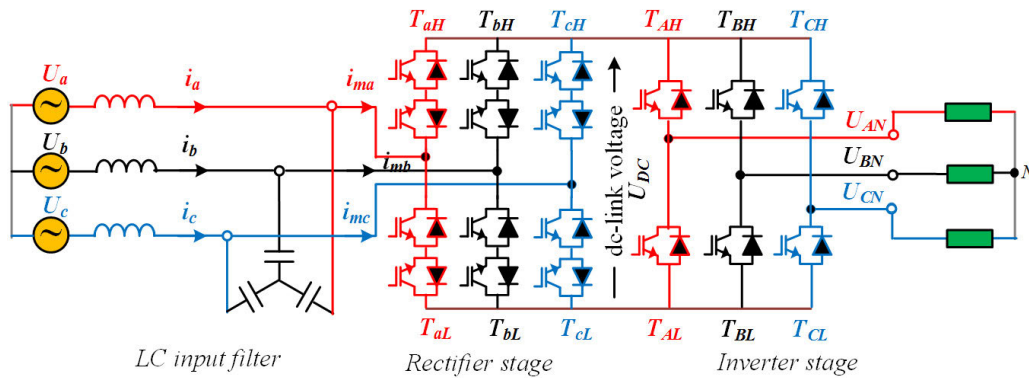


FIGURE 1. The power circuit of indirect matrix converter topology IMC.

stages. Fig. 1 shows the power circuit of the grid-connected indirect matrix converter topology (IMC). Rectification for alternating current AC to direct current DC takes place in stage 1 through the grid-connected four-regional rectifier. During this stage, the rectifier receives fixed grid voltage signals and controls grid current signals to safely deliver positive DC voltage at its output. A capacitor-free indirect matrix converter behaves with the DC voltage as a virtual entity. Inversion from direct virtual current DC to alternating current AC takes place in stage 2 through the load-connected four-regional inverter. During this stage, the inverter receives variable virtual DC voltage and controls the load voltage to safely deliver targeted quantities at its output. Indirect matrix converters hold several appealing hallmarks over direct matrix converters. The considerably advantageous features of IMC are the ease in the commutation process and the reduced need for clamps. Indirect matrix converters are encouraging for industries that work for distributed generation systems (DG), multi-phase drives, and multi-phase machines [5]–[10].

Modulation strategies are set to adjust input-grid current properties and alter output-load voltage properties. Various modulation approaches were suggested and applied to IMC such as the double space vector pulse width method (DSVPWM) and carrier pulse width method (CPWM). Comparative analysis for DSVPWM and CPWM is conducted to illustrate the following; DSVPWM ensures the utmost flexibility in terms of distributing switches' sequences, guarantees minor levels of load current harmonics, and mitigates the common-mode voltage gain. Contrarily, this modulation discloses complex accounts and formulation. As for CPWM, it ensures direct application and fewer calculation requirements. Conversely, sequencing flexibility is not touched and real-time implementation is difficult relative to in-market controllers' availability. Sophisticated studies in the literature were previously announced in terms of closed-loop control methods such as, but not limited to, predictive control, sliding mode control, and repetitive control, to improve the overall system's dynamic response, raise accuracy, & reinforce bodies' robustness [11]–[15].

The absence of bulk energy storage devices in matrix converter topologies grounds the necessity of complex

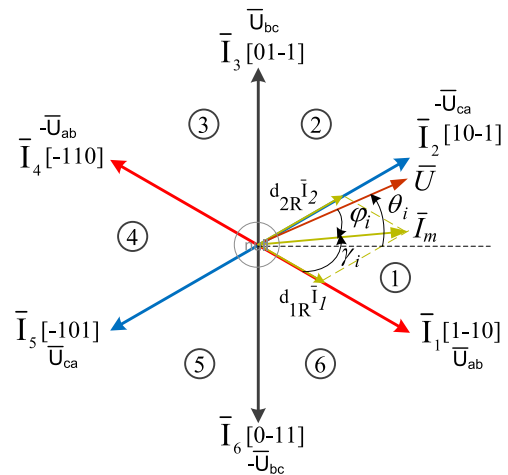


FIGURE 2. Input current reference vector reflected through SVPWM.

algorithmic methods' platforming such as digital signal processor (DSP), complex programmable logic device (CLPD), or field-programmable gate array (FPGA) bases. The former platforming is high-priced, nonintegrated, and in demand for software development expertise. Besides, DSP sets out total synchronization of input source and establishes gate signals without supplementary circuitry.

This paper is entitled to the original approach towards indirect matrix converters through hybrid PWM modulation and DSP implementation. The AC-AC power topologic converter to be considered in this research is the indirect matrix converter. As for the originality of the modulation, a hybrid combination of two algorithms; the SVPWM and the simple, easily understood, scalar modulation (SPWM), is set forward to modulate electrical entities of the power system. SVPWM is annexed to the rectifier stage while SPWM is annexed to the inverter stage. As for the originality of the real-time implementation, simplicity rules the situation owing to the fact that 1 DSP controller chip is employed avoiding any FPGAs. Both united approaches reveal around 40% reduction in count time without affecting the good operation of topology.

This well-developed research paper is organized point to point. In the introduction, the power topology studied is clearly specified. Section II thoroughly narrates the original approach through hybrid PWM modulation by putting into hand the modulation of the grid-connected rectifier and the load-connected inverter stages. Section III lists all design parameters and displays the verification of the former approach through Simulink Simulation. Section IV precisely reports the original approach through both stages' control and DSP real-time implementation. Section V ensures the originality of the approach by displaying the experimental setup and results. Section VI compares analytically the converter's performance under DSVPMW versus Hybrid combination. In the conclusion section, the main advantages of the proposed algorithm and the overall proposed solution are underlined.

II. ORIGINAL APPROACH THROUGH HYBRID PWM MODULATION

A. MODULATION OF THE GRID-CONNECTED RECTIFIER STAGE OF THE IMC

As it is clear in Fig. 1, the main electrical power is delivered from the grid, which is considered the input to the topologic rectifier. Assign letters (a, b, c) to the three-phase input source where grid voltages are sinusoidal, symmetrical, and balanced denoted by (U_a, U_b, U_c) and specified in Equation (1) [16]–[18]:

$$\begin{aligned} U_a &= \hat{U} \cos(\omega_i t) \\ U_b &= \hat{U} \cos(\omega_i t - \frac{2\pi}{3}) \\ U_c &= \hat{U} \cos(\omega_i t - \frac{4\pi}{3}) \end{aligned} \quad (1)$$

Input currents denoted by (i_a, i_b, i_c) sustain inductance-capacitance input filtering before turning into the converter's input currents (i_{ma}, i_{mb}, i_{mc}). Straightaway, the aim of the modulation and the function of the rectifier stage are primarily to keep (U_a, U_b, U_c) and (i_a, i_b, i_c) constantly in-phase and secondly to deliver positive voltage at the stage's output where this voltage is to be of virtual DC nature (U_{dc}). In this sub-section, the modulation of the grid-connected rectifier stage through SVPWM is clarified. The AC-DC rectifier, considered in Fig. 1, consists of 6 bi-directional power switch, each of which consists of 2 MOSFETs and 2 diodes joined in an anti-parallel manner. Assign letters (H, L) to indicate the position of each power switch through rectifier phases. (T_{aH}) is the switch located in the input rectification phase at the higher end of the topology. The space vector theory is applied and the three-phase instantaneous electrical quantities are represented in a single space vector. (T_{aH}) can be either ON holding the value 1 or OFF holding the value of 0. Alternating between 0 and 1 for both switches (T_{aH}) and (T_{aL}) located in phase a , 3 status combinations per phase are possible and 27 status combinations per stage are present. Taking into account that no source short circuit and no open load circuit are permitted, 9 out of these 27 combinations are admissible.

These 9 combinations represent \bar{I} , the input current space vector displacement in space where 3 of them are null and 6 space vectors are allowable [19]–[24].

Fig. 2 shows the 6 active space vectors. \bar{I}_1 is an active input current space vector with coordinates $[1, -1, 0]$. This means:

$$\begin{aligned} leg_a &= 1, \text{“}T_{aH} \text{ is ON \& } T_{aL} \text{ is OFF”} \\ leg_b &= -1, \text{“}T_{bH} \text{ is OFF \& } T_{bL} \text{ is ON”} \\ leg_c &= 0, \text{“}T_{cH} \text{ is OFF \& } T_{cL} \text{ is OFF”} \end{aligned}$$

9 current combinations bring forth 9 values of the rectifier's output virtual DC-Link voltage (U_{dc}). The 6 active input current states correspond to 6 input grid voltage states. Let \bar{U} resemble the state of (U_a, U_b, U_c). Using an angular phase detector controller, the input instantaneous phase angle θ_i which is equal to $\omega_i t$ is estimated and the sector location (k_i) is determined as is clear in Fig. 2. The first step into the modulation is to make known the reference input current space vector. The goal is to obtain the unity input displacement factor that is achieved when \bar{U} and \bar{I} are always in phase. Generally discussing, consider that the power factor is variable and there exists a value for input displacement angle denoted by φ_i . All data considered, \bar{I}_m being the reference input current vector is skillfully located in the space graph with an angle $\gamma_i = \theta_i + \frac{\pi}{6} + \varphi_i$. Back to Fig. 2, suppose that the input voltage vector is located in sector 1. Subsequently, is positioned and can be realized through partial operations of the active combinations reflecting the status of rectifier switches. Active vectors that are responsible to achieve the reference current located in sector 1 are \bar{I}_1 and \bar{I}_2 in a fraction of a period application [25]–[27]. Define d_{1R} as the duty ratio of application of \bar{I}_1 and d_{2R} as the duty ratio of application of \bar{I}_2 . Equations (2), (3), (4), (5), and (6) depict the geometrical analysis [28]–[35].

$$d_{1R} |\bar{I}_1| = \sin(\frac{\pi}{3} - \gamma_i) |\bar{I}_m| \quad (2)$$

$$d_{2R} |\bar{I}_2| = \sin(\gamma_i) |\bar{I}_m| \quad (3)$$

In order to benefit from the full power, null status vectors are not exploited and duty ratios of any 2 out of the 6 active vectors add up to 100%.

$$d_{1R} + d_{2R} = 1 \quad (4)$$

$$d_{1R} = \frac{\sin(\frac{\pi}{3} - \gamma_i)}{\cos(\frac{\pi}{6} - \gamma_i)} \quad (5)$$

$$d_{2R} = \frac{\sin(\gamma_i)}{\cos(\frac{\pi}{6} - \gamma_i)} \quad (6)$$

Under each switching period of 100 μ s, the duty ratios are modified yielding new status vector switching and new average value described below.

$$\langle U_{dc} \rangle = d_{1R} U_{ab} + d_{2R} (-U_{ca}) \quad (7)$$

$$\langle U_{dc} \rangle = \frac{3}{2} \hat{U} \frac{\cos(\varphi_i)}{\cos(\frac{\pi}{6} - \gamma_i)} \quad (8)$$

The ripple designation, evident in the Equation (9), is transferred from the rectifier stage to the inverter stage through

the intermediate DC link. The inverter is hereby in charge to remove it as it will be deliberated in the following sections.

$$Ripple = \frac{1}{\cos(\frac{\pi}{6} - \gamma_i)} \tag{9}$$

Due to the presence of 6 space sectors, there exist 6 possible reference current positions relative to sector number. Equation (10) is a general formula for γ_i varying the sector number k_i .

$$\bar{\gamma}_i = \gamma_i - (k_i - 1)\frac{\pi}{3} \tag{10}$$

B. MODULATION OF THE LOAD-CONNECTED INVERTER STAGE OF THE IMC

In this subsection, the scalar modulation of the load-connected inverter stage through SPWM is clarified. The main electrical power should be delivered to the load, which is considered the output of the topologic inverter. Assign letters (A, B, C) to the three-phase output load where voltages, denoted by (U_{AN} , U_{BN} , U_{CN}) are normalized and their fundamental components referenced to the neutral phase are specified in Equation (11).

$$\begin{aligned} U_{AN} &= M_i \cos(\omega_o t) \\ U_{BN} &= M_i \cos(\omega_o t - \frac{2\pi}{3}) \\ U_{CN} &= M_i \cos(\omega_o t - \frac{4\pi}{3}) \end{aligned} \tag{11}$$

The goal of this modulation is to safeguard sinusoidal output voltages with controllable frequency and amplitude. The DC-AC inverter consists of 6 bi-directional power switch, each of which consists of 1 MOSFET and 1 diode joined in an anti-parallel manner. For easier analysis, it is considered that the virtual DC-Link voltage input of the inverter is ripple-free as in Equation (12).

$$U_{dc} = \frac{3}{2} \hat{U} \cos(\varphi_i) \tag{12}$$

Back to Equation (11), the angular velocity of the output voltages is ω_o , M_i is the dedicated inverter modulation index, and the peak value of the fundamental component is \hat{U}_o tracked in Equation (13).

$$M_i = \frac{\hat{U}_o}{\frac{U_{dc}}{2}} \tag{13}$$

Replacing Equation (12) into (13), the value M_i is as follows:

$$M_i = \frac{\hat{U}_o}{\frac{3}{2} \hat{U} \frac{\cos(\varphi_i)}{2}} \tag{14}$$

Let q be the output/input voltage transfer ratio such that:

$$q = \frac{\hat{U}_0}{\hat{U}} \tag{15}$$

Therefore, M_i and q will relate as below:

$$q = M_i \frac{3}{4} \cos(\varphi_i) \tag{16}$$

Injection of a zero-sequence signal into the PWM method is imposed here for the sake of increasing to a maximum value 1.155 . Consequently, q has a maximum value of $0.866 \cos(\varphi_i)$. which is, in turn, the generalized maximum value for the voltage transfer ratio of all three by three matrix converters. The modified output reference voltage is acquired after the common-mode injection through the initial sinusoidal reference vectors. It should be pointed out that the injections disappear from line-line voltage signals. Denote by (U_A , U_B , U_C) the modulation signals and by U_{zs} zero-sequence signal injected; stated in Equation (17).

$$\begin{aligned} U_A &= U_{AN} + U_{zs} \\ U_B &= U_{AB} + U_{zs} \\ U_C &= U_{CN} + U_{zs} \end{aligned} \tag{17}$$

Another injection into the modulation signals takes place for the purpose of demounting the ripple term stated in Equation (18) so the final modulation signals are as below:

$$\begin{aligned} U_A^* &= (U_{AN} + U_{zs}) \cos(\frac{\pi}{6} - \bar{\gamma}_i) \\ U_B^* &= (U_{BN} + U_{zs}) \cos(\frac{\pi}{6} - \bar{\gamma}_i) \\ U_C^* &= (U_{CN} + U_{zs}) \cos(\frac{\pi}{6} - \bar{\gamma}_i) \end{aligned} \tag{18}$$

(T_{AH}) is the switch located in the output inversion phase at the higher end of the topology. T_{AH} is turned on by means of its duty cycle with reference to U_A^* . Equation (19) shows the duty cycles of T_{AH} , T_{BH} , and T_{CH} .

$$\begin{aligned} d_A &= \frac{U_A^* + 1}{2} \\ d_B &= \frac{U_B^* + 1}{2} \\ d_C &= \frac{U_C^* + 1}{2} \end{aligned} \tag{19}$$

d_A , d_B , and d_C cannot take a value greater than 1 or less than 0 and for this restriction is enforced by inducing a translational term μ in the expression of the common-mode added voltage waveform such that $\mu(0 \leq \mu \leq 1)$ as per Equation (20).

$$\begin{aligned} U_{zs} &= \frac{2(\mu - \frac{1}{2})}{\cos(\frac{\pi}{6} - \bar{\gamma}_i)} - \\ &\mu \max(U_{AN}, U_{BN}, U_{CN}) \\ &+ (\mu - 1) \min(U_{AN}, U_{BN}, U_{CN}) \end{aligned} \tag{20}$$

Suppose, for instance, that SVPWM is applied to issue the modulating signals of the inverter's switches. When upper power switches, characterized by ($T_{AH}T_{BH}T_{CH}$) are set to 1, the 7th null space vector V_7 is therefore customarily applied. This application is considered a partial contribution to the freewheeling phase of the inverter stage. Let t_{V7} be the time of application of V_7 , and let t_0 be the time of the freewheeling phase. Equation (21) depicts that t_{V7} is directly proportional to via the slope μ .

$$t_{V7} = \mu t_0 \tag{21}$$

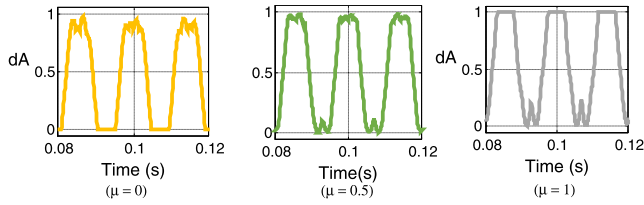


FIGURE 3. d_A Waveforms for three different values of μ .

Accordingly, the time of application of the following null space vector t_{V7} is alternatively expressed in Equation (22);

$$t_{V7} = \mu t_0 \quad (22)$$

Referring back to Equation (19), the overall equation governing d_A has only one variable that can be interchangeable which is μ . Simulation is done to obtain the waveforms of d_A given that the source frequency is considered 60Hz, and the load frequency is to be 70Hz with a transfer rate of 0.86. Fig. 3 shows the waveforms of Where μ shifts from 0, 0.5, and finally 1.

Graph interpretation of waveforms displayed in Fig. 3 indicates the following:

- When $\mu = 0$, and during the low cycle, the waveform is held tightly to 0
- When $\mu = 1$, and during the high cycle, the waveform is held tightly to 1
- When $\mu = 0.5$, and during the low and high cycles, the waveform is neither held tightly to 0 nor to 1.

For $\mu = 0$ & $\mu = 1$, losses of the inverter resulting from the switching process are reduced but on the other hand, the rectifier stage will not operate in safe commutation conditions.

In this research, μ is set to 0.5 to hand out equal distribution and assure the rectifier's safe commutation.

In Fig. 4, PWM sequences during all topological stages are rendered. Considering that the input current reference space vector lies in sector 1, as previously shown in Fig. 2, matching current status space vectors are $\bar{I}_1[1, -1, 0]$ and $\bar{I}_2[1, 0, -1]$ where \bar{I}_1 is applied for d_{1R} and \bar{I}_2 is applied for d_{2R} as appeared in Fig. 4(a). Respective values for the DC-link voltage are U_{ab} and $-U_{ca}$ for each instant cycle as appeared in Fig. 4(b). $\bar{I}_1[1, -1, 0]$ is founded by making $T_{aH} = 1$ and $T_{aL} = 0$, $T_{bH} = 0$ and $T_{bL} = 1$, with $T_{cH} = 0$ and $T_{cL} = 0$. In the same manner, $\bar{I}_2[1, 0, -1]$ is founded as appeared in Fig. 4(c).

When it comes to computing the duty cycles of the inverter stage, absolute synchronization between both stages must be conducted to accomplish the desired results reflected in output voltage and input current waveforms. Back to Equation (19), and given that the load voltage angle varies between $[0, \frac{\pi}{3}]$, duty ratios can take 3 values of maximum, minimum, and middle estimation.

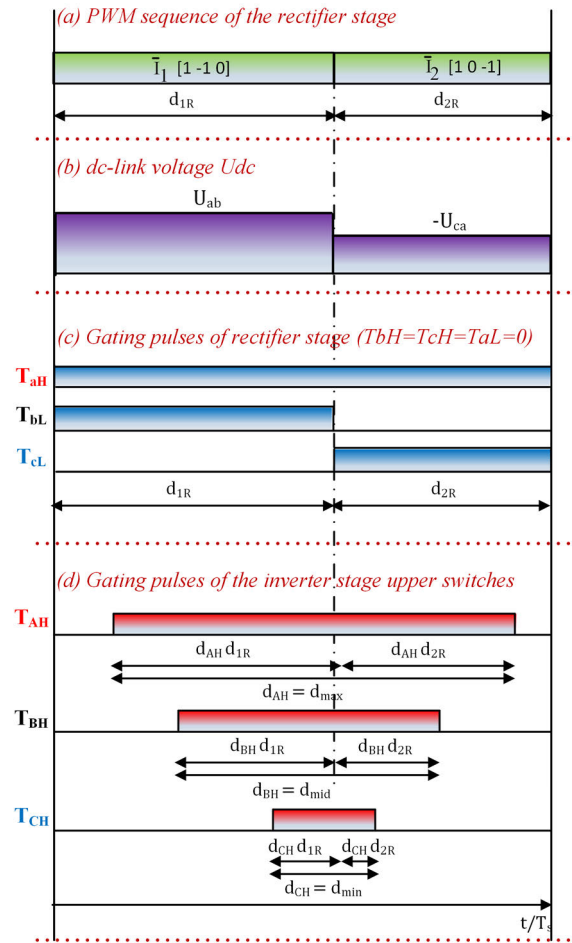


FIGURE 4. PWM Sequences during all topological stages.

Equation (23) sets the ratios as below:

$$\begin{aligned} d_{\max} &= d_A \\ d_{\text{mid}} &= d_B \\ d_{\min} &= d_C \end{aligned} \quad (23)$$

In what follows, (d_A, d_B, d_C) are proportioned between duty ratios of the rectifier stage, (d_{1R}, d_{2R}) . As is clear in Fig. 4(d), gate pulses of the inverter switches are deliberated as follows: T_{aH} is operational during $d_{1R}d_A$ when \bar{I}_1 is employed, and is operational during $d_{2R}d_A$ when \bar{I}_2 is employed. A profound study of PWM sequences in all stages of conversion clearly states that during one period T_s , and within the commutation of the rectifier, the three phases of the inverter are either clamped to the high end of the topology or all clamped to the opposite low end. This reveals that no current is given birth to during commutation and both stages are completely disconnected during commutation ensuring the safety rules discussed previously. The positive clamping happens during μt_0 whereas the negative clamping happens during $(1 - \mu)t_0$. Equation (24) reveals the relation between μ and T_s .

$$\mu t_0 = \frac{d_{\min}}{T_s} \quad (24)$$

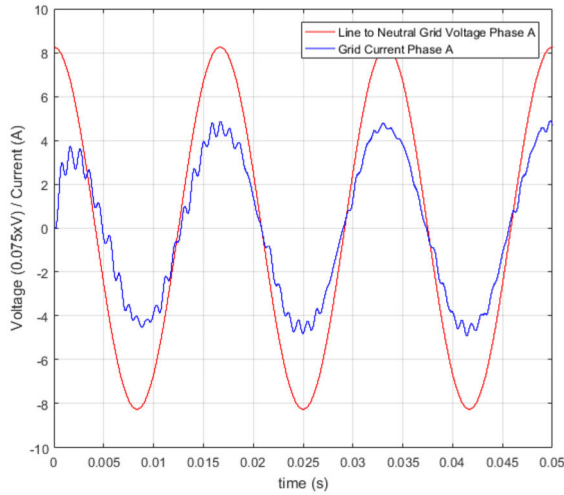


FIGURE 5. (U_a, i_a) the line-neutral grid reduced voltage (red) & current (blue) of phase a.

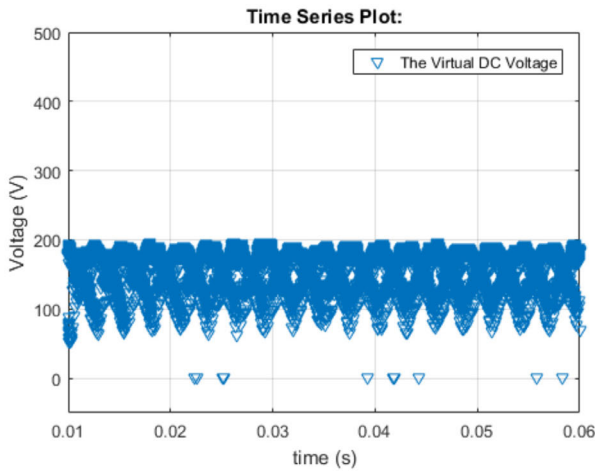


FIGURE 6. (U_{DC}) the virtual DC-link intermediate voltage.

III. THE APPROACH VERIFIED THROUGH SIMULATION RESULTS

The topology along with the hybrid modulation is tested using Matlab/Simulink/SimPowerSystems and the results are shown in Fig. 5, 6, 7, 8, and 9. The results prove that the topology and control work well enough. Table 1 below states the parametrical values used. Fig. 5 proves that the input current waveforms are sinusoidal and in phase with the grid voltages. In addition, Fig. 8 and 9 show that the waveforms of the output voltage is also sinusoidal and follows the inductive load current waveforms shown in Fig. 10. Fig. 6 reflects the virtuality aspect of the No DC-Link Voltage value with acceptable levels and values of harmonics.

IV. ORIGINAL APPROACH THROUGH DSP IMPLEMENTATION

A. REAL-TIME IMPLEMENTATION

As compared to the signals' analysis related to the conventional pulse width modulated voltage source inverters, the pulses to be applied directly on the gate power

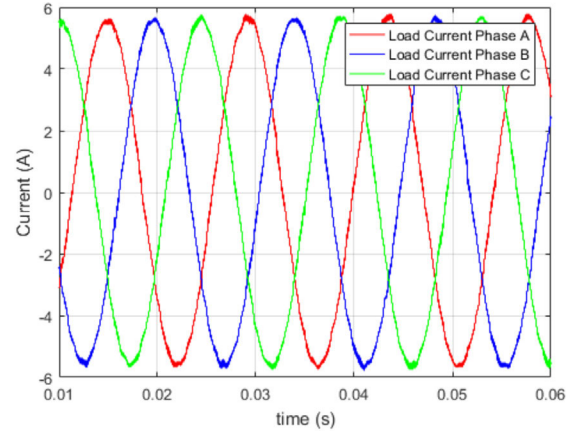


FIGURE 7. (i_A, i_B, i_C) the line load output currents.

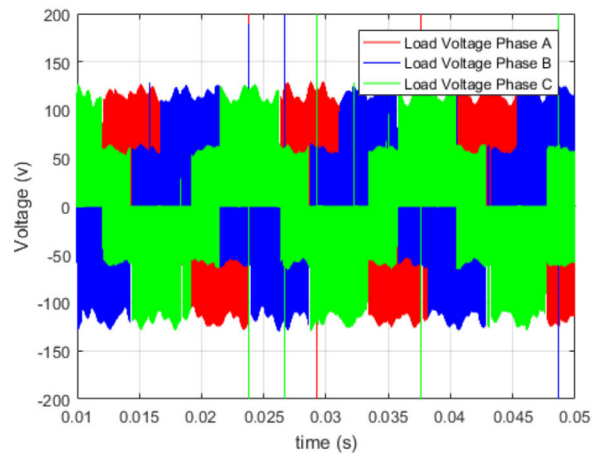


FIGURE 8. (U_{AN}, U_{BN}, U_{CN}) the line-neutral load output voltages.

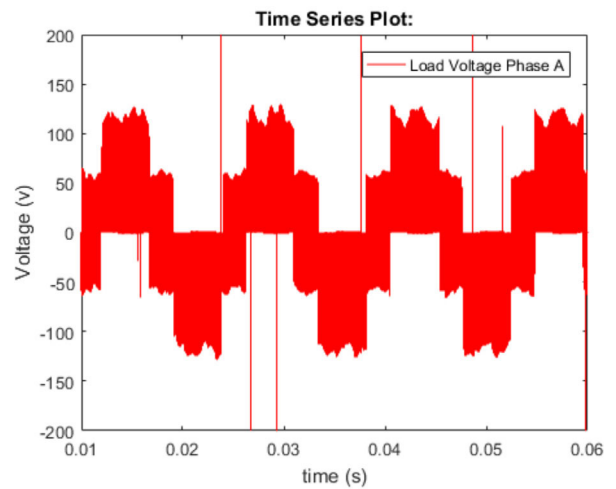


FIGURE 9. (U_{AN}) the line-neutral load output voltage.

switches of the indirect matrix converter are moderately dissimilar. Fig. 4 delineates that the pulses particular to the load-connected inverter stage are intrinsically not lined up centrally. Besides, the pulses particular to the grid-connected

TABLE 1. Design parameters' values.

General Parameters	Value
Switching Frequency	10 KHZ
Grid Input Parameters	Value
Phase to Neutral Voltage (Peak Amplitude)	110 v
Grid Frequency	60 Hz
Input Filter Parameters	Value
Capacitance	12 μ F
Inductance	2 mH
Resistance	0.5 Ω
Load and Output Parameters	Value
Voltage Transfer Ratio q	0.86
Output Frequency	70 Hz
Load Inductance	9 mH
Load Resistance	15 Ω

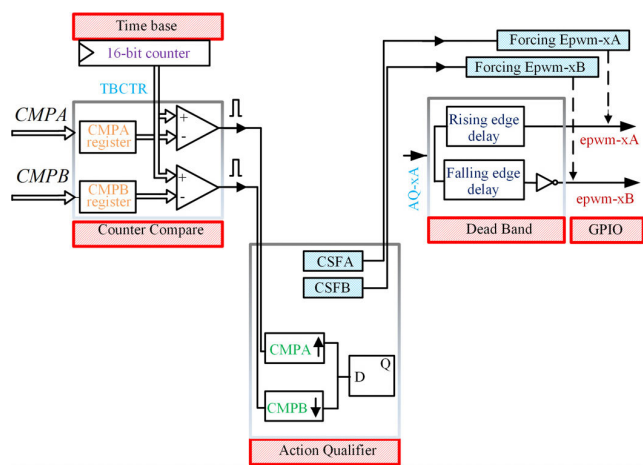


FIGURE 10. The enhanced pulse width modulator blueprint.

rectifier stage undergo, during a complete period of switching, modulation resulting in first, left / right lining up, and second, high/low forcing.

Additionally, the bidirectional power switches located along with the same leg of the rectifier, are gated in a way that their relative pulses are not restricted to be complementary. To date, almost all electric circuit arrangements that upshots logic results are founded by using *complex programmable logic devices (CPLD)* and *Field-programmable gate arrays (FPGA)* for the sake of building pulse width modulated switching sequences in real-time execution [36], [37].

In this article division, a forthright achievement of the objectives is realized through the evident application of the *Enhanced Pulse Width Modulator - Texas Instruments (ePWM)* of the digital signal processing DSP TMS320F28335.

The blueprint of the ePWM is revealed in Fig. 10 where its elementary building block is envisioned. This modular package is capable of engendering double signals that are primarily not dependant and secondly pulse width modulated. They are referenced by epwm-xA & epwm-xB and acquired

at the *General Purpose Input / Output GPIO* which portrays the periphery of the DSP.

CMP stands for compare function, where there exist, in the assembly, two counters of comparison CMPA & CMPB. CMPA & CMPB are prone to enforce epwm-xA & epwm-xB to become in high status or contrarily, in low status. This capability is accorded to the pattern arrangement of Control System Force CSFA & CSFB.

The pattern of the CSF is made up of 2 bits (0 & 1) combined and permuted. Three alterations out of four possible commutations are feasible to be set and attributed to CSFA & CSFB.

Equations (25) & (26) describe the dedicated allocation process.

$$\begin{aligned}
 CSFA = 00 & \quad ePWMxA = \text{disabled} \\
 CSFA = 01 & \quad ePWMxA = \text{status} - \text{low} \\
 CSFA = 10 & \quad ePWMxA = \text{status} - \text{high} \\
 CSFB = 00 & \quad ePWMxB = \text{disabled} \\
 CSFB = 01 & \quad ePWMxB = \text{status} - \text{low} \\
 CSFB = 10 & \quad ePWMxB = \text{status} - \text{high}.
 \end{aligned}
 \tag{25}$$

B. CONTROL OF THE LOAD-CONNECTED INVERTER STAGE

In furtherance of easiness in clarification, the upper transistor of the first phase A of the load-connected inverter will be addressed and detailed below. Immediately after the final acquisition of T_{AH} gate signal, a direct inverse manner is applied on this output signal so that it is applied on the gate of T_{AL} transistor. T_{AH} transistor gate is fed by the output of epwm-xA and similarly, T_{AL} transistor gate is fed by the output of epwm-xB.

Let TBCTR be the time base counter and define by TBPRD the maximal assess count of TBCTR. Equations (27) and (28) outline values that are charged into the comparison record CMPA & CMPB.

$$\begin{aligned}
 CMPA &= [d_{1R}(1 - d_{AH})]TBPRD \\
 CMPB &= [d_{1R}(1 - d_{AH}) + d_{1R}]TBPRD
 \end{aligned}
 \tag{27}$$

Continually, and within every entire switching period, a comparison process intervenes between TBCTR and CMPA / CMPB. Equation (29) points out the comparing occurrence:

$$\begin{aligned}
 TBCTR &= CMPA \\
 TBCTR &= CMPB
 \end{aligned}
 \tag{29}$$

These two instances are dispatched to the *Action Qualifier* AQ. Equations (30) & (31) reveal the output of the AQ.

$$\begin{aligned}
 TBCTR &= CMPA \text{ AQx} - \text{Status} - \text{high} \\
 TBCTR &= CMPB \text{ AQx} - \text{Status} - \text{low}
 \end{aligned}
 \tag{30}$$

AQx is afterward, submitted to the *Dead Band (DB)* as an input term. DB's outputs are the pulse width modulated signals. These two signals are additionally characterized by a time delay period that can be turned on and programmed.

Fig. 11 below demonstrates the following:

- a) Synthesize of gates pulses of T_{AH} and T_{AL} within an epwm module.

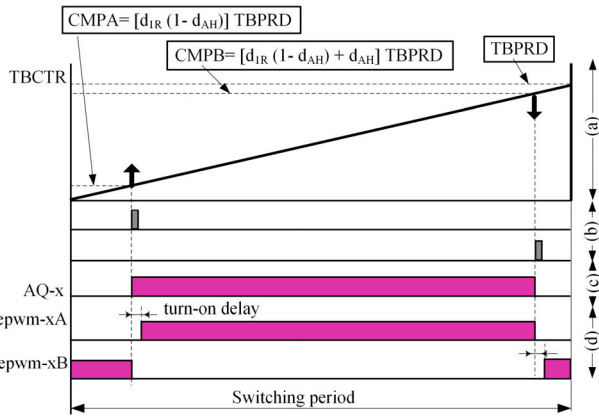


FIGURE 11. Gate pulses' synthesis for phase A switches.

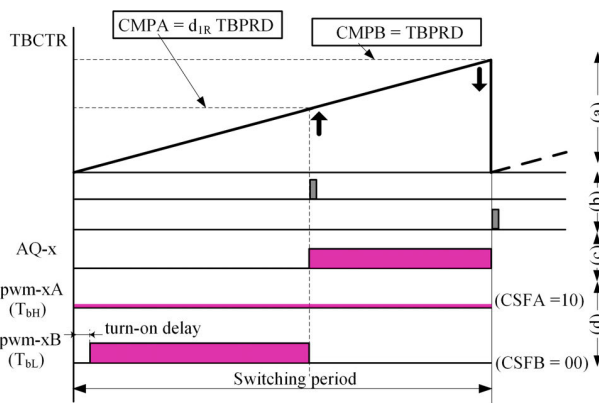


FIGURE 12. Gate pulses' synthesis for phase b switches.

- b) The instantaneous value of time base counter TBCTR-counter compare submodule output events.
- c) Action Qualifier output signal AQ-x.
- d) PWM output signals epwm-xA and epwm-xB.

An extremely significant benefit is remarked when zooming into Fig. 11 (a) and examining the geometrical nature of the TBCTR. The former is represented by a straight line indicating that its slope is approximately constant and this makes the method way more advantageous over the Carrier PWM approach.

C. CONTROL OF THE GRID-CONNECTED RECTIFIER STAGE

A similar approach to what was depicted in IV. B. will be interpreted in this coming section but the main difference is that the issues related to gates of the grid-connected rectifier will be dealt with. The upper and lower transistors of the second phase b of the grid-connected rectifier will be addressed and detailed below.

A back reference to Fig. 4 section (c) clearly states that while the pulse, that is transmitted to the gates of the lower transistors T_{bL} , undergo modulation, the gates of the higher transistors of, as well, phase b T_{bH} , undergo a low-status order.

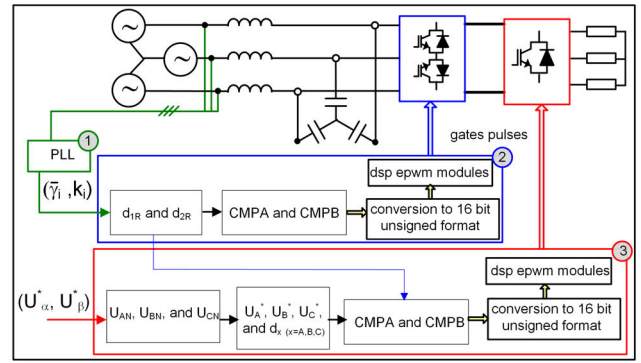


FIGURE 13. Simplified converter's block diagram and control algorithm.

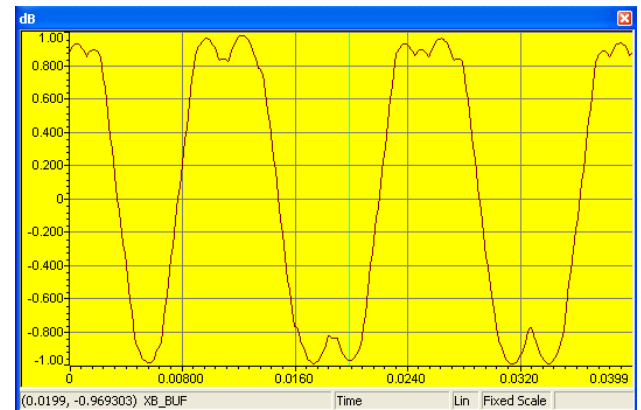


FIGURE 14. The waveform of a modulation signal.

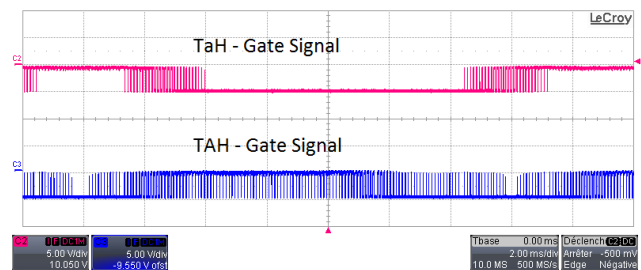


FIGURE 15. Real switching signal/gate pulses waveform of TaH and TAH.

Here, the two upper transistors T_{bH} gates are fed by the output of epwm-xA and similarly, the two lower transistors T_{bL} gates are fed by the output of epwm-xB.

Equations (31) and (32) outline values that are charged into the comparison record CMPA & CMPB.

$$CMPA = d_{1R} * TBPRD \tag{31}$$

$$CMPB = TBPRD \tag{32}$$

And again, within every entire switching period, a comparison process intervenes between TBCTR and CMPA / CMPB. A similar Equation (33) as in (29) points out the comparing occurrence:

$$TBCTR = CMPA$$

TABLE 2. Assigned opportune values to comparison registers.

Sector	T_{bH} pulse	T_{bL} pulse	CMPA	CMPB	CSFA	CSFB
1	forced low	modulated	$d_{1R} * TBPRD$	TBPRD	01	00
2	modulated	forced low	$d_{1R} * TBPRD$	TBPRD	00	10
3	forced high	forced low	-----	-----	10	10
4	modulated	forced low	0	$d_{1R} * TBPRD$	00	10
5	forced low	modulated	0	$d_{1R} * TBPRD$	01	00
6	forced low	forced high	-----	-----	01	01

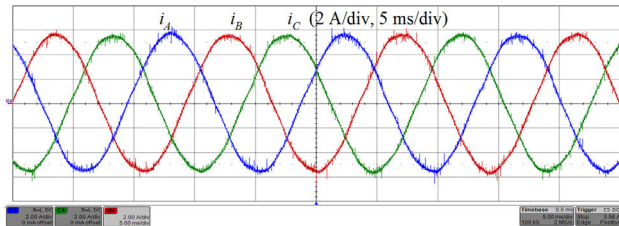


FIGURE 16. The inductive load current signals (i_{ANR} , i_{BNB} , i_{CNC}).

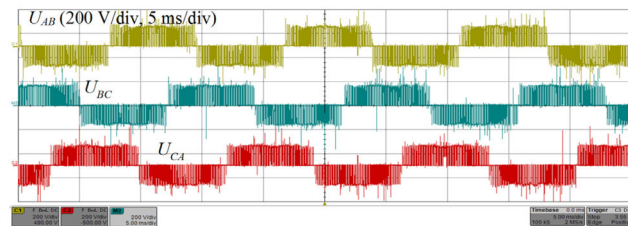


FIGURE 17. The line-line three-phase output-load voltage signals.

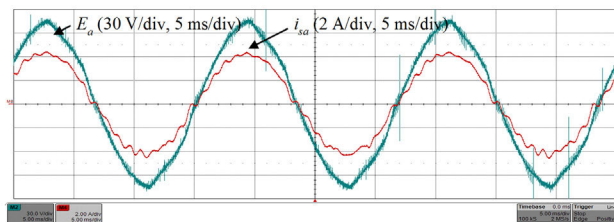


FIGURE 18. Line-neutral grid voltage (blue) & current (red).

$$TBCTR = CMPB \quad (33)$$

AQ-x runs down to the falling-edge delay blocking submodule and to the inverted gate of the (DB). Subsequently, the epwm-xB, which is the output signal that feeds the transistors' gates of T_{bL} , is shaped from the previously mentioned AQ-x. Fig. 12 section (d) explicitly shows that epwm-xB originates a pulse that has the right alignment and distinguished by a turn-on delay.

In contrast, and through the complete switching period, the signals supplying the upper transistors T_{bH} must stay in low-status.

Accordingly, CSFA bits are set to (01) as indicated in Equation (25) to acquire the above results.

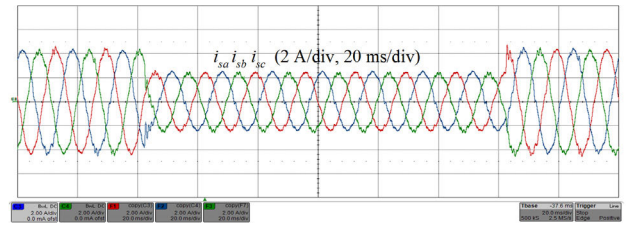


FIGURE 19. $f_{out} 70 \rightarrow 40$ qvoltage 0.86 \rightarrow 0.6 input currents.

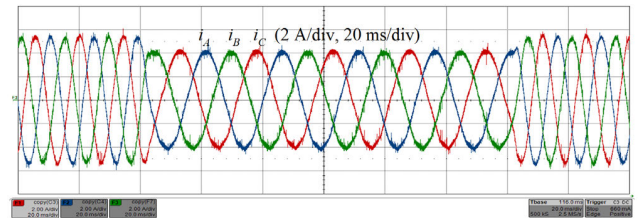


FIGURE 20. $f_{out} 70 \rightarrow 40$ qvoltage 0.86 \rightarrow 0.6 output currents.

TABLE 3. Time-consuming operations used in the hybrid and DSPWM modulation algorithms.

Time-Consuming Blocks	Hybrid		SVPWM	
	Rectifier	Inverter	Rectifier	Inverter
Arctan Function	0	0	0	1
Lookup Tables	CMPA/B: 6# D(1x1) SFA/B: 6# D(1x1)	0	CMPA/B: 6# D(1x1) SFA/B: 6# D(1x1)	CMPA/B: 6# D(1x1)
Trigonometric Functions	2	3	2	3

TABLE 4. The computation time required to run the hybrid and SVPWM modulation algorithms.

	Hybrid	SVPWM
PLL block	10.60 μ s	10.60 μ s
Rectifier stage modulation	6.69 μ s	6.69 μ s
Inverter stage modulation	3.26 μ s	16.09 μ s
Total computation time	20.55 μ s	33.38 μ s

Taking into consideration that the reference input current vector in the complex space plane may be located in any of the sectors numbered from 1 and up to 6, a comprehensive study is performed and results are briefly declared as in Table 2.

Table 2 shows the general waveforms of T_{bH} and T_{bL} pulses as well as the opportune values assigned to comparison registers (CMPA and CMPB) and the two couples of bits (CSFA and CSFB) for the six possible positions of the input current reference vector in the complex plane.

Demonstrating an example for the Table, suppose that the reference input current vector is located in sector 4, therefore, T_{bH} pulse is modulated, T_{bL} is forced low, $CMPA = 0$, $CMPB = d_{1R} * TBPRD$, $CSFA = 00$, and $CSFB = 10$.

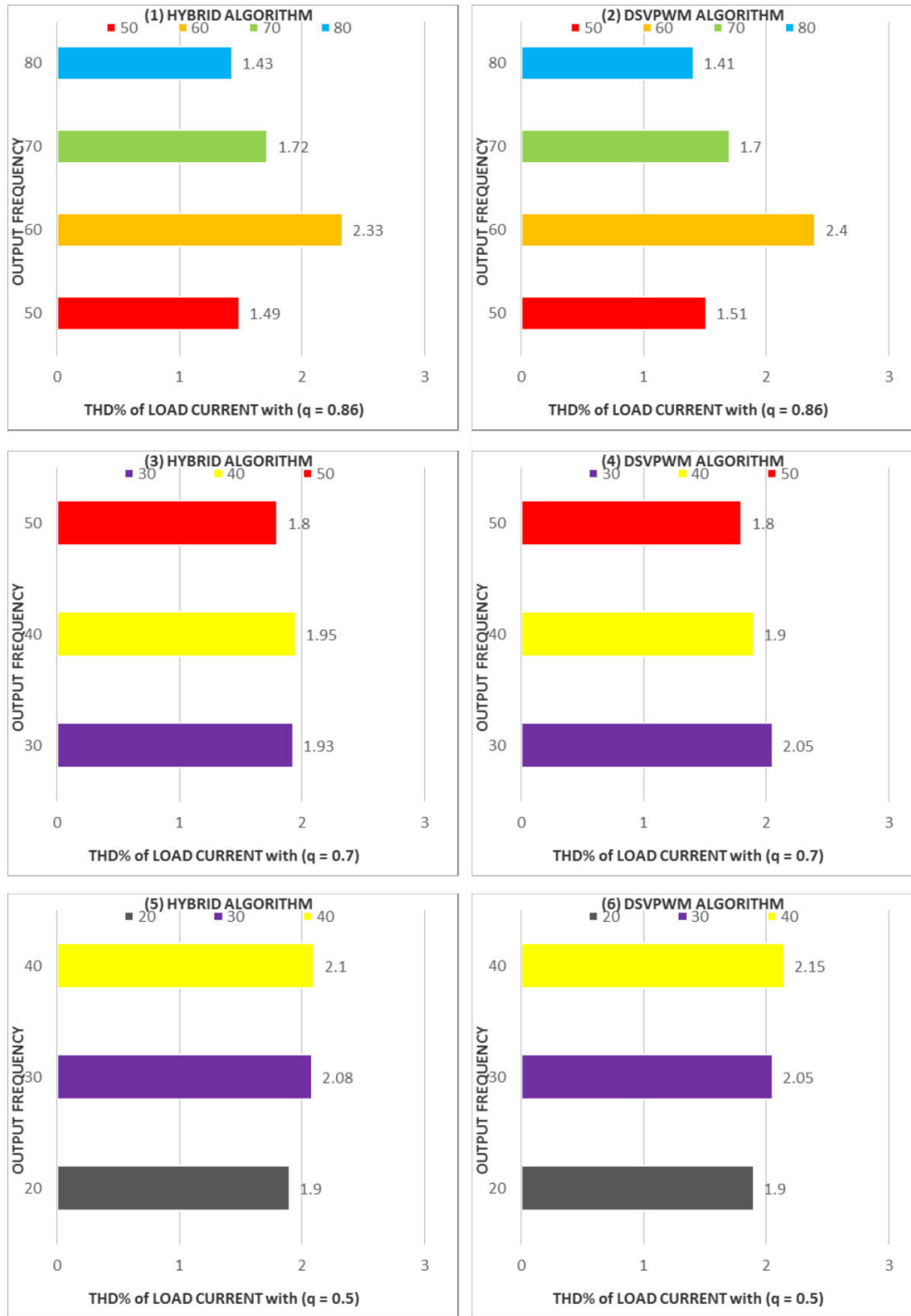


FIGURE 21. Comparison of total harmonic distortions of load currents.

Fig. 12 demonstrates the synthesis of gates pulses of T_{bH} and T_{bL} within an epwm module when the input current reference vector is located in sector 1 as follows:

- The instantaneous value of time base counter TBCTR.
- Counter compare submodule output events.
- Action Qualifier output signal AQ-x.
- PWM output signals epwm-xA and epwm-xB.

V. THE APPROACH VERIFIED THROUGH EXPERIMENTAL RESULTS

An experimental prototype of the Indirect Matrix Converter is developed to test the proposed modulation algorithm. A simplified block diagram of the converter and control algorithm is illustrated in Fig. 13. The converter is connected to the grid through an LC filter and supplies a three-phase star-connected

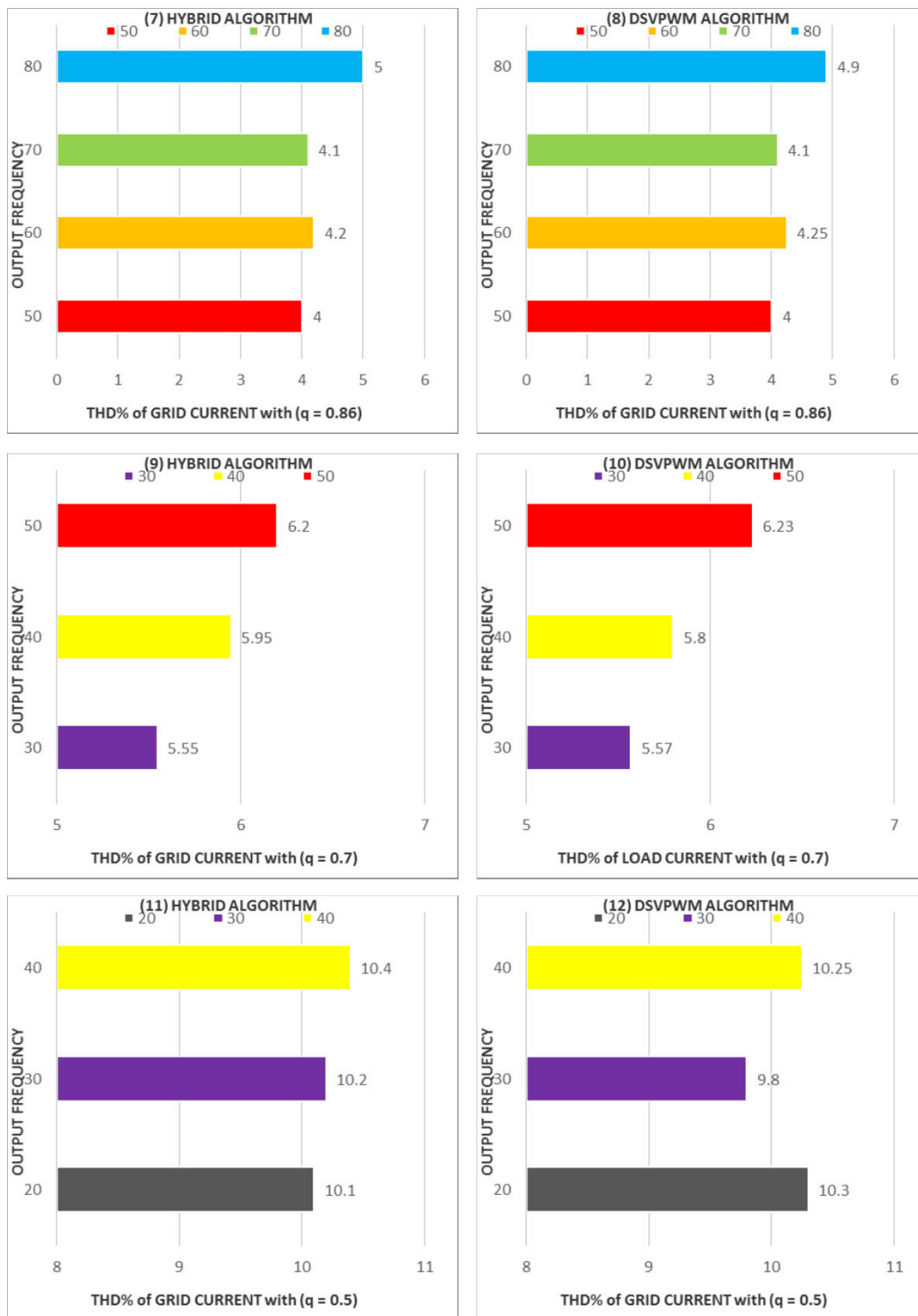


FIGURE 22. Comparison of total harmonic distortions of line currents.

RL-load. The modulation algorithm implemented on the DSP TMS320F28335 consists of three fundamental parts.

A PLL block continuously computes the instantaneous phase angle of grid voltages and therefore determines the position of the input current reference vector \bar{I}_m in the complex plane. The second block computes the duty ratios d_{1R}

and d_{2R} determines the opportune values of CMPA and CMPB registers of each epwm module as explained earlier in section IV-B.

The last block computes first the reference output voltages (U_{AN}, U_{BN}, U_{CN}), from the target references U_{α}^* and U_{β}^* which are usually generated by an outer loop. Then, it

computes the modulating signals U_A^* , U_B^* , and U_C^* according to (18) and the duty ratios d_A , d_B , and d_C as reported in (19). Finally, the opportune values of CMPA and CMPB registers of each epwm module are determined as explained above in section IV-A. To make compatibility with the data type format of epwm modules compare registers, all CMPA and CMPB values computed by the arithmetic unit are converted into 16-bit unsigned format.

The whole algorithm is first implemented using Simulink toolbox and the target support package “Texas Instruments C2000”. Then, the TI code generation tools for windows to generate a project file for code composer studio and download the real-time executable into the DSP memory. Finally, the build process automatically runs this executable file on the DSP. The sampling and switching periods are both set to $100\mu s$.

Fig. 14 displays the waveform of a modulation signal computed according to (18) where the voltage transfer ratio is set to:

$$\begin{aligned} f - input &= 60Hz \\ f - output &= 70Hz \\ q &= q_{max} = 0.86 \end{aligned} \quad (34)$$

This figure is obtained from a screen snapshot of Code Composer Software (CCS) running in real-time.

As can be seen, the modulating signal is inherently non-sinusoidal because of the injection of zero-sequence-term and the compensation of the dc-link voltage ripple.

On the other hand, it can be observed that the waveforms are quite within the bounds $(-1, 1)$ which means that full utilization of the virtual dc-link voltage is achieved in the linear region.

In addition, the real switching signal/gate pulses waveform of TaH (upper switch in the first leg of the Rectifier) and of TAH (upper switch in the first leg of the Inverter) are illustrated in the Fig. 15.

All signals associated with the input electrical parameters are to be displayed below respecting the previous conjecture. Fig. 16 shows the inductive load current signals (i_{AN} , i_{BN} , i_{CN}). The output load current waveforms are promptly cognate by the virtual DC-Link voltage character & nature. Fig. 16 displays sinusoidal and balanced signals highlighting that ripples suspended in the DC bus are redressed and distortions resulting from lower frequency signals are the slightest. As a conclusion, and as clear through depicted figures, the signals requested for modulation act upon the linear region in an effective manner.

Fig. 17 shows the line-line three-phase output load voltage signals. Fig. 18 represents the line-neutral input voltage and input current that is blindly sinusoidal and in phase. The figure explains the unity displacement factor characteristic that is attained through the modulation.

Now fix $f_{1out} = 70Hz$ and $q_{1voltage} = 0.86$ and consider it the 1st operational status; and let $f_{2out} = 40Hz$ and $q_{2voltage} = 0.6$ and consider it the 2nd sudden changeable

operational status. Fig. 19 shows the input grid current signal under a sudden changeable condition affecting output frequency and voltage transfer ratio. Fig. 20 shows the inductive load current signal under the same conditional status.

Fig. 19 & 20 together demonstrate that signals preserve their sinusoidal nature during the steady-state phase. In addition, and even though input signals barely oscillate during the transient state, the input filters are well operating to prevent harmful overshooting.

VI. DSVPWM VERSUS HYBRID MODULATION: COMPARATIVE ANALYSIS

A comparative study between the conventional DSVPWM method and the proposed one is presented [39]–[41].

The latter is based on the computing time that is required to run the algorithm as well as the THDs of line and load currents. The conventional DSVPWM algorithm is therefore implemented on the same DSP running at 150 MHz where the digital scalar modulation scheme included in the third block of Fig. 13 was replaced by the conventional DSVPWM scheme. Table 3 shows the number of time-consuming operations used in both algorithms and the obtained results are shown in Table 4. The times needed by the blocks namely “conversion to 16-bit unsigned format” shown in Fig. 13 are not included in the obtained results. The results show that the proposed hybrid method allows reducing near 38% of the total computation time. This is due to the simplified hybrid control algorithm of the inverter stage that needs only $3.26\mu s$ (see Table 4) while the conventional SVPWM algorithm needs $16.09\mu s$. The large computational time of the conventional SVPWM algorithm is mainly due to two key procedures: The lookup tables that determine the opportune switching sequence for each transistor according to the position of the reference vector in the complex plane. The time needed for this operation is near $3.35\mu s$. The “arctan” trigonometric function and lookup table needed to determine the phase angle of the output voltage space vector and its operating sector in the complex plane. The time needed for this procedure is near $8.74\mu s$. These two time-consuming procedures do not exist in the scalar modulation algorithm, which justifies the substantial reduction of the time interval needed for the control of the inverter stage.

Fig. 21 encompasses 6 charts. Charts (1), (3), and (5) show the total harmonic distortion THD% of the load output current under the previously proposed Hybrid modulation. The output frequency alternates between 20, 30, 40, 50, 60, 70, and 80 Hz. Moreover, the voltage ratio varies respectively from 0.86, 0.7, and 0.5. Under Similar conditions, charts (2), (4), and (6) show the THD% of the load currents under traditional Double Space vector modulation.

Fig. 22 encompasses 6 charts as well. Charts (7), (9), and (11) show the total harmonic distortion THD% of the source input current under Hybrid modulation. The output frequency as well as alternates between previously listed values. The voltage ratio also changes between the above values. Charts (8), (10), and (12) show THD% of the source

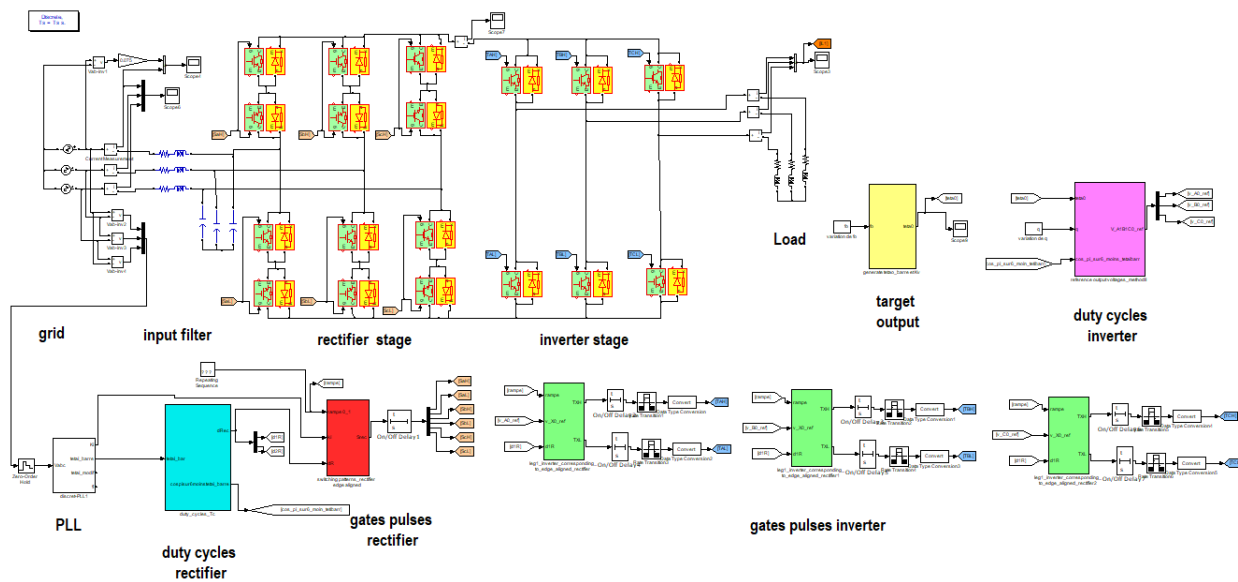


FIGURE 23. Simulink model.

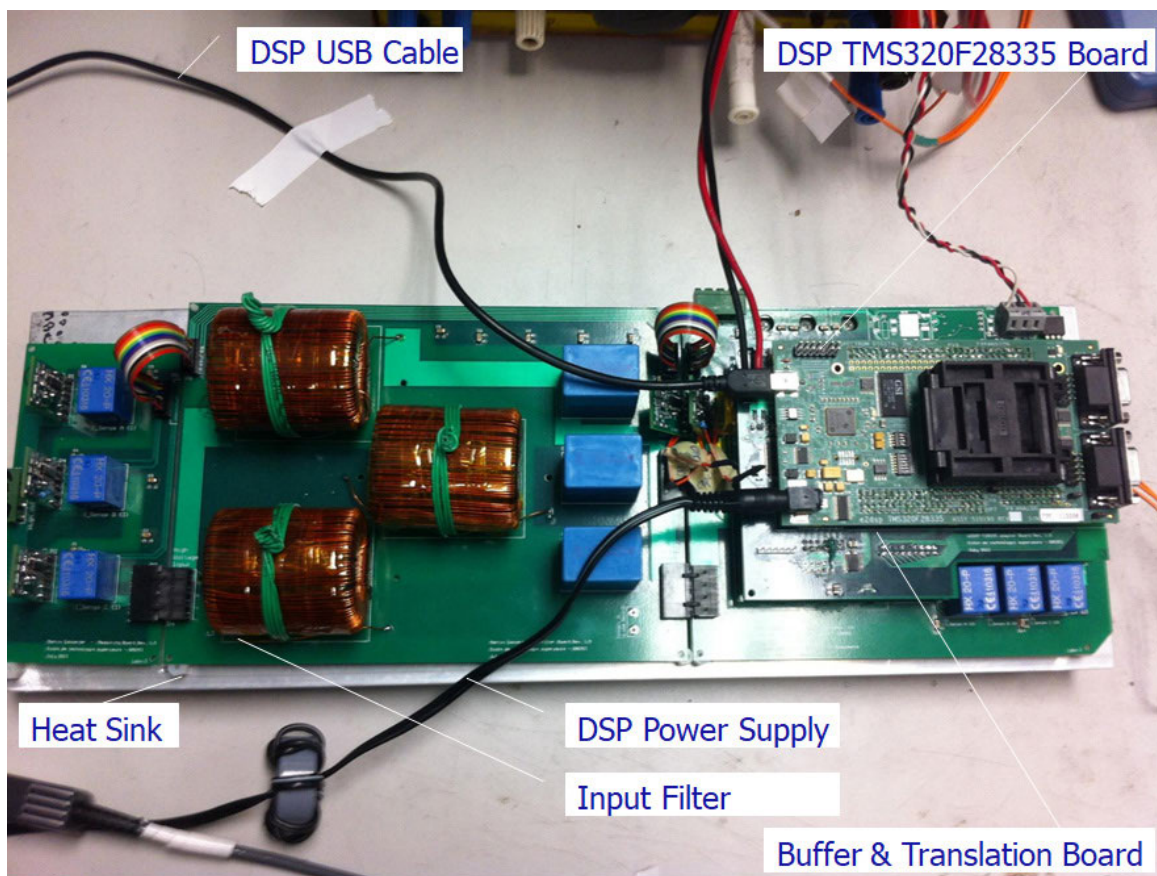


FIGURE 24. Experimental prototype of the indirect matrix converter 1/2.

currents under DSVPWM. Section VI. displays a comparative THD evaluation of line and load currents as a function of the voltage transfer ratio q and the output frequency f_o and as can be observed, both modulation algorithms provide

quite similar performance. Therefore, it can be concluded that the proposed hybrid modulation algorithm provides the same performance as the SVPWM while reducing the software design complexity and the computation time. Fig. 23 shows

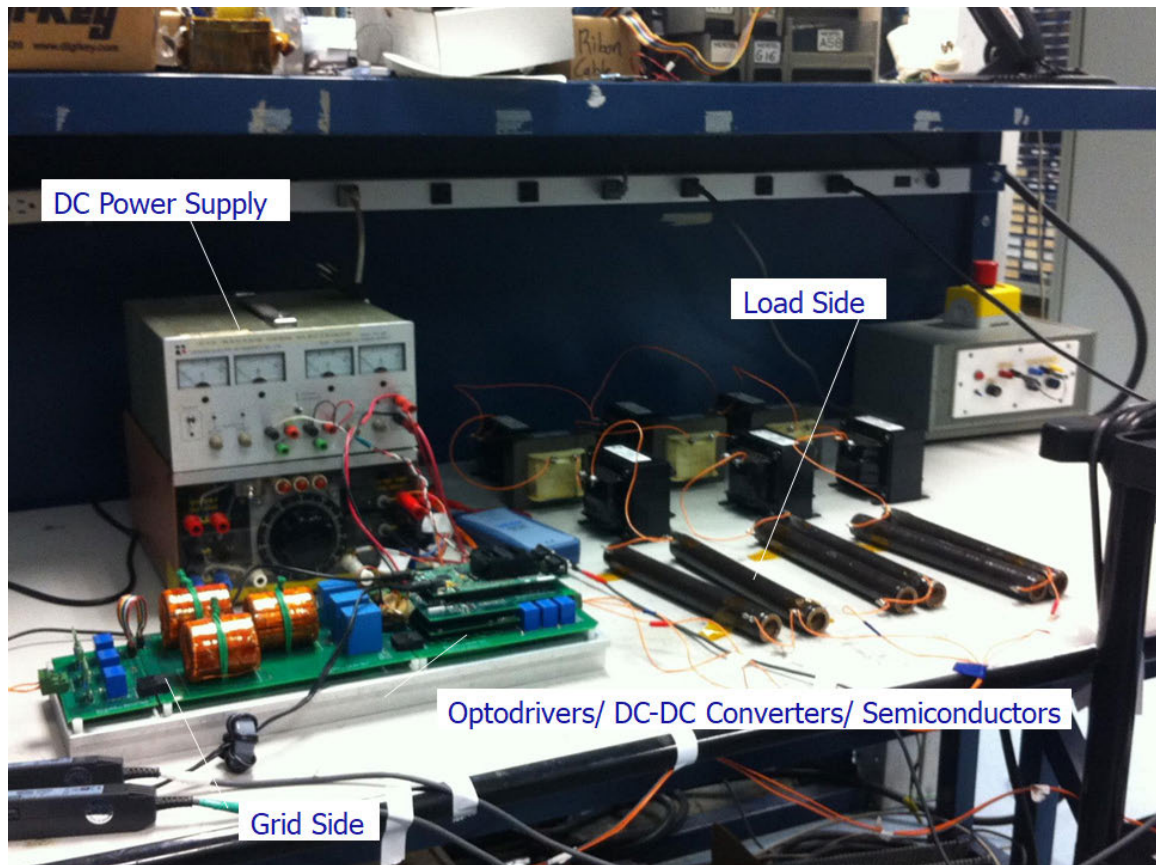


FIGURE 25. Experimental prototype of the indirect matrix converter 2/2.

a snapshot of the Simulink Model. Fig. 24 & 25 reflect the experimental prototype setup of the indirect matrix converter.

VII. CONCLUSION

The main objective of this research work is to propose cheaper and simple software and hardware solution for real-time implementation of an indirect matrix converter's controller without affecting its performance. From the point of view software, a simplified modulation algorithm that is much less complex for implementation on a digital processor and needs less computational time than the SVPWM algorithm is proposed. The main drawback of the SVPWM technique is the very important computational effort to implement it in real-time. This is because it needs time-consuming operations such as the use of the arctan function to localize the position of the reference vector in the complex plane and large lookup tables to determine the opportune switching vectors. From the point of view hardware, only a single DSP board is used to implement the overall control removing thus the additional FPGA/CPLD chip usually needed in the most of former implementations.

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AMIRA AMMAR (Member, IEEE) was born in Lugano, Switzerland, in 1991. She received the Diploma degree in electrical and electronics engineering from Lebanese University (LU), Hadath, Lebanon, in 2014, the M.S. degree in industrial control from the University of Technology of Compiègne (UTC), Compiègne, France, in 2014, and the Ph.D. degree in electrical engineering from Saint Joseph University (USJ-ESIB), Lebanon, in partnership with the Doctoral School of Science

and Technology (EDST-LU), Hadath.

In 2016, she visited the Ecole de Technologie Supérieure (ETS), Montréal, Canada, to pursue her research internship. She has authored 13 technical papers published in the international IEEE conferences. Her research interests include the fields of power electronics and power converters, and specifically matrix converters along with their control and applications.

Dr. Ammar was a recipient of the Best Paper Award from the IEEE ICIT 2017, held in Toronto, Canada, and a recipient of the IES Student Paper Travel Assistance Award from ICIT 2018, held in Lyon, France. Her awards and honors include the Lebanon Most Active Women in Engineering Member Award, the Lebanese Center for Scientific Research CNRS Doctoral Scholarship, and the Research Council of Saint Joseph University Doctoral Scholarship. She is the Vice-Chair of the IEEE Women in Engineering Lebanon Section (WIE), and she was the industry ambassador of the affinity group in Lebanon.



HADI Y. KANAAN (Senior Member, IEEE) received the Diploma degree in electromechanical engineering from Saint Joseph University, Beirut, in 1991, the Ph.D. degree in electrical engineering from the Ecole de Technologie Supérieure (ETS), Montréal, Canada, in 2002, and the Habilitation à Diriger des Recherches (HDR) from the Université de Cergy-Pontoise, Paris, France, in 2009.

He is currently a Full-Professor and the Head of the Electrical and Mechanical Department, Ecole Supérieure d'Ingénieurs de Beyrouth (ESIB), Saint Joseph University, Beirut, where he joined, in 2001. He has been a Visiting Researcher with ETS, since 2004, and an Associate Member of the Canada Research Chair of energy conversion and power electronics, since 2001. His research interests concern the modeling and control of switch-mode converters, modern rectifiers, power factor correction, active power filters, and the grid-connectivity of renewable energy systems. He has authored one book, two book chapters, and more than 200 technical papers, which are published in international journals and conferences, and holds one patent.

Dr. Kanaan is also the Vice-Chair of the IEEE Lebanon Section and an EXCOM Member of the IE/PE/CAS/PEL Joint Chapter in Lebanon. He has served as an Associate Editor for the IEEE TRANSACTIONS INDUSTRIAL ELECTRONICS, and he is currently a member of the IEEE Power Electronics Society (PELS), the Industrial Electronics Society (IES), and the Industry Applications Society (IAS).



NAZIH MOUBAYED (Senior Member, IEEE) received the Dipl.Eng. degree in electricity and electronics from Lebanese University (UL), in 1995, the master's degree in electrical engineering from the Polytechnic National Institute of Toulouse (INPT), in 1996, and the Ph.D. degree from the Polytechnic National Institute of Lorraine (INPL), 1999, and HDR from UL, in 2011.

In 1999, he joined the Faculty of Engineering, UL, as an Associate Professor, and then he became a Professor, in 2014. He is associated with other engineering societies. He organized and participated in more than 20 international conferences. He is a Reviewer of different international journals and conferences, and he has participated in international research projects. He has authored more than 200 papers published in scientific journals, conferences, and books. He had supervised more than 35 Eng., 10 M.Sc., and 8 Ph.D. degree students. His current research interests include the areas of renewable energy, power electronics, and the diagnosis of the converter-machine set and energy management of power systems.



MAHMOUD HAMOUDA (Member, IEEE) received the B.S. degree in aggregation, M.S. degree, and Ph.D. degrees from ENSET and the École Supérieure des Sciences et Techniques, University of Tunis, Tunis, Tunisia, in 1995, 1996, 2004, and 2010, respectively, all in electrical engineering, and the HDR degree in electrical engineering from the University of Sousse, Sousse, Tunisia, in 2017.

He is currently an Associate Professor of electrical engineering with the ISSAT, University of Sousse. He is affiliated with the Canada Research Chair of Electric Energy Conversion and Power Electronics, École de Technologie Supérieure, Montréal, QC, Canada. He is also a member of the Research Laboratory LATIS, National Engineering School of Sousse, and the University of Sousse. His main research interests include renewable energy conversion systems, digital signal processors, and field-programmable gate arrays for embedded real-time control, grid-connected converters, and fault diagnosis of power converters.



KAMAL AL-HADDAD (Life Fellow, IEEE) received the B.Sc.A. and M.Sc.A. degrees in electrical engineering from the University of Québec 'a Trois-Rivières, Trois-Rivières, QC, Canada, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from the Institut National Polytechnique, Toulouse, France, in 1988.

Since June 1990, he has been a Professor with the École de Technologie Supérieure, Université du Québec, Montréal, QC, Canada, where he has been the holder of the Senior Canada Research Chair in Electric Energy Conversion and Power Electronics, since 2002. He has supervised more than 150 Ph.D. and M.Sc.A. degree students and coauthored more than 600 articles and 2 books. His research interests include high-efficiency power electronic converters, active and hybrid filters, modular multilevel converters, multilevel converters, and active rectifiers, including modeling, control, and development of industrial prototypes.

Dr. Al-Haddad was the President of the IEEE Industrial Electronics Society, from 2016 to 2017, and a Fellow of the Canadian Academy of Engineering.

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