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A Fully Static True-Single-Phase-Clocked Dual-Edge-Triggered Flip-Flop for Near-Threshold Voltage Operation in IoT Applications

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ABSTRACT A Dual-Edge-Triggered (DET) flip-flop (FF) that can reliably operate at low voltage is proposed in this paper. Unlike the conventional Single-Edge-Triggered (SET) flip-flops, DET-FFs can improve energy efficiency by latching input data at both clock edges. When combined with aggressive voltage scaling, significant efficiency improvement is expected. However, prior DET-FF designs were susceptible to Process, Voltage and Temperature (PVT) variations, limiting their operation at low voltage regimes. A fully static true-single-phase-clocked DET-FF is proposed to achieve reliable operation at voltages as low as a near-threshold regime. Instead of the two-phase or pulsed clocking scheme in conventional DET-FFs, a True-Single-Phase-Clocking (TSPC) scheme is adopted to overcome clock overlap issues and enable low-power operation. Fully static implementation also enables robust operation in a low voltage regime. The proposed DET-FF is designed in 28nm CMOS technology, and a comprehensive analysis including post-layout Monte Carlo simulation for wide PVT ranges is performed to validate the design approaches. Extensive analysis and comparison with prior-art DET-FFs confirmed that the proposed DET-FF can operate at the lowest voltage of 0.28 V for a temperature range of -40°C to 120°C while maintaining nearly-best energy efficiency and power-delay-product.

INDEX TERMS Flip-flop, dual-edge-triggered (DET), single phase, low power, near-threshold voltage.

I. INTRODUCTION

Flip-flops are one of the most essential circuit elements for modern digital circuit design since they provide local data storage and synchronize the data flow. Since such synchronization should be done throughout the entire clock domain, a large number of flip-flops are utilized in a typical processor, often hundreds of thousands [1]. Because of their sheer number, flip-flops occupy a large portion of the overall circuit architecture in terms of both power and physical area. Therefore, reducing the power consumption of flip-flops has great impact on system-level energy efficiency, especially for energy-constrained IoT applications. Minimizing power consumption in IoT Integrated Circuits (ICs) is very important for maximizing battery life [2]. However, flip-flops, which are toggled by the clock every cycle, consume a large portion

of the dynamic power in a synchronous system. For this reason, many research works have been performed to develop flip-flops with lower power consumption and better energy efficiency to date [3]–[27].

The most popular approach for implementing a flip-flop is using either the rising or falling edge of the clock as the triggering source for the latching operation. This type of flip-flop is called a Single-Edge-Triggered flip-flop (SET-FF), and they are widely used for their simple implementation and ease of timing characterization [3]–[7]. In contrast, Dual-Edge-Triggered flip-flops (DET-FFs) take advantage of the unused clock edge in SET-FFs, i.e. the latching operation is triggered at both the rising and falling clock edges. Utilizing both clock edges potentially achieves better energy efficiency because it allows twice the data throughput compared to SET-FFs with the same clock frequency. Therefore, DET-FFs have been proposed as an alternative sequential circuit element for reducing power consumption compared to SET-FFs [8]. To

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implement dual edge sensitivity, various topologies, including complementary latch pair and pulse-triggered latch, have been studied [9]–[27], as will be discussed in Section II.

Meanwhile, a simple but widely used design technique for maximizing energy efficiency in an electronic system is voltage scaling [28]–[30]. By scaling down the supply voltage, quadratic reduction in dynamic energy consumption can be achieved. Therefore, voltage scaling is widely adopted among energy-constrained IoT applications [31], [32] and battery-operated miniature sensors [33]–[35]. To apply such voltage scaling to flip-flops, aggressive voltage scalability is of critical concern. However, due to increased sensitivity to the process variation in low voltage regimes, guaranteeing robust flip-flop operation at low supply voltage is a non-trivial challenge, especially with the advanced technologies where process variation is becoming increasingly prominent.

In this paper, a DET-FF suitable for aggressive voltage scaling down to a near-threshold voltage regime is presented. By adopting a single-phase clocking scheme and removing all internal dynamic nodes, robust operation at voltage as low as 0.28 V is verified for temperatures ranging from -40°C to 120°C with Monte Carlo simulations.

The rest of this paper is organized as follows: Section II analyzes the prior-art DET-FFs, categorized as three different types, and discusses their strengths and weaknesses. Section III presents the proposed fully static true-single-phase-clocked DET-FF designed for robust operation at low voltage regimes. Section IV shows the simulation results and comparisons with other DET-FFs, and Section V concludes the paper.

II. REVIEW OF THE PRIOR-ART DUAL-EDGE-TRIGGERED FLIP-FLOPS

The prior-art DET-FFs can be categorized into three types: Latch-Multiplexer, Pulsed-Latch, and C-element. Through the analysis of these 3 types of DET-FF topologies, the characteristics and limitations of the conventional DET-FF designs are highlighted. A new DET-FF design that overcomes these limitations will be introduced in the following section.

A. LATCH-MULTIPLEXER-TYPE DET-FF

Fig. 1 shows two Latch-Multiplexer (MUX) Dual-Edge-Triggered flip-flops (LM-DET FFs). In this type of DET-FF, a pair of latches is utilized for latching data at the positive and negative clock edges, and a multiplexer selects either of the latches to drive the output.

Fig. 1(a) shows one example of an LM-DET FF, a Static DET FF (SDET FF) presented in [20]. In this FF, each latch consists of back-to-back connected inverters and a transmission gate. The original structure of the SDET FF in [20] utilizes single nmos (or pmos) as the pass gates, which makes it vulnerable to process and voltage variations. In this paper, for comparison with other DET-FFs with improved reliability, the pass gates are replaced with transmission gates for analysis and simulations. Two latches

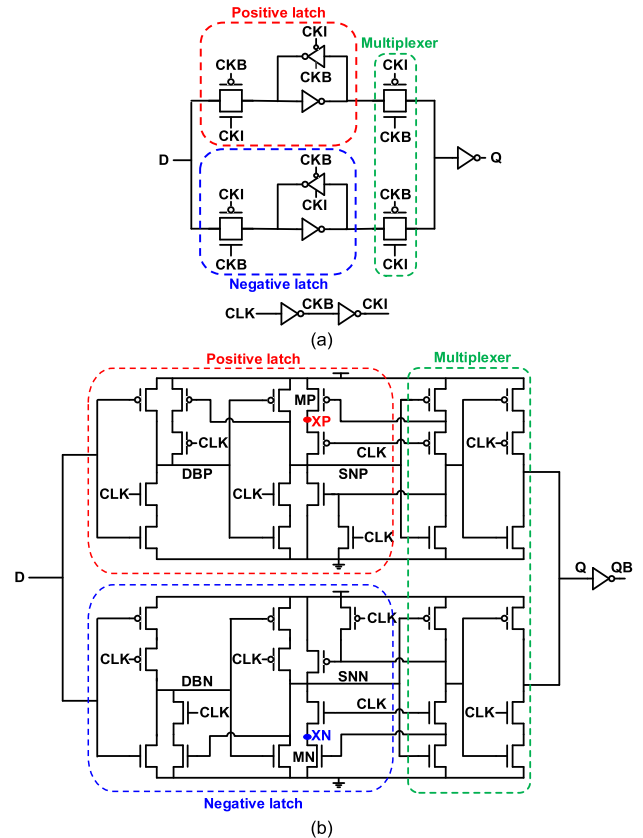


FIGURE 1. Latch-MUX-type DET-FFs: (a) Static DET-FF (SDET FF) [20] (b) True-single-phase-clock SDET FF (TSPC-SDET FF) [27].

and a multiplexer are controlled by complementary internal clock signals (CKB, CKI), which are generated from the CLK signal through 2-stage inverters.

When $\text{CLK} = '1'$, the input transmission gate of the positive latch is turned on, and the input data is stored in the positive latch. On the other side, the input transmission gate of the negative latch is turned off, keeping the value stored in the last cycle in the negative latch. Meanwhile, the multiplexer is controlled to forward the value stored in the negative latch to output as long as the CLK stays high. At the falling transition of the CLK ($'1' \rightarrow '0'$), the data in the positive latch is forwarded to the output node Q by the multiplexer. At the same time, the input transmission gate of the positive latch is turned off so that the current input data can be safely latched, fulfilling the latching operation at the falling edge of the CLK. The negative latch performs a complementary operation, storing the following inputs for the next latching operation at the rising transition of the CLK.

In this SDET FF, two-phase clock signals are required to control the tri-state inverters and prevent contention. The two latches are required to operate in a complementary manner. However, CKB and CKI can overlap for a short time since they are generated with 2-stage inverters. Such a problem can worsen in low voltage regimes where delay variation is exacerbated. As demonstrated in [27], the two transmission gates that form a multiplexer can be turned on at the same

time during clock overlap, making it possible for one latch's data to upset the other latch's data.

A True-Single-Phase-Clock static DET flip-flop (TSPC-SDET FF) [27], shown in Fig. 1(b), is proposed to address this issue. The positive and negative latches operate in a complementary manner just like in [20]. But unlike in the SDET FF, a single-phase clocking scheme similar to C2MOS [36] is adopted to fundamentally eliminate the two-phase clock overlap issue at the cost of an increased number of transistors.

However, weak pull-up and pull-down in the TSPC-SDET FF make its voltage scalability limited and prone to variation. For example, when $CLK = '0'$ and $SNP = '1'$ in the positive latch, the gate of transistor MP is not fully pulled down to ground due to a PMOS on the pull-down path. Therefore, the node XP is weakly pulled up by MP. Similarly, when $CLK = '1'$ and $SNN = '0'$ in the negative latch, the node XN is weakly pulled down. Therefore, although it claims to be a 'static' DET FF, it is not fully static (i.e., it does not swing across the full voltage range), and, because of this problem, it is not suitable for aggressive voltage scaling and near-threshold voltage operation.

B. PULSED-LATCH-TYPE DET-FF

As alternatives to the Latch-Multiplexer-type DET-FF, many pulse-triggered DET FFs have been proposed [9]–[18]. In this topology, a pulse generator generates a clock-synchronized pulse at both the rising and falling clock edges. These clock-synchronized pulses are used as triggers for the latching operation of the pulsed latches.

Pulsed-Latch-type DET FFs (PL-DET FFs) consist of a pulse generator and a pulsed latch and can be classified into two types – implicit pulse [13]–[18] and explicit pulse [9]–[12]. Fig. 2 shows a PL-DET FF using an implicit pulse (Fig. 2(a)) and one using an explicit pulse (Fig. 2(b)) [11], [17]. The Dual-edge Conditional Pre-charge flip-flop (DECP FF) [17] shown in Fig. 2(a) utilizes control signals generated by the input CLK. The delayed version of CLK (CK4), the inverted version of CLK (CKD), and the CLK signal generate a short transparency window after both the rising and falling edge of the CLK. During these windows, the input data is forwarded to the output node Q in the pulsed latch. This implicit pulse-type DET-FF requires a robust timing window for reliable operation, so the careful sizing of transistors is an important design issue.

An example of a pulsed-latch-type DET-FF with explicit pulse is the Sense-Amplifier DET flip-flop (SA-DET FF) [11] shown in Fig. 2(b). This DET-FF utilizes pulses generated by complementary two-phase clock signals, namely CLK1 and CLK2. When these signals become equal for a very short period of time due to their generation circuit structure (series-connected inverters), a pulse generator circuit generates a short pulse signal, which is used to trigger the latching operation in a pulsed latch. Since the pulses are generated whenever CLK1 and CLK2 are both '1' or both '0', the data is latched at both CLK edges.

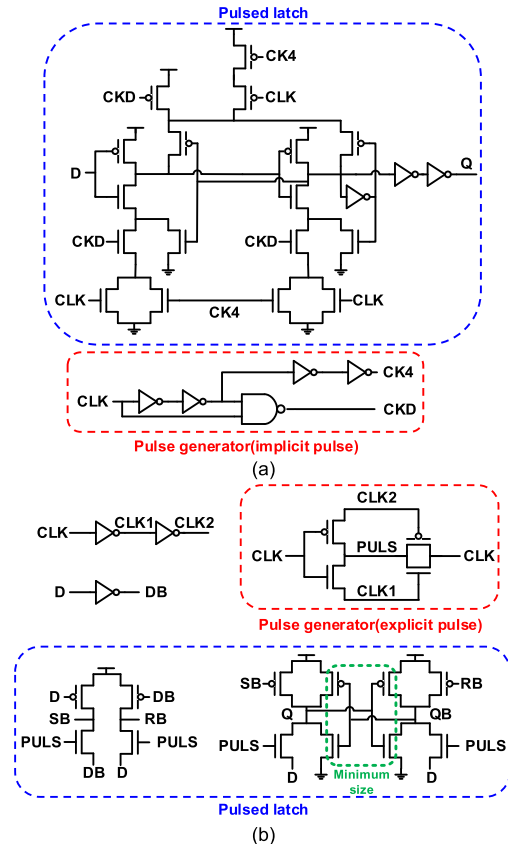


FIGURE 2. Pulsed-Latch-type DET-FF. (a) Dual-Edge Conditional Pre-charge (DECP) FF [17] (b) Sense-Amplifier (SA) DET FF [11].

Pulsed-latch-type DET-FFs require pulse-generating circuits. Since the transparency window of pulsed latches is determined by the pulse length, timing is very important. However, since typical pulse-generating circuits rely on transistor delay to control the pulse length, the pulse characteristics can be easily affected by Process, Voltage and Temperature (PVT) variations. Therefore, careful pulse-generation circuit design is required to make it robust against PVT variations. Such careful design often requires large margins for variation tolerance, resulting in large power and area overhead.

C. C-ELEMENT-TYPE DET-FF

Another type of recently designed DET-FF includes a circuit element called a 'C-element' [23], [24]. As illustrated in Fig. 3(a), when the two inputs of a C-element are the same, the output is updated to the input value, whereas the earlier output value is retained when the two input values differ from each other. Thanks to the ability of C-element-type DET-FFs to latch new data or retain data depending on the input conditions, many different topologies have been proposed to implement them.

Fig. 3(b), (c) show examples of DET-FF designs using C-elements. The New low-power C-element Dual Data Rate flip-flop (NCDDR FF) [23] shown in Fig. 3(b) includes two latches that store the input values in opposite phases. The latched input is stored in nodes A and B, which are used as

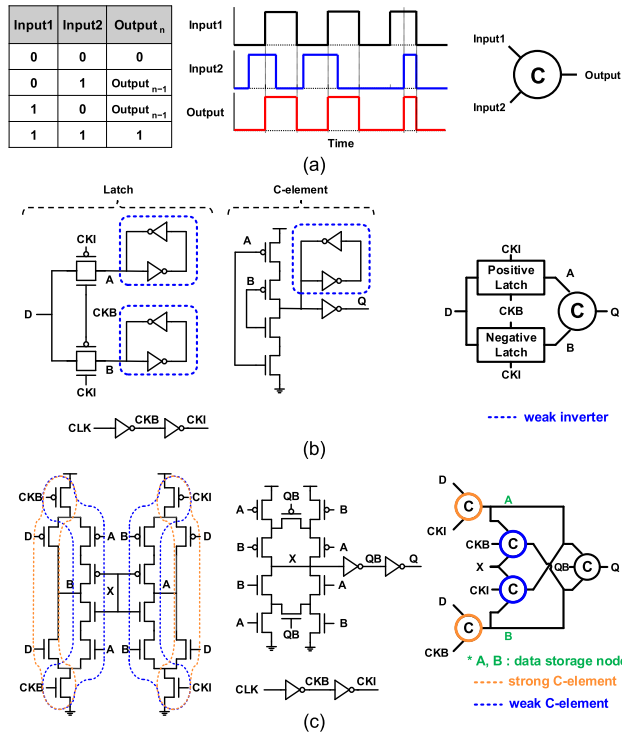


FIGURE 3. C-element-type DET-FF. (a) Truth table and operation waveforms of C-element (b) NCDDR FF [23] (c) FN_C-DET FF [24].

input for the C-element. In this manner, the C-element can latch input data at both clock edges. However, in this DET-FF design, the latched data is held by back-to-back connected weak inverters, which incur contention when new data is written to the storage node by overpowering the feedback inverter. For reliable operation, the feedback inverters and overriding transistors should be carefully sized. In addition, two input transmission gates controlled by the two-phase clock can potentially cause a clock overlap issue, as observed for SDET FFs.

The Floating Node C-element DET flip-flop (FN_C-DET FF) [24] shown in Fig. 3(c) uses five C-elements in total: two 2-input C-elements at the input, two 3-input C-elements in the middle, and one output C-element. At the input C-elements, D, CKB and CKI signals determine the logical values of the internal nodes A and B. These A and B signals control the output C-element, which determines the value of Q. The node X is used as a feedback signal at the inner C-element pair. By using five C-elements, an FN_C-DET FF forwards the input data at both clock edges. However, when the value of A or B switches, contention can occur at the data storage node of the C-element. To reduce contention, the two inner C-elements should be designed to be weaker than the two C-elements at the input so that the internal storage data can be flipped correctly.

Although C-element-type DET-FFs offer some advantages, the usage of back-to-back inverters for retaining data [23], [24] creates inevitable contention. Therefore, C-element-based DET-FFs require careful design to improve reliability and apply aggressive voltage scaling.

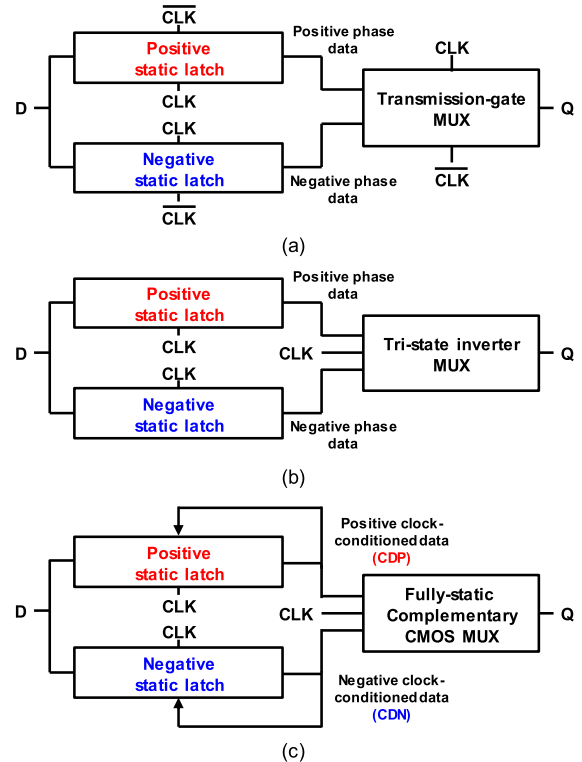


FIGURE 4. Simplified illustration of operation principle of Latch-MUX-type DET-FFs. (a) SDET FF [20] (b) TSPC-SDET FF [27] (c) proposed FS-TSPC-DET-FF.

III. PROPOSED FULLY STATIC TRUE-SINGE-PHASE-CLOCKED DUAL-EDGE-TRIGGERED FLIP-FLOP

For energy-efficient digital circuit operation with aggressive voltage scaling in IoT applications, DET-FFs that are robust against PVT variations are required. Among the three types of DET-FFs discussed in Section II, Pulsed-latch-type DET-FFs require precisely timed short pulses, which are prone to PVT variation. In addition, C-element-type DET-FFs suffer from weak feedback, which inevitably creates contention during the latching operation. As a result, these two types of DET-FFs have limited voltage scalability and are not suitable for low-voltage operation. Therefore, a new DET-FF based on Latch-MUX topology is proposed to allow aggressive voltage scaling by avoiding contention during the latching operation. The proposed DET-FF is 1) fully static without weak pull-up/down, 2) true single-phase clocked, and 3) contention free. Therefore, the proposed DET-FF is robust against PVT variations and does not require transistor sizing to overcome contention, which allows compact sizing of the FF, enabling small area and power overhead. These advantages enable reliable operation with aggressive voltage scaling across a wide temperature range.

Fig. 4 shows the block-level diagrams of the conventional Latch-MUX-type DET-FFs and the proposed Fully Static True-Single-Phase-Clock DET flip-flop (FS-TSPC-DET FF). In the SDET FF [20], shown in Fig. 4(a), a pair of complementary phase clocks is applied to complementary latches to enable either of the latches at a given point in time.

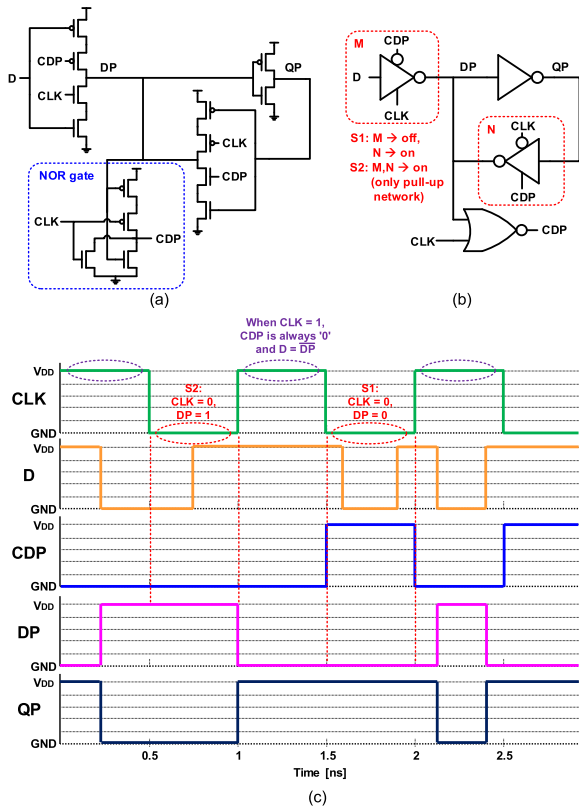


FIGURE 5. Positive latch in proposed DET-FF. (a) Transistor-level schematic (b) Gate-level schematic (c) Waveforms of positive latch.

At the same time, a multiplexer (MUX), which is a pair of transmission gates controlled by a two-phase clock, forwards the latched data in either of the latches to output Q. The TSPC-SDET FF [27] in Fig. 4(b) utilizes a single-phase clock so that it can avoid a clock-overlap issue and operate reliably with low supply voltage. However, the TSPC-SDET FF still has limitations in near-threshold operations due to the weak pull-up/pull-down, as stated earlier.

For better voltage scalability with robust low-voltage operation, the FS-TSPC-DET FF is proposed, whose concept is shown in Fig. 4(c). Similar to a TSPC-SDET FF, the proposed DET-FF utilizes only a single-phase clock. But compared to TSPC-SDET FF, the proposed DET-FF utilizes a complementary CMOS logic gate as a multiplexer, preventing potential issues with transmission gate MUX or tri-state inverter MUX. To make the CMOS logic gate function as a MUX, two clock-conditioned data signals – CDP and CDN – are generated with clock and data input and used as inputs for the MUX. These signals simultaneously 1) forward latched values to output and 2) control the behavior of each latch without weak pull-up or pull-down. The details of the proposed latch are described in the following sub-sections.

A. POSITIVE AND NEGATIVE LATCH

Fig. 5(a) and (b) show schematics of the positive latch in the proposed DET-FF. CDP is a positive clock-conditioned data signal generated by NOR operation of the CLK and latched data (DP). When CLK = ‘1’, CDP is always 0 regardless of the DP value. In this condition, the input clocked inverter

(M in Fig. 5(b)) is activated, while the feedback clocked inverter is deactivated, making the positive latch transparent (QP = DP = D). In contrast, when CLK = ‘0’, the NOR gate acts as an inverter (CDP = DP). In this case, two scenarios (S1, S2) are possible depending on the DP value: S1) If DP = ‘0’, hence CDP = ‘1’, the back-to-back connected inverters are activated, and the DP and QP nodes remain static state; or S2) If DP = ‘1’, hence CDP = ‘0’, the feedback-clocked inverter (N in Fig. 5(b))’s pull-down path is off since nmos controlled by CDP is turned off. However, the feedback-clocked inverter’s pull-up network is on since QP = CLK = ‘0’, allowing stable DP data retention with static DP and QP nodes. As a result, every node in this positive latch is always static, which is desired for stable operation at low voltage.

Fig. 5(c) shows the simulation waveform for the positive latch. It can be clearly seen that the latch is transparent while CLK = ‘1’. The negative latch in the proposed DET-FF is complementary to the presented positive latch – it utilizes the NAND gate instead of the NOR gate as a negative clock-conditioned data signal generator and becomes transparent while CLK = ‘0’. These two static latches are symmetric elements required for complementary operation.

B. FULLY STATIC COMPLEMENTARY CMOS MULTIPLEXER

Fig. 6(a) shows an LM DET-FF topology using the positive and negative latches described earlier, whose outputs are combined with the transmission-gate-based multiplexer. As with the prior SDET FF [20], either of the latched data at the QP or QN node is transferred to the output Q through the MUX to function as a DET-FF. For controlling the transmission-gate-based MUX, two-phase clock signals are required, which can be generated by a simple inverter chain.

However, as discussed in Section II, such topology can incur data upset during clock overlap due to delay mismatch of CLK and CLKB at the transmission gate MUX. Introducing a tri-state inverter-based MUX [27] still results in weak pull-up/down.

Therefore, in the proposed DET-FF, a fully static complementary CMOS MUX is utilized to 1) prevent data upset due to clock overlap and 2) keep every node fully static (full swing) at any given time.

The fully static complementary CMOS MUX is derived by logic minimization, where multiplexing operation is performed only with existing internal signals. Since all of the nodes in the positive/negative latches are static with full voltage swing, the complementary CMOS MUX can operate without any stability issue. The logic minimization process for the complementary CMOS MUX is as follows:

Firstly, the latched data DP/DN and their inverted value QP/QN can be written as

$$DP = \overline{CDP} \cdot \overline{CLK} + \overline{D} \cdot \overline{CDP} \cdot CLK \tag{1}$$

$$DN = \overline{CDN} \cdot CLK + \overline{D} \cdot \overline{CDN} \cdot \overline{CLK} \tag{2}$$

$$QP = \overline{DP} \tag{3}$$

$$QN = \overline{DN} \tag{4}$$

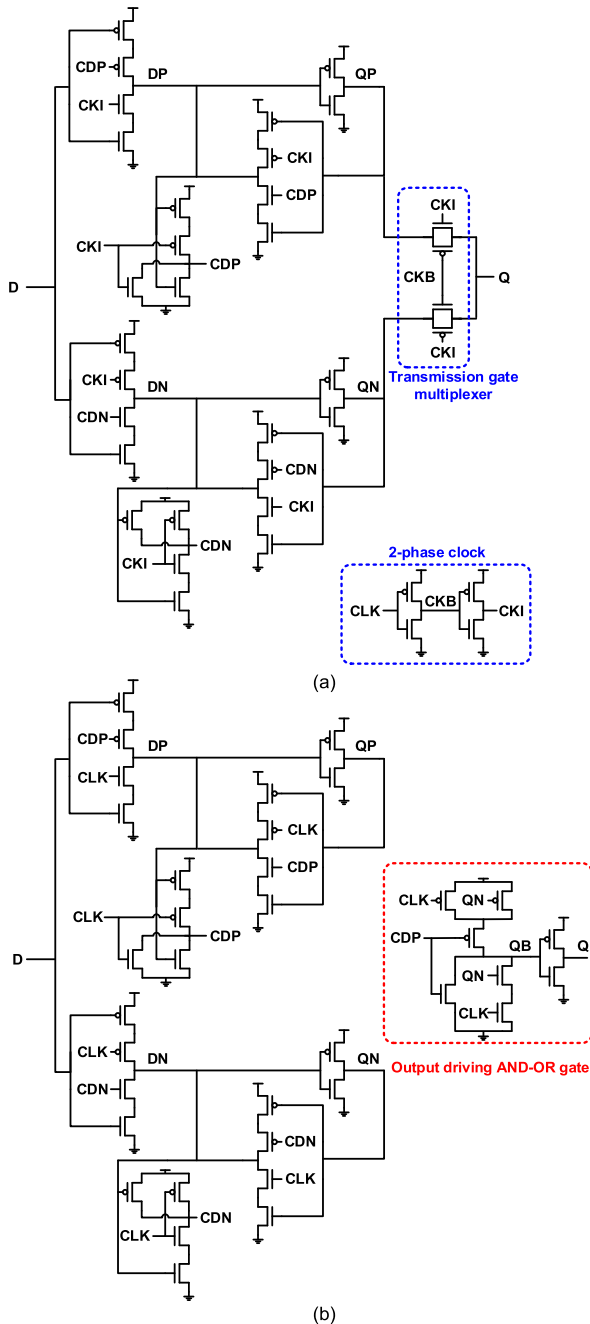


FIGURE 6. (a) The Latch-MUX DET-FF with the proposed two static latches and the transmission gate MUX (before logic minimization) (b) proposed fully static DET-FF with the fully static complementary CMOS MUX using TSPC.

Secondly, the clock-conditioned data CDP/CDN can be obtained with NAND/NOR operation as

$$CDP = \overline{DP + CLK} \quad (5)$$

$$CDN = \overline{DN \cdot CLK} \quad (6)$$

Meanwhile, the final output Q should be the output of the MUX, which selectively forwards QP or QN depending on the clock phase. Its logic function can be written as

$$Q = QP \cdot \overline{CLK} + QN \cdot CLK \quad (7)$$

In this equation, the term related to QP can be rewritten as follows by using (3) and (5):

$$QP \cdot \overline{CLK} = \overline{DP} \cdot \overline{CLK} = \overline{DP + CLK} = CDP \quad (8)$$

Therefore, equation (7) can be rewritten as

$$Q = CDP + QN \cdot CLK \quad (9)$$

Therefore, the transmission-gate-based MUX in Fig. 6(a) can be replaced with a complementary CMOS AO (AND-OR) gate as shown in Fig. 6(b). In the proposed DET-FF design, a total of 36 transistors are used, which is less than a prior TSPC-DET FF [27] with 38 transistors.

Fig. 7 illustrates the operation of a FS-TSPC-DET FF in each clock and input data condition. The top row shows the case where the initial DP value is ‘0’ and the input D is ‘0’, whereas the bottom row shows the case where the initial DP is ‘1’ and the input D is ‘1’. The detailed behavior is presented as the CLK toggles from ‘0’ to ‘1’ and then from ‘1’ to ‘0’.

In the initial state (CLK = ‘0’), the positive latch holds the internal data (DP). Note that CDP = ‘0’ when DP = ‘1’ (bottom left in Fig. 7); hence, the stacked NMOS in the feedback-clocked inverter is turned off. However, since QP = ‘0’, only the pull-up path of the feedback inverter matters, and all nodes are still statically driven to V_{DD} or GND. Meanwhile, the output QB is determined solely by CDP since QN is ANDed with CLK at the MUX.

As the clock rises (CLK = ‘1’), the data stored in the negative latch is now forwarded to QB through the MUX since CDP is forced to be ‘0’ and CLK is ‘1’. The internal data at the positive latch (DP) can be updated since 1) the input clocked inverter is fully on (CDP = ‘0’) and 2) the feedback clocked inverter is fully off (CLK = ‘1’ and CDP = ‘0’).

At the clock falling transition, the negative latch becomes transparent again, and the updated data in the positive latch will be forwarded to the output QB/Q. Although the TSPC-SDET FF [27] also utilizes the same single-phase clocking method, the clock-conditioned data signals (CDP/CDN) in the proposed DET-FF can reduce the number of transistors connected to the input clock (from 14 to 10), resulting in lower power consumption caused by clock transition.

IV. SIMULATION ANALYSIS AND COMPARISON

The proposed FS-TSPC-DET FF is designed and its layout is modeled in 28nm LP bulk CMOS technology for detailed analysis. In addition, 6 other DET-FFs described in section II (SDET FF [20], TSPC-SDET FF [27], DECP FF [17], SA-DET FF [11], NCCDR FF [23], and FN_C-DET FF [24]) are also designed for comparison. In advanced technology nodes, the reliability and performance of the digital circuits rapidly degrade in a low-voltage regime due to exacerbated PVT variations. Therefore, to verify the proposed design in challenging conditions, relatively advanced process node (28nm), among those that can be accessed, is selected for design and analysis. In addition, since the proposed FF is

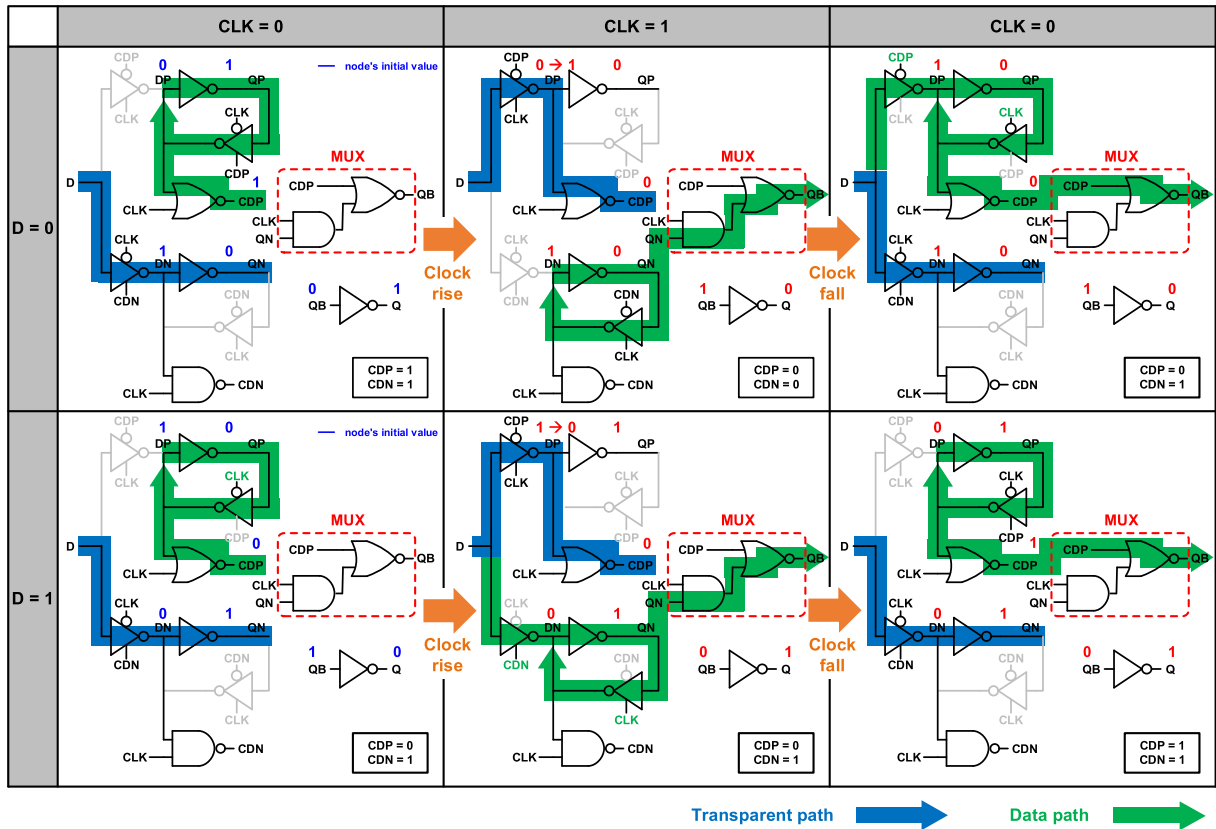


FIGURE 7. FS-TSPC-DET FF gate-level schematic and its operation.

targeted for IoT applications, Low-Power (LP) process, rather than General Purpose (GP), is chosen.

Fig. 8 presents the layout of the 7 DET-FFs designed for post-layout analysis. All DET-FF designs are carefully sized to guarantee reliable operation at room temperature and standard supply voltage (0.95 V) while keeping the size as small as possible for energy efficiency. RC parasitics are extracted for the layouts shown in Fig. 8 so that the post-layout simulations can be performed at various operation conditions.

Among the 3 types of DET-FFs, the pulsed-latch-type DET-FF (DECP FF [17], SA-DET FF [11]) and the C-element-type DET-FF (NCDDR FF [23], FN_C-DET FF [24]) are more susceptible to PVT variations than the Latch-MUX-type DET-FF (SDET FF [20], TSPC-SDET FF [27] and FS-TSPC-DET FF) since the pulsed-latch-type DET-FF requires precise pulse timing and the C-element-type DET-FF has contention with the weak inverters. Therefore, these DET-FFs require proper transistor sizing for stable operation. However, sizing up transistors to ensure a minimum reliable pulse length for pulsed-latch-type DET-FFs or making a weak inverter for C-element-type DET-FFs would incur greater power and area overhead. Due to this trade-off, the transistor sizes are carefully chosen for these two types of DET-FF designs so that stable operation at the standard supply voltage and room temperature is guaranteed while keeping the area compact and energy efficiency reasonable.

This approach also includes the use of non-minimum-length transistors for reliable pulse lengths in pulsed-latch-type DET-FFs.

A. STANDARD SUPPLY VOLTAGE OPERATION

Fig. 9 shows the simulation setup for fair data measurement and comparison, which is similar to the one used in [16], [37]. Two inverters are utilized as input drivers for the input clock (CLK) and data (D). To precisely model the power consumption of the DET-FFs, the power consumed for driving each pin is estimated by measuring the power consumed on these drivers. For example, the power consumed for driving the CLK input (P_{CLK}) can be calculated as

$$P_{CLK} = P_{Driver_CLK} - P_{Driver_CLK_int} \quad (10)$$

where P_{Driver_CLK} is the total measured power consumption of the power supply of the CLK-driving inverter, and $P_{Driver_CLK_int}$ is the CLK-driving inverter's intrinsic power consumption, which can be measured by measuring the power consumption of the CLK-driving inverter without the DET-FF's CLK pin loading. Similarly, the power consumed for driving D input (P_D) can be calculated as

$$P_D = P_{Driver_D} - P_{Driver_D_int} \quad (11)$$

and the power consumed for the internal switching of the flip-flop ($P_{Flip-Flop}$) can be measured by the power consumption

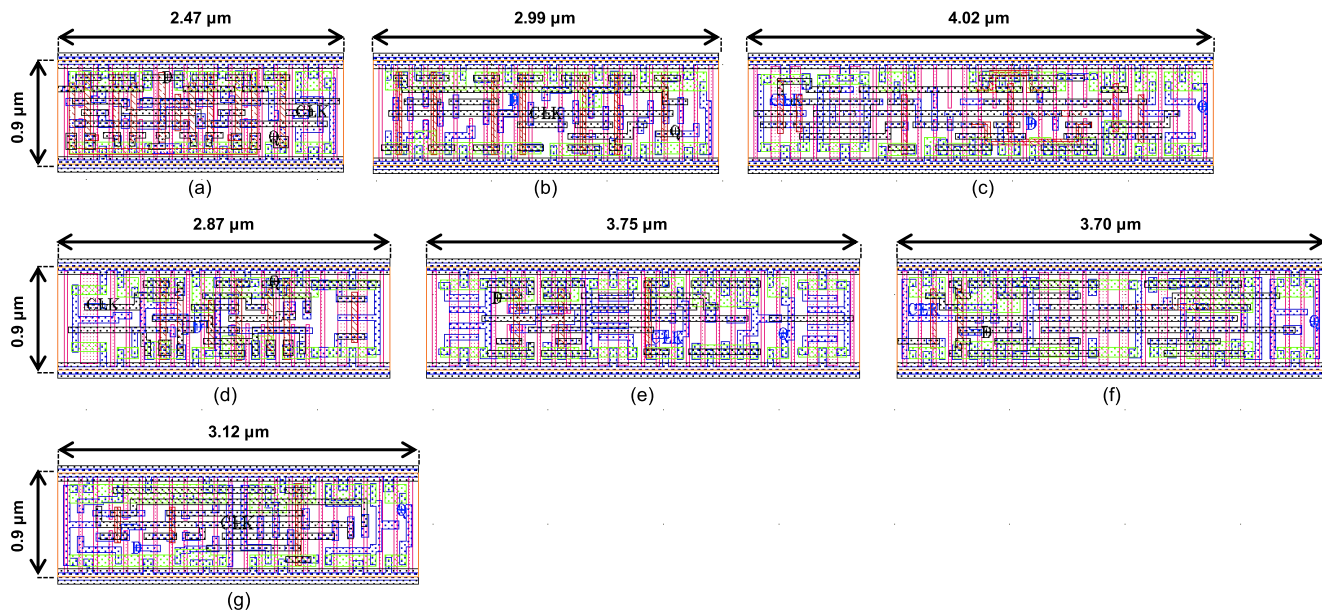


FIGURE 8. Layout of 7 DET-FFs. (a) SDET FF (b) TSPC-SDET FF (c) DECP FF (d) SA-DET FF (e) NCDDR FF (f) FN_C-DET FF (g) FS-TSPC-DET FF.

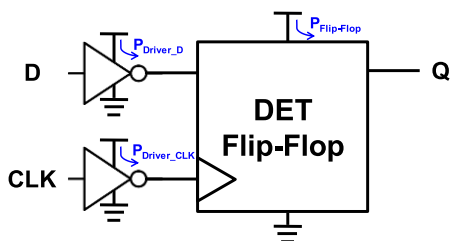


FIGURE 9. DET-FF simulation setup including the input driver.

of the flip-flop’s power supply. Then the total power consumption of a DET-FF can be represented as

$$\begin{aligned}
 P_{Total} &= P_{Flip-Flop} + P_D + P_{CLK} \\
 &= P_{Flip-Flop} + (P_{Driver_D} - P_{Driver_D_int}) \\
 &\quad + (P_{Driver_CLK} - P_{Driver_CLK_int}) \quad (12)
 \end{aligned}$$

Meanwhile, the potential wire capacitance and resistance outside the DET-FF layout are not included in the simulation since they can vary significantly depending on the implementation.

To evaluate the standard voltage operation of the 7 DET-FFs, each DET-FF is simulated with the nominal supply voltage (0.95 V) at room temperature (27 °C) assuming TT (typical) process corner. A clock frequency of 1 GHz is used, and a varying data switching activity ratio (α) of 10%, 25% or 50% is applied. Fig. 10 shows the measured power consumption of the DET-FFs, and the power consumption is broken down into $P_{Flip-Flop}$, P_D and P_{CLK} . A few interesting trends can be observed with the power consumption analysis in Fig. 10.

Firstly, the power consumption of the clock (CLK) input driver (P_{CLK}) is proportional to the number of transistors at

the clock input. For example, three DET-FFs using complementary two-phase clocking – namely SDET FF, NCDDR FF, and FN_C-DET FF – consume the least amount of power since they have only 2 transistors at the CLK input. In contrast, the proposed FS-TSPC-DET FF has 10 transistors and TSPC-SDET FF has 14 transistors at the CLK input, resulting in relatively higher CLK driver power consumption. Meanwhile, if contention exists on the CLK node, the CLK driver can consume more power than is proportional to the transistor count. For example, DECP FF, shown in Fig. 2, has 7 transistors and SA-DET FF has 6 transistors on the CLK input. However, the pulse generator in SA-DET FF has contention during the pulse generation at the PULS node. Therefore, SA-DET FF consumes more CLK driver power than DECP FF despite its lower CLK input transistor count. Since the CLK node activity does not change with α , P_{CLK} does not change with α .

Secondly, the power consumption of the data (D) input driver (P_D) is directly proportional to the activity ratio (α) and accounts for a relatively small percentage of the total power consumption if there is no contention on D input. It can be seen that P_D is less than 10 % for TSPC-SDET FF, DECP FF, FN_C-DET FF and FS-TSPC-DET FF. With SDET FF, SA-DET FF and NCDDR FF, D input can be directly connected to the data retention node in certain phases or for a short time period, which creates contention and draws more power from D input driver. In the SDET FF and NCDDR FF, two latches and the D node can be shorted due to clock-phase misalignment, which makes P_D sharply increase at $\alpha = 25\%$ and 50% compared to when $\alpha = 10\%$.

Thirdly, the power consumption through a flip-flop’s power supply ($P_{Flip-Flop}$) increases with a higher α but at a lower ratio compared with α . This is because internal switching of a flip-flop is related to both the clock and data.

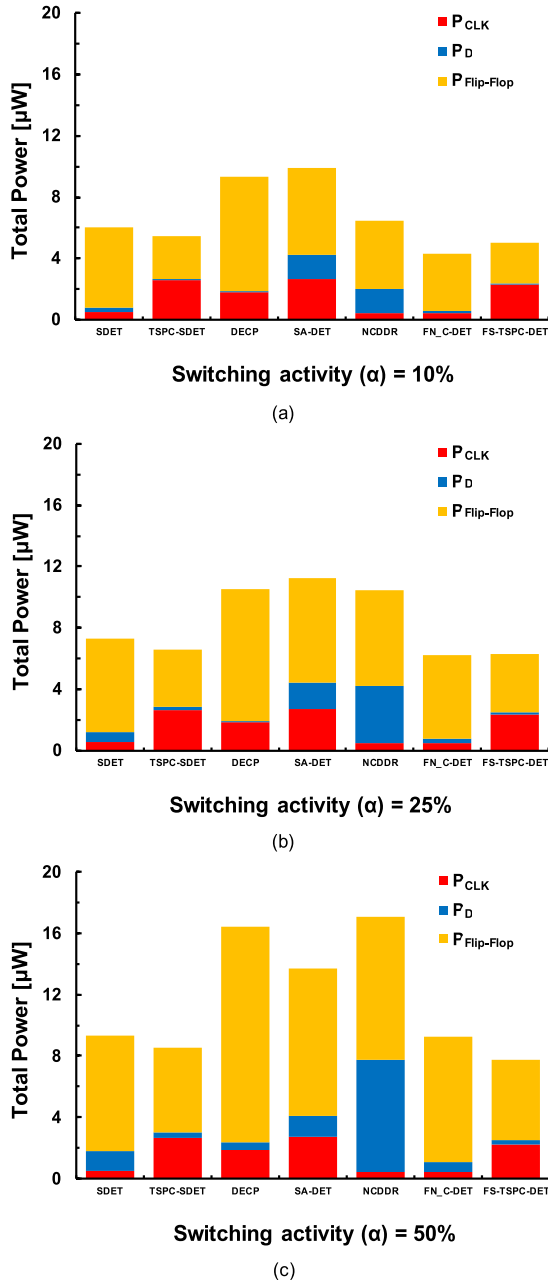


FIGURE 10. Power consumption of 7 DET-FFs at standard V_{DD} (0.95 V). Switching activity is (a) 10% (b) 25% (c) 50%.

For example, the amount of power consumed for driving an inverted clock signal (CLKB) in flip-flops with a two-phase clocking scheme is not correlated with and hence does not change with α . On the other hand, the amount of power consumed for switching the latched data is directly correlated with α . Therefore, the increase in $P_{\text{Flip-Flop}}$ with higher α can be minimized by minimizing the data-related internal switching activity.

In regards to these trends, the following observations can be made for the proposed FS-TSPC-DET FF: 1) A large portion of the proposed DET-FF’s power consumption is due to the CLK driver. This is due to the large number of clock-loading transistors. 2) Negligible power is consumed

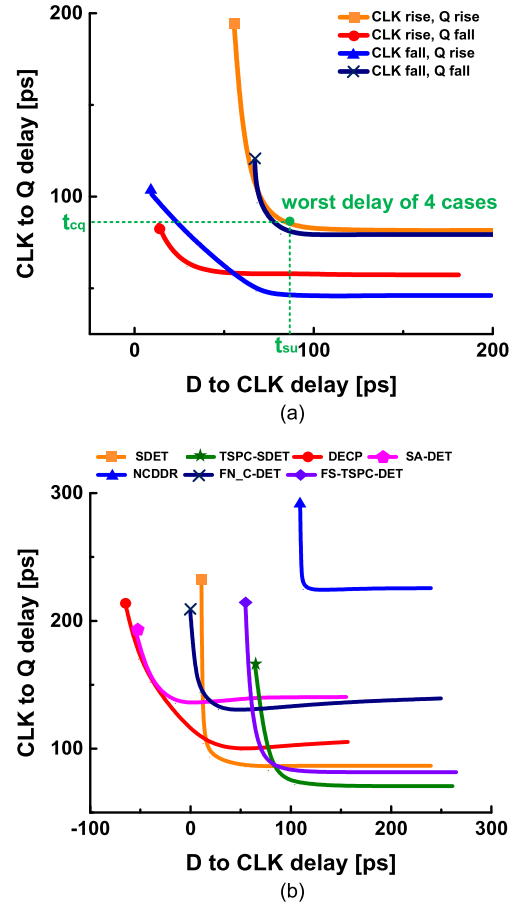


FIGURE 11. CLK-to-Q delay versus D-to-CLK delay. (a) all output transitions at both clock edges in the proposed FS-TSPC-DET FF. (b) setup time comparison with 7 DET-FFs.

by D input, thanks to the lack of contention. 3) The baseline $P_{\text{Flip-Flop}}$ is relatively small compared with that of the other DET-FF. This is because there is no potential contention within the flip-flop. Overall, the proposed FS-TSPC-DET FF has low power consumption compared with the other analyzed DET FFs: second lowest when $\alpha = 10\%$ or 25% and the lowest with $\alpha = 50\%$. This means that the penalty for increased data activity is smaller, thanks to the reduced internal switching activity.

Fig. 11 shows the CLK-to-Q delay (T_{cq}) as a function of D to CLK delay in standard $V_{\text{DD}} = 0.95 \text{ V}$. For accurate setup/hold time measurement, D-to-CLK delay is swept for every 0.02 ps, and more than 10,000 data points were measured. In Fig. 11(a), the T_{cq} values for all 4 types of transition cases are shown for the proposed FS-TSPC-DET FF. In this figure, T_{cq} and the setup time are determined by the case where Q is rising at the rising edge of the CLK. Fig. 11(b) shows T_{cq} for all 7 DET-FFs. In general, the Latch-MUX-type DET-FFs (SDET FF, TSPC-SDET FF and FS-TSPC-DET FF) provide a shorter T_{cq} than other types of DET-FFs.

B. NEAR-THRESHOLD SUPPLY VOLTAGE OPERATION

The DET-FFs are simulated under near-threshold voltage to examine voltage scalability for low-voltage operation in IoT

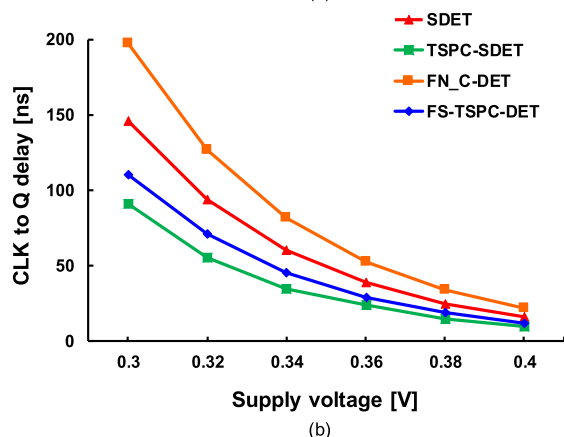
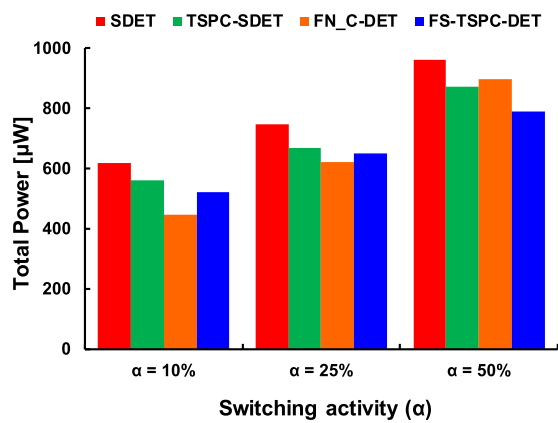


FIGURE 12. Comparisons of 4 DET-FFs with low supply voltages (a) Total power consumption (P_{Total}) at varying switching activity ratios (b) Supply voltage versus CLK-to-Q delay (T_{cq}) plots.

applications. To evaluate the near-threshold voltage operation of the DET-FFs, each DET-FF is simulated with a supply voltage of 0.3 V at room temperature (27 °C) and a clock frequency of 1 MHz, assuming TT (typical) process corner. Under the given conditions, the 3 DET-FFs (SA-DET FF, DECP FF and NCDDR FF) failed to function properly for at least one clock edge due to failure in pulse generation or data contention. Therefore, only the remaining 4 DET-FFs (SDET FF, TSPC-SDET FF, FN_C-DET FF and FS-TSPC-DET FF) are reported in this section.

Fig. 12 shows the total power consumption (P_{Total}) and CLK-to-Q delay (T_{cq}) of these 4 DET-FFs with varying switching activities ($\alpha = 10\%, 25\%, 50\%$). In Fig. 12(a), the proposed FS-TSPC-DET FF shows the second lowest P_{Total} at low α of 10% and 25% and the lowest P_{Total} at high α of 50%, which is similar to the results obtained under standard voltage. In addition to P_{Total} , another metric that requires attention under low voltage operation is T_{cq} . With aggressive voltage scaling down to near-threshold regimes, T_{cq} can exponentially increase and impact the overall performance of digital circuits. Fig. 12(b) show how T_{cq} changes with aggressive voltage scaling. As the supply voltage is decreased from 0.4 V to 0.3 V, T_{cq} rapidly increases. It can be seen that T_{cq} increases more sharply with the FN_C-DET FF

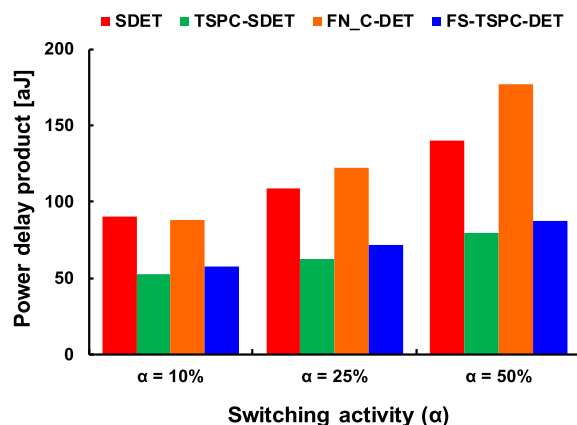


FIGURE 13. Comparisons of power-delay-product (PDP) in low supply voltage with 4 DET-FFs.

than with the other 3 DET-FFs, and the designs with true-single-phase clocking schemes (TSPC-SDET FF, FS-TSPC-DET FF) maintain faster operation than the other DET-FFs even at low supply voltage conditions.

The total power consumption (P_{Total}) and CLK-to-Q delay (T_{cq}) are both important metrics for DET-FF operation in low-voltage conditions, but there can be trade-off between these two metrics. For this reason, the power delay product ($PDP = P_{Total} \times T_{cq}$) is often used [11], [27], [23] to evaluate FFs. Fig. 13 shows the PDPs of the 4 DET-FFs under near-threshold voltage operation. Although the FN_C-DET FF has the lowest P_{Total} , TSPC-SDET FF and FS-TSPC-DET FF present significantly better PDPs regardless of α due to significantly lower T_{cq} . This implies that the proposed FS-TSPC-DET FF can be a suitable solution for low-voltage operation in IoT applications.

C. MONTE CARLO SIMULATION WITH SUPPLY VOLTAGE AND TEMPERATURE SCALING

Even though the proposed FS-TSPC-DET FF has low power consumption and small delay, its robustness against PVT variation should be verified for near-threshold voltage operation since the impact of variation is exaggerated in this voltage regime. To evaluate the robustness of the DET-FFs, Monte Carlo simulations (for process corner and mismatch) are performed with aggressive supply voltage scaling and a wide temperature range. In this simulation, the 4 DET-FF designs evaluated for near-threshold voltage operation are examined again.

Fig. 14 shows the input test pattern used for the Monte Carlo simulations, which is carefully designed to check the functionality of each DET-FF for all possible input combinations. All possible transition scenarios of input D and CLK (up to 3 transitions of one signal while the other signal is unchanged) are included in this test pattern, as shown in the truth table. The input clock frequency is set to 1 kHz, which is sufficiently low to allow functional failures with long delay to be checked. A long delay between the CLK and

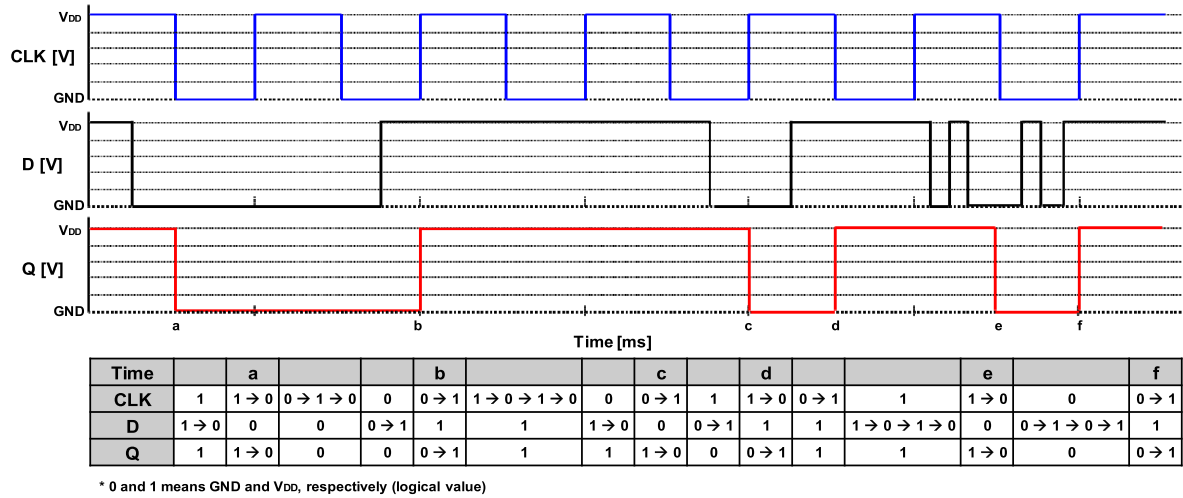


FIGURE 14. Test pattern and truth table for Monte Carlo simulation.

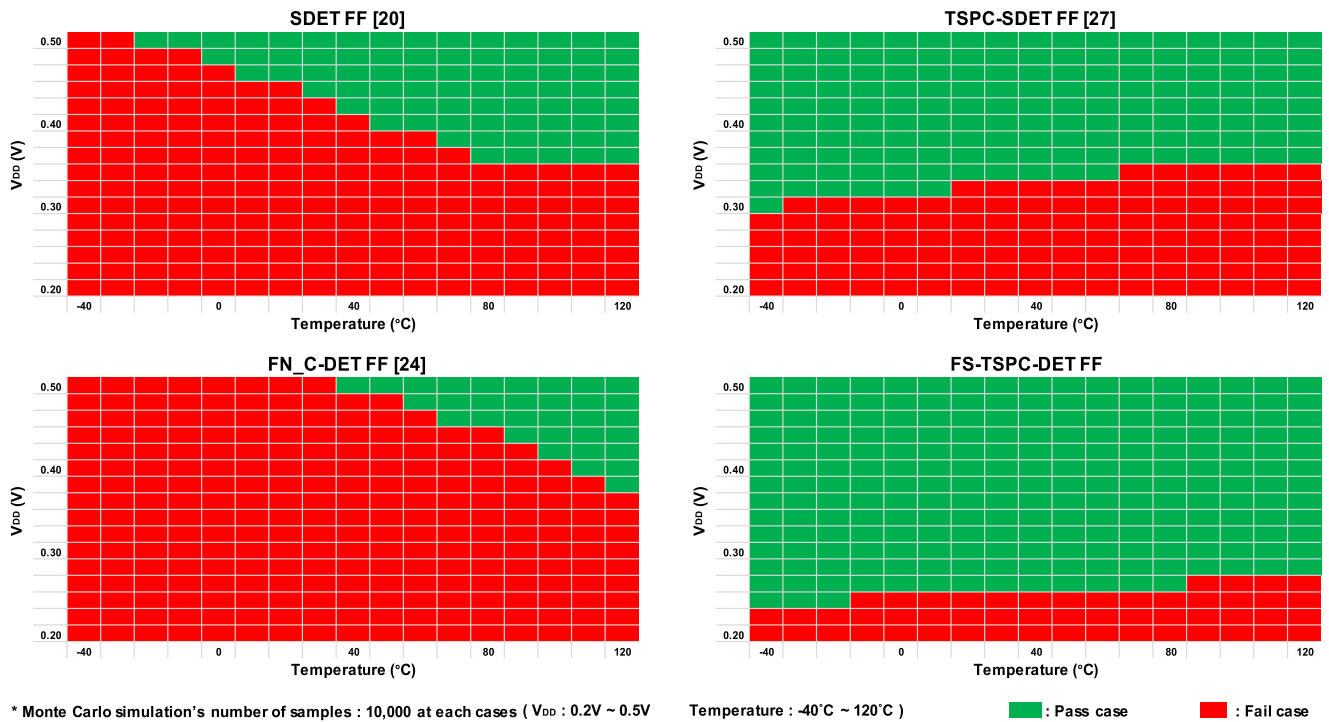


FIGURE 15. Monte Carlo simulation results with 4 DET-FFs with aggressive voltage and temperature scaling.

data transition is assumed so that only the functional failures not related to setup or hold-time violations are checked. If a DET-FF operates with no functional failure, the output Q is expected as shown Fig. 14, synchronizing the input data at each marked point (a–f).

Monte Carlo simulations were performed for a supply voltage range of 0.2 V to 0.5 V with 20-mV steps and a temperature range of -40 °C to 120 °C with 10 °C steps. For each condition, 10k Monte Carlo points were simulated for accurate evaluation. The Shmoo plots for the 4 DET-FFs are shown in Fig. 15. In these Shmoo plots, a green box

represents ‘pass’ in 10k Monte Carlo simulations and a red box represents ‘fail’ for failing at least 1 test case. Among the 4 evaluated DET-FFs, the SDET FF and FN_C-DET FF have limited functionality at low voltage and low temperature. This is because these DET-FFs utilize a two-phase clocking scheme, where the clock overlap issue can be worse with PVT variations. Furthermore, in the FN_C-DET FF, the strong and weak C-elements have contention on the data storage node, making it susceptible to PVT variations. Thanks to their single-phase clocking scheme, TSPC-SDET FF and FS-TSPC-DET FF can operate without failure at the lower

TABLE 1. DET-FF comparison of simulation results at standard conditions.

DET-FF design	SDET [20]	TSPC-SDET [27]	DECP [17]	SA-DET [11]	NCDDR [23]	FN_C-DET [24]	FS-TSPC-DET This work
# of Tr.	26	38	35	22	28	34	36
Type	Latch-MUX	Latch-MUX	Pulsed-latch	Pulsed-latch	C-element	C-element	Latch-MUX
Clock phase (Trigger-type)	Two-phase (Complementary)	Single-phase	Two-phase (Implicit pulse)	Two-phase (Explicit pulse)	Two-phase (Complementary)	Two-phase (Complementary)	Single-phase
Normalized Area	0.79	0.96	1.29	0.92	1.20	1.19	1
Power _{0.1} (μW)	6.01	5.52	9.38	9.91	6.47	4.31	5.03
Power _{0.25} (μW)	7.27	6.58	10.5	11.2	10.5	6.20	6.30
Power _{0.5} (μW)	9.35	8.55	12.4	13.7	17.1	9.28	7.71
PDP _{0.1} (fJ)	0.73	0.41	1.62	1.39	1.44	0.71	0.41
PDP _{0.25} (fJ)	0.88	0.49	1.81	1.58	2.33	1.03	0.51
PDP _{0.5} (fJ)	1.13	0.63	2.14	1.92	3.80	1.53	0.62
T _{eq} (ps)	121	75.0	173	140	223	166	81.6
Setup time (ps)	20.9	88.9	8.32	-0.34	111	46.2	82.5
Hold time (ps)	50.5	2.77	143	128	218	114	11.8
Minimum V _{DD} (Temp. -40~120 °C)	> 0.5 V	0.36 V	-	-	-	> 0.5V	0.28 V

* Power_α, PDP_α : α is switching activity ratio
 * The power includes CLK and D driver’s power except the driver’s internal power
 * Minimum V_{DD}: Monte Carlo simulation result in Fig. 15

voltages and temperatures. However, TSPC-SDET FF cannot function below 0.3 V due to the weak pull-up/pull-down (at node XP or XN in Fig. 1(b)). Thanks to the fully static implementation, the proposed FS-TSPC-DET FF has the lowest functional supply voltage and temperature – it could operate without failure at 0.28 V for the entire tested temperature range.

Table 1 summarizes the evaluation results with standard supply voltage conditions (V_{DD} = 0.95 V, input clock frequency = 1 GHz, temp. = 27 °C at TT corner). The normalized areas of the 7 DET-FFs are compared based on the layout sizes shown in Fig. 8 (FS-TSPC-DET FF = ‘1’). The area is not directly proportional to the transistor counts since some designs require careful transistor sizing for robust operation, especially when they have contention. Thanks to their symmetric and static structure, Latch-MUX-type DET-FFs (the SDET FF, TSPC-SDET FF and FS-TSPC-DET FF) can have smaller layout areas compared to other DET-FF designs despite the use of a large number of transistors.

The proposed FS-TSPC-DET FF has low power consumption comparable to the best performing FN_C-DET FF. In addition, it also has low CLK-to-Q delay comparable to the best performing TSPC-SDET FF, resulting in the lowest PDP for α = 10% and 50% and second lowest PDP for α = 25%. Besides the excellent trade-off between power and performance, the proposed FS-TSPC-DET FF also exhibits robust operation at low voltage. Thanks to its fully static design without contention, the minimum operational supply voltage was as low as 0.28 V. Such high energy efficiency and wide voltage scalability suggest that the proposed FS-TSPC-DET FF not only consumes relatively lower power compared to

prior-art designs at a given supply voltage but also can operate with the lowest supply voltage. These properties make the proposed FF an excellent candidate as an energy-efficient sequential circuit element for energy/cost-sensitive IoT applications with aggressive dynamic voltage scaling down to a near-threshold voltage of 0.28 V.

V. CONCLUSION

A dual-edge-triggered flip-flop for high energy efficiency and robust near-threshold operation is proposed in this paper. Unlike most of the conventional DET-FFs, such as the Pulsed-latch-type or Latch-MUX-type DET-FF using a complementary two-phase clock, the proposed FS-TSPC-DET FF utilizes a true single-phase clock and implements a fully static structure without floating state and contention. The comprehensive post-layout analysis of the DET FFs implemented in 28nm CMOS technology showed that the proposed FS-TSPC-DET FF achieves excellent power-delay trade-off and high tolerance against PVT variation, thanks to the simple and fully static implementation. Extensive comparison with prior-art DET-FFs confirmed that the proposed DET-FF can operate at the lowest voltage of 0.28 V for a temperature range of -40 °C to 120 °C, making it an excellent candidate as an energy-efficient flip-flop for energy/cost-sensitive IoT applications.

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