IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 8, 2020, accepted February 22, 2020, date of publication February 27, 2020, date of current version March 10, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2976729

Dynamic SOC Balance Strategy for Modular Energy Storage System Based on Adaptive Droop Control

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This work was supported in part by the National Natural Science Foundation of China under Grant 61903158, and in part by the National Science Foundation of Jiangsu Province of China under Grant BK20180595.

ABSTRACT This paper proposes a dynamic state-of-charge (SOC) balance control strategy for the modular super capacitor energy storage system (ESS). The strategy takes SOC information as the droop variable and introduces the SOC of each module into its independent current closed loop by inverse droop control, so that the system can adjust the average operating current of each sub-module according to its SOC in the system dynamic charging and discharging process. Moreover, a concise unified current compensation method is proposed to minimize system current deviation caused by the balance algorithm. Compared with the traditional control strategies, the proposed strategy does not need to exchange SOC information between sub-modules, thus effectively reduces system communication data. In addition, the proposed strategy not only has favorable voltage control ability and stability, but also has a concise control structure. The proposed balance control strategy can further improve the modularity and reliability of the modular ESS, which is helpful to promote the application of the system in medium and high voltage applications.

INDEX TERMS SOC balance control, modular multilevel DC/DC converter (MMDDC), droop control, bidirectional DC/DC converter, energy storage system.

I. INTRODUCTION

Super capacitor is a kind of energy storage device with the features of high power density, long lifetime and wide working temperature range [1]. Super capacitor based energy storage system is widely used in renewable energy system, rail transit system and electric vehicle [1]–[3]. Due to the low voltage level, super capacitors are usually used in series to supply high voltage applications. However, because of the manufacturing errors and frequent charging and discharging operations, the capacitance of super capacitor will be inconsistent after long-term use, which will lead super capacitors to be overcharged or over-discharged. Therefore, SOC balance control is one of the key issues in the ESS [4]. At present, many SOC balance strategies have been proposed and these strategies can be summarized as active balance strategy, passive balance strategy and direct balance strategy, as shown in Figure 1 [5].

Active balance strategy needs to transfer the energy from the high SOC cells or modules to the low SOC ones with the aid of external equipment, such as capacitors or isolated converters [6]–[11]. Capacitor-based balance strategy has the advantages of simple circuit structure and low cost [7], [8]. Yet, the energy transfer between non-adjacent modules will reduce system efficiency. In order to solve this issue, soft-switching balance technique is proposed in [9], but the control of the balance circuit becomes more complex. In contrast, the balance strategy using isolated converter can improve energy transfer efficiency [10], [11]. However, the requirement for designing the transformer increases with the number of super capacitors.

Passive balance strategy uses power resistor or zener diode to consume the redundant energy in high SOC super capacitors [12]. Although this strategy has the advantages of easy implementation and simple control, the energy utilization is very low and the system heats seriously.

Unlike the former strategies, direct balance strategy can use the system main power circuit to achieve SOC balance control in system dynamic process [13], [14]. Therefore, the external balance circuit can be avoided, which can not only improve the system reliability, but also avoid the energy loss caused by the balance circuit. Huang *et al.* [13]

The associate editor coordinating the review of this manuscript and approving it for publication was Eklas Hossain.

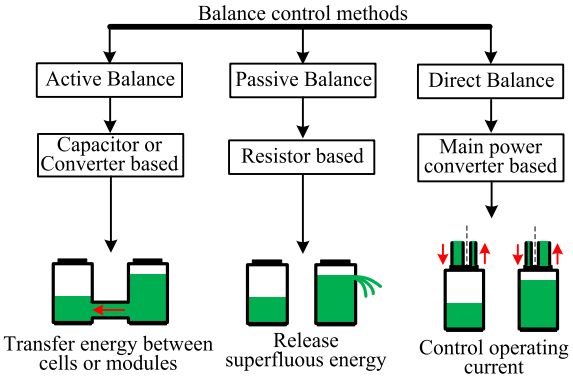

FIGURE 1. Classification of SOC balance methods.

synthesized DC bus voltage control and SOC balance control into a single control system, and used the average SOC to control each sub-module. A decoupled dynamic balance control strategy was proposed in [15]. The decoupled SOC control loop is superposed with the current loop to achieve SOC balance control during system dynamic process. In addition, model predictive control [16] and novel cascaded topology [17] are also studied. These direct SOC balance strategies need to share SOC information with others by communication lines. Yet, the communication between sub-modules leads to the complexity of system control increasing with the number of sub-modules, at the same time, the large amount of communication data will increase the system computational burden and any sub-module failure will affect the system normal operation. Reference [18] proposed to build independent SOC balanced control closed loops for sub-modules, and applied the traditional droop control to sub-module's current loop to achieve power balance control. However, the output bias caused by droop control is not studied in this paper. Reference [5] proposed a SOC balance control strategy based on a common balance bus, which can reduce communication data and improve system modularity. However, the change of system hardware circuit brings some disadvantages: 1) The balance bus and digital to analog converters (DACs) make the system design more complex, which not only increases system cost, but also greatly enhances system potential risk; 2) The voltage signal in the long balance bus is easily affected by external electromagnetic environment in high power systems, and then affects the system control performance; 3) The balance bus makes it impossible for each sub-module to achieve electrical isolation. The electrical fault of any sub-module will be transmitted to other sub-module through the balance bus. This is a fatal defect for the modular system to achieve the electrical isolation control of each sub-module. 4) Each sub-module is still unable to achieve completely independent control, and there is still room for further improvement of system modularization. In summary, the method proposed in [5] is not the optimal SOC balance control scheme for the modular ESS.

Droop control is often used in the parallel system to achieve power balance control [22]–[26]. Lu *et al.* [22] proposed the SOC droop method for the parallel system to achieve power balance control for the first time. On this basis, [24] proposed a dual quadrant SOC droop strategy for energy storage units to achieve energy balance control. Reference [26] proposed to use frequency scheduling instead of adaptive droop gain to regulate the active power, so each energy storage unit can schedule its own frequency reference according to the SOC values of all other units. However, due to the difference of application background and converter topology, these strategies are only suitable for distributed systems, not for cascaded systems. An integrated SOC balance control strategy with voltage compensation for the ESS is proposed in [27]. However, the output voltage deviation is not eliminated by the proposed compensation method, and the voltage compensation method requires different current compensation according to the voltage error level, which results in the strategy to be complex. Droop control is a balance control strategy with simple principle and high reliability, its disadvantage lies in the deviation in system control [28], [29]. The compensation method of parallel system is more complex than that of cascade system because of the decentralized equipment. Therefore, it is necessary to consider the actual condition to design the balance strategy for the ESS, such as the converter topology and the system working requirements, so as to find the optimal solutions.

In order to achieve the SOC balance control of modular ESS and further improve the modularity and reliability of the system, this paper proposes a dynamic SOC balance control strategy. The proposed strategy takes SOC as the inverse droop variable to design the current closed loop, and a concise current compensation method is proposed to minimize the positive current deviation caused by the balance algorithm. Compared with the traditional strategies, this strategy has favorable voltage control ability. It not only greatly simplifies the digital communication required by the SOC balance control, but also effectively simplifies the hardware and software structure of the cascade modular energy storage system, which helps to further improve the reliability and modularity of the system. In summary, this strategy is more suitable for the multi-module ESS in medium and high voltage applications.

The organization of this paper is as follows: The basic principles of the proposed strategy are presented in Section II. Detailed design and analysis of the proposed strategy are carried out in Section III. Section IV shows the experimental results to verify the effectiveness of this strategy and presents the comparison with other strategies. The conclusion of this paper is presented in Section V.

II. BASIC CONCEPT BEHIND THE PROPOSED BALANCE STRATEGY

A. OPERATION PRINCIPLE OF THE MODULAR ENERGY STORAGE SYSTEM

Figure 2 illustrates the schematic of the super capacitor ESS based on the modular multilevel DC/DC converter (MMDDC) [15]. The converter consists of multiple

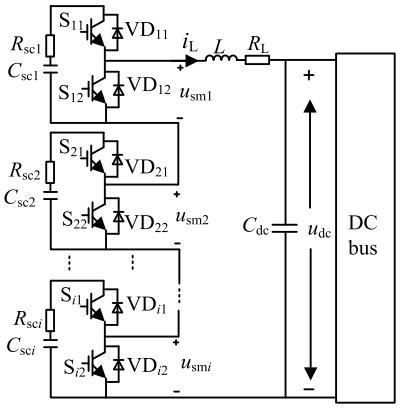

FIGURE 2. Schematic of modular super capacitor ESS.

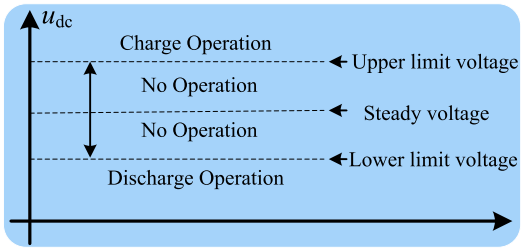

FIGURE 3. Switching basis of ESS operation mode.

sub-modules SM_i, ($i = 1,2,3\ldots n$). Each super capacitor module (SCM) occupies one sub-module. In Figure 2, u_{dc} is the DC bus voltage, L represents the system inductance, R_L is the inductance equivalent resistance, C_{dc} represents the filter capacitor of the ESS, and i_L is the system current.

Super capacitor ESS is used to keep DC bus voltage constant when the power on the grid is unbalanced. When the load power exceeds DC bus input power, the ESS releases the stored energy to prevent bus voltage from dropping. When the load feeds back energy to DC bus, the ESS stores the feedback energy to prevent the bus voltage from rising. Hence, the ESS operation mode is determined by DC bus voltage level. Figure 3 shows the system operation mode switching basis. Because the judged voltage has a hysteresis interval, the system operation modes are independent of each other, and there is no mutual interference when the operation mode is switched.

B. ESTIMATION OF SUPER CAPACITOR MODULE SOC

The simplified circuit model of SCM is shown in Figure 4, which can be used to analyze the dynamic characteristics of SCM. In Figure 4, C_{kj} represents the capacitance of the jth super capacitor cell in the ith module ($k, j = 1, 2, 3\ldots n$), R_{kj} is the equivalent resistance of super capacitor cell. When multiple super capacitor cells are connected in series, the equivalent capacitance and the equivalent resistance can be expressed as C_{sci} and R_{sci}, u_{sci} represents the voltage of C_{sci}.

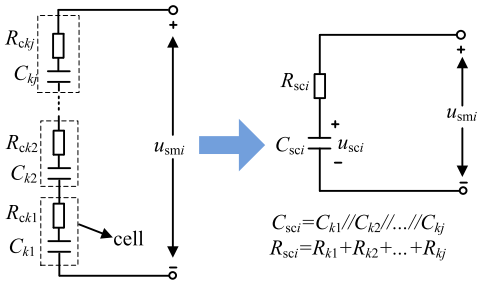

FIGURE 4. Simplified super capacitor module circuit.

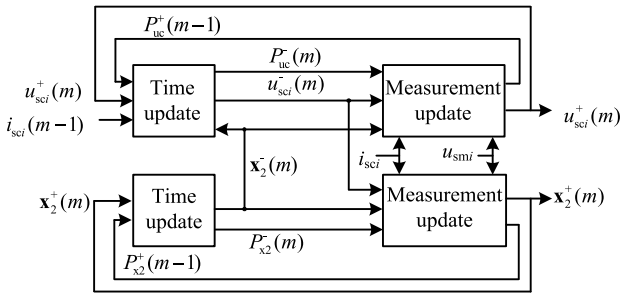

FIGURE 5. Observation model of SCM based on dual Kalman filters.

Super capacitor's SOC is related to its charge[22], which can be expressed as:

$$\mathrm{SOC}_i = \frac{C_{sci} u_{sci}}{Q_r} \tag{1}$$

where Q_r is the rated charge.

As shown in (1), the capacitance C_{sci} and the actual voltage u_{sci} are required to calculate the SOC. Due to only u_{smi} can be measured in the actual system and the existence of R_{sci}, the measured voltage cannot be used directly. In order to solve this issue, state observer is usually employed to estimate the indirectly measurable parameters [20], [21]. The estimation methods of SOC, available power and state-of-health (SOH) of batteries using Kalman filter are designed and analyzed in detail in [20]. Here, the dual Kalman filter observation model is adopted to calculate the SCM SOC.

According to Figure 4, the SCM state equation in discrete state can be derived as:

$$\begin{cases} u_{sci}(m+1) = u_{sci}(m) + \dfrac{1}{C_{sci}(m)} i_{sci}(m) T_c + w(m) \\ u_{smi}(m) = u_{sci}(m) + i_{sci}(m) R_{sci}(m) + v(m) \end{cases} \tag{2}$$

where i_{sci} is the operating current of SCM, T_c is the sample period, m represents the sampling times, $w(m)$ and $v(m)$ are assumed to be the mutually uncorrelated white Gaussian random processes with zero mean.

In order to obtain the SOC accurately, it is necessary to get the value of C_{sci} and R_{sci}. A new state variables expressed as $\mathbf{x}_2(m) = [C_{sci}(m)\ R_{sci}(m)]^T$ is constructed. According to the method proposed in [21], an observer based on dual Kalman filters is built to get the value of C_{sci} and R_{sci}, as shown in Figure 5. $\mathbf{x}^-(m)$ and $P^-(m)$ are the predicted

state and error covariance vector, which are calculated from the prior moment. The optimal estimate of state and error covariance $\mathbf{x}^+(m)$ and $P^+(m)$ are obtained though refining processes based on the predicted state and error covariance. It can be seen that the calculation process has two Kalman filters running in parallel—one is used to achieve the state, the other is used to achieve the parameters.

C. BASIC PRINCIPLE OF THE PROPOSED BALANCE STRATEGY

Phase-shifting control is adopted by the MMDDC to improve system current ripple frequency [15]. According to the analysis presented in [5], the relationship between i_{L} and the average current flowing through SCM $i_{\mathrm{a\_sc}i}$ can be obtained:

$$i_{\mathrm{a\_sc}i} = d_i \cdot i_{\mathrm{L}} \tag{3}$$

where d_i is the duty ratio of arbitrary sub-module.

According to (1), the relationship between SCM charge and its SOC value can be derived:

$$\Delta Q_{i(T)} = Q_{\mathrm{r}} \Delta \mathrm{SOC}_{i(\Delta T)} \tag{4}$$

where $\Delta \mathrm{SOC}_i(T)$ is the changed SOC value in ΔT time, Q_i represents the changed charge of SCM.

Meanwhile, according to the Coulomb's law, we can have:

$$\Delta Q_{i(T)} = \Delta T i_{\mathrm{a\_sc}i(T)} \tag{5}$$

According to (4) and (5) we can have:

$$i_{\mathrm{a\_sc}i(T_{\mathrm{s}})} = \frac{\Delta Q_{i(T_{\mathrm{s}})}}{T_{\mathrm{s}}} = \frac{Q_{\mathrm{r}} \Delta \mathrm{SOC}_{i(T_{\mathrm{s}})}}{T_{\mathrm{s}}} \tag{6}$$

where T_{s} is the switching period.

The total power of ESS is the sum power of all sub-modules, hence the system power in any switching period can be expressed as:

$$P_{(T_{\mathrm{s}})} = \sum_{i=1}^{n} \left[u_{\mathrm{sm}i(T_{\mathrm{s}})} \cdot i_{\mathrm{a\_sc}i(T_{\mathrm{s}})} \right] \tag{7}$$

Substituting (6) into (7), it yields:

$$P_{(T_{\mathrm{s}})} = \frac{Q_{\mathrm{r}}}{T_{\mathrm{s}}} \sum_{i=1}^{n} \left[u_{\mathrm{sm}i(T_{\mathrm{s}})} \cdot \Delta \mathrm{SOC}_{i(T_{\mathrm{s}})} \right] \tag{8}$$

According to (6), we can have the relationship between sub-module operation current and its SOC variation:

$$\frac{i_{\mathrm{a\_sc}i(T_{\mathrm{s}})}}{\mathrm{SOC}_{i(T_{\mathrm{s}})}} = \frac{Q_{\mathrm{r}}}{T_{\mathrm{s}}} \tag{9}$$

Substituting (9) into (8), it yields:

$$i_{\mathrm{a\_sc}i(T_{\mathrm{s}})} = \frac{\Delta \mathrm{SOC}_{i(T_{\mathrm{s}})} P_{(T_{\mathrm{s}})}}{\sum_{i=1}^{n} \left[u_{\mathrm{sm}i(T_{\mathrm{s}})} \cdot \Delta \mathrm{SOC}_{i(T_{\mathrm{s}})} \right]} \tag{10}$$

From (3) and (10), the relationship between the duty ratio of each sub-module and the SOC variation of SCM can be obtained as follows:

$$d_1 : d_2 : \ldots : d_n = \Delta \mathrm{SOC}_1 : \Delta \mathrm{SOC}_2 : \ldots \Delta \mathrm{SOC}_n \tag{11}$$

It can be known from (11) that the SOC variation of each sub-module is proportional to the duty ratio, which means that the SOC balance control can be achieved by controlling sub-module duty ratio. To achieve this purpose, the higher SOC module in charge mode should be charged by a small average current, and the one with lower SOC should work with a large average current. In discharge mode, the sub-module working principle is opposite to that in charge mode.

III. DESIGN AND ANALYSIS OF THE PROPOSED CONTROL STRATEGY

A. CONTROL STRATEGY DESIGN

Assume that the current direction in discharge mode is positive. Figure 6 shows the unified schematic diagram of the proposed strategy for charge and discharge mode. The strategy has a master-slave structure. All sub-modules share a common voltage loop and each sub-module has an independent current loop with the same structure. The communication content between master and slave controllers is only the original current reference. The SOC information of each sub-module no longer needs to be processed centrally. This design method not only minimizes the communication data, but also guarantees the independence of each sub-module in system control.

The structure of the proposed strategy in charge mode is basically the same as that in discharge mode. But in order to ensure the original current reference and feedback current are positive in any mode, the feedback voltage and current signals must be adjusted. For example, due to $u_{\mathrm{dc}} > u_{\mathrm{ref}}$ in charge mode, the voltage loop input is designed as $(u_{\mathrm{dc}} - u_{\mathrm{ref}})$. At the meantime, the feedback current in charge mode needs to be reversed.

As shown in Figure 6, the SOC of each sub-module is treated as the droop variable and is introduced into the current loops. The final current reference of each sub-module can be expressed as:

$$\begin{cases} i^*_{\mathrm{ref}i} = i_{\mathrm{A}i} + i_{\mathrm{B}i} \\ i_{\mathrm{A}i} = i_{\mathrm{ref}}(1 + m_0 \mathrm{SOC}_i), \\ i_{\mathrm{B}i} = -\begin{cases} \alpha_0 (i_{\mathrm{L}} - i_{\mathrm{ref}}) & i_{\mathrm{L}} > i_{\mathrm{ref}} \\ 0 & i_{\mathrm{L}} \le i_{\mathrm{ref}} \end{cases} \end{cases} \tag{12}$$

where $i^*_{\mathrm{ref}i}$ is the final current reference; $i_{\mathrm{A}i}$ is the balance current reference; $i_{\mathrm{B}i}$ is the system current compensation reference; i_{ref} is the original current reference, which is generated by voltage loop; m_0 is the balance coefficient; α_0 is the system current compensation coefficient.

The balance current reference $i_{\mathrm{A}i}$ is the critical part in the proposed strategy to achieve SOC balance control. It can be seen from (12) that the high SOC module will have a larger final current reference than the low SOC one. Therefore, when the system operates in discharge mode, the high SOC module will work with a larger duty ratio and discharge more power. While, the one with low SOC will release less power.

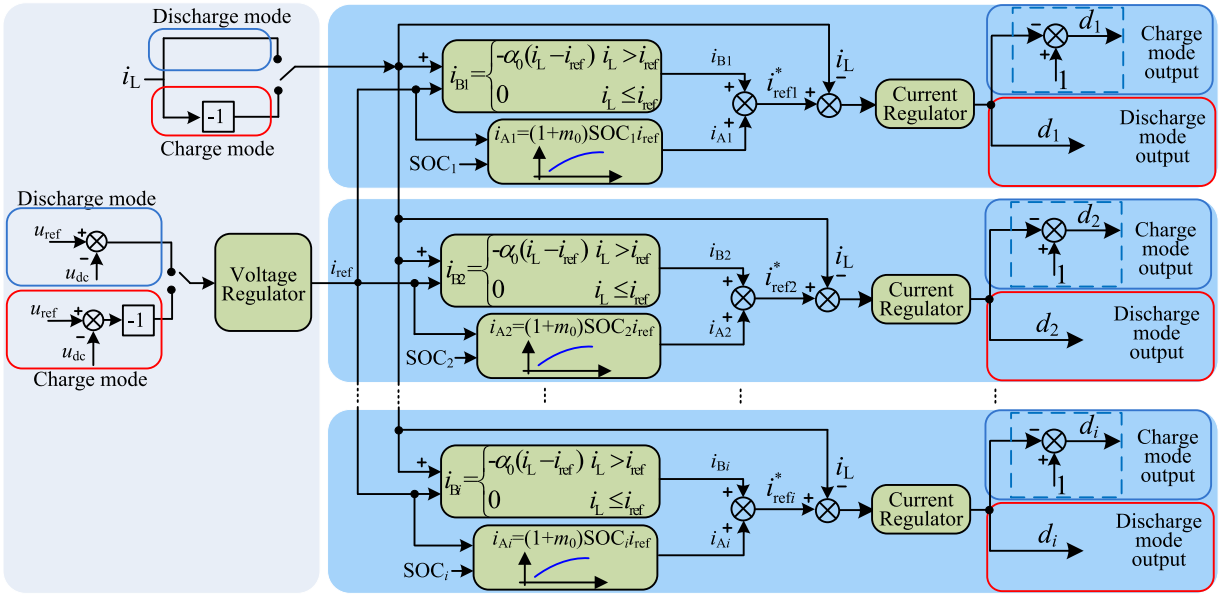

FIGURE 6. Control block diagram of the proposed SOC balance control strategy.

The system equivalent equation can be written as:

$$u_{dc} = \sum_{i=1}^{n} u_{sci} d_i - (L\frac{di_L}{dt} + i_L \cdot R_L) \tag{13}$$

It can be known from (13) that the system current is inversely proportional to the duty ratio in charge mode. Therefore, the final output duty ratio is reversely designed, which is shown in Figure 6. By this way, the duty ratio of high SOC sub-module in charge mode will be always smaller than the low SOC one until the SOC difference between sub-modules is eliminated.

B. SYSTEM CURRENT PERFORMANCE ANALYSIS

Assume that all the SCMs have the same SOC and the current compensation in (12) is ignored, in the steady state we can have:

$$I_L = (1 + m_0 \mathrm{SOC}_i) I_{ref} \tag{14}$$

where I_L and I_{ref} are the system current and original current reference in the steady state, respectively.

According to (14), we can have the effect of the balance coefficient and SOC on system current, which is shown in Figure 7.

As shown in Figure 7, the proposed SOC balance strategy is similar to the droop control method used in the parallel operation system to achieve load current sharing [22]–[24]. The common advantage of the proposed strategy and conventional droop control method is that the communi- cation data in the system control can be minimized, thus the system modularity can be improved. The shortage of droop method is the poor output voltage regulation performance. However, the proposed control strategy sacrifices system current

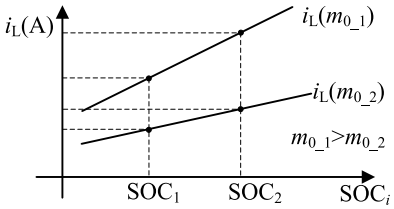

FIGURE 7. Effect of balance coefficient and SOC on system current.

regulation performance to achieve distributed SOC balance control, leading to a positive current deviation.

According to (14), the current positive deviation rate k_{ui} can be expressed as:

$$k_{ui} = m_0 \mathrm{SOC}_i \tag{15}$$

The role of k_{ui} is to generate the current reference deviation between sub-modules to balance the SOC. A larger m_0 is beneficial to achieve SOC balance control. However, it will cause a larger deviation in system current.

In order to reduce system current deviation, a unified current compensation reference is added to the current reference, which is expressed as i_{Bi} in (12). After adding the current compensation, in the steady state we can have:

$$I_L = (1 + m_0 \mathrm{SOC}_i) I_{ref} - \alpha_0 (I_L - I_{ref}) \tag{16}$$

According to (16), we can obtain:

$$I_L = I_{ref} + \frac{m_0 \mathrm{SOC}_i}{1 + \alpha_0} I_{ref} \tag{17}$$

So, the modified current positive deviation rate k_{umi} is

$$k_{umi} = \frac{m_0 \mathrm{SOC}_i}{1 + \alpha_0} \tag{18}$$

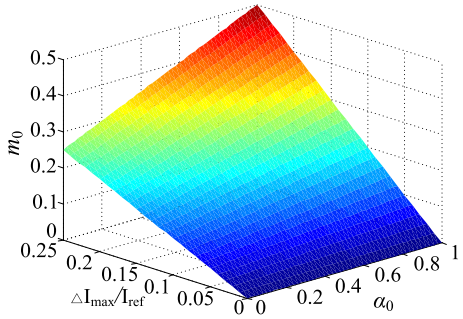

FIGURE 8. Design principles of m_0 and α_0.

It can be seen from the comparison between (15) and (18) that the current compensation can help to reduce the current positive deviation. However it can only minimize but not completely eliminate the current deviation. Therefore, it needs to compromise the balance control and system current control according to system operation requirements to design the parameters.

The design of m_0 and α_0 should satisfy the following principles: (1) The system current deviation must be within the maximum allowable range. (2) The current compensation reference has no effect on the original current reference. The two principles can be expressed by the following equations:

$$m_0 \leq \frac{\Delta I_{\max}}{I_{\text{ref}}}(1+\alpha_0) \tag{19}$$

$$I_{\text{ref}} m_0 \text{SOC}_i - \alpha_0 (I_{\text{L}} - I_{\text{ref}}) \geq 0 \tag{20}$$

where $\Delta I_{\max}/I_{\text{ref}}$ is the system current deviation ratio.

So as to prolong the lifetime of super capacitors, the SCM SOC should be kept larger than 0.5 [1]. Substituting (20) into (19), we can get the value of α_0, which can be designed within the range of 0∼1. Under this range, the design principle of m_0 and α_0 can be derived according to (19), which is shown in Figure 8.

According to Figure 8, the maximum allowable system current deviation should be determined firstly, and then design m_0 and α_0 by synthesizing other performance requirements, such as balance performance or system response speed. For example, assume that the maximum current deviation rate is 0.05, at the meantime the parameters should ensure the fastest system dynamic performance, thus, according to the analysis in Section III (D) and Figure8, α_0 should be designed as 1 and the maximum value of m_0 is 0.1. The value of m_0 can be selected less than 0.1 to improve system current regulation performance. But, when the balance speed is considered first, m_0 should be designed as 0.1.

C. STABILITY ANALYSIS

Because of the large capacity, the voltage of each SCM can be viewed as a constant value in a short time [22]. Thus, we can have:

$$u_{\text{sc}i} = U_{\text{sc}i} \tag{21}$$

where $U_{\text{sc}i}$ is the voltage of SCM at steady state.

By perturbing (13), the perturbed expression of system state equation is shown as:

$$\hat{u}_{\text{dc}} = \sum_{i=1}^{n} U_{\text{sc}i}\hat{d}_i - (sL + R_{\text{L}})\hat{i}_{\text{L}} \tag{22}$$

where $\hat{u}_{\text{dc}}$ is the perturbed DC bus voltage; $\hat{d}_i$ is the perturbed sub-module duty ratio and $\hat{i}_{\text{L}}$ is the perturbed system current.

The voltage variation of super capacitor during system dynamic process is shown as:

$$u_{\text{sc}i} = u_{\text{sc}i t=0} - \int_0^t i_{\text{sc}i} d\tau / C_{\text{sc}i} \tag{23}$$

where $u_{\text{sc}i t=0}$ is the super capacitor initial voltage.

Substituting (23) and (3) into (1), the expression of SOC can be written as:

$$\text{SOC}_i = \frac{C_{\text{sc}i} u_{\text{sc}i t=0} - \int_0^t d_i i_{\text{L}} d\tau}{Q_{\text{r}}} \tag{24}$$

Substituting perturbation into (24), and transferring the final result into s-domain, the expression of the perturbed SOC can be obtained:

$$s\hat{\text{SOC}}_i = -(\hat{d}_i I_{\text{L}} + D_i \hat{i}_{\text{L}})/Q_{\text{r}} \tag{25}$$

where D_i is the sub-module duty ratio at steady state.

By perturbing (12), the perturbed expression of final current reference is derived:

$$\hat{i}^*_{\text{ref}i} = m_0 I_{\text{ref}} s\hat{\text{SOC}}_i - \alpha_0 \hat{i}_{\text{L}} + (1 + m_0 \text{SOC}_i + \alpha_0)\hat{i}_{\text{ref}} \tag{26}$$

where $\hat{i}_{\text{ref}}$ is the perturbed original current reference.

Substituting (25) into (26), the relationship between $\hat{i}^*_{\text{ref}i}$ and $\hat{d}_i$ is obtained:

$$\hat{i}^*_{\text{ref}i} = -m_0 I_{\text{ref}} \frac{I_{\text{L}}}{sQ_{\text{r}}}\hat{d}_i - (\alpha_0 + m_0 I_{\text{ref}} \frac{D_{\text{i}}}{sQ_{\text{r}}})\hat{i}_{\text{L}} + (1 + m_0 \text{SOC}_i + \alpha_0)\hat{i}_{\text{ref}} \tag{27}$$

The original current reference and sub-module duty ratio are generated by the voltage loop and current loop, respectively, and their expressions are shown as:

$$i_{\text{ref}} = (u_{\text{ref}} - u_{\text{dc}}) G_{\text{dcpi}}(s) \tag{28}$$

$$d_i = (i^*_{\text{ref}i} - i_{\text{L}}) G_{\text{ipi}}(s) \tag{29}$$

where $G_{\text{dcpi}}(s)$ and $G_{\text{ipi}}(s)$ are the voltage loop regulator and system current loop regulator, respectively.

The classical proportional integral (PI) regulator is used by the system, and their transfer functions are shown as:

$$\begin{cases} G_{\text{dcpi}}(s) = k_{\text{dcp}} + k_{\text{dci}}/s \\ G_{\text{ipi}}(s) = k_{\text{ip}} + k_{\text{ii}}/s \end{cases} \tag{30}$$

where k_{dcp} and k_{dci} are the proportional coefficient and integral coefficient of voltage loop regulator, respectively; k_{ip} and k_{ii} are the proportional coefficient and integral coefficient of current loop regulator, respectively.

By perturbing (28) and (29), the perturbed expression of i_{ref} and d_i can be obtained:

$$\hat{i}_{\text{ref}} = -\hat{u}_{\text{dc}} G_{\text{dcpi}}(s) \tag{31}$$

$$\hat{d}_i = (\hat{i}^*_{\text{ref}i} - \hat{i}_{\text{L}}) G_{\text{ipi}}(s) \tag{32}$$

Substituting (32) into (27), the perturbed final current reference can be removed. Thus, the perturbed duty ratio of each sub-module can be expressed by $\hat{i}_{\text{L}}$ and $\hat{i}_{\text{ref}}$, which is shown as:

$$\hat{d}_i = \frac{sQ_{\text{r}}G_{\text{ipi}}(s)}{G_{\text{ipi}}m_0 I_{\text{ref}} I_{\text{L}} + sQ_{\text{r}}} \begin{bmatrix} -(\alpha_0 + m_0 I_{\text{ref}} \frac{D_i}{sQ_{\text{r}}})\hat{i}_{\text{L}} \\ +(1 + m_0 \text{SOC}_i + \alpha_0)\hat{i}_{\text{ref}} \end{bmatrix} \tag{33}$$

Substituting (33) into (22), and combining the result with (31), the system characteristic equation is reached:

$$As^4 + Bs^3 + Cs^2 + Ds + E = 0 \tag{34}$$

where A, B, C, D and E are listed in (35).

$$\begin{cases} A = k_{\text{dcp}} L Q_{\text{r}} \\ B = k_{\text{dci}} L Q_{\text{r}} + k_{\text{dcp}} (R_{\text{L}} Q_{\text{r}} + L k_{\text{ip}} m_0 I_{\text{ref}} I_{\text{L}} \\ \quad + \sum_{i=1}^{n} U_{\text{sc}i} k_{\text{ip}} \alpha_0 Q_{\text{r}}) \\ C = k_{\text{dci}} (R_{\text{L}} Q_{\text{r}} + L k_{\text{ip}} m_0 I_{\text{ref}} I_{\text{L}} + \sum_{i=1}^{n} U_{\text{sc}i} k_{\text{ip}} \alpha_0 Q_{\text{r}}) \\ \quad + k_{\text{dcp}} \begin{bmatrix} R_{\text{L}} k_{\text{ip}} m_0 I_{\text{ref}} I_{\text{L}} + L k_{\text{ii}} m_0 I_{\text{ref}} I_{\text{L}} \\ + \sum_{i=1}^{n} U_{\text{sc}i} k_{\text{ii}} \alpha_0 Q_{\text{r}} + \sum_{i=1}^{n} U_{\text{sc}i} D_i m_0 I_{\text{ref}} k_{\text{ip}} \end{bmatrix} \\ D = k_{\text{dcp}} (R_{\text{L}} k_{\text{ii}} m_0 I_{\text{ref}} I_{\text{L}} + \sum_{i=1}^{n} U_{\text{sc}i} D_i m_0 I_{\text{ref}} k_{\text{ii}}) \\ \quad + k_{\text{dci}} \begin{bmatrix} R_{\text{L}} k_{\text{ip}} m_0 I_{\text{ref}} I_{\text{L}} + L k_{\text{ii}} m_0 I_{\text{ref}} I_{\text{L}} \\ + \sum_{i=1}^{n} U_{\text{sc}i} k_{\text{ii}} \alpha_0 Q_{\text{r}} + \sum_{i=1}^{n} U_{\text{sc}i} D_i m_0 I_{\text{ref}} k_{\text{ip}} \end{bmatrix} \\ E = k_{\text{dci}} (R_{\text{L}} k_{\text{ii}} m_0 I_{\text{ref}} I_{\text{L}} + \sum_{i=1}^{n} U_{\text{sc}i} D_i m_0 I_{\text{ref}} k_{\text{ii}}) \end{cases} \tag{35}$$

To simplify the system stability analysis, an ESS consists of three sub-modules is studied. System parameters are shown in Table 1, which are verified by Matlab/Simulink. The system root locus under different conditions are shown in Figure 9∼11. According to (34), we can know that the system has four poles. Because one pole is far away from the imaginary axis and locates on the left plane, it is not shown in the figures. The pole marked with a circle means that it does not change with the analyzed parameter. The arrow shows the changing trend of the pole as the analyzed parameter increases.

Figure 9 shows the system root locus when the parameters of voltage loop regulator change. In Figure 9(a), k_{dci} keeps the value shown in Table 1 unchanged and k_{dcp} increases from 0.1to 10 with the step size of 1.1. It can be seen that

TABLE 1. System parameters.

Symbol	Parameters	Value
Q_{r}	Super capacitor capacity	480C
α_0	Current compensationfactor	1
L	System inductance	2mH
R_{L}	Inductance equivalent resistance	0.01Ω
m_0	Balance coefficient	0.2
k_{dcp}	Voltage loop proportional factor	5
k_{dci}	Voltage loop integral factor	3
k_{ip}	Current loop proportional factor	0.1
k_{ii}	Current loop integral factor	0.1
U_{sc1}, U_{sc2}, U_{sc3}	SCM voltage at initial state	31V,34V,37V
D_1, D_2, D_3	Sub-module duty ratio at steady state	0.5, 0.75,0.95
I_{L}	System current	15.4A
I_{ref}	System current original reference	15A

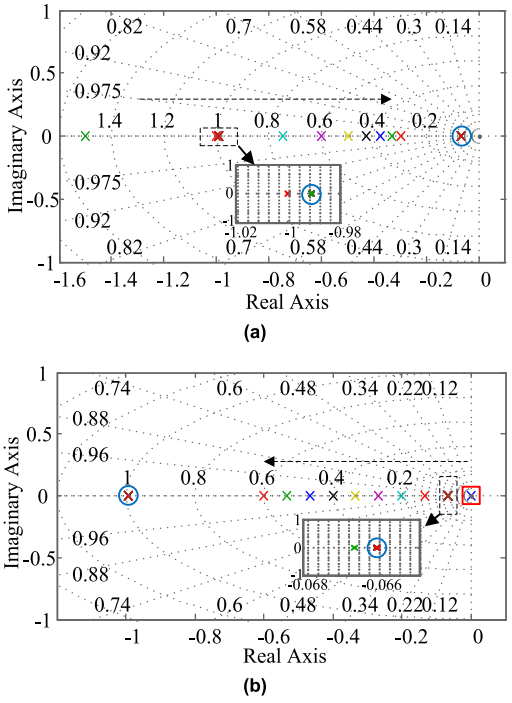

FIGURE 9. System root locus under different voltage regulator parameters. (a) k_{dcp} increasing (b) k_{dci} increasing.

the increasing of k_{dcp} leads to one pole moving toward the imaginary axis. Figure9(b) shows the system root locus when k_{dcp} does not change and k_{dci} increases from 0 to 5 with the step size of 0.5. One pole locates on the origin when k_{dci} is 0, but with the increasing of k_{dci}, this pole gradually moves away from the imaginary axis.

It can be seen from Figure10 that only one pole is controlled by the current loop regulator. When k_{ip} increases from 0.05 to 0.5 with the step of 0.05 and other parameters remain unchanged, the system root locus is shown in Figure10(a). It can be seen that the increasing of k_{ip} weakens the system stability. Figure10(b) shows the root locus when k_{ii} varies from 0.05 to 0.5 with the step of 0.045. The increasing of k_{ii} leads to this pole moving away from the imaginary axis.

Figure 11(a) shows the poles with the balance coefficient varies from 0.05∼0.5 with the step of 0.045, and α_0 is set

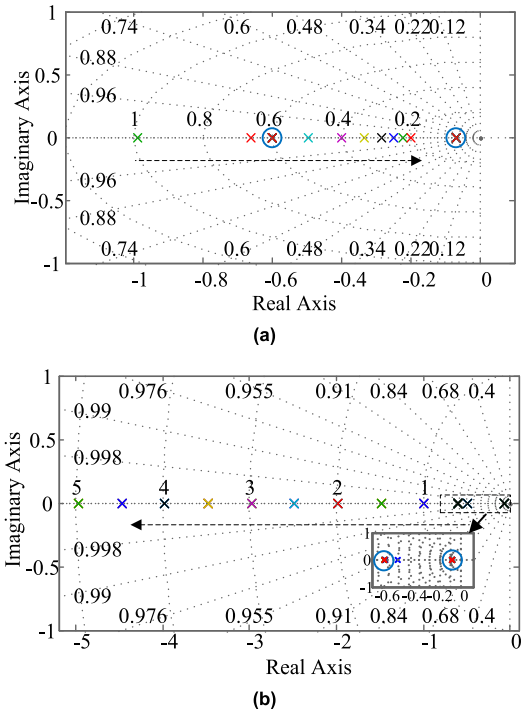

FIGURE 10. System root locus under different current regulator parameters. (a) k_{ip} increasing (b) k_{ii} increasing.

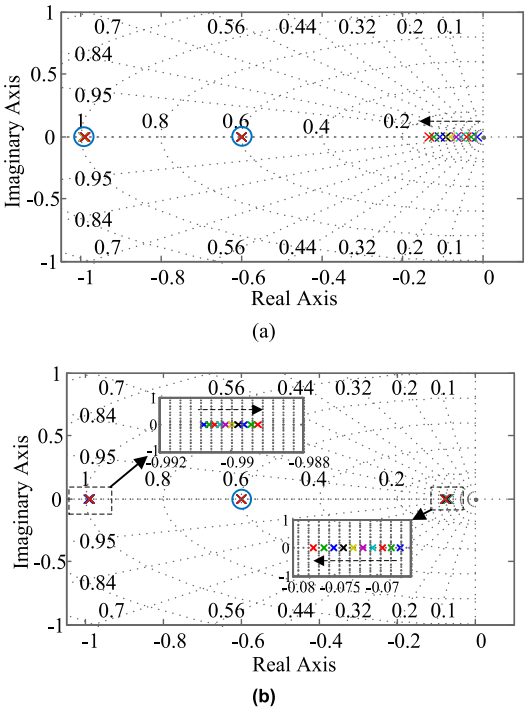

FIGURE 11. System root locus when m_0 and SCM voltage change. (a)m_0 increasing (b) SCM voltage increasing.

to be the maximum value 1. It can be seen that m_0 mainly affects the system dominant pole and a larger m_0 can help to improve system stability. Figure11(b) shows the system root locus when the voltage of the three SCMs gradually reduces from the value shown in Table 1 to 30V and the final duty ratio of each sub-module gradually reaches 0.89. It can be seen that the SCM voltage does not influence the system stability obviously. Due to the voltage can reflect SCM SOC, Figure11(b) also can be used to demonstrate the influence of SOC on system stability.

The dominant closed-loop pole of the system is mainly decided by m_0. As shown in the Figure 9∼11, all the poles are located on the left half plane, so that the stability of the control system can be confirmed.

D. ANALYSIS OF VOLTAGE STABILIZATION CAPABILITY

The current in a series system is determined by all modules together. Due to the current loop of each sub-module has the same structure, all current loops can be represented by a unified average current loop. From this point, the system control block diagram can be simplified, which is shown in Figure 12.

M_0 is the gain of the original current reference, $M_0 = (1 + m_0\mathrm{SOC}_0)$. Even though the final current reference of each module is different, the system current will approach the average final current reference when the number of series modules is large. Therefore, SOC_0 can be considered as the average SOC of all modules. i_{dc} is the load current. K_i and K_u are the feedback gains of system current and bus voltage, respectively, which are set to be 1. The transfer functions of $G_{dcpi}(s)$ and $G_{ipi}(s)$ are shown in (30). $G_s(s)$ is the transfer

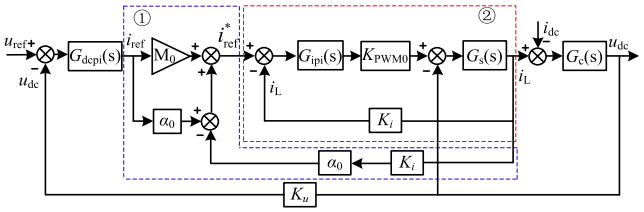

FIGURE 12. The simplified control block diagram of modular ESS.

function from inductance voltage to system current. $G_c(s)$ is the transfer function from system current to DC bus voltage. The expressions of $G_s(s)$ and $G_c(s)$ are shown as follows:

$$\begin{cases} G_s(s) = \dfrac{1}{sL + R_L} \\ G_c(s) = \dfrac{1}{sC_{dc}} \end{cases} \tag{36}$$

As shown in Figure 12, the system current loop can be divided into two parts: the improved current reference and the current closed loop. Since the balance strategy only changes the current reference and the response of the current loop is much faster than that of the voltage loop, part ② in Figure12 can be simplified to a first-order inertial item.

$$\frac{i^*_{ref}}{i_L} = \frac{1}{\tau s + 1} \tag{37}$$

where τ is the inertia time constant.

Substituting (36) and (37) into Figure12, the voltage closed loop transfer function of the proposed control strategy can be

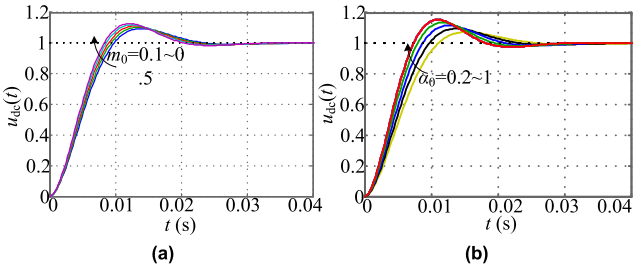

FIGURE 13. Unit step response of the proposed strategy. (a) m_0 increasing (b) α_0 increasing.

obtained as follow:

$$\frac{u_{\text{ref}}}{u_{\text{dc}}} = \frac{k_{\text{dcp}}LWs^2 + (k_{\text{dci}}L + k_{\text{dcp}}R_{\text{L}})Ws + k_{\text{dci}}R_{\text{L}}W}{N_4s^4 + N_3s^3 + N_2s^2 + N_1s + N_0} \tag{38}$$

where $W = (1 + m_0\text{SOC}_0 + \alpha_0)$. The expressions from N_0 to N_4 are shown as follows:

$$\begin{cases} N_4 = \tau C_{\text{dc}}L \\ N_3 = (1+\alpha_0)C_{\text{dc}}L + \tau R_{\text{L}}C_{\text{dc}} \\ N_2 = k_{\text{dcp}}LW + \alpha_0 R_{\text{L}}C_{\text{dc}} + \tau \\ N_1 = (k_{\text{dci}}L + k_{\text{dcp}}R_{\text{L}})W + \alpha_0 \\ N_0 = k_{\text{dci}}R_{\text{L}}W \end{cases} \tag{39}$$

The system unit step response results are derived according to (38), which are shown in Figure13. In addition to the parameters shown in Table 1, SOC_0 is set to be 0.8 and K_{pwm0} is 1. Figure 13(a) shows the response results when α_0 is set to be 1 and m_0 increases from 0.1 to 0.5 with the step size of 0.1. Figure13(b) shows the results when m_0 is set to 0.2 and α_0 varies from 0.2 to 1 with the step size of 0.2. According to the curves shown in Figure13, the following conclusions can be obtained: 1) The unit step response of voltage closed-loop is convergent, which means the proposed strategy has favorable voltage control capability; 2) Larger balance parameters are conducive to improve system dynamic response speed.

IV. EXPERIMENTAL VERIFICATION

In order to verify the validity of the proposed control strategy, a laboratory scale prototype has been developed, which consists of three sub-modules. A 32-bit floating-point DSC (TMS320F28335) and an FPGA (XC3S500E) are utilized for the system control. The DSC is in charge of sampling and data computation, and the FPGA is used to generate drive signals. Infineon IRFP90N20D is employed as the power device.

It can be known from the analysis presented in Section II(A) that the system operation modes are independent of each other, thus the verification of the proposed strategy under the two modes can be carried out independently. Because of the limited experimental conditions, two super capacitor modules connected in series are employed to simulate the DC bus to achieve bidirectional energy flow. Figure14(a) shows the schematic of the experimental platform which consists of charging part, DC bus and the modular ESS. Except for the parameters shown in Table 1, other experimental parameters are listed in Table 2. DC bus and the modular ESS are pre-charged by the charging part before experiment starts. The discharge resistances including R_{dc} and R_{dsc} are used to adjust the voltage of DC bus and SCM to the set value. The physical experiment platform is shown in Figure 14(b).

TABLE 2. Experimental parameters.

Symbol	Parameters	Value
f_{s}	Switching frequency	4kHz
C_{sc}	Capacitance of SCM	9.6F
V_{sc}	Rated voltage of SCM	50V
C_{dc}	DC bus filter capacitor	4400uF
R_{dc}	Discharge resistance of DC bus	10Ω
R_{dsc}	Discharge resistance of SCM	3Ω
C_{sdc}	Capacitance of simulated DC bus	4.8F
L_{cp}	Inductance of the charge converter	4mH
C_{cp}	Filter capacitor of the charge converter	4400uF
f_{cp}	Switching frequency of the charge converter	10kHz

A. EXPERIMENTAL RESULTS

Figure15 shows the experimental results in charge mode. The initial voltage of DC bus is 98V, and the initial SOC of the three SCMs is 0.62, 0.68 and 0.74, respectively. As can be seen from Figure15(a) that the ESS is charged with the maximum current of 15.5A and the DC bus voltage is finally stabilized at 80V. The charge time at steady state is about 4 seconds. Figure 15(b) shows the response results without adding current compensation. It can be seen from Figure 15(b) that the maximum current in charge mode is larger than 15.5A, and the current deviation increases with the increase of SOC value. The charge time at steady state lasts 3.6 seconds, which is less than that with current compensation.

In order to better display the variation of SOC curves, the initial SOC value of the minimum SOC module is set to be the zero level in charge mode. The SOC curves in charge mode are shown in Figure 15 (c). The SOC increases gradually as the charging process continues, and the SOC differences between SCMs decreases obviously. Figure15(d) shows the SOC difference curves, where ΔSOC_{i-j} represents the SOC difference between the ith module and the jth module. At the end of the charging process, the final values of ΔSOC_{2-1} and ΔSOC_{3-2} reach 0.038 and 0.04, respectively. Thus, ΔSOC_{2-1} has been reduced by 36.7% and ΔSOC_{3-2} has been reduced by 33%. Due to the sub-module #1 has the smallest initial SOC, it can be seen from Figure15(e) that, with the aid of the proposed control strategy, sub-module #1 is fully turned on to absorb energy.

The experimental results in discharge mode are shown in Figure16. The initial voltage of DC bus is 70V, and the initial SOC of the three SCMs is 0.64, 0.76 and 0.7, respectively. The system response curves are shown in Figure16(a). It can be seen that the DC bus is charged by the ESS with the current of 15.5A, and the steady-state discharge time is about 1.4 seconds. The system response curves without

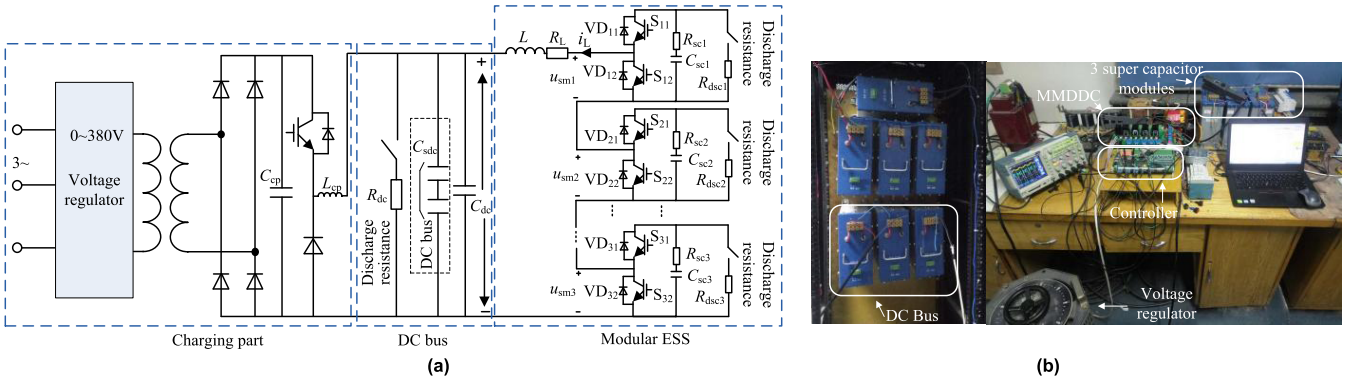

FIGURE 14. Schematic and physical diagrams of experimental platform. (a) Schematic diagram of experimental platform. (b) Physical diagram of experiment platform.

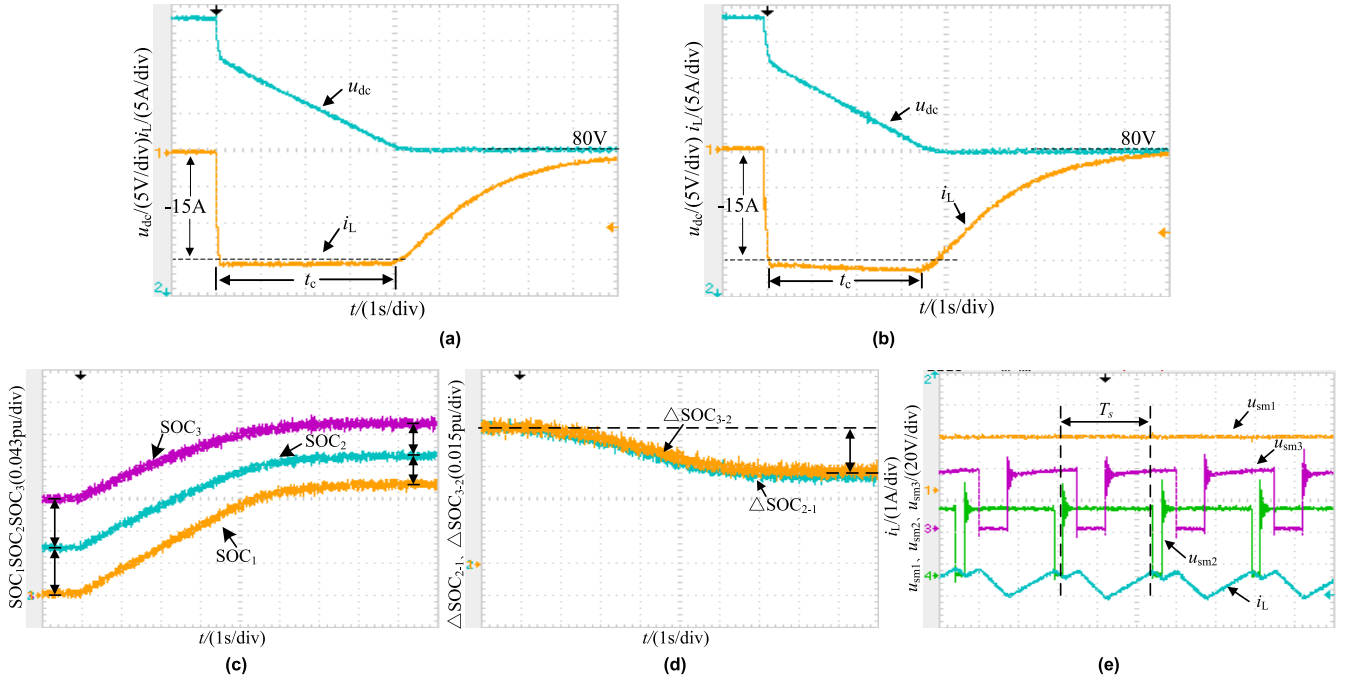

FIGURE 15. Experimental results in charge mode. (a) Waveforms of DC bus voltage and system current with current compensation. (b) Waveforms of DC bus voltage and system current without current compensation. (c) SOC waveforms of each SCM. (d) SOC variation waveforms. (e) Sub-module output voltage and system current.

current compensation are shown in Figure16(b). The maximum discharge current reaches 16.5A and the steady-state discharge time is 1.2 seconds. The initial SOC value of the maximum SOC module is set to be the zero level in discharge mode, and the SOC curves are shown in Figure16(c). Figure16(d) shows the SOC difference between SCMs. The final values of ΔSOC_{3-1} and ΔSOC_{2-3} are 0.049 and 0.041, respectively. Compared with the initial state, ΔSOC_{3-1} has been reduced by 18.3%, and ΔSOC_{2-3} has been reduced by 31.67%. Figure16(e) shows the waveforms of system current and sub-module output voltage. Sub-module #2 operates with the largest duty ratio and the duty ratio of sub-module #1 is 0.5, which is the smallest. The duty ratio lower limit of MMDDC is 0.5, which means that sub-module #1 has operated under the smallest duty ratio to prevent discharging energy.

The following conclusions also can be drawn from the above experimental results: (1) The proposed current compensation method can efficiently minimize the current deviation, thus the current regulation performance is improved. (2) Super capacitor has the characteristic high power density, the charging and discharging time of the system used in the experiment is relatively short. So, multiple charging and discharging times are required for the system to achieve completely SOC balance control. (3) From the current curves in Figure 15(e) and Figure 16(e), it can be seen that different sub-module voltages and their duty cycles lead to an increase in current ripple. Yet, in the practical system, the proposed strategy will not cause SOC difference as large as the experimental settings in this paper, so the current ripple will not increase significantly. Considering the system security, the system

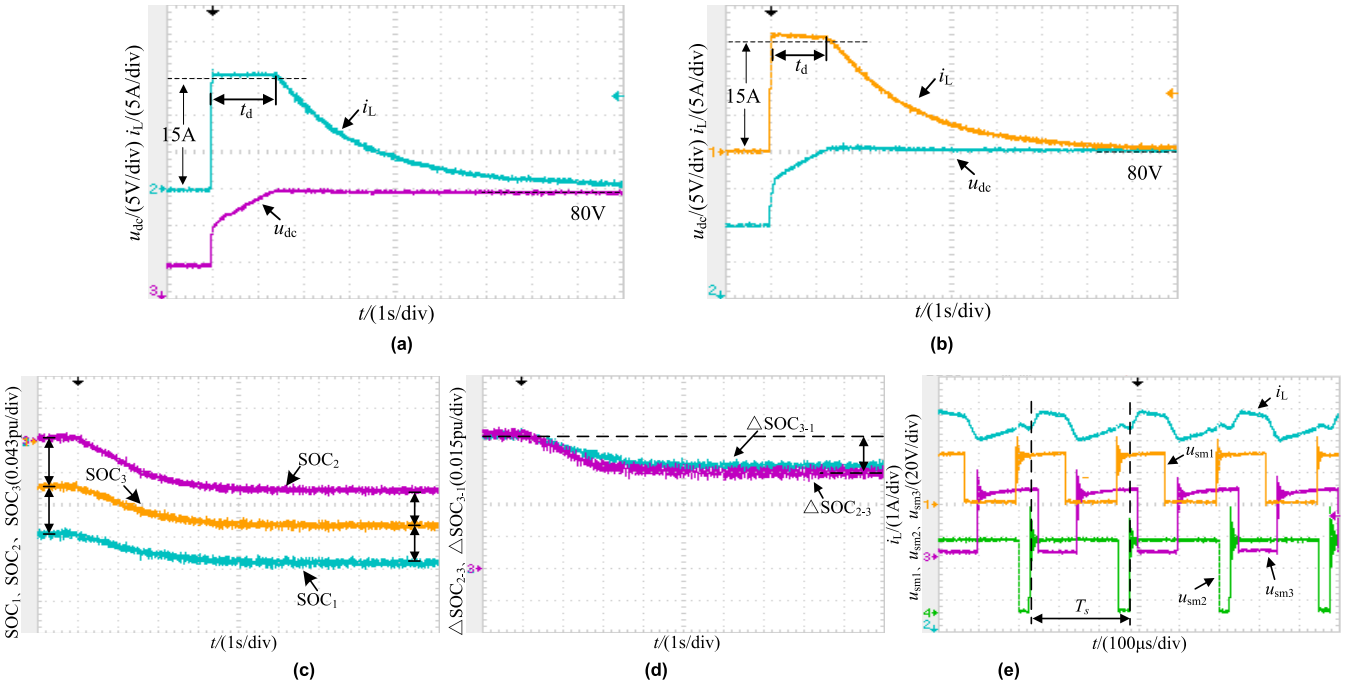

FIGURE 16. Experimental results in discharge mode. (a) Waveforms of DC bus voltage and system current with current compensation. (b) Waveforms of DC bus voltage and system current without current compensation. (c) SOC waveforms of each SCM. (d) SOC variation waveforms. (e) Sub-module output voltage and system current.

inductance can be increased appropriately to suppress the current ripple.

To verify the effectiveness of the strategy under other unbalanced conditions, the experiment with single unbalanced module is carried out under the same experimental conditions, and the experiment results are shown in Figure17. In Figure17(a) the initial SOC values are 0.68, 0.68 and 0.74, respectively. During the charging process, ΔSOC_{1-2} keeps zero all the time and ΔSOC_{3-2} decreases gradually. When the charging process is over, the final value of ΔSOC_{3-2} reaches 0.027, as shown in Figure17(b). Thus, the SOC difference has been reduced by 55% compared with initial state. Fig17(c) shows the SOC curves in discharge mode, and the initial SOC values are 0.7, 0.76 and 0.7 respectively. As shown in Figure17(d), ΔSOC_{2-1} reaches 0.034 and ΔSOC_{3-1} is always 0. Thus, the SOC difference has been reduced by 43.3%. In order to clarify the effect of the proposed strategy more clearly, the key experimental data in Figure15, 16 and 17 are sorted out and presented in Table 3. From the results we can know that the proposed strategy has favorable SOC balance control ability.

B. COMPARISON WITH OTHER METHODS

A comparison analysis is carried out to highlight the effectiveness of the proposed control strategy. The subjects selected are the SOC balance strategy proposed in [5] and [13]. The balance control strategy proposed in [13] is also applicable to the MMDDC topology, so we compare and analyze the three balance strategies under the same MMDDC. The comparison results are as follows.

TABLE 3. Experimental results.

Experiment item	ΔSOC_{i-j} before experiment	ΔSOC_{i-j} after experiment	Balanced Results
Two unbalanced modules in charge mode	ΔSOC_{2-1}:0.06	ΔSOC_{2-1}:0.038	36.7%
	ΔSOC_{3-2}:0.06	ΔSOC_{3-2}:0.04	33%
Two unbalanced modules in discharge mode	ΔSOC_{2-3}:0.06	ΔSOC_{2-3}:0.049	18.3%
	ΔSOC_{3-1}:0.06	ΔSOC_{3-1}:0.041	31.67%
Single unbalanced module in charge mode	ΔSOC_{1-2}:0.00	ΔSOC_{1-2}:0.00	—
	ΔSOC_{3-2}:0.06	ΔSOC_{3-2}:0.027	55%
Single unbalanced module in discharge mode	ΔSOC_{2-1}:0.06	ΔSOC_{2-1}:0.034	43.3%
	ΔSOC_{3-1}:0.00	ΔSOC_{3-1}:0.00	—

1) COMPARISON OF BALANCE EFFICIENCY

Figure 18 shows the experimental results of the strategy proposed in [13] under single unbalance module. Figure18(a) and (b) shows the experimental results in charge mode. The initial SOC values in charge mode are 0.68, 0.68 and 0.74, respectively. After charging, ΔSOC_{1-2} remains zero, while ΔSOC_{3-2} gradually decreases to 0.023, which is 61.67% lower than the initial state. Figure 18 (c) and (d) shows the discharge experiment results. The initial SOC values are 0.7, 0.76 and 0.7 respectively. After discharge termination, ΔSOC_{2-1} reaches 0.031, which has been reduced by 48.3% compared with initial state. In the same case, the balance efficiency of active SOC balance strategy for charge and discharge mode can be found in [5], which are 66.7% and 50%, respectively.

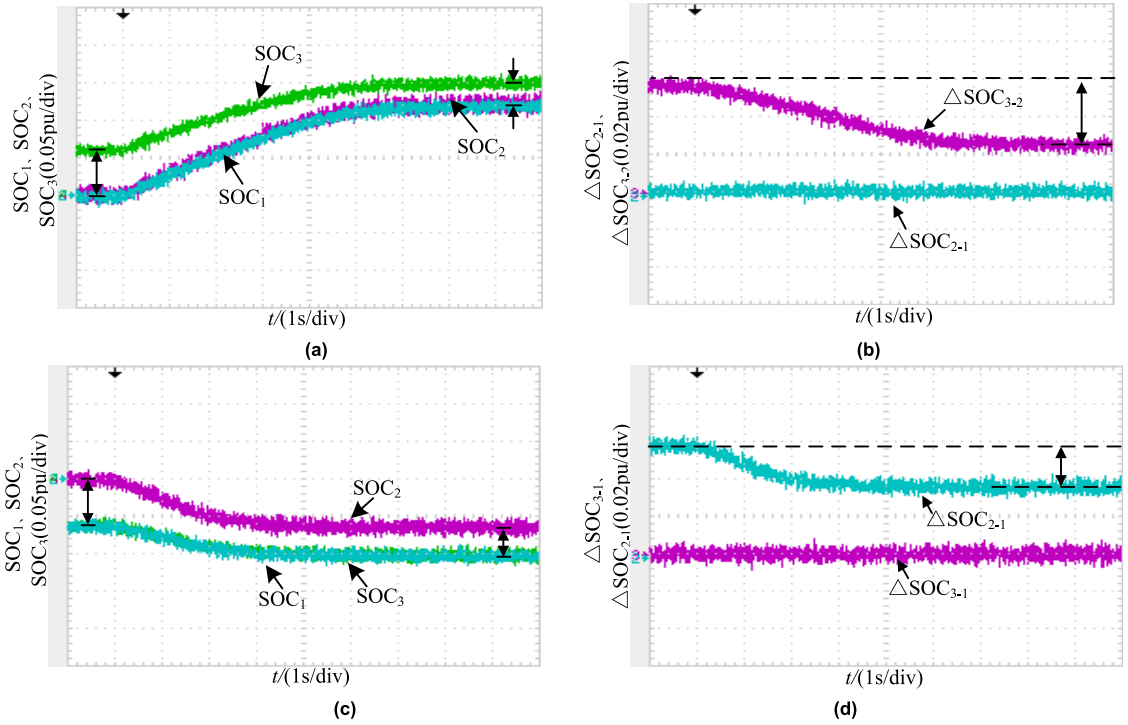

FIGURE 17. Experimental results under single unbalanced SCM. (a) SOC waveforms in charge mode. (b) SOC difference waveforms in charge mode. (c) SOC waveforms in discharge mode. (d) SOC difference waveforms in discharge mode.

2) COMPARISON OF POWER LOSS

The ESS power loss can be classified as system line loss P_L and power device loss P_s, which can be expressed as:

$$\begin{cases} P_L = i_L^2 R_{SL} \\ P_s = P_{con} + P_{on} + P_{off} + P_D \end{cases} \tag{40}$$

where R_{SL} is the system circuit equivalent impedance, P_{con} is the conduction loss, P_o and P_{off} are the switching-on and switching-off losses, respectively, and P_D is the power loss of body diode. The expressions of the above power loss are shown as follows [30], [31]:

$$\begin{cases} P_{con} = (U_{ce0} + i_L R_{ch}) i_L \delta_t \\ P_{on} = f_{sw} E_{sw\_on} \dfrac{i_L}{I_N} \dfrac{U_{sc}}{U_N} K_{Rg\_on} K_T \\ P_{off} = f_{sw} E_{sw\_off} \dfrac{i_L}{I_N} \dfrac{U_{sc}}{U_N} K_{Rg\_off} K_T \\ P_D = (u_{D0} \cdot i_L + r_D \cdot i_L^2) + E_{rec} \cdot f_{sw} \end{cases} \tag{41}$$

where U_{ce0} is the threshold voltage of IGBT, R_{ch} is the conduction resistance of IGBT, δ_t is the conduction time, f_{sw} is the switching frequency, E_{sw_on}, E_{sw_off} are the switching-on and switching-off energy consumption respectively, i_L/I_N and U_{sc}/U_N express the conversion coefficients for IGBT, KRg_on and KRg_off are the correction coefficients for the switching-on and switching-off energy consumption respectively, KT is the temperature coefficient on switching loss, u_{D0} is conduction voltage drop of body diode, r_D is the equivalent resistance of body diode, and E_{rec} is the reverse recovery losses of body diode.

The system energy loss is determined by both the power loss and the running time of the system. Assuming that the total transferred energy is E_w, which is expressed as:

$$E_w = \int_{t_1}^{t_2} u_{dc} i_L dt \tag{42}$$

According to (42) we can obtain system running time. According to the running time and (41), we can have the expression of system total energy loss:

$$\begin{aligned} E_{loss} = {} & \frac{E_w i_L}{u_{dc}} \left[R_{SL} + \sum_{i=1}^{n} (R_{chi} \delta_{ti} + r_D) \right] + n E_{rec} f_{sw} \\ & + \sum_{i=1}^{n} \frac{E_w}{u_{dc}} \left[U_{ce0i} \delta_{ti} + \frac{f_{sw} K_{Ti} U_{sci}}{I_N U_N} (E_{sw\_on} K_{Rg\_on} \right. \\ & \left. + E_{sw\_off} K_{Rg\_off}) \right] \end{aligned} \tag{43}$$

It can be known from (43) that when the number of cascade modules is large, the switching losses tend to be the same and the system energy loss will be determined by system current. Therefore, reducing the system current can reduce the energy loss. However, both the methods in [5] and in this paper contain current compensation, and the system current difference is very small. At the same time, the equivalent impedance of the system and the conduction resistance of the power device are very small. So, the energy loss of three control strategies is basically the same.

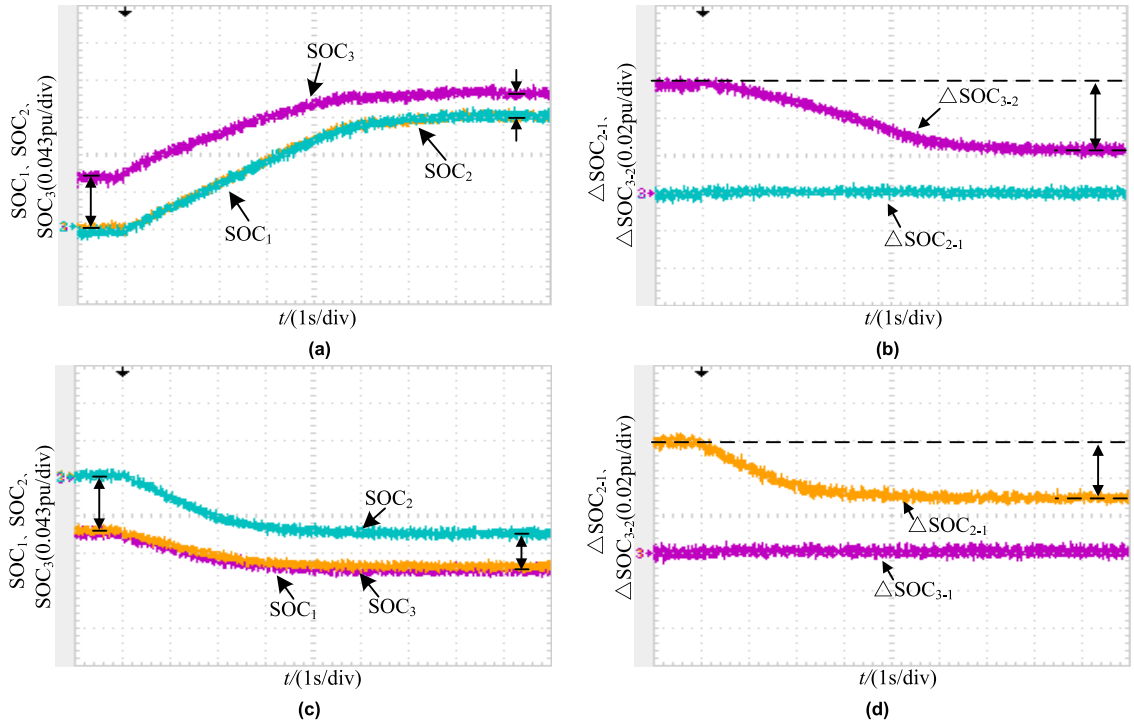

FIGURE 18. Experimental results of the SOC balance strategy proposed in [13] under single unbalanced SCM. (a) SOC waveforms in charge mode. (b) SOC difference waveforms in charge mode. (c) SOC waveforms in discharge mode. (d) SOC difference waveforms in discharge mode.

3) COMPARISON OF IN PRACTICAL APPLICATIONS

In addition to the balance efficiency and system power loss, it is also necessary to evaluate the control strategy from the perspective of practical application, which is carried out from the aspect of system hardware architecture and communication data in this paper. All the three balance strategies require digital communication. In addition to the digital control and communication circuits, the strategy proposed in [5] requires additional DAC circuits and a long balance bus. As analyzed in the introduction, the additional circuits not only increase system cost, but also bring great potential risks to the system. In terms of communication data, the strategies proposed in [5] and in this paper require very little communication, and both strategies have fault tolerant control capability. But the strategy in [13] needs to collect the SOC information of all modules by means of digital communication, which not only needs to deal with a large amount of communication data, but also leads to the poor fault-tolerant control ability, and any sub-module fault will affect its normal operation. Therefore, in a comprehensive view, the control strategy proposed in this paper has more obvious advantages in the actual conditions.

V. CONCLUSION

This paper proposes a dynamic SOC balance control strategy for the modular super capacitor ESS. SOC is used as the droop variable in the proposed strategy to redesign the independent current loop of each sub-module, so that the sub-modules can operate with the droop characteristic. Thus, the SOC balance control is realized in the system dynamic process, and the communication data for system control is minimized. Moreover, a unified system current compensation method is proposed to reduce system current deviation, which is caused by the SOC balance algorithm. The proposed strategy has favorable energy balance ability, stability and control performance. Compared with the traditional balance strategies, the proposed strategy not only has a concise structure and control method, but also improves the modularity of the system. Therefore, it is more suitable for the practical applications. Furthermore, this strategy can be extended to other cascaded modular ESS to balance the SOC of energy storage device, such as cascaded modular battery ESS.

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